Technische Universität Braunschweig

IMAB Institut für Elektrische Maschinen, Antriebe und Bahnen TU Braunschweig

Final Project

Analysis and design of resonant dc/dc converters for automotive applications

Institut für Elektrische Maschinen, Antriebe und Bahnen

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List of Contents

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List of Tables

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List of Figures

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Acronyms

AC	Alternating Current
DC	Direct Current
EMI	Electromagnetic Interference
EV	Electric Vehicle
FM	Frequency Modulation
HEV	Hybrid Electric Vehicle
PRC	Parallel Resonant Converter
PWM	Pulse-Width Modulation
SPRC	Series-Parallel Resonant Converter
SR	Synchronous Rectification
SRC	Series Resonant Converter
ZCS	Zero Voltage Switching
ZVS	Zero Current Switching

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Abstract

With automobiles getting more electrified, DC-DC resonant converters are developed with renewed interest. Since, it is desirable to reduce the size of power supplies and the higher switching losses through zero-voltage switching (ZVS) feature. This thesis provides detailed information on designing LLC and bidirectional CLLC resonant converter topologies as well as the simulation of four typical converters in automotive applications. Furthermore, the hardware design and manufacture of an EV auxiliary power supply prototype is implemented.

Keywords related to this work:

- **DC-DC resonant converter design**
- **LLC**
- **Bidirectional CLLC**
- **Zero-voltage switching (ZVS)**

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Kurzfassung

Aufgrund zunehmender Elektrizierung von Automobilantrieben werden DC-DC Resonanz-wandler mit neuem Interesse entwickelt. Entscheidend für den Einsatz im Automobilbereich sind geringe Abmessungen. Daher ist es wünschenswert die Größe der Stromversorgung und die höheren Schaltverluste durch Nullspannungsschaltung (ZVS) zu reduzieren. Dieses Masterarbeir bietet sowohl ausführliche Informationen zur LLC-Gestaltung und Auslegung der bidirektionalen CLLC-Resonanzwandler als auch die Simulation von vier typischen Wandlern in der Automobilanwendung. Ferner ist die Konstruktion der Hardware und Herstellung eines Prototypen der EV Hilfstromversorgung umzusetzen.

Stichwörter zu dieser Arbeit:

- **DC-DC Resonanzwandler**
- **LLC**
- **Bidirektionaler CLLC**
- **Nullspannungsschaltung (ZVS)**

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1 INTRODUCTION

The increasing demand for electric power in automobiles requires larger number of applications where DC-DC converters are used. To reduce the size of power supplies intended to use in modern electric power systems, it is desirable to raise the operating frequency to reduce the size of components. To decrease the higher switching losses resulting from higher frequency operation, resonant power conversion is receiving renewed interest.

Resonant converters, which were very investigated some decades ago, may achieve low switching loss and operate at high switching frequency. In resonant topologies, Series Resonant Converter (SRC), Parallel Resonant Converter (PRC), Series Parallel Resonant Converter (SPRC), LLC and CLLC are the most common topologies.

This thesis presents a design procedure for LLC and CLLC resonant converters, beginning with an overview on common topologies and operation behavior. To demonstrate how a design is created, four step-by-step automotive applications are presented. The thesis concludes with the hardware design and manufacture of one proposed application.

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2 RESONANT THEORY

This chapter introduces the resonant theory of DC-DC converters as well as an overview on common topologies. Moreover, a description of the process to obtain a suitable set of parameters for a specific design is proposed.

2.1 Resonant Switching theory and converter classification

A way to reduce or eliminate some of the switching loss mechanisms (Figure 2.1 shows soft and hard switching of a MOSFET) is achieved when turn-on and turn-off transitions of semiconductors devices occur at zero voltage or current waveforms.

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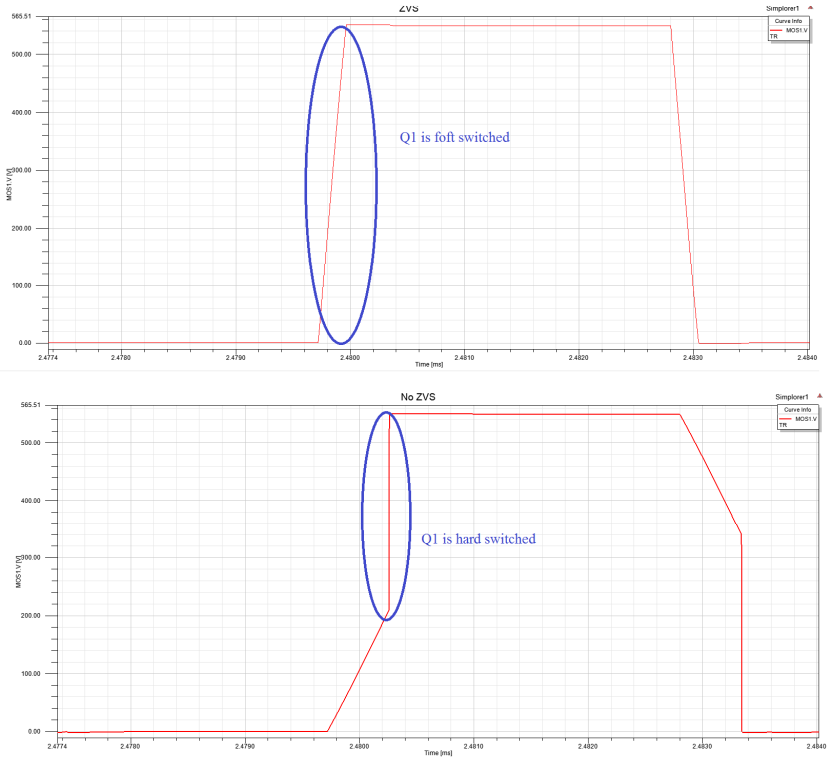

Figure 2.1 Comparative soft and hard switching

2.1.1 Zero Voltage Switching

The ZVS turn-on is achieved by discharging the output capacitance of the switches before turning them on. Transistor turn-on transition occurs at zero voltage. ZVS brings some benefits such as low switching losses, reduction of the energy needed to drive switches, low noise and EMI generation.

The ZVS approach is preferred for the majority of carrier semiconductor devices such as MOSFETs.

2.1.2 Zero Current Switching

The ZCS turn-off transition occurs at zero current. The ZCS approach is suitable for the minority of carrier semiconductor devices such as insulated-gate bipolar transistors and

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power diodes

2.2 Overview on resonant DC-DC converter topologies

A general description of each circuit, advantages and disadvantages are presented here.

The difference between each topology is found in the resonant tank. Figure 2.2 shows a switching network, rectifier block and resonant tank.

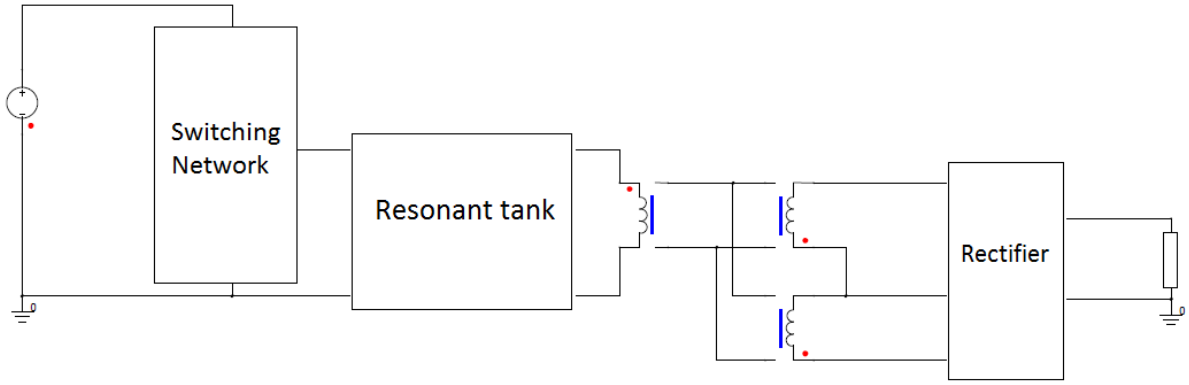

Figure 2.2 Resonant converter block diagram

2.2.1 Series Resonant Converter (SRC)

In series resonant converter, the tank is formed by resonant inductor (Lr) and resonant capacitor (Cr) and they constitute a series resonant tank as seen in Figure 2.3.

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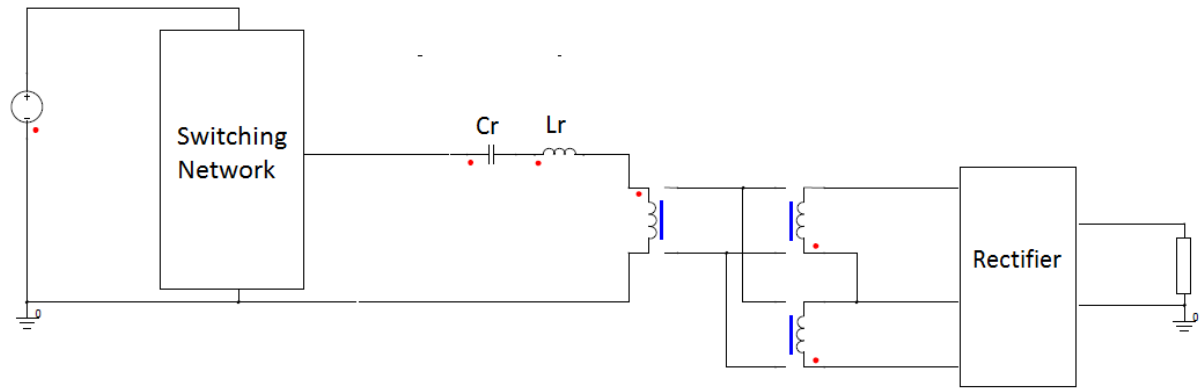

Figure 2.3 Series resonant converter block diagram

They are also in series with the load and it works as a voltage divider. The gain is always lower than the unity thus it works as a voltage divider. The maximum gain is obtained at resonant frequency since the impedance of series resonant tank will be lower at this frequency.

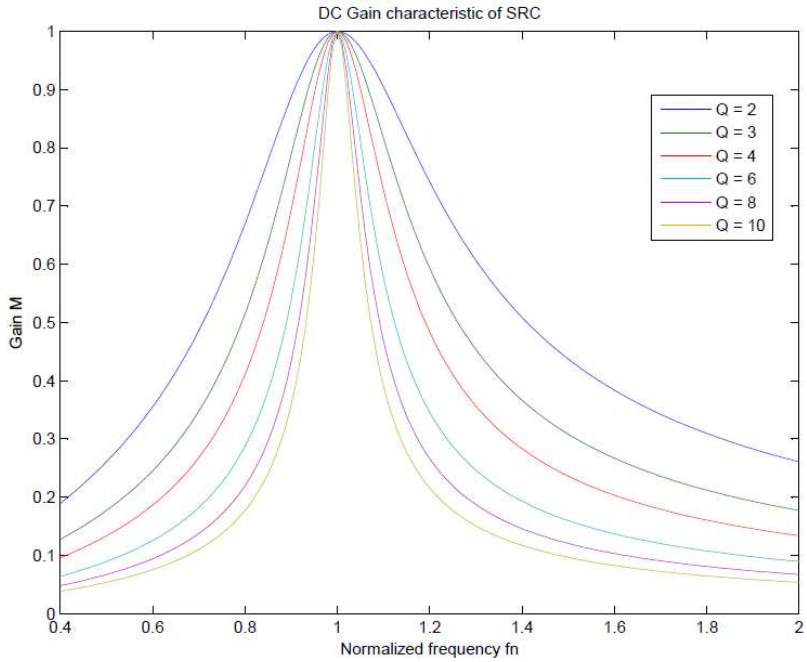

Figure 2.4 Gain characteristic of SRC

Two zones are differentiated in Figure 2.4 by the vertical of the resonant frequency. When the switching frequency is higher than resonant frequency, the converter will work under

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ZVS condition. This region is chosen for the operating region because of ZVS. For lower frequency the converter will work under ZCS as explained in (1).

Main advantages and disadvantages of series resonant converter are presented here:

- ✖ No regulated output-voltage for no load case is the principle disadvantage in series resonant converter. Only applications with no load regulation required are available for this converter, since, as seen in Figure 2.4, low Q curves would be more horizontal.
- ✖ For applications with low output-voltage and high current is a disadvantage to have an output DC filter flowing high ripple current. High output-voltage and low output-current applications are more appropriate for these converters than low output-voltage and high output-current converters which are not perceived as suitable.
- ✓ Series resonant converter is suitable for full-bridge high power applications because of series resonant capacitors on the primary side act as a DC blocking capacitor.
- ✓ High load efficiency is preserved because of the current in the power devices decrease as the load decreases. It lets the power device conduction losses to be reduces as the load decreases.

2.2.2 Parallel Resonant Converter (PRC)

In this case this converter is called parallel resonant converter thus the load is in parallel with the resonant capacitor as seen in Figure 2.5. However, the resonant tank is still in series.

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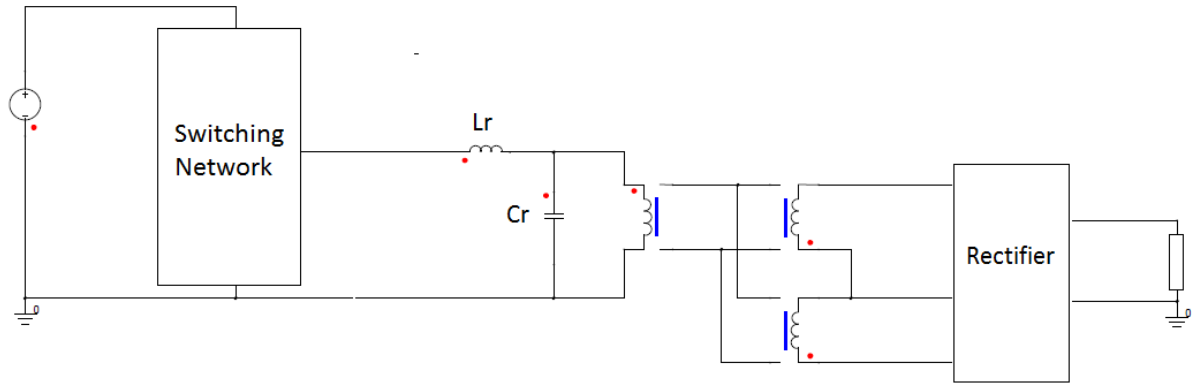

Figure 2.5 Parallel resonant converter block diagram

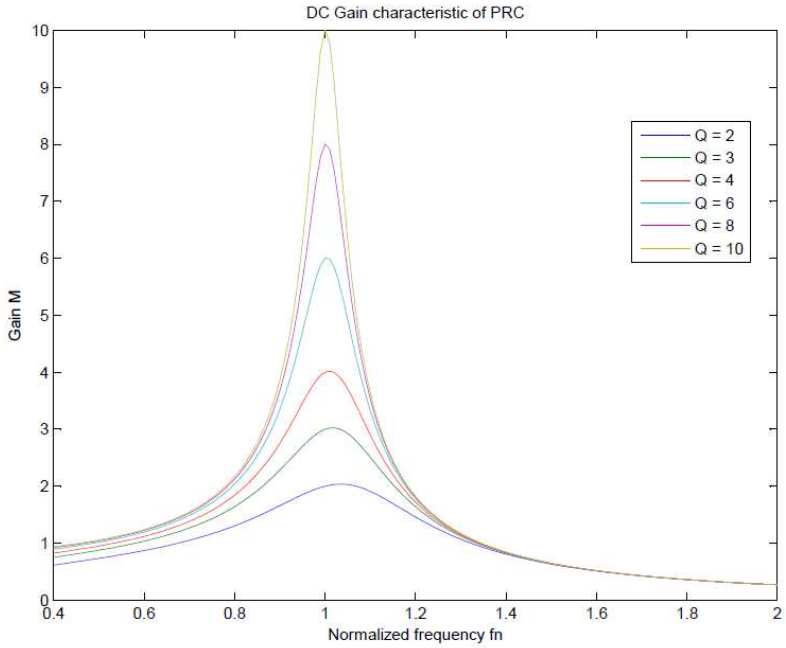

Figure 2.6 Gain characteristic of PRC

As seen in (1), ZVS is achieved on the right zone and for this converter the operation zone is also designed to obtain ZVS. To maintain the output-voltage regulated, high frequency variation is not needed. PRC has no regulation problem with light load and the operation region is smaller.

With higher frequency than resonant frequency the converter can control the output-voltage at no load condition (Q=0) how shows Figure 2.6.

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Main advantages and disadvantages of parallel resonant converter are presented here:

- ✖ The conduction losses are almost constant in the converter, since the current into the resonant tank keeps constant when the frequency varies to regulate the output-voltage.
- ✓ Applications which have a narrow input voltage range and a relatively constant load to maintain the working point near the maximum design power are more appropriate.
- ✓ The parallel-resonant converter is suitable for low-output-voltage and high-output-current applications. The current is limited by the resonant inductor making the PRC desirable for applications with high short-circuit requirements.
- ✓ Output-voltage is controlled with higher frequency than resonant frequency at no – load condition.

2.2.3 Series Parallel Resonant Converter (SPRC)

The combination of series-converter and parallel-resonant results in a converter with better characteristics than both and removes their disadvantages. A wider frequency range and optimal selection of the resonant components are required.

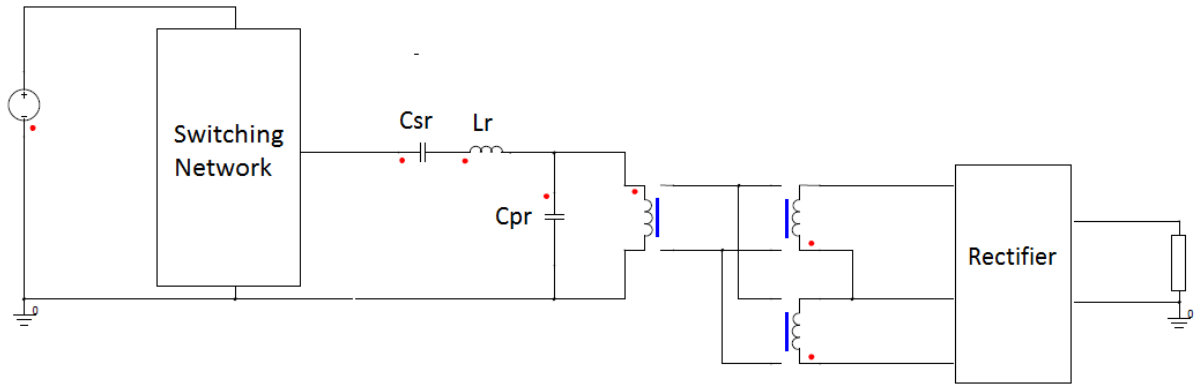

Figure 2.7 Series parallel resonant converter block diagram

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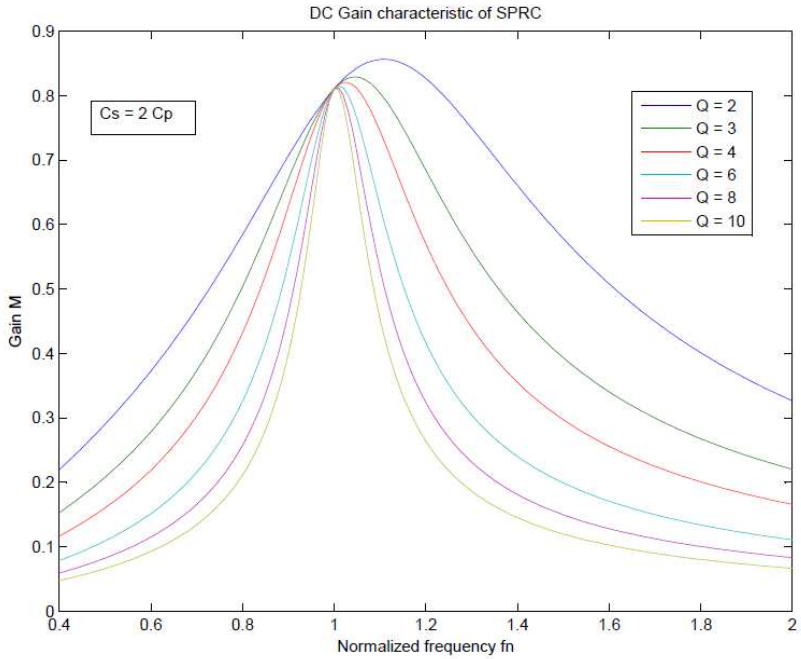

Figure 2.8 Gain characteristic of SPRC

ZVS is achieved designing the operation region on the right hand side. Highest resonant frequency makes normally the converter more efficient.

Main advantages and disadvantages of parallel resonant converter are presented here:

- ✓ No load regulation is achieved for SPRC when C_{pr} is not too small. Main disadvantage of SRC is removed.
- ✓ Constant circulating current independent of the load is avoided.
- ✘ Switching losses will increase at high input voltage when the input range is wide. Switching loss is still, a big penalty, similar to PWM converter at high input voltage.

A more detailed explication about these converters is found in (1).

2.2.4 LLC Converter

The characteristics and operation of this converter are different; despite of LLC has the same

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form as SPRC apart of magnetizing inductance as seen in Figure 2.9. Three resonant components form the LLC converter (L_r, C_r and L_m) and two resonant frequencies are induced. Low frequency is induced by C_r and $L_m + L_r$ and the high frequency by C_r and L_r.

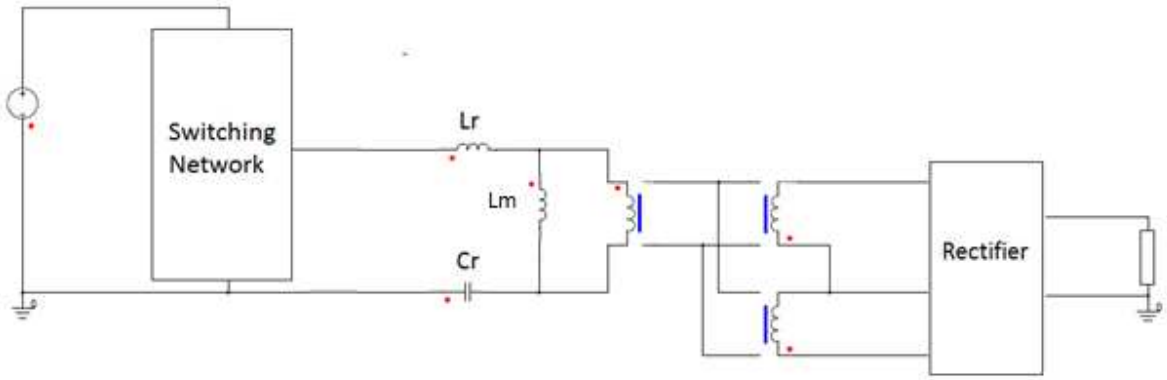

Figure 2.9 LLC resonant converter block diagram

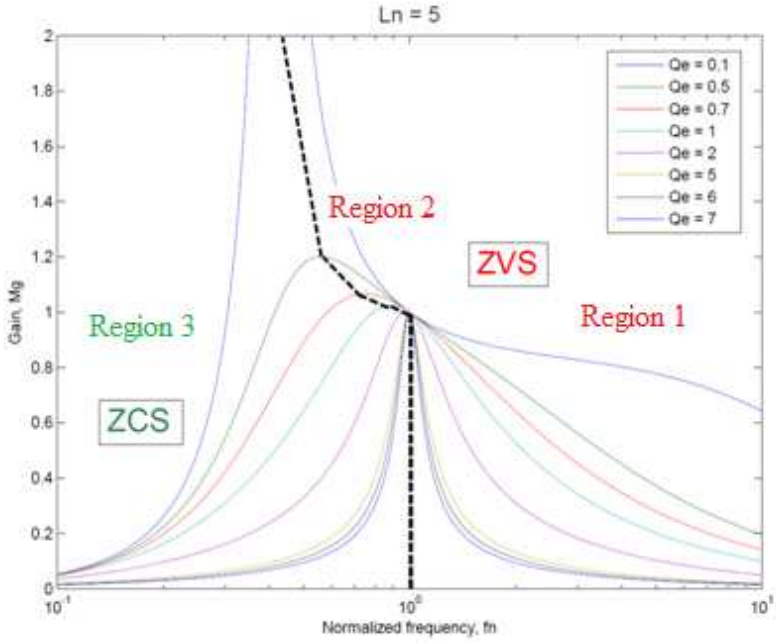

Figure 2.10 Gain characteristic of LLC

In Figure 2.10 is possible to see how when the load becomes lighter the peak moves closer to f_1. On the other hand, the peak moves to f0 when the load becomes heavier. Comparing the converter behavior, it works more as PRC when the load is light and more as SRC when

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the load is heavy. The gain characteristics can be either boost type or buck type, which means buck-boost converter.

As seen previously, Figure 2.10 is divided in three regions:

- Region 1: Switching frequency is higher than f_{r1}. ZVS is achieved in this region and it is also SRC operation region.
- Region 2: Between f_{r1} and f_{r2} is a multi resonant converter region. Depending on the load the converter will be under ZCS and ZVS condition.
- Region 3: Only ZCS is achieved in this overloaded region.

In general, LLC resonant converter is designed to operate in Region 1 and 2 because of output regulation and ZVS operation. To ensure ZVS operation, the operating range of this converter is above the f_{r2} and the L_r and C_r are chosen to ensure at heavy load. The choice of the L_m determines the switching frequency range and MOSFET turn-off current. With smaller L_m more narrow operating range is set. However, MOSFET turn-off current will be higher which increases switching losses.

The most efficiency working point is to allow LLC converter to work at the resonant frequency f_{r1}, thus switching losses and circulating energy are reduced working under these conditions. To maintain the output voltage regulated when the load and the input voltage vary, the operation frequency is modified. The ZVS operation of the MOSFETs is very important for the efficiency of the LLC resonant converter. A more detailed analysis about operating modes in LLC converter is presented in (2).

Main advantages and disadvantages of LLC resonant converter are presented here.

- ✓ Output regulation is controlled whit variations of switching frequency.
- ✓ ZVS capability for whole load range produces lower switching losses.
- ✓ The magnetic components can be integrated into magnetic core. The leakage inductance of a transformer can participate in resonant operation.
- ✗ Conventional LLC converter is unidirectional.

Several variants are proposed to improve the converter possibilities (three level ZVS PWM

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converter, secondary-side control); however, full-bridge topology is the most common. Lower current values are obtained with this topology in high voltage applications. It is also proposed full-bridge topology in the secondary side trying to reduce power losses through Synchronous Rectification (SR).

2.2.5 CLLC Converter

Apart for the extra resonant capacitor, the converter configuration is very similar to LLC converter. It has also ZVS but an additional property is obtained, bidirectionality.

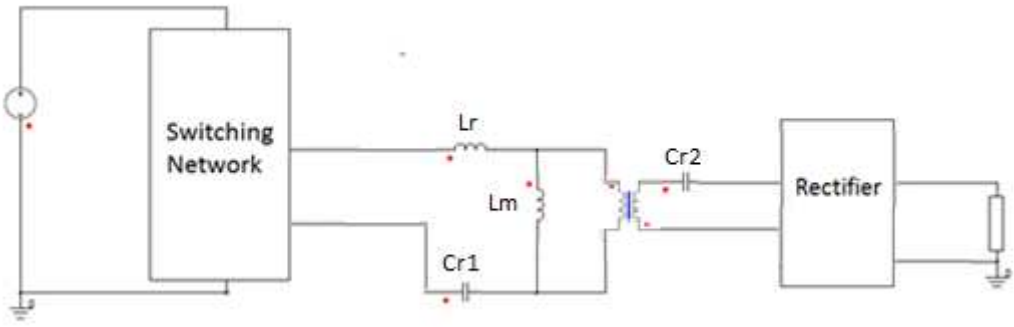

Figure 2.11 CLLC resonant converter block diagram

In (3) a detailed analysis of different combinations of MOSFETs and IGBTs is carried out. For this converter ZVS + ZCS is preferred (ZVS primary side devices and ZCS secondary side devices) regardless of the direction of the power flow. The primary side changes depending on the power flow direction and the benefits of MOSFETs (associated with ZVS) in the primary side make that the MOSFETs are chosen in both sides. Since, with this topology the switching losses can be minimized.

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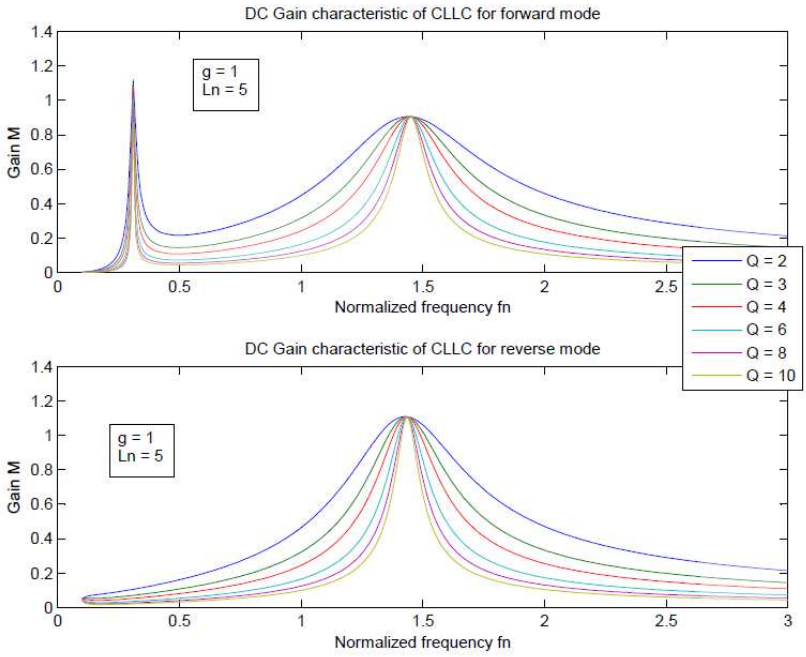

Figure 2.12 Gain characteristic of CLLC

Theoretically, ZVS + ZCS can be obtained through PWM and FM. However, this topology is not the best option for PWM converters, thus it may work in discontinuous current mode (DCM) and this is not very suitable for high-power rating applications. Because of that ZVS + ZCS feature is not commonly used for PWM and FM is designed.

ZVS feature for the inverting network can be easily achieved with FM and the ZCS feature for the rectifier switches can also be achieved if there is no filter inductor at the output side.

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2.3 LLC RESONANT HALF – BRIDGE CONVERTER

A general description about resonant converters has been proposed previously. A suitable converter for unidirectional operation flow applications is half-bridge LLC Resonant Converter as demonstrated in (4), (5), (1)and (3).

A design procedure of LLC Resonant Converters is presented here. It is suitable for high-voltage and high-frequency applications and allows the output voltage regulation against variations from light- to full-loaded conditions. This section describes a typical LLC resonant half-bridge converter with its operation mode, its parts and its relationship between the input and the output voltages.

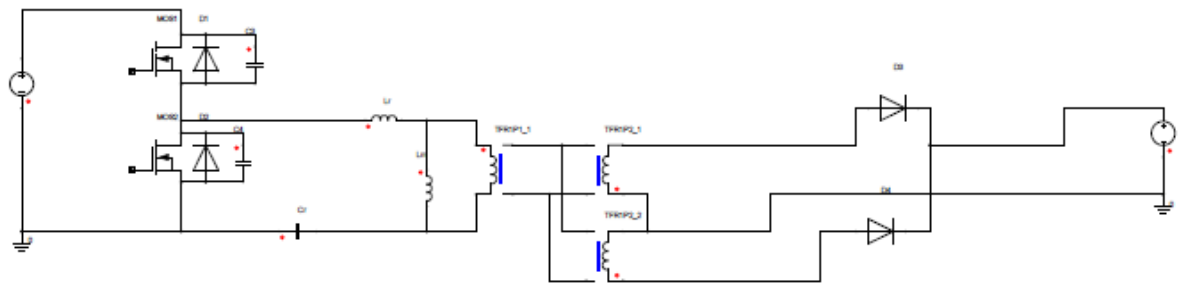

Figure 2.13 Half-Bridge LLC Resonant Converter

2.3.1 Configuration

Figure 2.13 shows a typical topology of LLC resonant half-bridge converter. Two MOSFET's are connected in a bridge configuration (MOS1, MOS2) connected to the resonant tank. Complementary mode with a fixed duty cycle (50%) is chosen to configure the converter. It also needs some dead time serving two purposes: Prevent short-circuits and the interval time used to charge / discharge the MOSFETs drain-to-source capacitance used for ZVS.

A resonant capacitance (C_r), and two inductances (the series resonant inductance, L_r, and the

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transformer's magnetizing inductance, L_m) form the resonant circuit or resonant tank. The transformer turn ratio is n and it provides electrical isolation. Thus, the energy between the resonant tank and the load circulates throw the transformer.

Two diodes constitute a rectifier to convert AC input to DC output and supply the load.

2.3.2 Modeling

As seen previously, LLC converter has two resonant frequencies

$$\mathbf{f_0} = \frac{\mathbf{1}}{\mathbf{2\pi\sqrt{L_r C_r}}} \quad (1)$$

$$\mathbf{f_1} = \frac{\mathbf{1}}{\mathbf{2\pi\sqrt{(L_r + L_m) C_r}}} \quad (2)$$

and most of the time LLC converter is designed to operate nearly of f_0.

To design a converter for variable energy transfer and voltage regulation, a transfer function is very important. (6) shows how the gain formula is developed.

The relationship between the input voltage and the output voltage can be described by their ratio or gain

$$\boldsymbol{M_g} = \frac{\boldsymbol{n \cdot V_0}}{\boldsymbol{V_{in}/2}} \quad (3)$$

For giving a gain depending on detailed values, f_0 is selected as the base of normalization. Then the normalized frequency is expressed as

$$\mathbf{f_n} = \frac{\mathbf{f_{sw}}}{\mathbf{f_0}}. \quad (4)$$

An inductance ratio can be defined combining two inductances into one

$$\mathbf{L_n} = \frac{\mathbf{L_m}}{\mathbf{L_r}} \quad (5)$$

and the quality factor of the series resonant circuit is defined as

$$\mathbf{Q_e} = \frac{\mathbf{\sqrt{L_r/C_r}}}{\mathbf{R_e}}. \quad (6)$$

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With the help of these definitions, in (6) the voltage-gains is obtained as

$$\mathbf{M_g} = \left| \frac{\mathbf{L_n \cdot f_n^2}}{\mathbf{[(L_n+1)\cdot f_n^2 - 1] + j[(f_n^2 - 1)\cdot f_n \cdot Q_e \cdot L_n]}} \right| \quad 7$$

To understand the response of the resonant circuit Equation (7) is decisive. How changing f_n is possible to control M_g when L_n and Q_e are fixed.

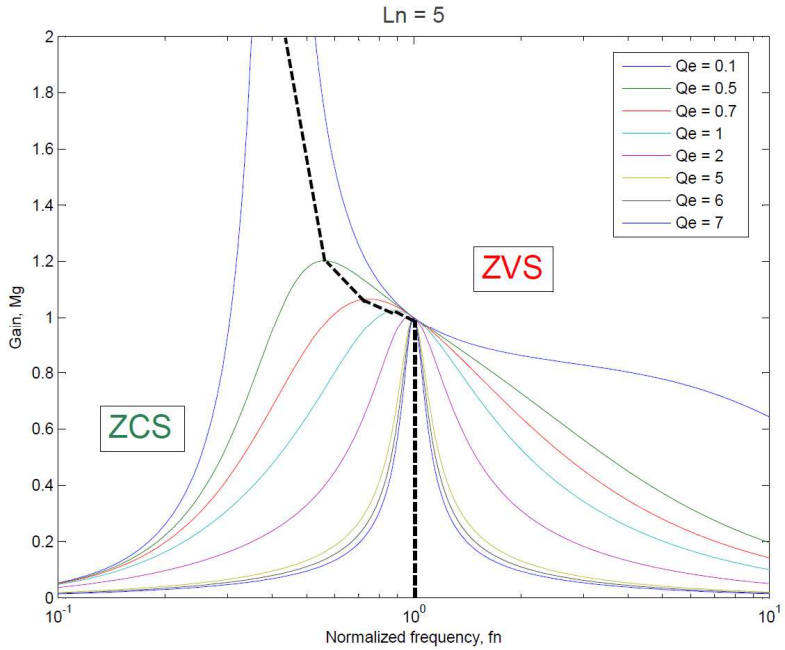

Figure 2.14 Plot of voltage-gain function (Mg) with Ln = 5

2.3.3 Design considerations

Three requirements must be considered for the designing. At first, output voltage (V_{0_min} and V_{0_max}) and input voltage (V_{in_min} and V_{in_max}) are studied. The converter requirements define the maximum and the minimum values of the voltages.

$$\mathbf{M_{g\_min}} = \frac{\mathbf{n \cdot V_{0\_min}}}{\mathbf{V_{in\_max}/2}} \quad 8$$

and,

$$\mathbf{M_{g\_max}} = \frac{\mathbf{n \cdot V_{0\_max}}}{\mathbf{V_{in\_min}/2}} \quad 9$$

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These Mg values are one of the limits for the operation zone.

The second requirement is Q_e, which is associated with the load current. The aim is to find the optimal value for each design, since a small Q_e makes the peak higher (Figure 2.14) while a gain curves have a larger frequency variation for a given gain adjustment ($Q_e = 0$ is "no load" condition). A very low peak gain means a large Q_e which may not meet the design requirements.

Finally, low switching losses is one of the principle advantages of LLC topology and it is achieved through ZVS. As it is possible to see in Figure 2.14 and studied previously, ZVS is only reached on the right side of the resonant side of the resonant gain curves which needs to be checked in every designing process. This step is very important to achieve successfully the optimal designing.

2.3.4 Selecting design parameters

- **F_{sw}, switching frequency**

  This parameter is previously defined considering different elements. For example, certain circuit components are more suitable for determined frequency. LLC has more benefits with higher switching frequency but other adverse factors appear when it is very high.

- **n, transformer turns ratio**

  Assuming $M_g = 1$, n can be designed as

$$\mathbf{n = M_g \cdot \frac{V_{in}/2}{V_0}} \qquad 10$$

- **L_n and Q_e**

  The most critical point in Figure 2.14 is the crossing point between M_{g_max} and the maximum value of Q_e. This point should be designed to prevent the operation zone entering in ZCS region. Following (6) a useful tool is to create the curve set up for the maximum M_g values for each Q_e curves, called M_{g_ap} as seen in Figure 2.15. Then Ln and Q_e can be selected, since M_{g_ap} is always higher than M_{g_max}.

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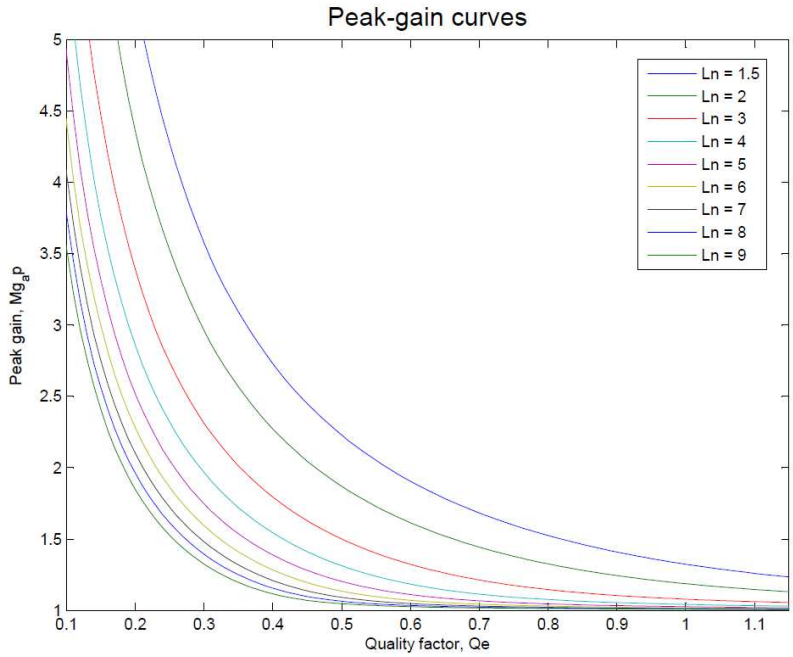

Figure 2.15 Peak-gain curve

A small L_n keeps the operation zone out of the capacitance region because it makes the peak gain higher. As indicates Equation (5) it helps with ZVS but introduces higher magnetizing current and increases conduction losses.

Working in different load conditions is a main property, being no load condition (I_o=0, Q_e = 0) a critical operation point for high input voltage. Since the gain curves are determined by L_n and Q_e then L_n becomes the only design parameter. A value for L_n needs to be selected to provide a gain curve crossing over the horizontal lines defined by Equations (8) and (9).

- **Re, Load resistance**

Depends on the output-current and the output-voltage

$$\mathbf{R_e = \frac{8 \cdot n^2}{\pi^2} \cdot \frac{V_0}{I_0}} \qquad 11$$

- **Resonant circuit's parameters**

$$\mathbf{C_r = \frac{1}{2 \cdot \pi \cdot Q_e \cdot f_0 \cdot R_e}} \qquad 12$$

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$$\mathbf{L_r = \frac{1}{(2 \cdot \pi \cdot f_0)^2 \cdot C_r}} \quad 13$$

$$\mathbf{L_m = L_n \cdot L_r} \quad 14$$

- **Dead time**

Enough dead time is an important requirement to assure ZVS in the converter and to avoid short circuit between the MOSFET's.

$$\mathbf{t_{dead} \geq n \cdot C_{eq} \cdot f_{sw} \cdot L_m} \quad 15$$

- **Frequency range, f_{n_max} and f_{n_min}**

F_{n_max} and f_{n_min} are obtained in M_g-f_n graph with M_{g_max}, M_{g_min} limits and Q_e plot.

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2.4 LLC RESONANT FULL – BRIDGE CONVERTER

Full-bridge LLC Resonant Converter is more suitable converter for lower current values applications than half-bridge topology.

The operation mode, parts and relationship between the input and the output voltages for the full-bridge converter are described in this section.

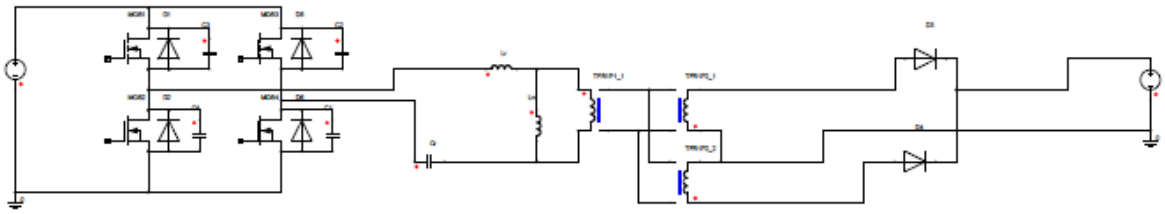

Figure 2.16 Full-Bridge LLC Resonant Converter

With the purpose of reducing the MOSFETs current in high-power applications, full-bridge topology is proposed with high-frequency galvanic isolation. This converter can improve power conversion efficiency using a zero-voltage transition feature.

2.4.1 Configuration

In Figure 2.16 is seen a LLC resonant full-bridge converter. A bridge configuration is used here to connect two couples of MOSFETs (MOS1, MOS2, MOS3, and MOS4) to the resonant tank. A fixed duty cycle in complementary mode (50% MOS1 – MOS3 and MOS2 – MOS4) is chosen to configure the converter. Two purposes are taken in care to define the dead time. Prevent short-circuits and the interval time used to charge / discharge the MOSFETs drain-to-source capacitance used for ZVS.

Three elements form the resonant tank, resonant capacitance (C_r), and two inductances (the series resonant inductance, L_r, and the transformer's magnetizing inductance, L_m). The

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transformer provides and important characteristic for the converter, electrical isolation. Half-bridge and full-bridge topology can be used for the rectifier to convert AC input to DC output and supply the load.

2.4.2 Modeling

The modeling is almost the same as in half-bridge topology (half-bridge modeling), equations (1) – (7). Only the relationship between the input voltage and the output voltage changes.

$$\mathbf{M_g} = \frac{\mathbf{n \cdot V_0}}{\mathbf{V_{in}}} \quad 16$$

2.4.3 Design considerations

The three requirements for the full-bridge converter are almost the same as the half-bridge (half-bridge design considerations). However, only the gain calculation is different in the process.

$$\mathbf{M_{g\_min}} = \frac{\mathbf{n \cdot V_{0\_min}}}{\mathbf{V_{in\_max}}} \quad 17$$

and,

$$\mathbf{M_{g\_max}} = \frac{\mathbf{n \cdot V_{0\_max}}}{\mathbf{V_{in\_min}}} \quad 18$$

2.4.4 Selecting design parameters

The process to select the optimal values for the resonant converter is similar to half-bridge topology (half-bridge selecting design parameters), equations (11) – (15). Only transformer turns ratio value is different

$$\mathbf{n} = \mathbf{M_g} \cdot \frac{\mathbf{V_{in}}}{\mathbf{V_0}} \quad 19$$

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2.5 CLLC BIDIRECTIONAL RESONANT CONVERTER

CLLC converter is considered the most suitable option for bidirectional operation flow applications as demonstrated in (3) and (7), and a previous description has been proposed. This section describes a design procedure and steps for CLLC Resonant Converters.

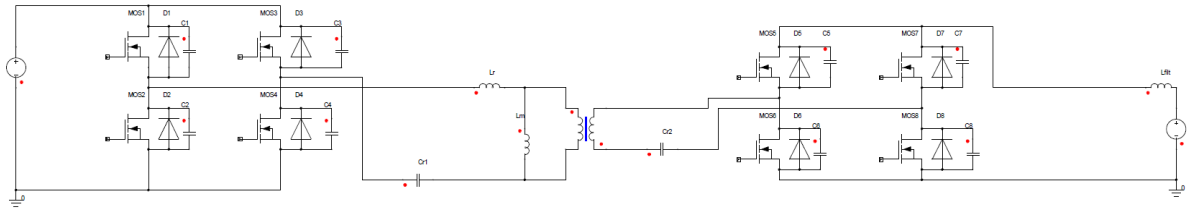

Figure 2.17 Full-Bridge CLLC Resonant Converter

2.5.1 Configuration

The circuit configuration of the proposed converter (Figure 2.17) is very similar to the conventional LLC resonant converter (seen before at LLC Configuration) from the topology point of view, except for the additional resonant capacitor.

Primary and secondary side are both connected in full-bridge configuration (MOS1, MOS2, MOS3, and MOS4 to the resonant tank and MOS5, MOS6, MOS7, and MOS8 to the load) respectively.

The configuration changes depending on the direction of the power flow (Mode-1, Mode-2). In Mode-1,the power flows from left to right and in Mode-2 flows in the opposite direction. The converter is also configured in complementary mode with a fixed duty cycle (50%, 180° out of phase) for one side and a synchronous rectification (SR) for the other side. It also need some dead time as LLC converter.

The extra capacitor (C_{r2}) in the right side makes this resonant tank different from LLC converter and allows working in bidirectional mode.

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2.5.2 Modeling

Mode-1 and Mode 2 have similar resonant properties, behavior over the switching frequency and even DC gain curves. However, as explained in (3) Mode-2 converter can be recognized as a LLC tank with an extra parallel resonant inductor. Mode-1 is more similar to the conventional SRC. C_{r2} acts like a dc blocking capacitor for both Modes.

For giving a gain depending on detailed values, f_0 is selected as the base of normalization. Then the normalized frequency is expressed as

$$\mathbf{f_n} = \frac{\mathbf{f_{sw}}}{\mathbf{f_0}}. \quad 4$$

An inductance ratio can be defined combining two inductances into one,

$$\mathbf{L_n} = \frac{\mathbf{L_m}}{\mathbf{L_r}} \quad 5$$

the quality factor of the series resonant circuit is defined as

$$\mathbf{Q_1} = \frac{\sqrt{\frac{\mathbf{L_r}}{\mathbf{C_{r1}}}}}{\mathbf{R_v}} \quad 20$$

$$\mathbf{Q_2} = \frac{\sqrt{\frac{\mathbf{L_r}}{\mathbf{C_{r2}}}}}{\mathbf{R_v}} \quad 21$$

and the capacitance ratio is

$$\mathbf{g} = \frac{\mathbf{C_{r2}}}{\mathbf{C_{r1}}} \quad 22$$

Based on the approach of fundamental mode approximation (FMA) (7), the equations of the dc gain for both modes can be expressed

$$\boldsymbol{M_{Mode-1}} = \left| \frac{\mathbf{1}}{\left[\frac{1}{L_n}+1-\frac{1}{f_{n1}^2}\right]+j[Q_1\cdot\left(\frac{1}{f_{n1}}-f_{n1}\right)+\frac{Q1\cdot(1+L_n)}{(g\cdot L_n\cdot f_{n1})}-\frac{Q_1}{g\cdot L_n\cdot f_{n1}^3}]} \right| \quad 23$$

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$$M_{Mode-2} = \left| \frac{1}{\left[1-\frac{1}{f_{n1}^2 \cdot Ln}\right]+j[Q_2 \cdot \left(\frac{1}{f_{n2}}-f_{n2}\right)+\frac{Q2 \cdot (1+Ln \cdot g)}{(Ln \cdot f_{n2})}-\frac{g \cdot Q_2}{Ln \cdot f_{n2}^2}]} \right| \quad 24$$

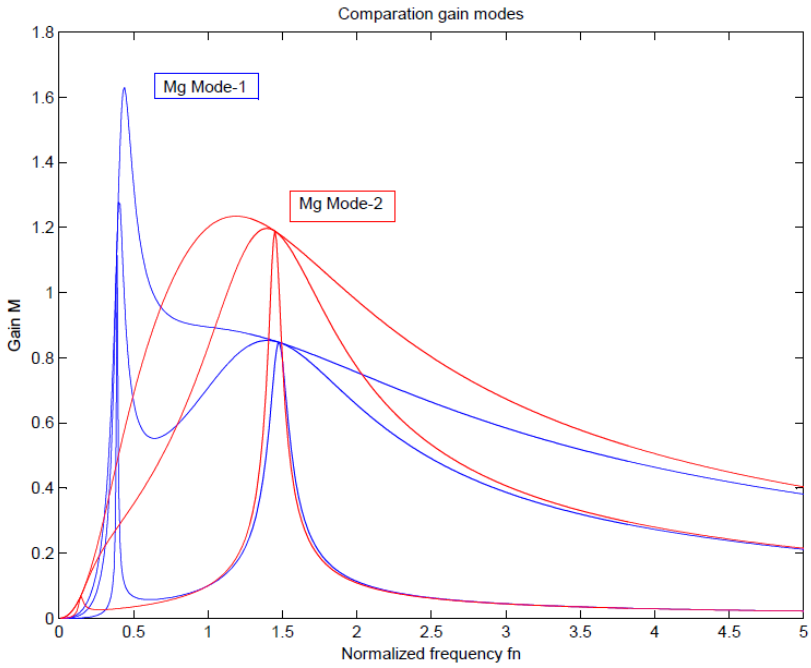

Figure 2.18 Comparative gain between Mode-1 and Mode-2

2.5.3 Design considerations

To alleviate the design difficulties, it is more suitable to start with the design of Mode-1 LLC resonant tank as seen in previous chapters and later Mode-2. It has the same design considerations and requirements as LLC converter.

2.5.4 Selecting design parameters

Only the step to obtain capacitance ratio is different from LLC converter process, seen in (10) – (15) equations (LLC converter design parameters).

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- **Fsw, switching frequency**
- **n, transformer turns ratio**
- **Ln and Q1**
- **Re, Load resistance**
- **Resonant circuit's parameters (Cr, Lr, Lm)**
- **Capacitance ratio, g**

The optimal selection of parameter *g* depends on how similar the curves of the dc gain of the two modes are, under the condition of the same parameter *g*. A proper *g* should make the two dc gain curves similar as much as possible in shape and amplitude.

As parameter g having been known, the second resonant capacitor C_{r2} can be calculated.

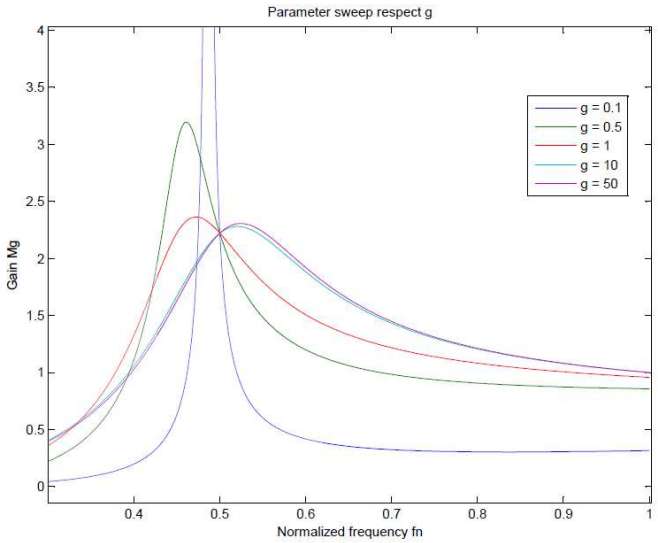

Figure 2.19 Parameter sweep respect to g for forward mode

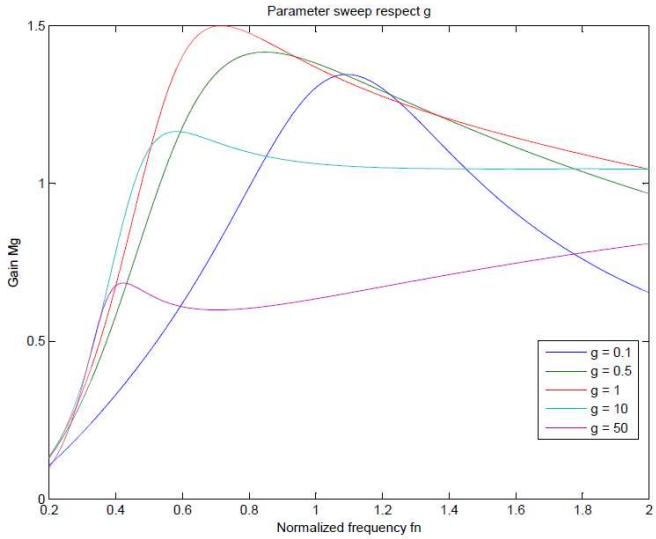

Figure 2.20 Parameter sweep respect to g for reverse mode

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3 DESIGN AND SIMULATION

This chapter presents the design process and simulation of four automotive applications such as EV Auxiliary power supply, Galvanic Insulation for standard EV Onboard charger, EV Auxiliary power supply for MILD HEV and Galvanic Insulation for EV fast charger with optimal “Vehicle to grid” feature.

3.1 DESIGNED EV AUXILIARY POWER SUPPLY

In this chapter, a simulation of LLC Resonant Converters for EV auxiliary power supply applications is presented. A resonant converter has been designed to operate in an input voltage range of 240 – 550 V with an output voltage of 14.4 V. It will be verified in: its operation principle, its attribute of soft switching, and its parameters will be calculated. Within these design specifications, a performance analysis of the LLC converter has been conducted, comparing the results obtained at different working conditions.

3.1.1 Design steps

The specifications and main parameters are specified as follows.

- P_0: 2500 W
- V_{in}: 240 – 550 V
- V_{out}: 14.4 V
- I_0: 174 A
- f_{sw}: 120 kHz

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With the required specifications, the design process is carried out:

- **Determine transformer turn ratio**

$$n = M_g \cdot \frac{V_{in\_nom}/2}{V_0} = 13.72$$

For transformer turns ratio calculation, $M_g = 1$ is used.

- **Determine M_{g_min} and M_{g_max}**

$$M_{g\_min} = \frac{n \cdot V_{0\_min}}{V_{in\_max}/2} = 0.718$$

$$M_{g\_max} = \frac{n \cdot V_{0\_max}}{V_{in\_min}/2} = 1.646$$

Maximum and minimum gains are obtained with the circuit requirements (V_{in} and V_{out}) and the transformer turn ratio.

- **Select Ln and Qe**

$L_n = 2$ is considered an optimal value for applications with no load condition and with M_{g_max}, Q_e is obtained (Figure 3.1).

$$Q_e = 0.57$$

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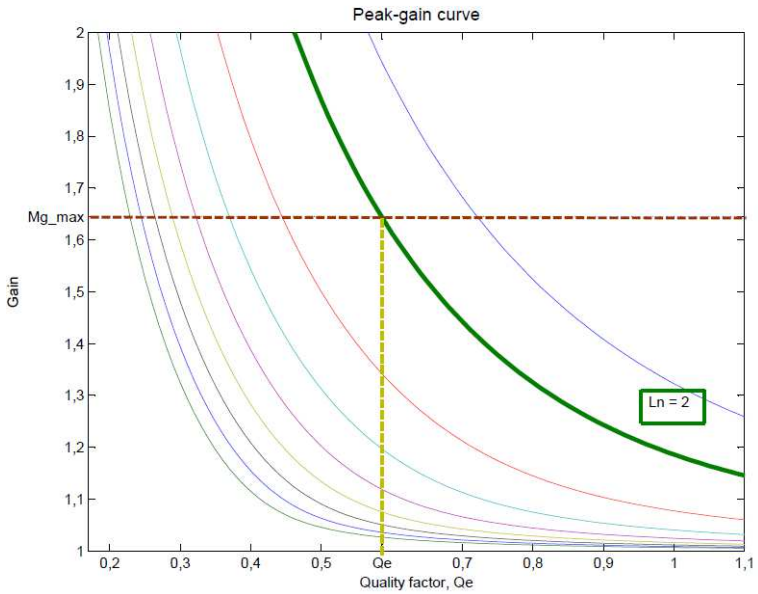

Figure 3.1 Peak-gain curve for Ln = 2

Properly behavior at no load working condition ($Q_e = 0$) is checked in Figure 3.2. The gain curve (blue) achieves M_{g_min} (red) around $f_n = 1.8$ and the no load working condition is guaranteed with a reasonable frequency value.

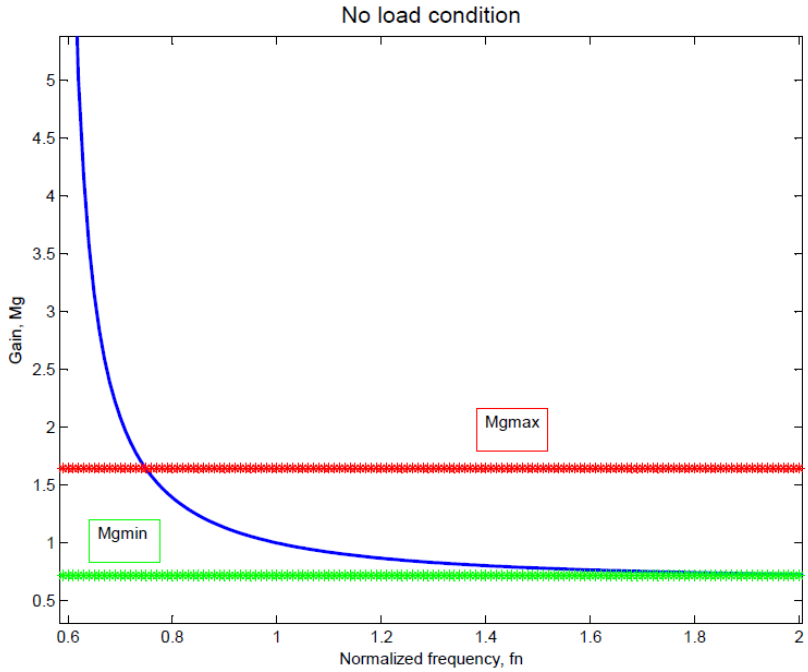

Figure 3.2 No load condition for Ln = 2

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- **Determine the equivalent load resistance (Re) at full load**

Determine the equivalent load resistance (R_e) at full load

$$R_e = \frac{8 \cdot n^2}{\pi^2} \cdot \frac{V_0}{I_0} = 12.65\ \Omega$$

- **Design resonant circuit's parameter**

$$C_r = \frac{1}{2 \cdot \pi \cdot Q_e \cdot f_0 \cdot R_e} = 184\ \text{nF}$$

$$L_r = \frac{1}{(2 \cdot \pi \cdot f_0)^2 \cdot C_r} = 9.6\ \mu\text{H}$$

$$L_m = L_n \cdot L_r = 19.2\ \mu\text{H}$$

Resonant parameters are calculated here, but the designed working zone needs to be checked.

- **Verify the resonant-circuit design**

In the proposed LLC converter, input-voltage varies between 240 and 550 V for a constant 14.4 V output, with a variable frequency (f_{n_min}, f_{n_max}). Maximum and minimum M_g values have been calculated in the previous steps.

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}} = 120\ \text{kHz}$$

$$L_n = \frac{L_m}{L_r} = 2$$

$$Q_e = \frac{\sqrt{L_r / C_r}}{R_e} = 0.571$$

Working zone plotted in Figure 3.3 shows that ZVS condition is guaranteed and the values are within limits.

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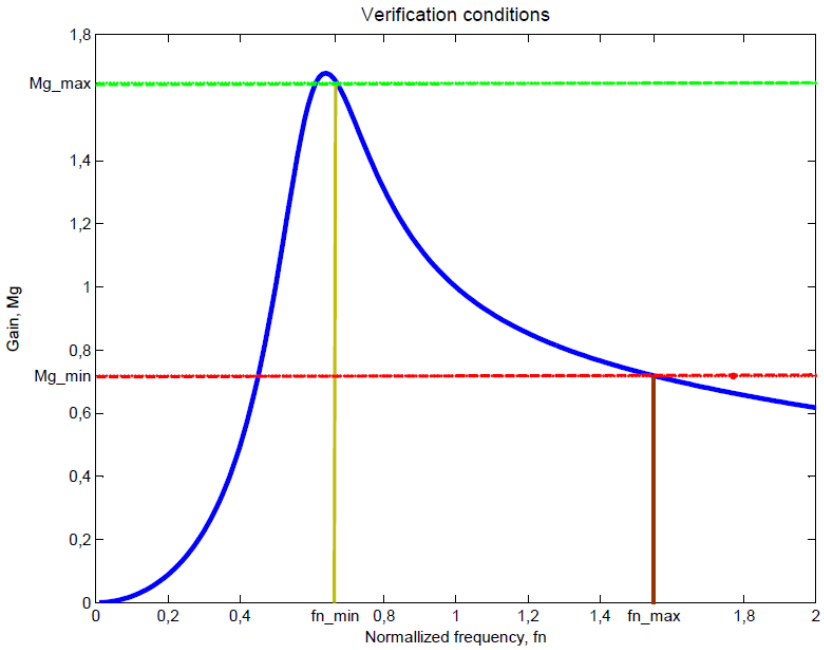

Figure 3.3 Verification of resonant-circuit design conditions

The frequency at no load (at M_{g_min}) is $f_{n\_max} \cdot f_0 = 120 \cdot 1.55 = 186$ kHz

The frequency at full load (at M_{g_max}) is $f_{n\_min} \cdot f_0 = 120 \cdot 0.67 = 80.4$ kHz

F_{n_max} and f_{n_min} give the frequency limits for the converter.

- **Dead time**

$$t_{dead} \geq n \cdot C_{eq} \cdot f_{sw} \cdot L_m = 221 \text{ ns}$$

A minimum dead time needs to be defined to avoid short-circuits and to assure ZVS.

For more information about LLC designing process consult Annex 1.

3.1.2 Simulation analysis and evaluation

For designing an LLC resonant half-bridge converter it is strongly recommended to use a computer simulation method. In this case, ANSYS Simplorer software is used for all the simulations in this project. In this section ZVS condition, resonant tank response, output

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response and no load condition are presented to prove the designing.

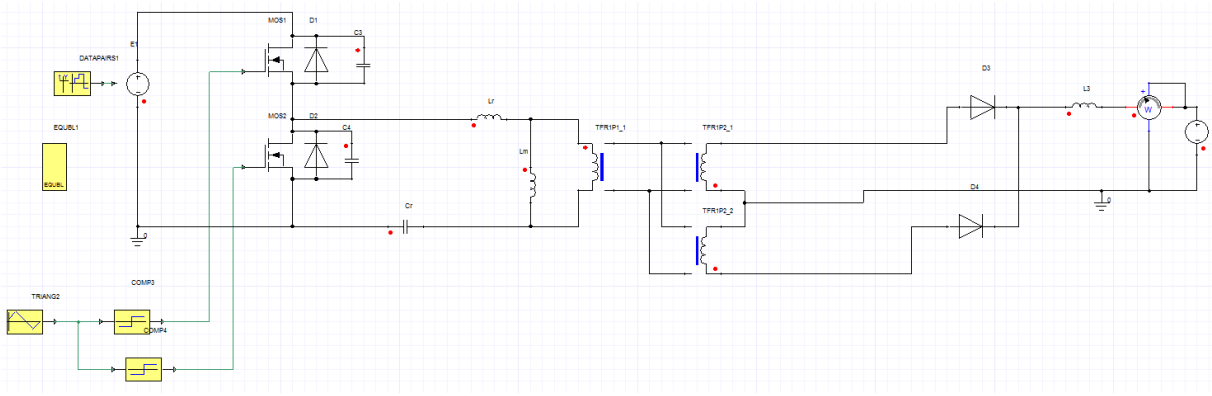

Figure 3.4 Simulated Half-Bridge LLC Resonant Converter

3.1.2.1ZVS condition

In this point, ZVS condition will be shown when the converter works at maximum input voltage, 550V.

As it is seen in Figure 3.5 and Figure 3.6, ZVS condition is achieved for both MOSFETs. When MOSFET starts to flow the current (purple), it does not see any voltage (blue), otherwise Diode is flowing the current (red). During the switching off, a progressive increasing of the voltage in MOSFET is produced.

- S1

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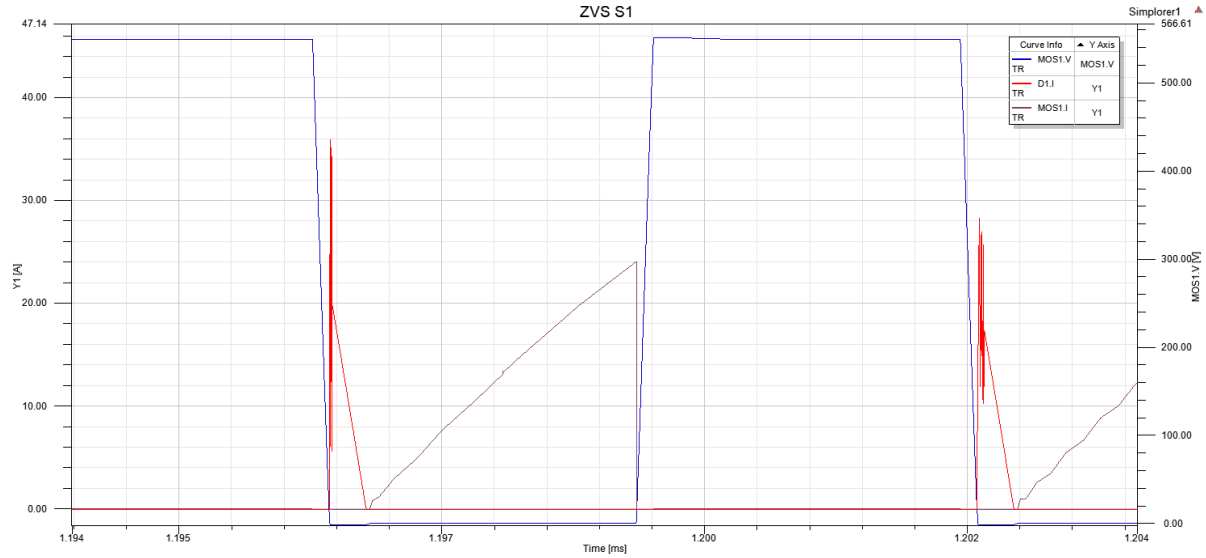

Figure 3.5 MOSFET voltage, diode current ands MOSFET current of S1

- S2

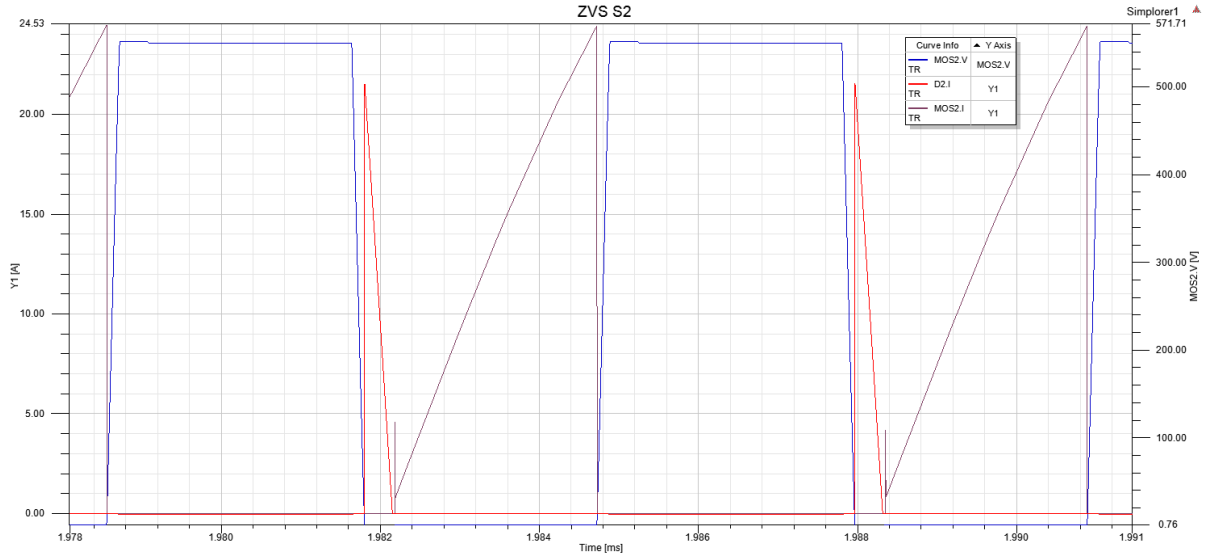

Figure 3.6 MOSFET voltage, diode current ands MOSFET current of S2

3.1.2.2Resonant tank response

Resonant tank current is shown in Figure 3.7 and Figure 3.8 to show soft flowing of the current in the resonant tank.

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- **550 V**

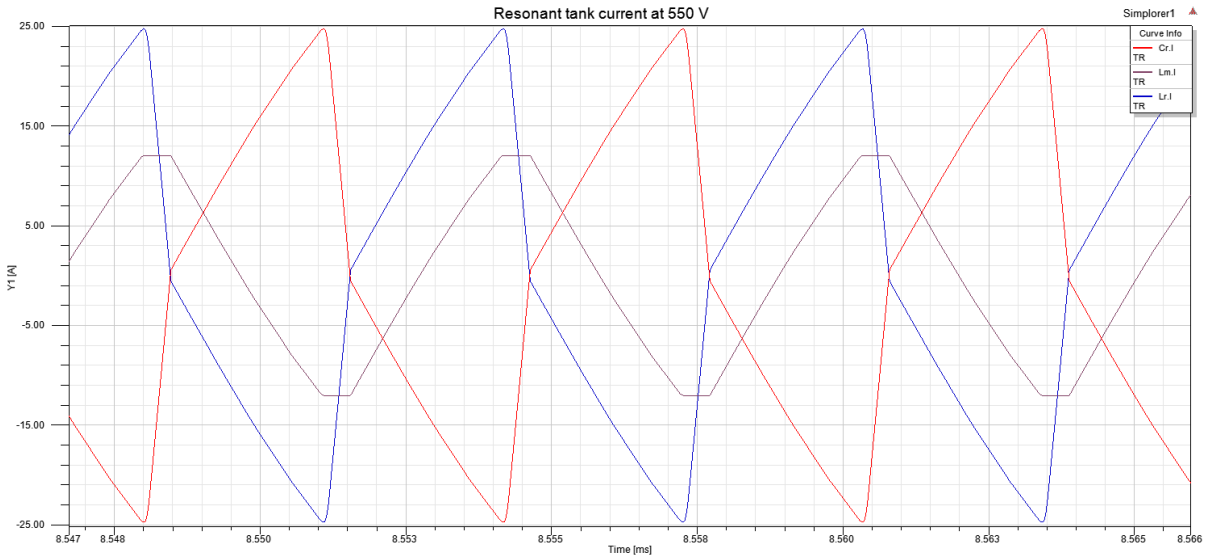

Figure 3.7 Resonant tank current at 550 V

- **240 V**

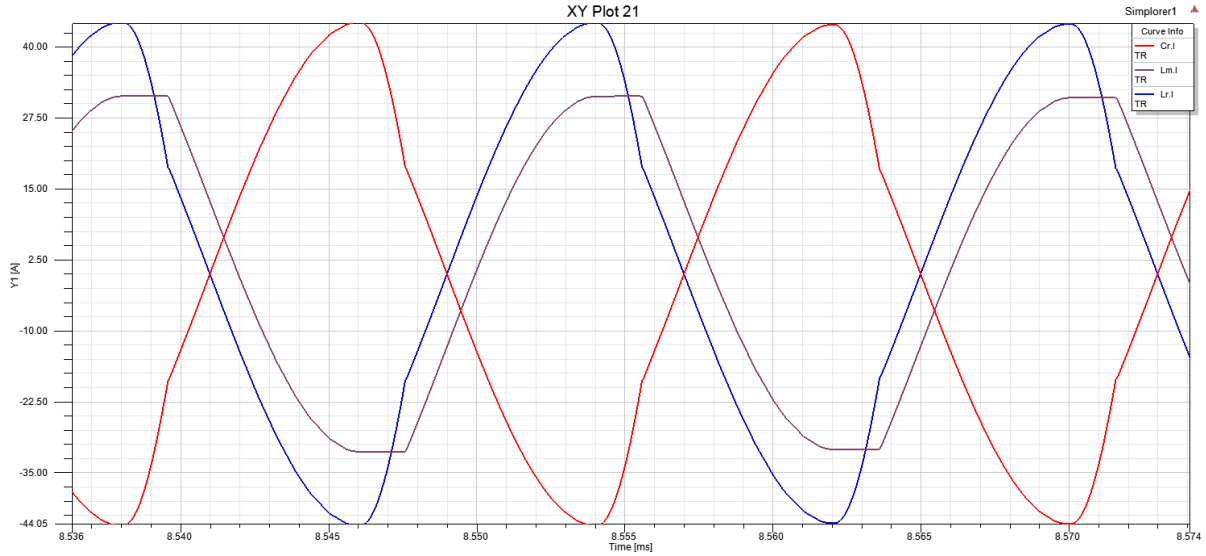

Figure 3.8 Resonant tank current at 240 V

The current in the resonant tank is higher for the minimum input voltage. Same as in the MOSFETs.

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3.1.2.3 LLC converter response

In Figure 3.9 is possible to see how the converter controls the output-power (purple) when an input voltage (red) variation between the maximum and the minimum values (and some intermediate values) is produced. In Figure 3.10 a sweep of whole input voltage is done between 240 V and 550 V.

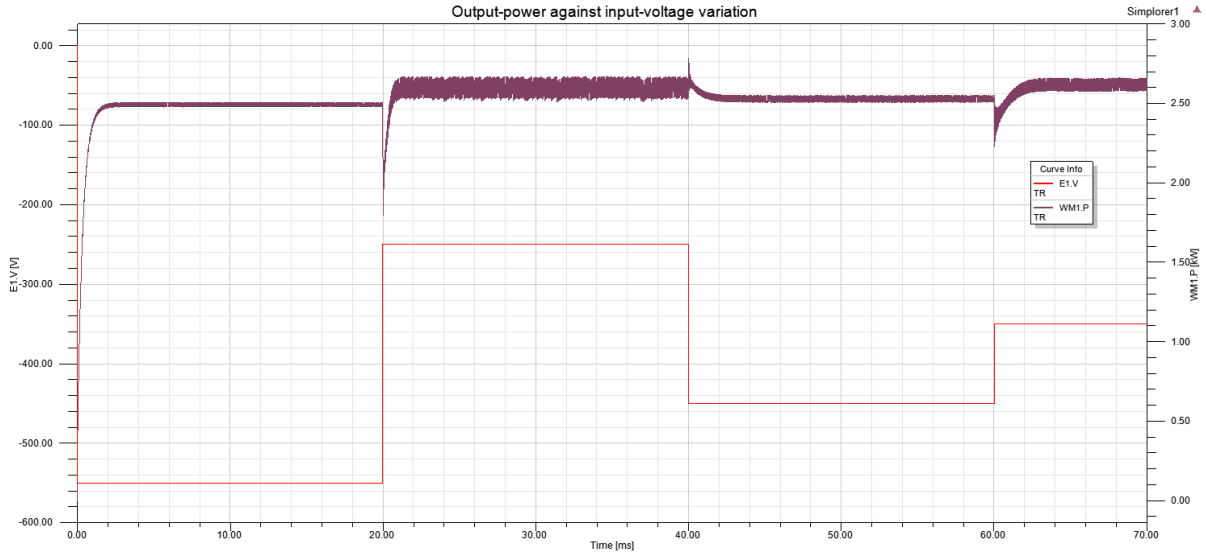

Figure 3.9 Output-power response against input-voltage variation

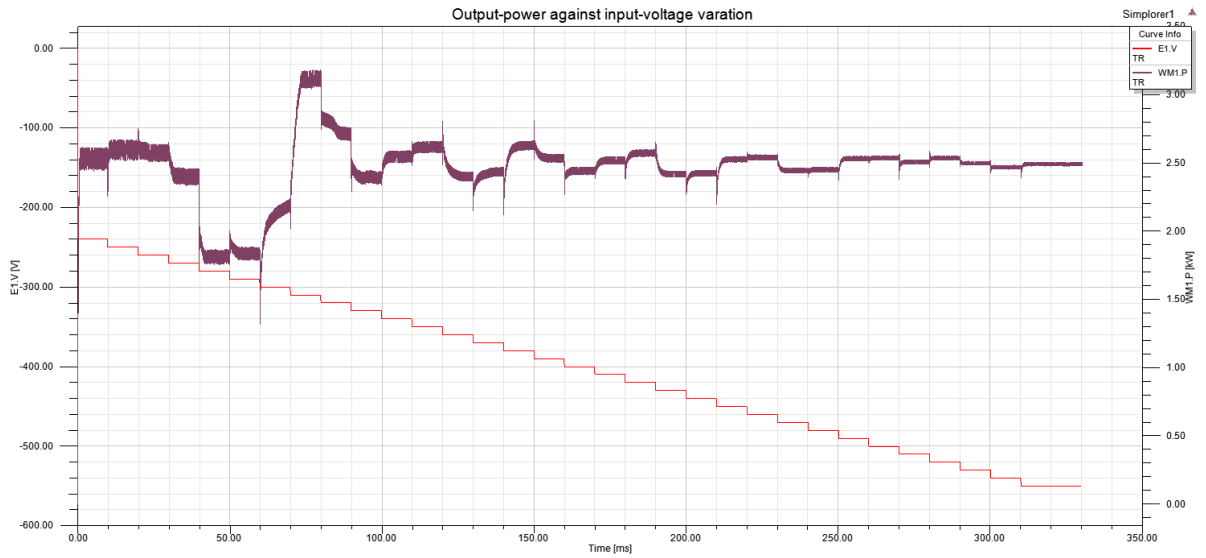

Figure 3.10 Output-power response against input-voltage variation

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Simulated converter responses against input-voltage variation through a feed-forward control, using a look-up table previously obtained. It causes that the converter spends a little time re-controlling the output power. A close-control can be a solution to avoid it.

To make clearer that the required output power is achieved, an output filter is used. Analyzing Figure 3.10, some values from the table are not good obtained since the output power (purple) does not give the expected values between 30 – 90 ms.

3.1.3 Converter response against 10% load

ZVS is an essential property, for this reason a method to guarantee ZVS at 10% load is presented.

For some applications it is essential to work in different load conditions, such as an auxiliary power supply. Work with 10% load changes conditions

$$R_e(10\%\ \text{load}) = \frac{8 \cdot n^2}{\pi^2} \cdot \frac{V_0}{I_0} \cdot 10 = 126.5\ \Omega$$

$$Q_e(10\%\ \text{load}) = \frac{\sqrt{L_r/C_r}}{R_e \cdot 10} = 0.0323$$

For high input voltage and low load conditions a proper response for the converter is more difficult. Figure 3.11 shows how the converter (L_n = 3) cannot response properly at 10% load condition because f_{n_max} would be too higher.

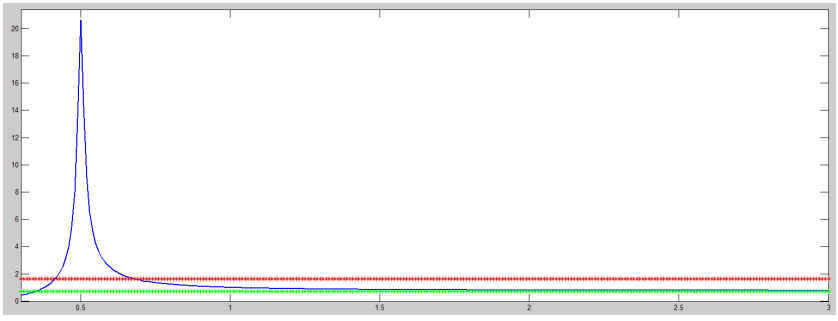

Figure 3.11 Converter response under 10% load condition

A new designing step is proposed here to guarantee a proper behavior. (8) calculates M_{g_min}

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value for a fixed V_{in}, V_o and n. Fixing a higher M_{g_min} and changing transformer turn ratio (n) allows the converter to work with the same input and output voltage. New values are obtained

$$M_{g\_min} = \frac{n \cdot V_{0\_min}}{V_{in\_max}/2} = 0.9$$

$$M_{g\_max} = \frac{n \cdot V_{0\_max}}{V_{in\_min}/2} = 2.07$$

$$n = 17.187$$

$L_n = 3$ is considered an optimal value and with M_{g_max}, Q_e is obtained.

$$Q_e = 0.33$$

Working zone plotted in Figure 3.12 shows that ZVS condition is guaranteed and the values are within limits.

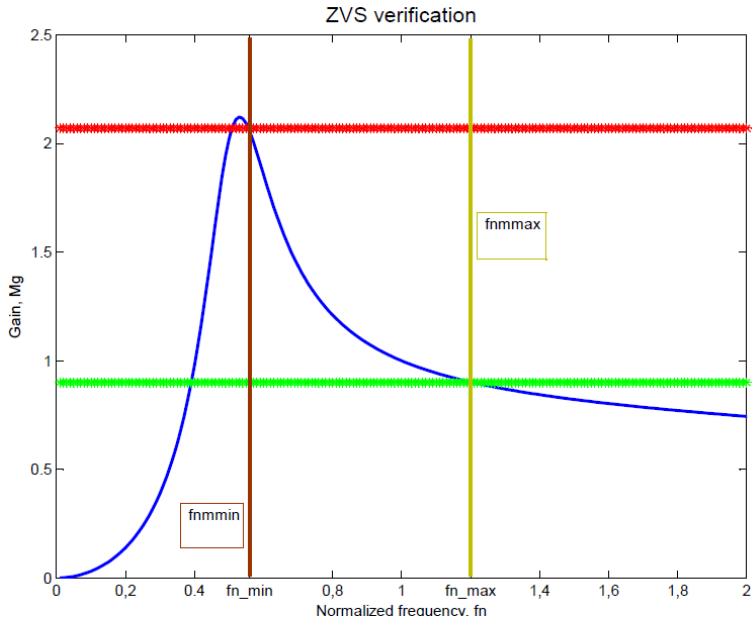

Figure 3.12 Verification of resonant-circuit design conditions

The frequency at no load (at M_{g_min}) is $f_{n\_max} \cdot f_0 = 120 \cdot 1.2 = 144$ kHz

The frequency at full load (at M_{g_max}) is $f_{n\_min} \cdot f_0 = 120 \cdot 0.56 = 67.2$ kHz

Converter's response at 10% load condition is verified in Figure 3.13 and an acceptable value of f_{n_max} is obtained. New resonant circuit's parameters are calculated

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$$C_r = \frac{1}{2 \cdot \pi \cdot Q_e \cdot f_0 \cdot R_e} = 202 \text{ nF}$$

$$L_r = \frac{1}{(2 \cdot \pi \cdot f_0)^2 \cdot C_r} = 8.7 \text{ µH}$$

$$L_m = L_n \cdot L_r = 26.1 \text{ µH}$$

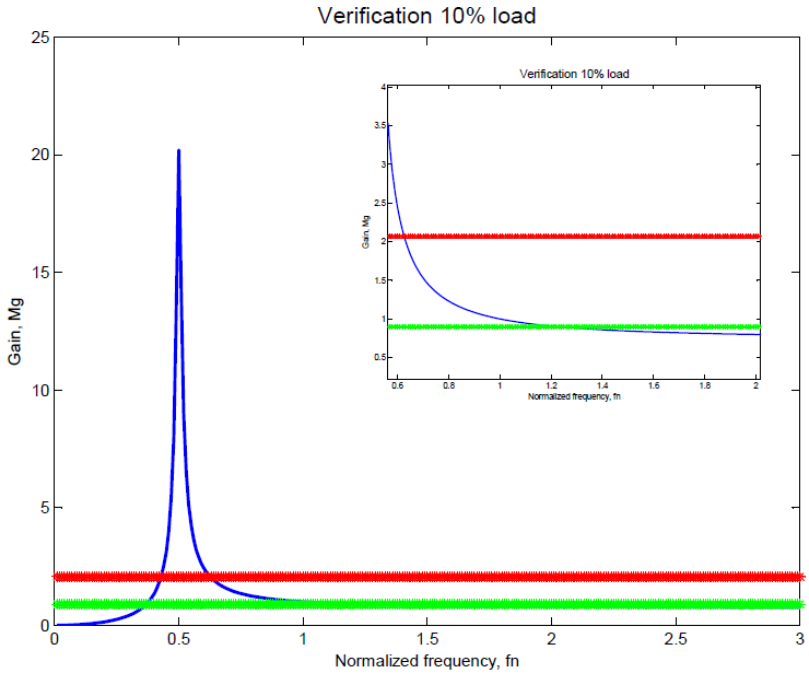

Figure 3.13 Converter response under 10% load condition (with zoom)

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3.2 GALVANIC INSULATION FOR STANDARD EV ONBOARD CHARGER RESONANT CONVERTER

Two resonant converters with an output power of 3600 W, which can be employed for an EV onboard charger, are designed here. The first converter has an output voltage range of 240 – 400 V within an input voltage of 360 V. The second resonant converter has an output voltage range of 360 – 530 V within an input voltage of 360 – 380 V.

3.2.1 Model 1

As seen in the requirements, Model 1 has fixed input voltage and variable output voltage between 240 – 400 V. No load condition is not required for Model 1.

3.2.1.1Design steps

The specifications and main parameters of the converter are:

- P_0: 3600 W
- V_{in}: 360 V
- V_{out}: 240 - 400 V
- I_0: 11.25 A
- f_{sw}: 150 kHz

With the required specifications, the design process is carried out:

- **Determine transformer turns ratio**

$$n = M_g \cdot \frac{V_{in}/2}{V_{0\_nom}} = 0.56$$

M_g = 1 is assumed to calculate the transformer turn ratio.

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- **Determine M_{g_min} and M_{g_max}**

$$M_{g\_min} = \frac{n \cdot V_{0\_min}}{V_{in}/2} = 0.75$$

$$M_{g\_max} = \frac{n \cdot V_{0\_max}}{V_{in}/2} = 1.25$$

Input voltage is always 360 V and the gains only vary depending on the output voltage.

- **Select Ln and Qe**

No load condition is not required for Model 1 and $L_n = 5$ is considered an optimal value for applications without no load requirements. Q_e is obtained with M_{g_max}.

$$Q_e = 0.465$$

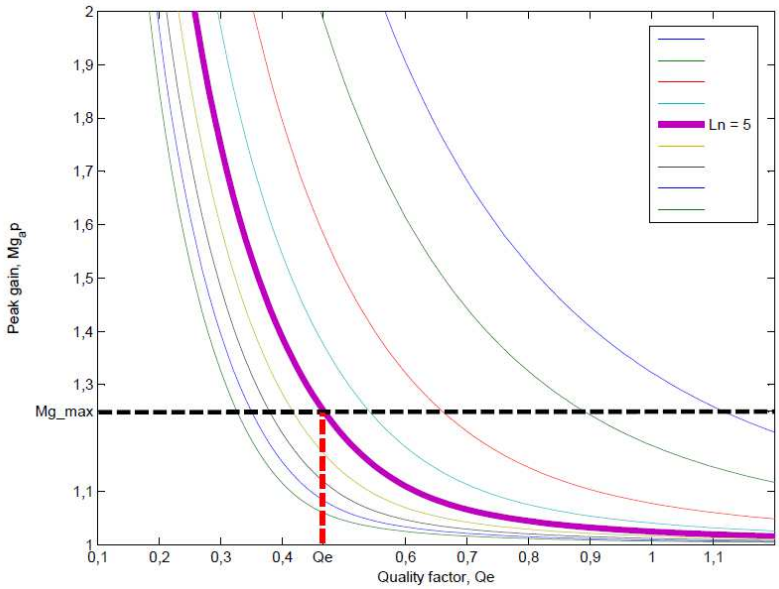

Figure 3.14 Peak-gain curve for Ln = 5

- **Determine the equivalent load resistance (Re)**

$$R_e = \frac{8 \cdot n^2}{\pi^2} \cdot \frac{V_0}{I_0} = 7.3\ \Omega$$

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- **Design resonant circuit's parameter**

$$C_r = \frac{1}{2 \cdot \pi \cdot Q_e \cdot f_0 \cdot R_e} = 312 \text{ nF}$$

$$L_r = \frac{1}{(2 \cdot \pi \cdot f_0)^2 \cdot C_r} = 3.6 \text{ µH}$$

$$L_m = L_n \cdot L_r = 18 \text{ µH}$$

Theoretical values of the resonant parameters are used.

- **Verify the resonant-circuit design**

Assumed values are recalculated through equations.

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}} = 150 \text{ kHz}$$

$$L_n = \frac{L_m}{L_r} = 5$$

$$Q_e = \frac{\sqrt{L_r/C_r}}{R_e} = 0.465 \text{ (at full load)}$$

These values are the same because theoretical values for the resonant parameters are used. Working zone plotted in Figure 3.15 shows that ZVS condition is guaranteed and the values are between limits.

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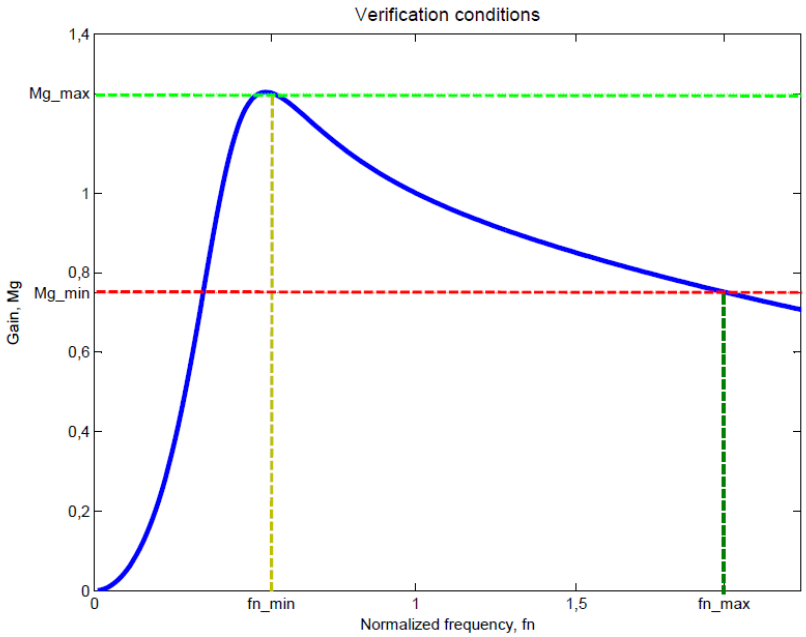

Figure 3.15 Verification of resonant-circuit design conditions

Frequency at no load (at M_{g_min}) is $f_{n\_max} \cdot f_0 = 150 \cdot 1.96 = 294$ kHz

Frequency at full load (at M_{g_max}) is $f_{n\_min} \cdot f_0 = 150 \cdot 0.55 = 82.5$ kHz

The frequency limits for the converter are distinct by f_{n_max} and f_{n_min}.

- **Dead time**

$$t_{dead} \geq n \cdot C_{eq} \cdot f_{sw} \cdot L_m = 10.6\, ns$$

A minimum dead time needs to be defined to avoid short-circuits and to assure ZVS.

For more information about LLC designing process consult Annex 1.

3.2.1.2 Simulation analysis and evaluation

As in previous chapter, ANSYS Simplorer software is used for the simulation. ZVS condition, resonant tank response and output response are shown in this chapter to demonstrate the designing process.

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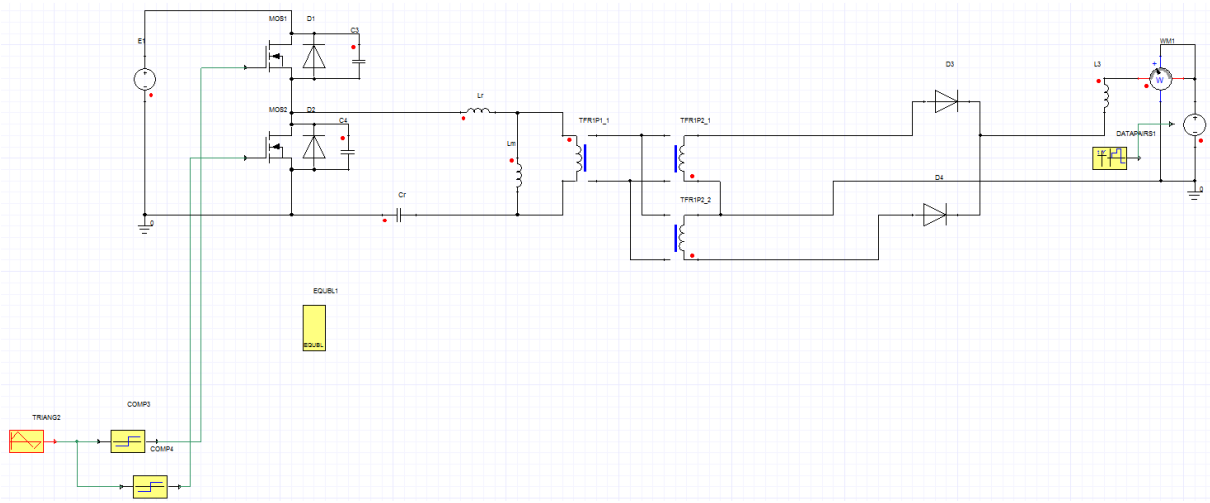

Figure 3.16 Simulated Half-Bridge LLC Resonant Converter

3.2.1.2.1 ZVS condition

ZVS condition will be shown in both limits of the frequency range in this point.

- **400 V**

Current diodes, MOSFETs voltage and current are shown in Figure 3.17 and Figure 3.18 for maximum output voltage (400 V) in S1 and S2.

o S1

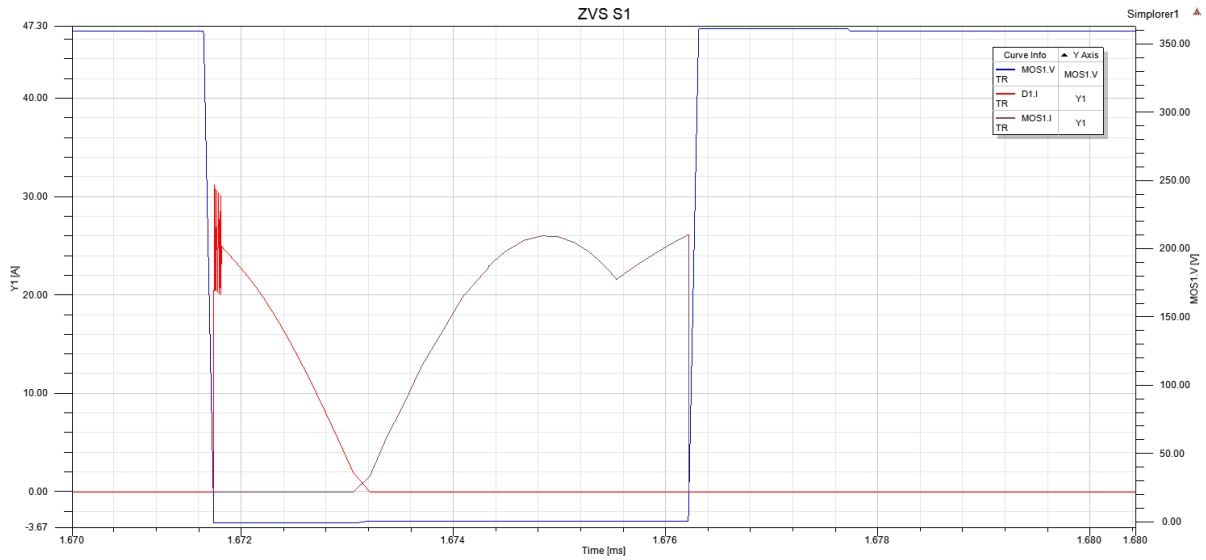

Figure 3.17 MOSFET voltage, diode current ands MOSFET current of S1 at 400V

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- S2

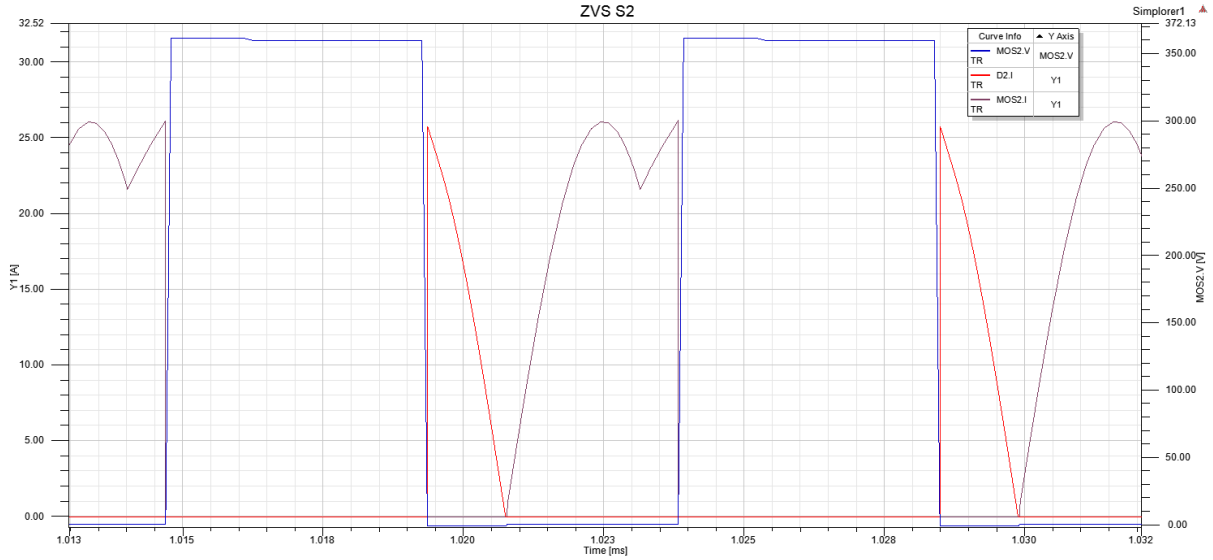

Figure 3.18 MOSFET voltage, diode current ands MOSFET current of S2 at 400V

- **240 V**

Current diodes, MOSFETs voltage and current are shown in Figure 3.17 and Figure 3.18 for minimum output voltage (240 V) in S1 and S2.

- S1

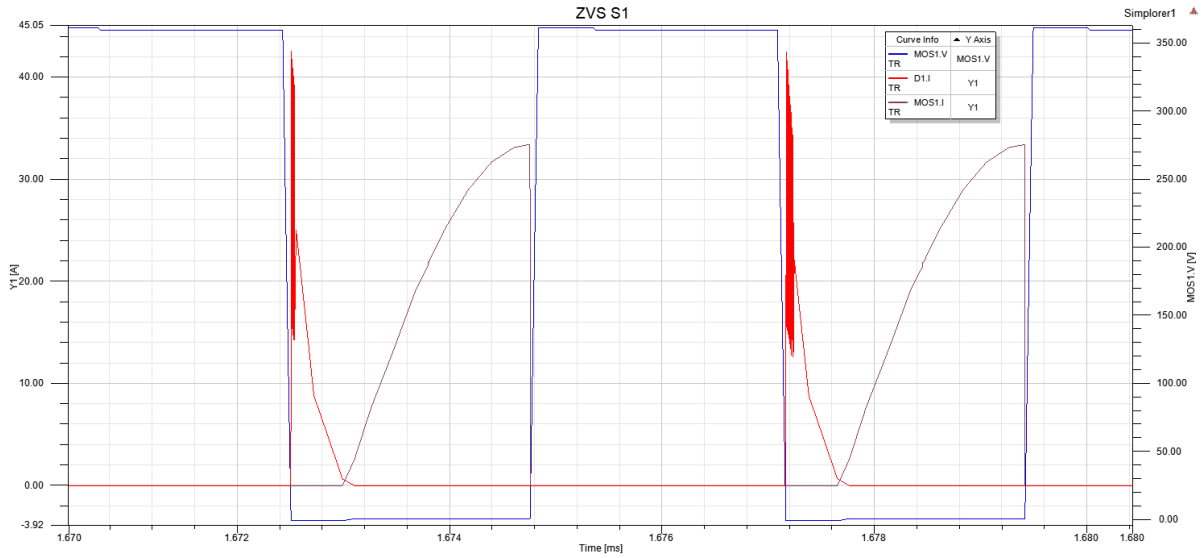

Figure 3.19 MOSFET voltage, diode current ands MOSFET current of S1 at 240V

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- S2

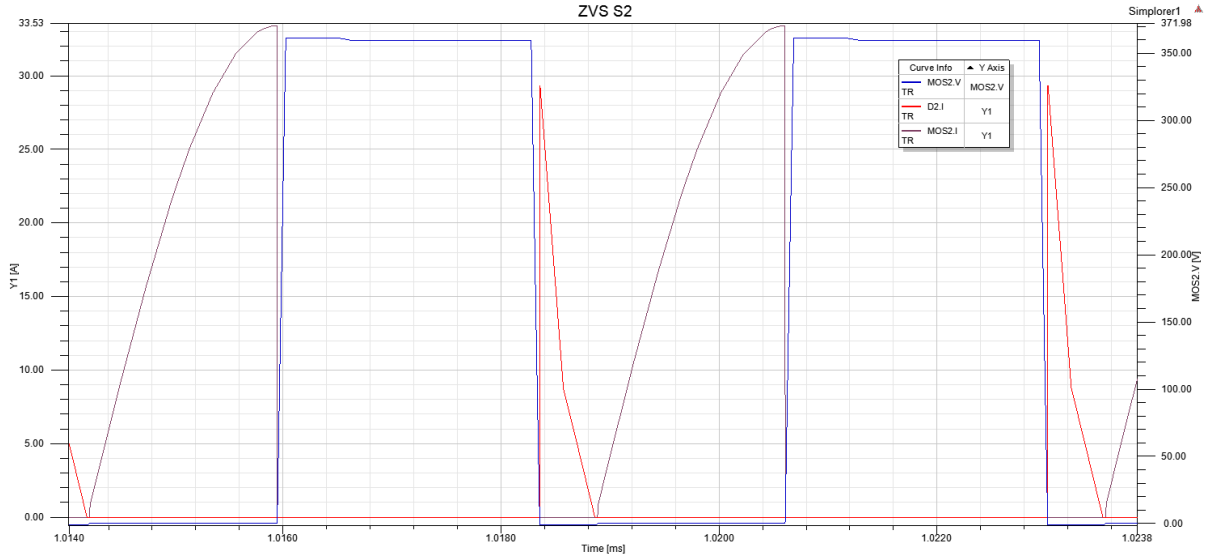

Figure 3.20 MOSFET voltage, diode current ands MOSFET current of S2 at 240V

In S1 for maximum and minimum voltage, the diodes flow some noisy current during the current peak. The simulation model should be studied detailed to propose a model which avoids this noise.

ZVS is achieved for both output voltage and for both MOSFETs.

3.2.1.2.2 Resonant tank response

Different tank waveforms are presented in Figure 3.21 and Figure 3.22 to show circuit's behavior under limits of the frequency range condition.

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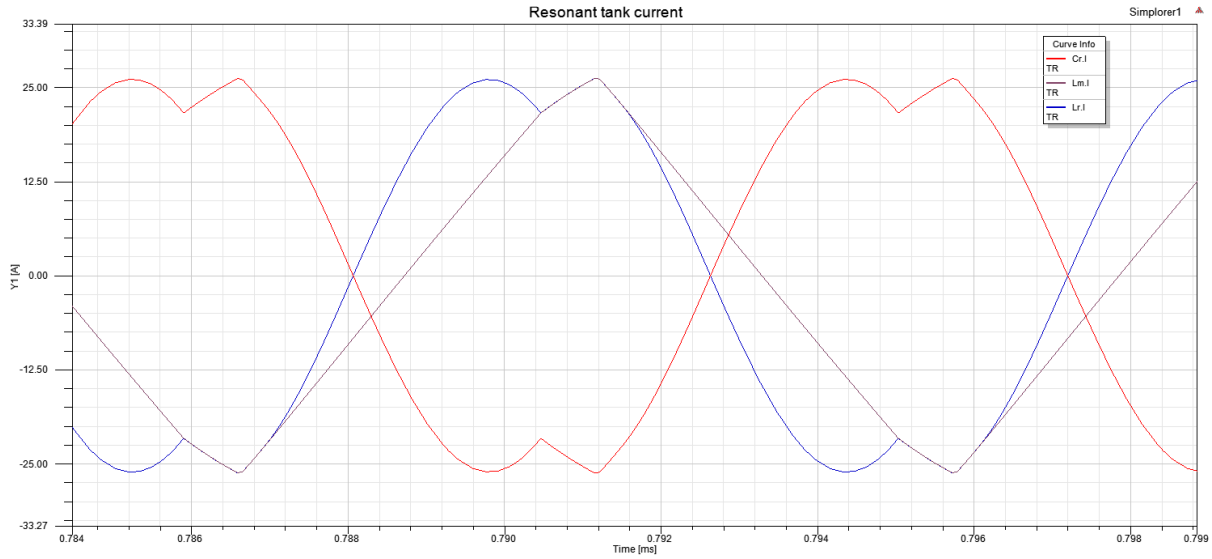

Figure 3.21 Resonant tank current at 400 V

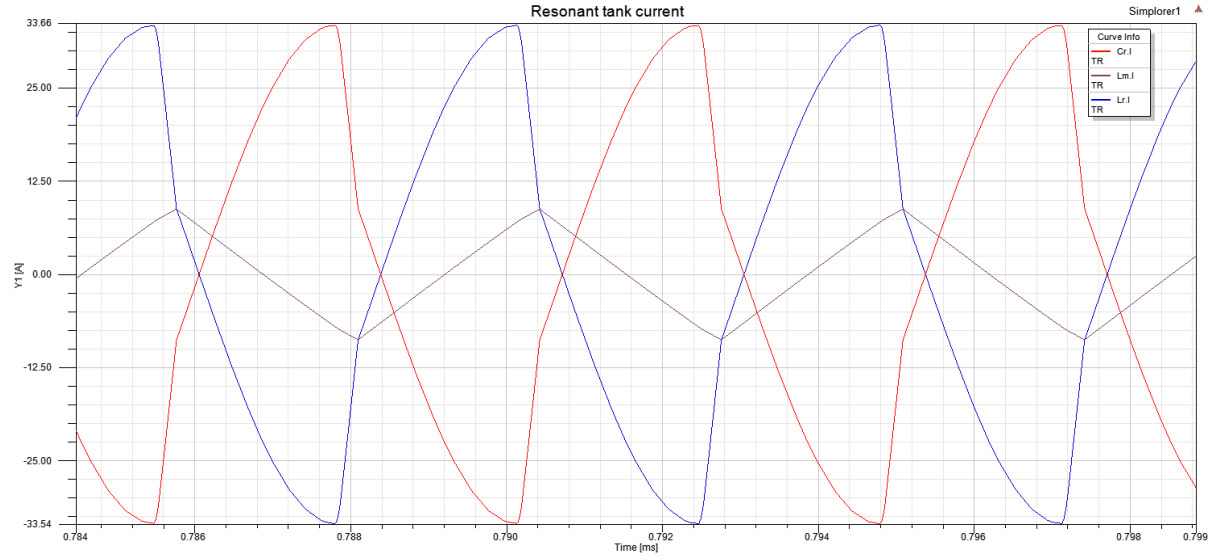

Figure 3.22 Resonant tank current at 240 V

It is seen how the current in the magnetizing inductance is higher for maximum output voltage (400 V). It means that the converter controls the current in the secondary side to keep the output power constant.

3.2.1.2.3 LLC converter response

Figure 3.23 shows how the converter controls the output-power (purple) when output-

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voltage (red) variation is produced. The output voltage varies between maximum (400 V) and minimum (240 V) values (and intermediates).

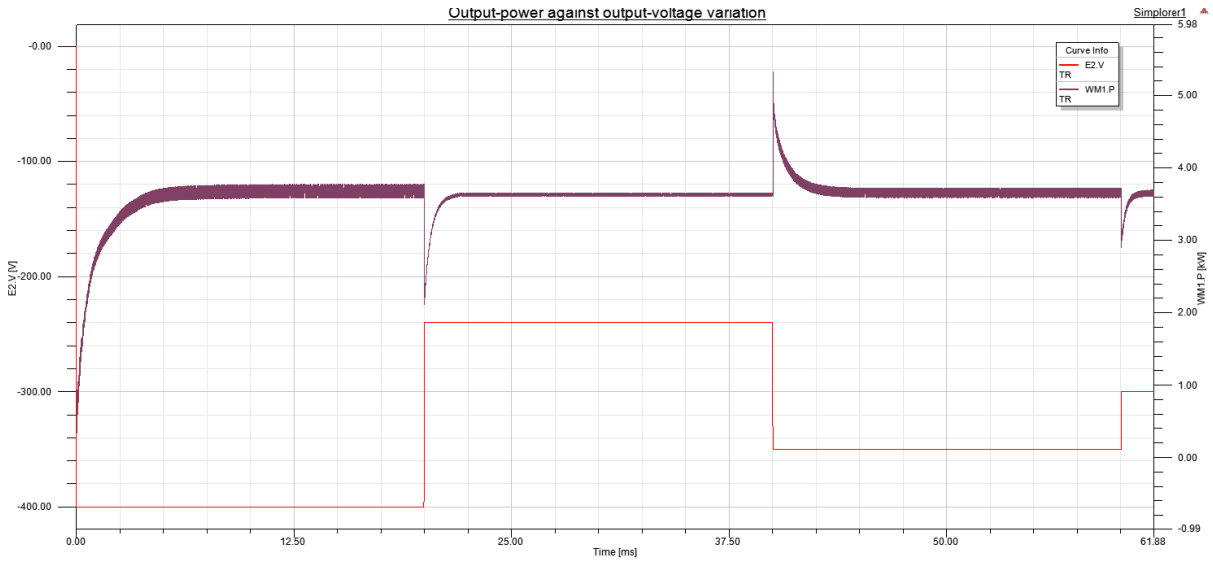

Figure 3.23 Output-power response against output-voltage variation

A feed-forward control using a look-up table previously obtained has been used to control the converter against the input-voltage variations. It causes that the converter spends a little time re-controlling the output power. A solution to avoid this could be a close-control.

To make clearer that the required output power is achieved, an output filter is used.

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3.2.2 Model 2

Model 2 is designed in half-bridge and full-bridge topologies, due to the currents in half-bridge topology are considered too high after having analyzed the simulation results. For hardware design, full-bridge topology currents are considered more suitable.

3.2.2.1 Design steps for Half-Bridge topology

Main parameters and specifications are listed here:.

- P_0: 3600 W
- V_{in}: 360 – 380 V
- V_{out}: 360 – 520 V
- I_0: 8.1 A
- f_{sw}: 150 kHz

With the required specifications, the design process is carried out:

- **Determine transformer turn ratio**

$$n = M_g \cdot \frac{V_{in\_nom}/2}{V_0} = 0.42$$

For transformer turns ratio calculation, $M_g = 1$ is used.

- **Determine M_{g_min} and M_{g_max}**

$$M_{g\_min} = \frac{n \cdot V_{0\_min}}{V_{in\_max}/2} = 0.7877$$

$$M_{g\_max} = \frac{n \cdot V_{0\_max}}{V_{in\_min}/2} = 1.224$$

In half-bridge Model 2 the gains vary depending on the output and the input voltage.

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- **Select Ln and Qe**

L_n = 2.5 (red) is considered an good value for applications with no load requirements. Entering with M_{g_max} (brown) in Figure 3.24, Q_e is obtained.

$$Q_e = 0.78$$

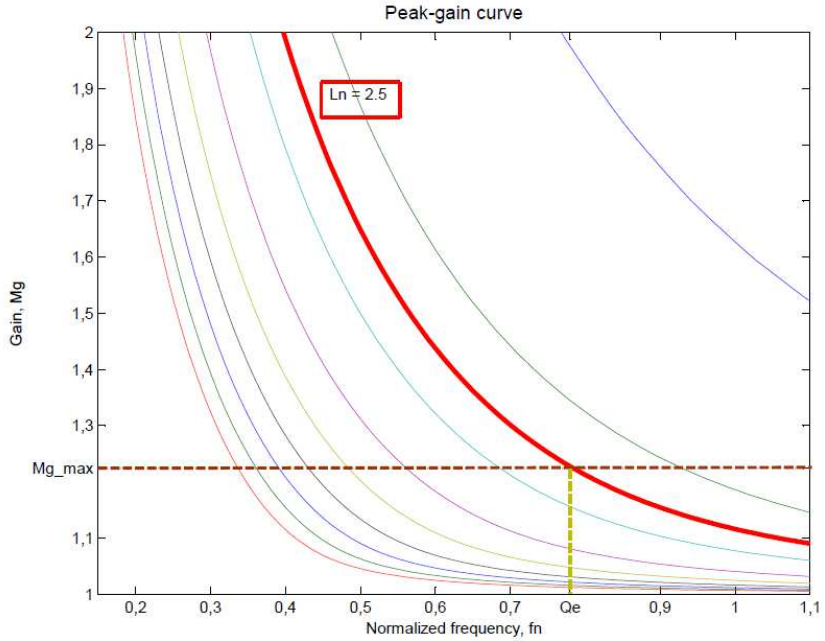

Figure 3.24 Peak-gain curve for Ln = 2.5

In Figure 3.25 no load (Q_e = 0) working condition is checked. The gain curve (blue) achieves M_{g_min} (red) around f_n = 1.7 and the no load working condition is guaranteed with a reasonable frequency value.

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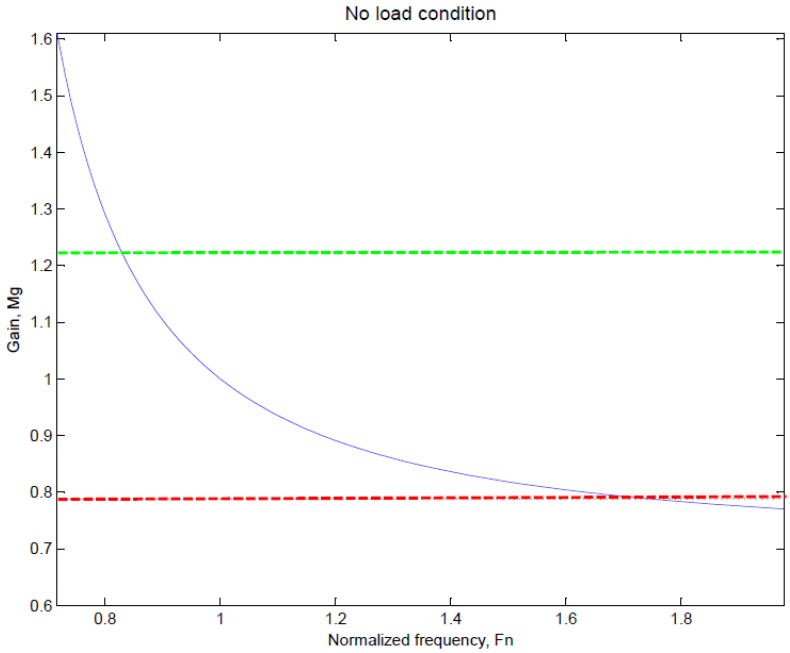

Figure 3.25 No load condition for Ln = 2.5

- **Determine the equivalent load resistance (Re) at full load**

$$R_e = \frac{8 \cdot n^2}{\pi^2} \cdot \frac{V_0}{I_0} = 7.706\ \Omega$$

- **Design resonant circuit's parameter**

$$C_r = \frac{1}{2 \cdot \pi \cdot Q_e \cdot f_0 \cdot R_e} = 176\ \text{nF}$$

$$L_r = \frac{1}{(2 \cdot \pi \cdot f_0)^2 \cdot C_r} = 6.4\ \mu\text{H}$$

$$L_m = L_n \cdot L_r = 16\ \mu\text{H}$$

Resonant parameters are calculated here for half-bridge topology.

- **Verify the resonant-circuit desig**

Assumed values are recalculated through equations:

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$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}} = 150 \text{ kHz}$$

$$L_n = \frac{L_m}{L_r} = 2.5$$

$$Q_e = \frac{\sqrt{L_r/C_r}}{R_e} = 0.782$$

Theoretical values for the resonant parameters are used and the recalculation is equal. Working zone plotted in Figure 3.26 shows that ZVS condition is guaranteed and the values are within limits.

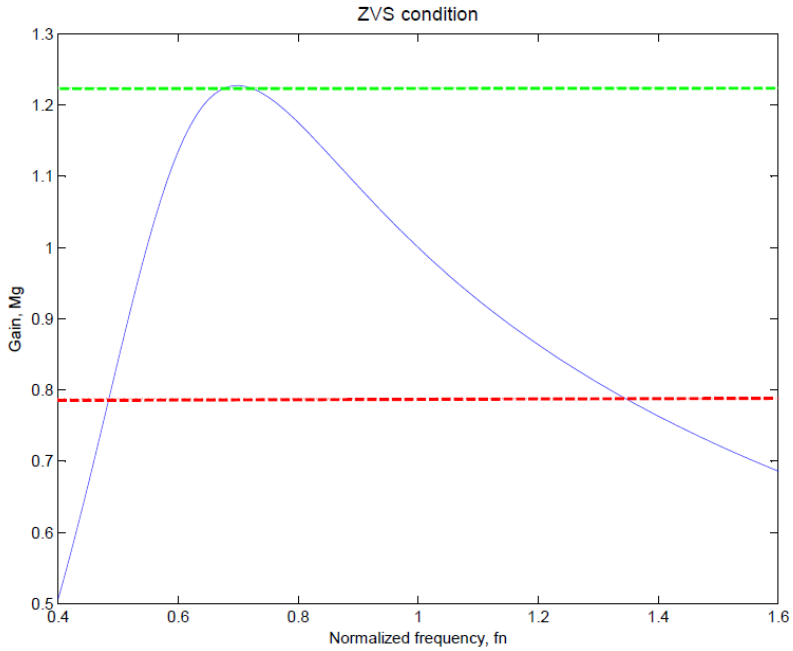

Figure 3.26 Verification of resonant-circuit design conditions

The frequency at no load (at M_{g_min}) is $f_{n\_max} \cdot f_0 = 150 \cdot 1.335 = 200.25$ kHz

The frequency at full load (at M_{g_max}) is $f_{n\_min} \cdot f_0 = 150 \cdot 0.725 = 108.75$ kHz

- **Dead time**

$$t_{dead} \geq n \cdot C_{eq} \cdot f_{sw} \cdot L_m = 13.6 \text{ ns}$$

A minimum dead time needs to be defined to avoid short-circuits and to assure ZVS.

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For more information about LLC designing process consult Annex 1.

3.2.2.2 Simulation analysis and evaluation of Half-Bridge topology

In this section ZVS condition, resonant tank response, output response and no load condition simulations (ANSYS Simplorer) are presented to prove the designing.

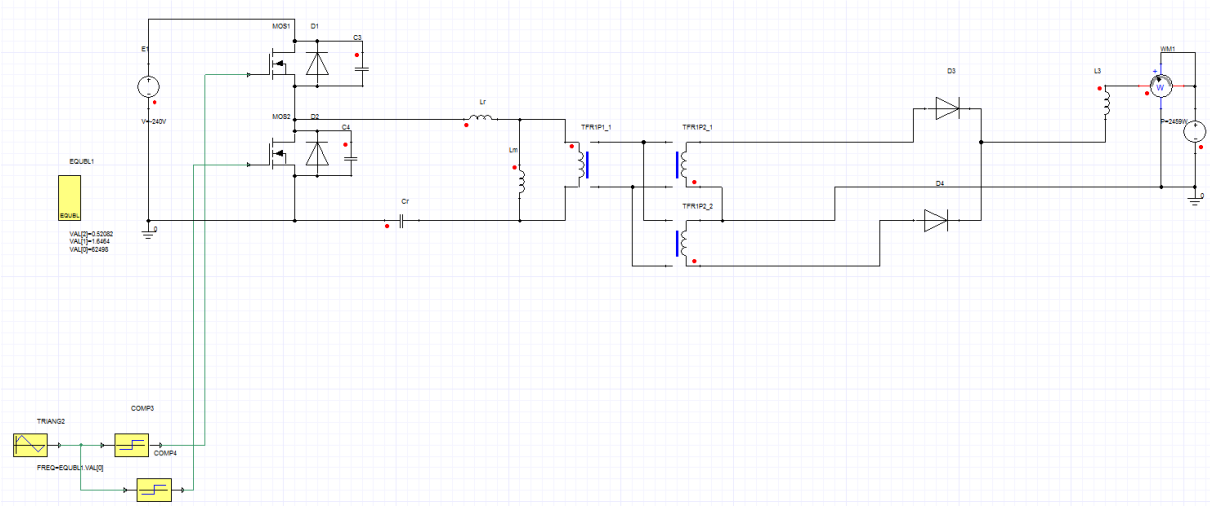

Figure 3.27 Simulated Half-Bridge LLC Resonant Converter

3.2.2.2.1 ZVS condition

Converter response is shown in both limits of the frequency range (V_{in} = 360 V – V_{out} = 360 V; V_{in} = 380 V – V_{out} = 520 V) to demonstrate ZVS.

- **520 V**

As seen in Figure 3.28 and Figure 3.29, ZVS condition is achieved for the MOSFET (S1) when the converter works at maximum output voltage, 520 V.

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- S1

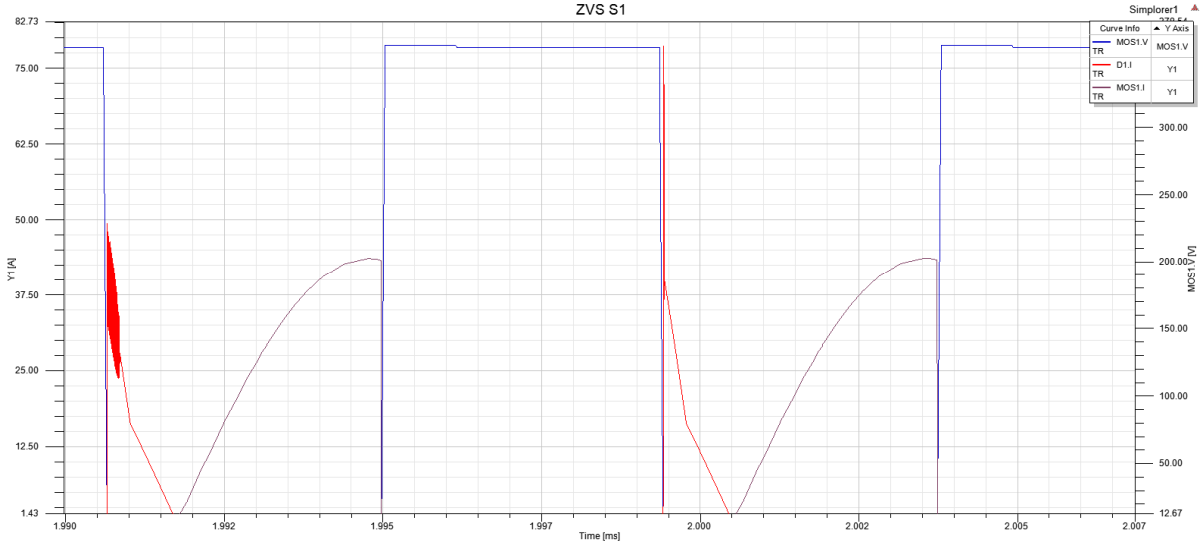

Figure 3.28 MOSFET voltage, diode current ands MOSFET current of S1 at 520V

- S2

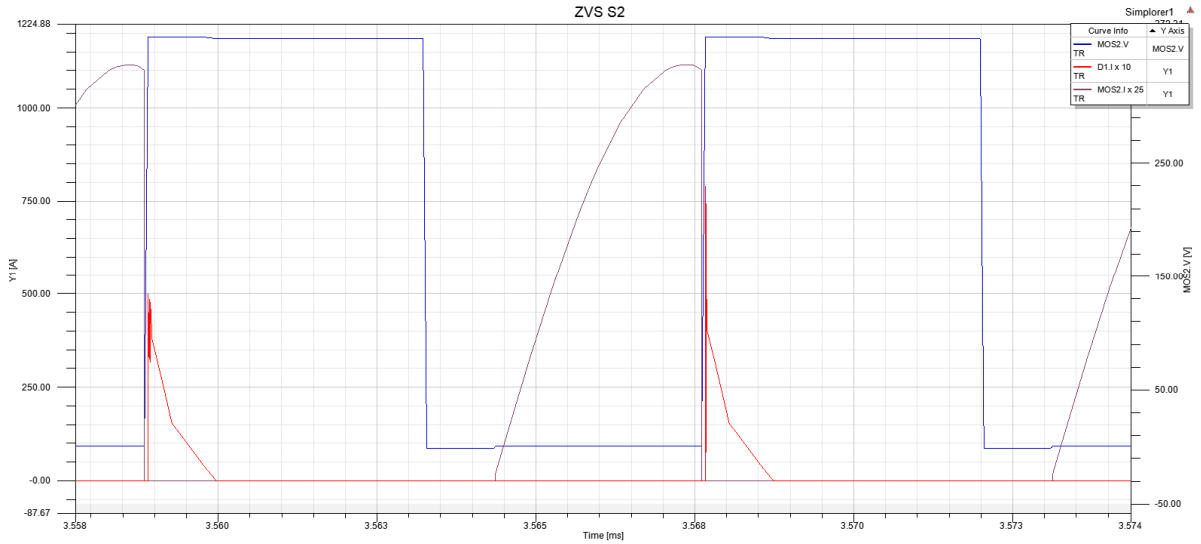

Figure 3.29 MOSFET voltage, diode current ands MOSFET current of S2 at 550V

- **360 V**

ZVS condition is achieved for the MOSFET (S2) when the converter works at minimum output voltage, 360 V (Figure 3.30 and Figure 3.31).

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- S1

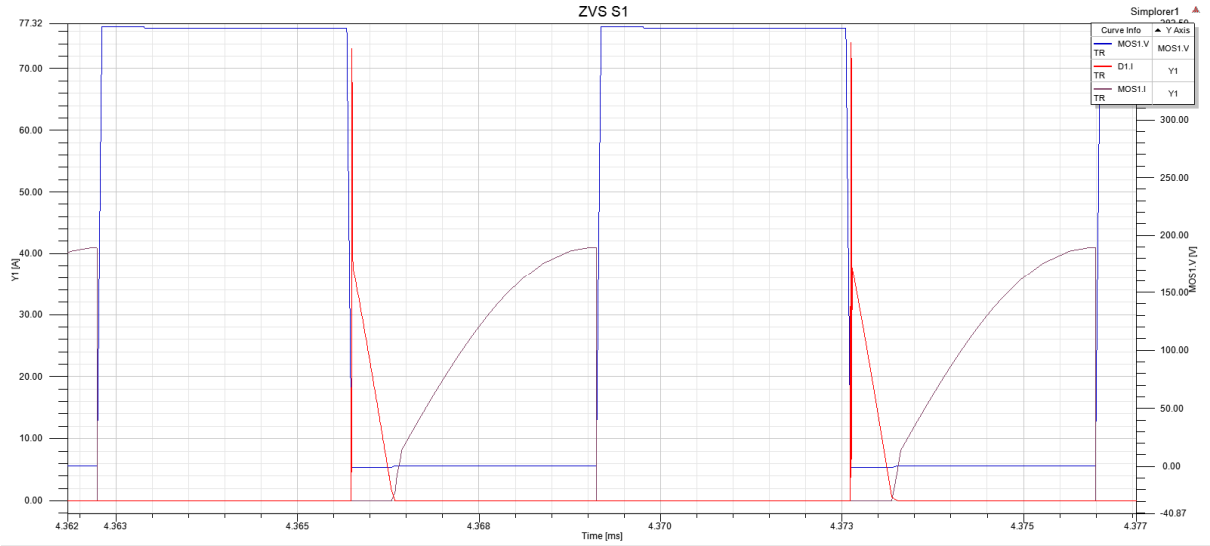

Figure 3.30 MOSFET voltage, diode current ands MOSFET current of S1 at 360V

- S2

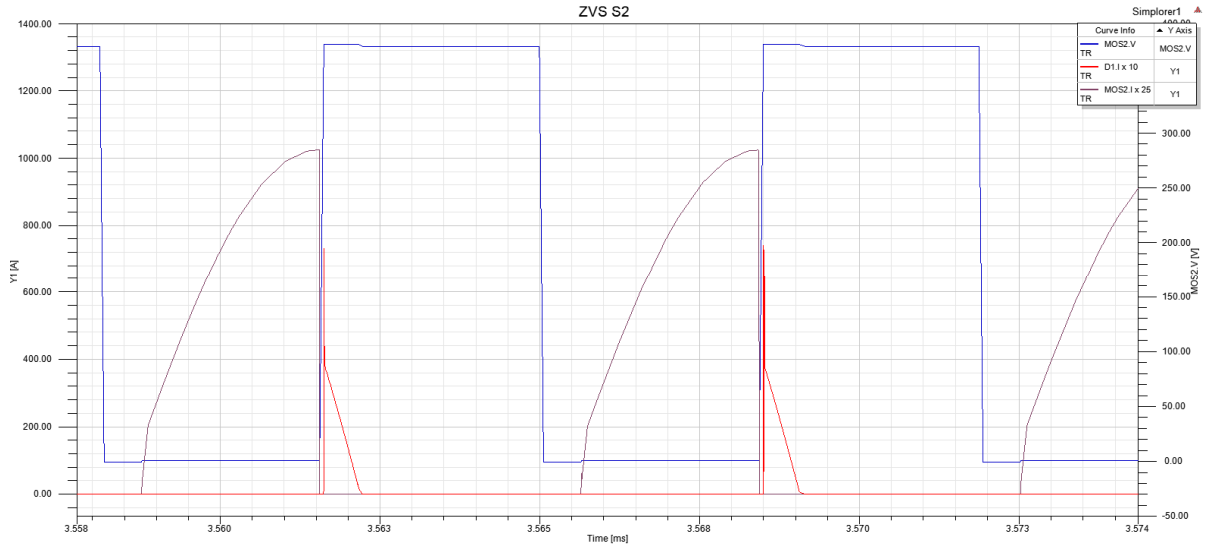

Figure 3.31 MOSFET voltage, diode current ands MOSFET current of S2 at 360V

Analyzing the converter response ZVS is achieved. However, as in other half-bridge LLC converter a noise is found in the diodes peak. The simulation model should be studied detailed to propose a model which avoids this noise.

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3.2.2.2.2 LLC converter response

The converter controls the output-power (green) when the input voltage (red) and output voltage (blue) variation is produced as seen in Figure 3.32.

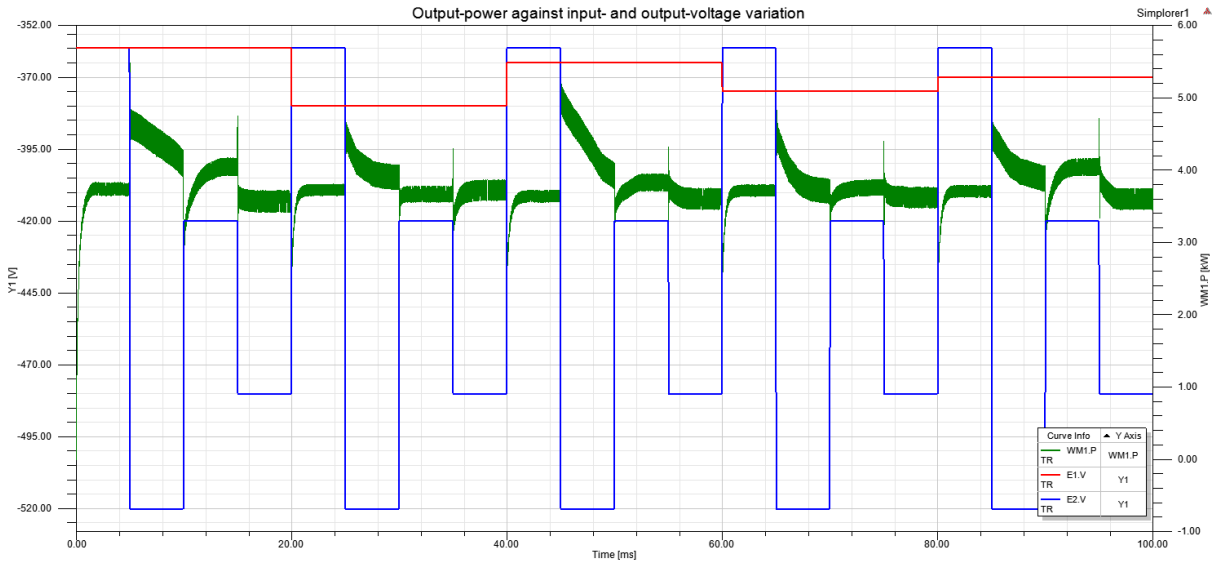

Figure 3.32 Output-power response against input/output-voltage variation

The step time for each variation is, in some cases, very short and the output power has not enough time to stabilize. Simulated converter responses against input-voltage variation through a feed-forward control, using a look-up table previously obtained. It causes that the converter spends time re-controlling the output power. A close-control can be a solution to avoid it. An output filter is used to make clearer that the required output power is achieved.

3.2.2.2.3 Zero load condition

For some applications is essential to work in zero load condition, such as an EV onboard charger. Theoretical no load response has been previously demonstrated and simulating response is demonstrated in Figure 3.33 and Figure 3.34 for maximum and minimum output-voltage. It is possible to see how the converter is capable to give all the output power range (purple) between zero and maximum output power. A frequency sweep (green) is used to vary the frequency.

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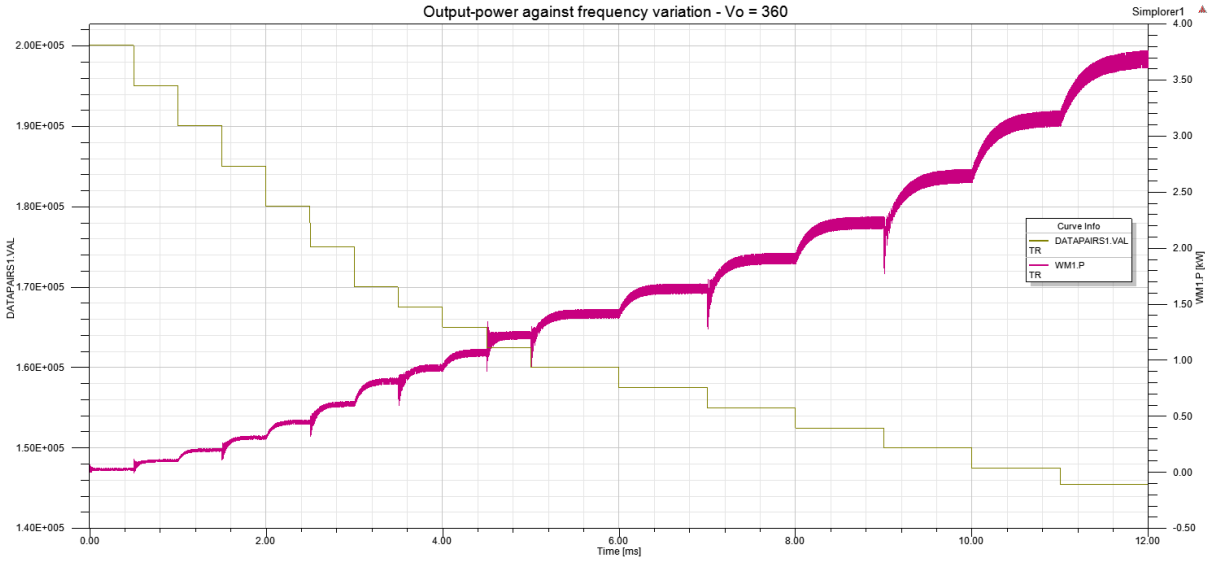

Figure 3.33 Output-power against frequency variation at Vo = 360 V

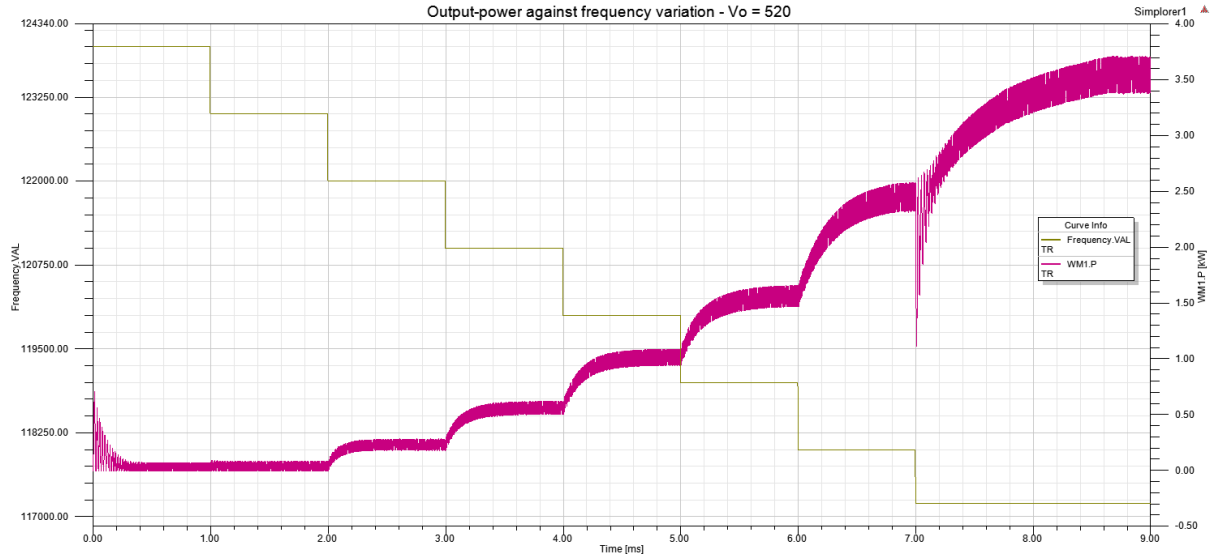

Figure 3.34 Output-power against frequency variation at Vo = 520 V

3.2.2.3 Design steps for Full-Bridge topology

After a detailed analysis of simulating MOSFETs response, the current is considered too high and a Full-Bridge topology is proposed.

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The specifications and main parameters are specified as follows.

- P_0: 3600 W
- V_{in}: 360 – 380 V
- V_{out}: 360 – 520 V
- I_0: 8.1 A
- f_{sw}: 150 kHz

With the required specifications, the design process is carried out:

- **Determine transformer turn ratio**

$$n = M_g \cdot \frac{V_{in\_nom}}{V_0} = 0.83$$

For transformer turns ratio calculation, M_g = 1 is used.

- **Determine M_{g_min} and M_{g_max}**

$$M_{g\_min} = \frac{n \cdot V_{0\_min}}{V_{in\_max}} = 0.786$$

$$M_{g\_max} = \frac{n \cdot V_{0\_max}}{V_{in\_min}} = 1.222$$

The gain formula for half-bridge is different from full-bridge topology, it is divided by 2. However, the values are the same for both because the transformer turn ratio is also divided by 2 in half-bridge topology.

- **Select Ln and Qe**

L_n = 2.5 is considered a good value for half-bridge and it is also used for full-bridge design.

$$Q_e = 0.78$$

Peak gain curve and no load condition are the same checking process and graphs than half-bridge design (no load and peak gain curve for half-bridge topology).

- **Determine the equivalent load resistance (Re) at full load**

$$R_e = \frac{8 \cdot n^2}{\pi^2} \cdot \frac{V_0}{I_0} = 30.716\ \Omega$$

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The transformer turns ratio is different for both topologies and the equivalent resistance is also different.

- **Design resonant circuit's parameter**

$$C_r = \frac{1}{2 \cdot \pi \cdot Q_e \cdot f_0 \cdot R_e} = 44.3\ \text{nF} \rightarrow 47\ \text{nF}$$

$$L_r = \frac{1}{(2 \cdot \pi \cdot f_0)^2 \cdot C_r} = 25.4\ \mu\text{H} \rightarrow 36.3\ \mu\text{H}$$

$$L_m = L_n \cdot L_r = 63.5\ \mu\text{H} \rightarrow 98.1\ \mu\text{H}$$

This design is used for hardware manufacture and the theoretical resonant parameters are not used because it is not possible to find a 44.3 nF capacitor. Normalized capacitor of 47 nF is used for the resonant capacitor. Most similar inductances values are obtained through the transformer design.

- **Verify the resonant-circuit desig**

With no theoretical resonant parameters the verification step is important to verify that the design is still suitable.

$$f_{n\_max} = \frac{1}{2\pi\sqrt{L_r C_r}} = 121.93\ \text{kHz}$$

$$f_{n\_min} = \frac{1}{2\pi\sqrt{(L_r + L_m) \cdot C_r}} = 63.33\ \text{kHz}$$

$$L_n = \frac{L_m}{L_r} = 2.707$$

$$Q_e = \frac{\sqrt{L_r/C_r}}{R_e} = 0.755$$

Values are very similar to the theoretical ones and the working zone plotted in Figure 3.35 shows that ZVS condition is guaranteed and the values are within limits.

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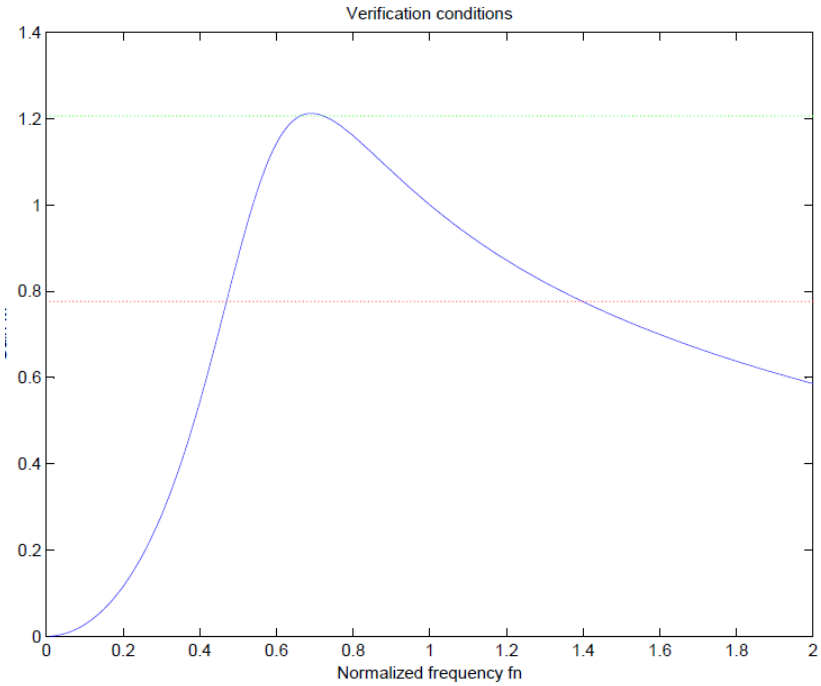

Figure 3.35 Verification of resonant-circuit design conditions

- **Dead time**

$$t_{dead} \geq n \cdot C_{eq} \cdot f_{sw} \cdot L_m = 26.51\, ns \rightarrow 167\, ns$$

The dead time for the full-bridge topology is quite different from the half-bridge because of the capacitors for the MOSFETs are also different. This capacitor is an important element to assure ZVS.

3.2.2.4Simulation analysis and evaluation of Full-Bridge topology

ZVS condition and output response are shown in this chapter to demonstrate the designing process.

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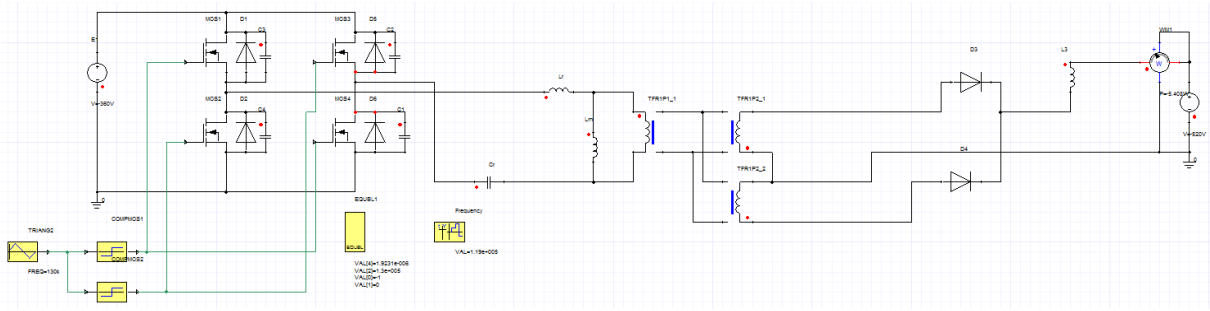

Figure 3.36 Simulated Full-Bridge LLC Resonant Converter

3.2.2.4.1 ZVS condition

In this point, ZVS condition will be showed in both limits of the frequency range (V_{in} = 360 V – V_{out} = 520 V; V_{in} = 380 V – V_{out} = 520 V).

- **520 V**

ZVS condition is shown in Figure 3.37 and Figure 3.38 for the maximum voltage, 520 V.

o S1

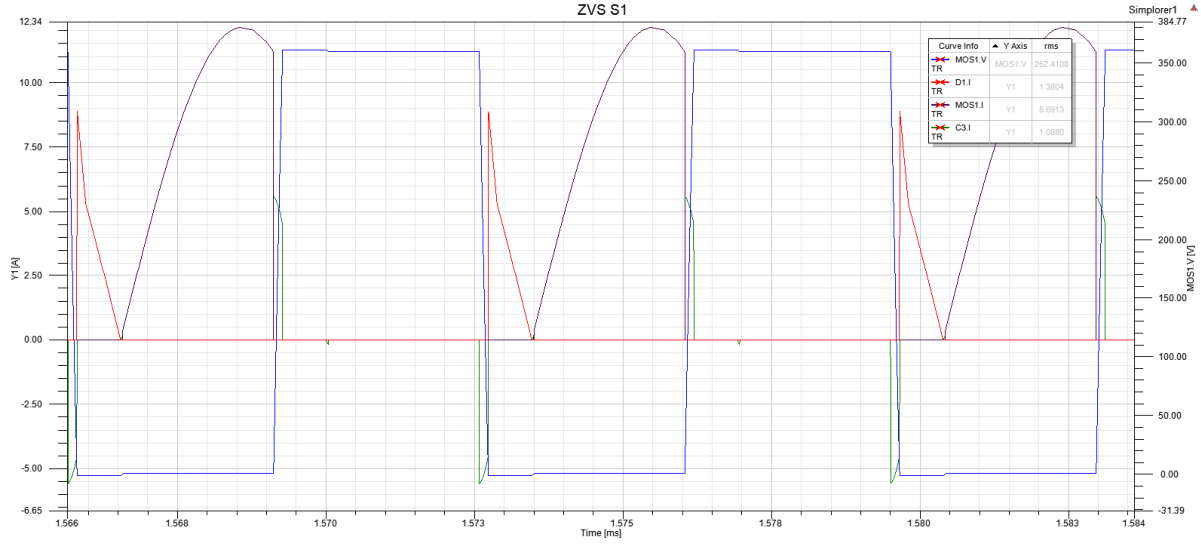

Figure 3.37 MOSFET voltage, diode current ands MOSFET current of S1 at 520V

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- S2

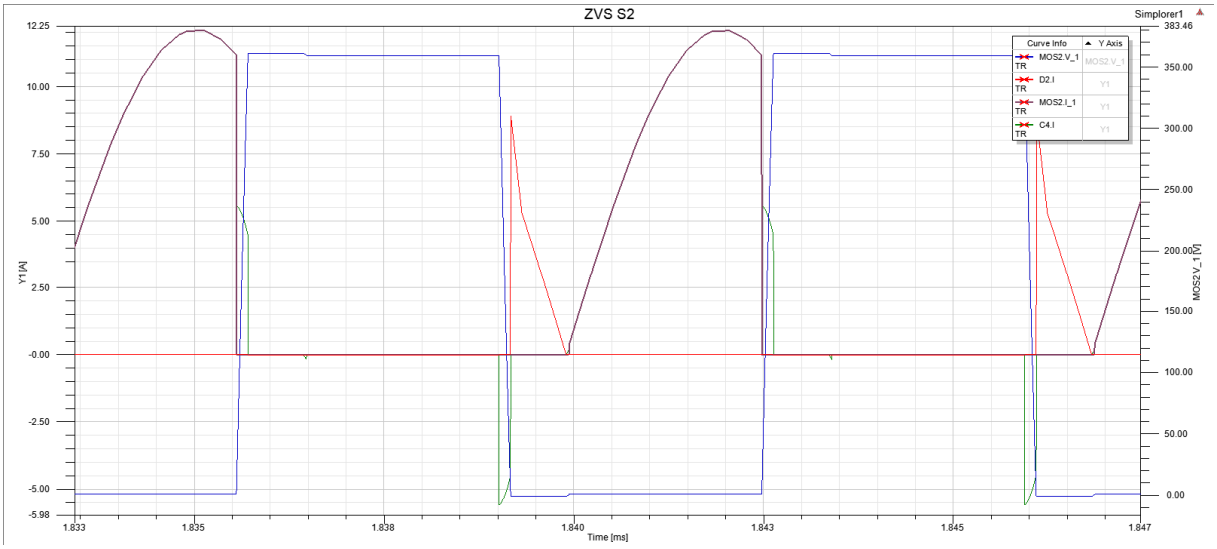

Figure 3.38 MOSFET voltage, diode current ands MOSFET current of S2 at 520V

- **360 V**

In Figure 3.39 and Figure 3.40 ZVS condition is shown for the minimum voltage, 3600 V.

- S1

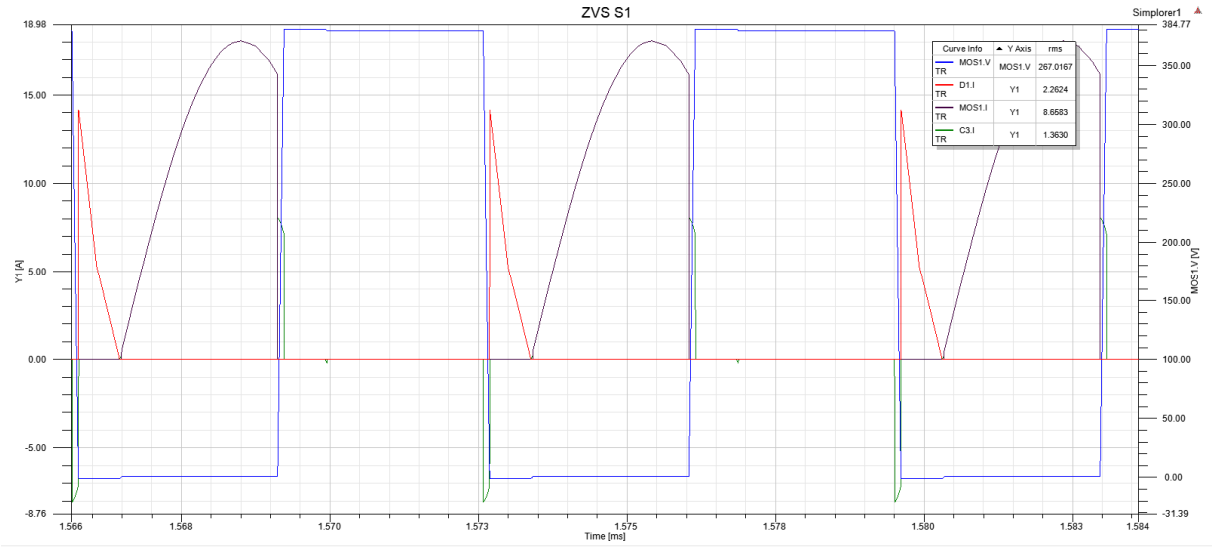

Figure 3.39MOSFET voltage, diode current ands MOSFET current of S1 at 360V

- S2

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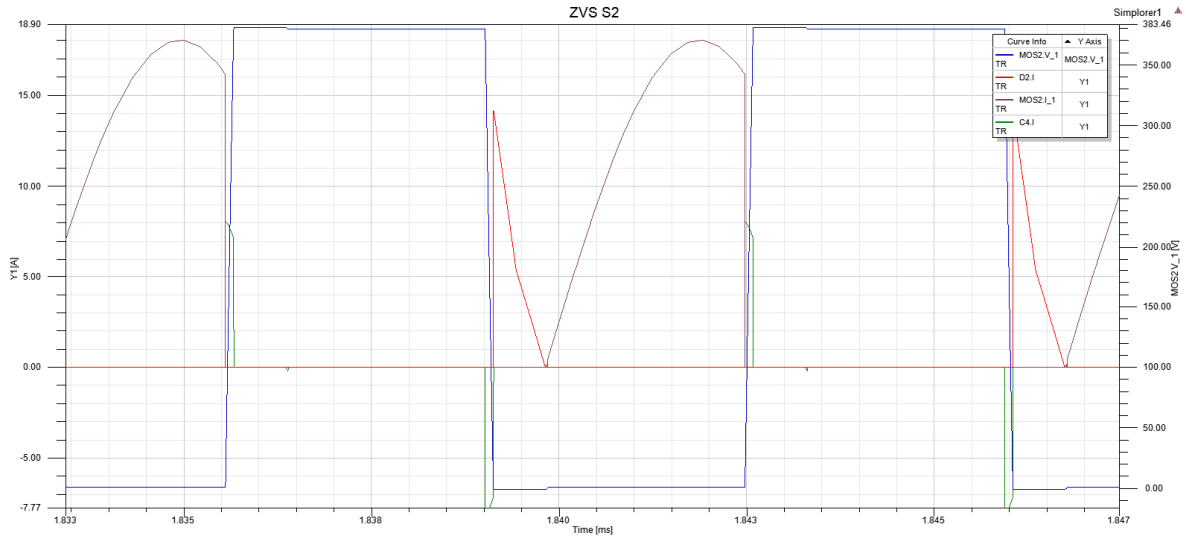

Figure 3.40 MOSFET voltage, diode current ands MOSFET current of S2 at 360V

Capacitor current is shown in full-bridge Model 2 to show how the capacitors flow the current (only when de voltage grows up and decreases) and help to achieve ZVS.

3.2.2.4.2 LLC converter response

In Figure 3.41 is possible to see how the converter controls the output power (red) when output voltage (blue) variation is produced.

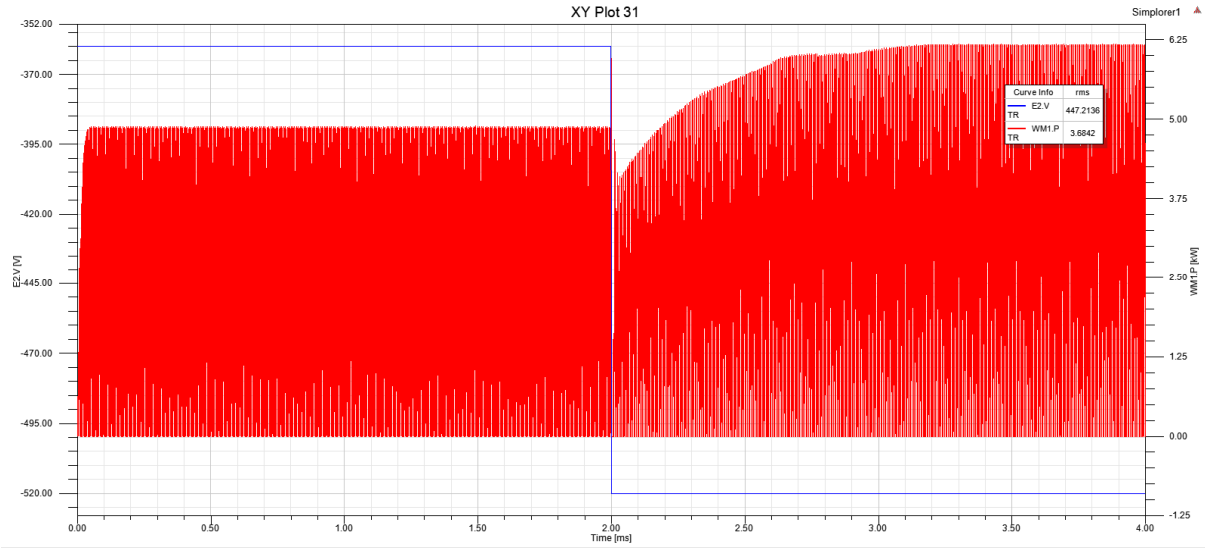

Figure 3.41 Output-power response against output-voltage variation

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For this converter an output inductance filter is not used. However, RMS value of the output power is calculated in the graphs. A close-control can be a solution to avoid that the converter spends time re-controlling the output power. Because of a feed-forward control with a look-up table has been used.

3.2.2.4.3 Zero load condition

Zero load condition is also essential for full-bridge. No load simulation response is demonstrated in Figure 3.42. Maximum output power (3.6 kW) is given until 2 ms. At this point the frequency is varied to show how the converter can give the minimum power (0 kW) between 2 – 4 ms.

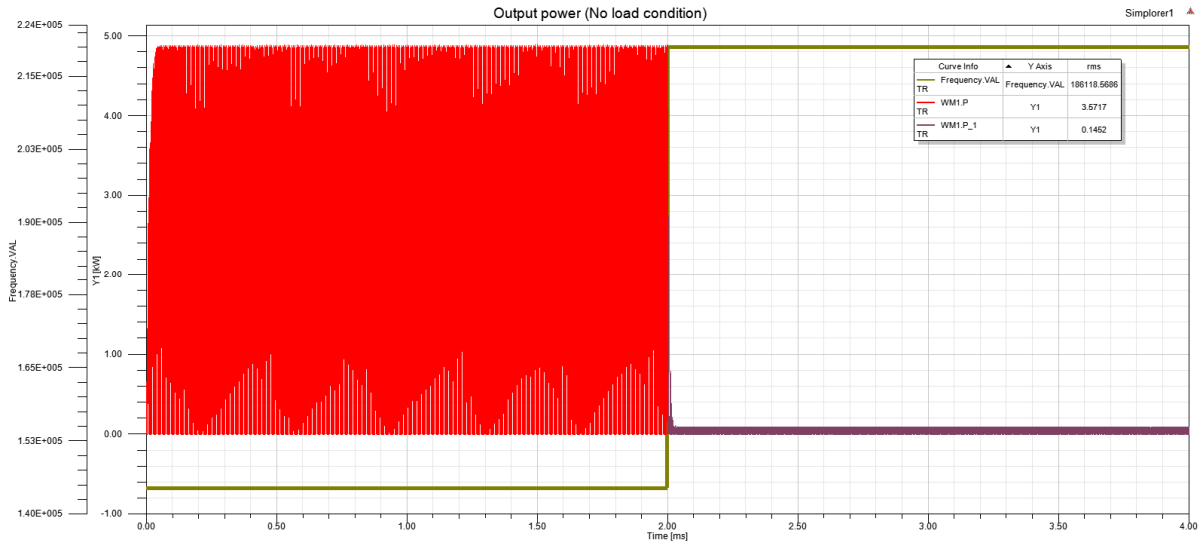

Figure 3.42 Output-power against frequency variation at Vo = 360 V

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3.3 EV AUXILIARY POWER SUPPLY FOR MILD HEV

A bidirectional converter is proposed in this chapter to be design with CLLC topology. The application is EV auxiliary power supply for Mild HEV to operate with 48 V in one side, 14.4 V in the other side and a maximum output power of 2500 W in both directions.

3.3.1 Design steps

The specifications and main parameters for forward mode and reverse mode are listed:

Forward Mode (Mode-1):		Reverse Mode (Mode-2):	
o P_0:	2500 W	P_0:	2500 W
o V_{in}:	48 V	V_{out}:	48 V
o V_{out}:	14.4 V	V_{in}:	14.4 V
o I_0:	173.6 A	I_0:	52.1 A
o f_{sw}:	120 kHz	f_{sw}:	120 kHz

The first design steps are the same for CLLC converter as the LLC.

- **Determine transformer turns ratio**

$$n = M_g \cdot \frac{V_{in\_nom}}{V_0} = 3.33$$

M_g = 1 is assumed to calculate the transformer turn ratio for forward direction.

- **Determine M_{g_min} and M_{g_max}**

$$M_{g\_Mode-1} = \frac{n \cdot V_0}{V_{in}} = 1$$

$$M_{g\_Mode-2} = \frac{\frac{1}{n} \cdot V_0}{V_{in}} = 1$$

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The gain is 1 for both modes. Since the input and output voltage is fixed and the transformer turns ratio is inverted for different directions.

- **Select Ln and Qe**

L_n = 2.5 is considered an optimal value and with M_{g_max}, Q_e is obtained.

$$Q_e = 0.4$$

- **Determine the equivalent load resistance (Re) at full load**

$$R_e = \frac{8 \cdot n^2}{\pi^2} \cdot \frac{V_0}{I_0} = 0.747\ \Omega$$

- **Design resonant circuit's parameter**

$$C_r = \frac{1}{2 \cdot \pi \cdot Q_e \cdot f_0 \cdot R_e} = 4.44\ \mu F$$

$$L_r = \frac{1}{(2 \cdot \pi \cdot f_0)^2 \cdot C_r} = 0.396\ \mu H$$

$$L_m = L_n \cdot L_r = 0.991\ \mu H$$

Until here the design process is the same as seen before in previous chapters.

- **Capacitance ratio**

A proper *g* should make the two dc gain curves alike both in the shape and amplitude as much as possible. With Figure 3.43 g = 1 is considered a properly value. Gain is close and in both cases is higher than Mg.

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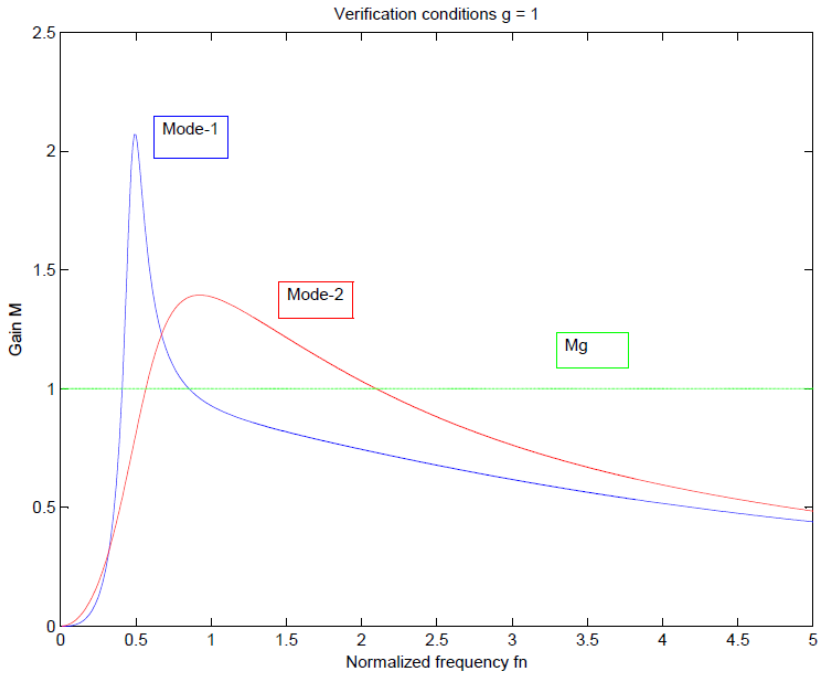

Figure 3.43 Verification conditions g = 1

- **Second resonant capacitance**

$$C_{r2} = g \cdot C_{r1} = 4.44\ \mu F$$

Once g is defined, C_{r2} is obtained.

- **Dead time**

$$t_{dead} \geq n \cdot C_{eq} \cdot f_{sw} \cdot L_m = 2.77\ ns$$

A minimum dead time needs to be defined to avoid short-circuits and to assure ZVS.

For more information about CLLC designing process consult Annex 2.

3.3.2 Simulation analysis and evaluation

ANSYS Simplorer software is used for the simulation as in previous chapters. ZVS condi-

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tion and output response are shown in this chapter to demonstrate the designing process.

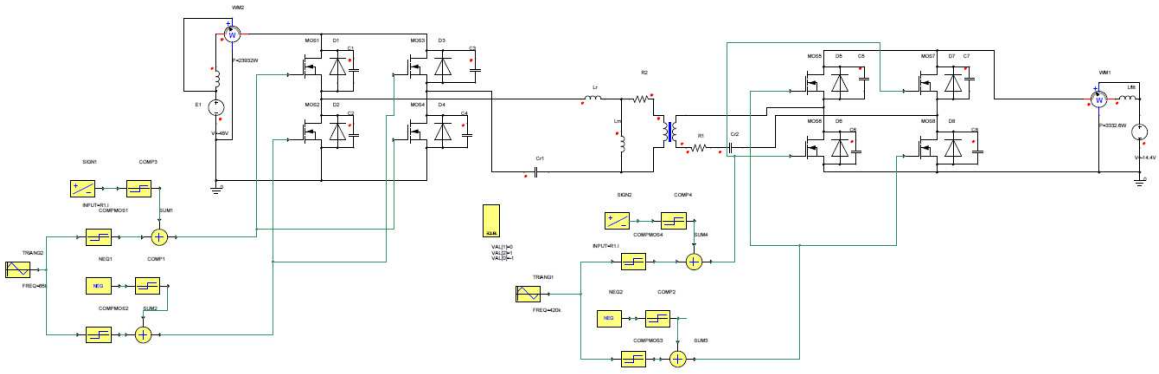

Figure 3.44 Simulated Full-Bridge CLLC Resonant Converter

3.3.2.1ZVS condition

In this point, ZVS condition will be showed in both directions.

- **Forward mode**

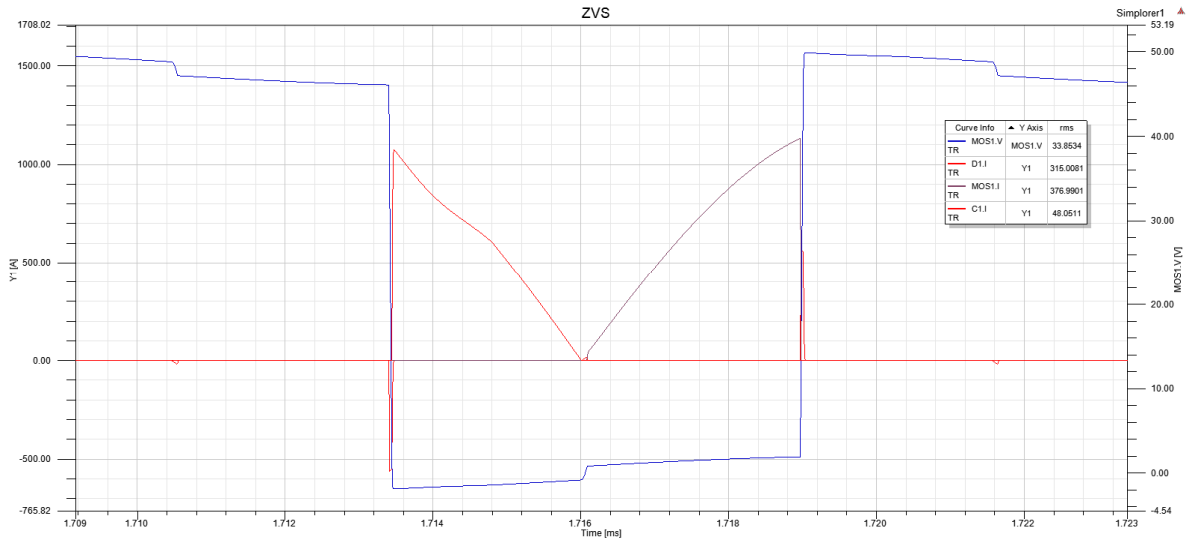

Figure 3.45 ZVS condition for forward mode

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- **Reverse mode**

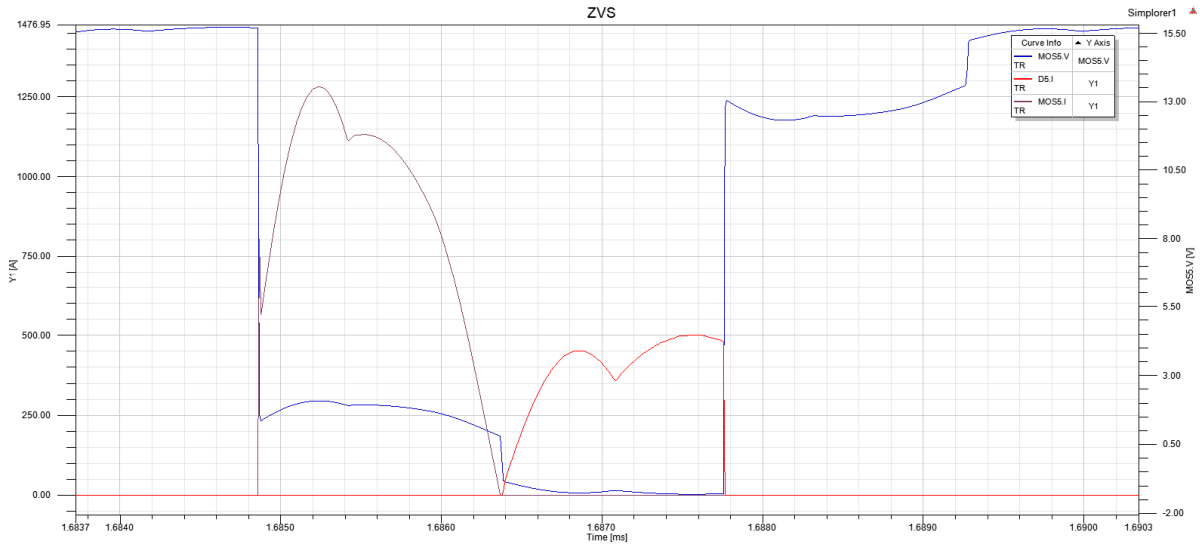

Figure 3.46 ZVS condition for reverse mode

Despite the currents are very high for both directions, ZVS is achieved for forward mode as seen in Figure 3.45. However, ZVS is not completely achieved in reverse mode (Figure 3.48), since the MOSFET start to flow the current when the zero voltage is not reached. Design should be rechecked in the future to assure ZVS in reverse mode.

3.3.2.2 CLLC converter response

Figure 3.47 shows output power (Red for Mode-1 and Blue for Mode-2) response for both flowing directions.

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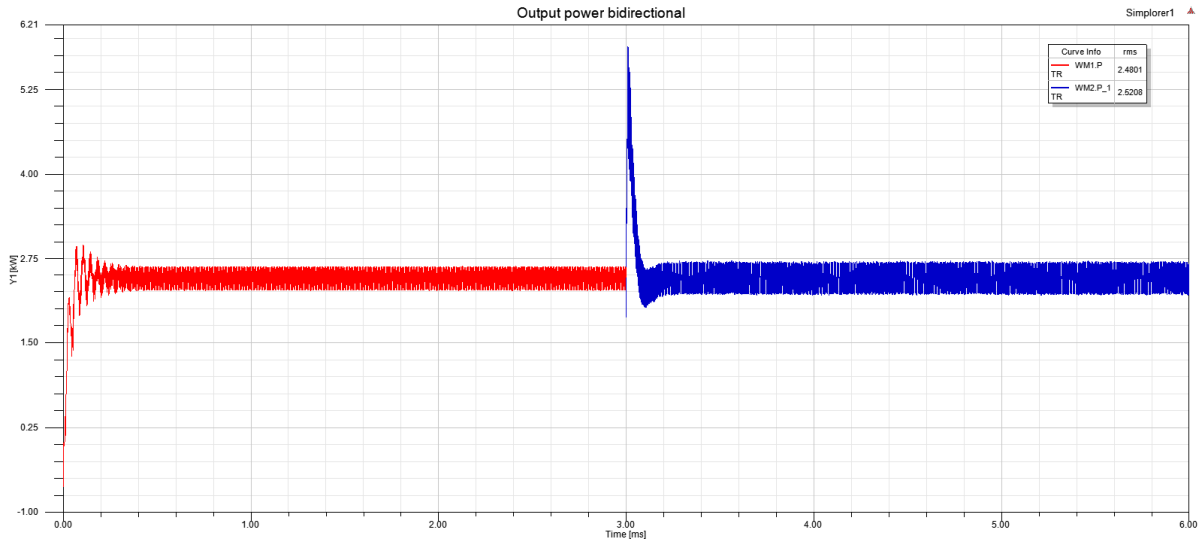

Figure 3.47 Output power for bidirectional response

The control needs some time to re-control the output power due to the look-up table used for the control.

Synchronous rectification is not achieved for the secondary side because of that ZCS is not attained. A possible solution is to eliminate the output inductance filter to facilitate the normal switching of the MOSFETs.

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3.4 GALVANIC INSULATION FOR EV FAST CHARGER WITH OPTIMAL "VEHICLE TO GRID" FEATURE

A simulation of CLLC Resonant Converter for a Galvanic insulation for EV fast charger with optional "vehicle to grid" feature application is presented in this chapter. Resonant converter has been designed to operate between a voltage range of 360 – 550 V for one side, within a voltage of 600 V for the other side and bidirectional output power of 22000 W.

3.4.1 Design steps

The specifications and main parameters are specified as follows for forward mode and reverse mode:

Forward Mode (Mode-1):		Reverse Mode (Mode-2):	
o P_0:	22000 W	P_0:	22000 W
o V_{in}:	600 V	V_{out}:	600 V
o V_{out}:	360 - 550 V	V_{in}:	360 - 550 V
o I_0:	68.8 A	I_0:	36.7 A
o f_{sw}:	150 kHz	f_{sw}:	150 kHz

The first design steps are the same for CLLC converter as the LLC.

- **Determine transformer turns ratio**

$$n = M_g \cdot \frac{V_{in\_nom/2}}{V_0} = 1.32$$

For forward transformer turns ratio calculation, $M_g = 1$ is used.

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- **Determine M_{g_min} and M_{g_max}**

$$M_{g\_max\_Mode-1} = \frac{n \cdot V_0}{V_{in}} = 1.21$$

$$M_{g\_min\_Mode-1} = \frac{n \cdot V_0}{V_{in}} = 0.791$$

$$M_{g\_max\_Mode-2} = \frac{n \cdot V_0}{V_{in}} = 1.27$$

$$M_{g\_min\_Mode-2} = \frac{n \cdot V_0}{V_{in}} = 0.827$$

In this converter four gains are calculated. Maximum and minimum gain for each direction.

- **Select Ln and Qe**

Q_e is obtained considering $L_n = 3$ an optimal value.

$$Q_e = 0.3$$

- **Determine the equivalent load resistance (Re) at full load**

$$R_e = \frac{8 \cdot n^2}{\pi^2} \cdot \frac{V_0}{I_0} = 13.3\ \Omega$$

- **Design resonant circuit's parameter**

$$C_r = \frac{1}{2 \cdot \pi \cdot Q_e \cdot f_0 \cdot R_e} = 267\ \text{nF}$$

$$L_r = \frac{1}{(2 \cdot \pi \cdot f_0)^2 \cdot C_r} = 4.22\ \mu\text{H}$$

$$L_m = L_n \cdot L_r = 1.27\ \mu\text{H}$$

These parameters are selected for forward mode, since the design process is alike as LLC.

- **Capacitance ratio**

The two dc gain curves should be both as similar as possible in shape and amplitude for a proper *g*. Looking Figure 3.48, g = 1 is considered a properly value. Gains are similar for both directions and higher than M_{g_max}.

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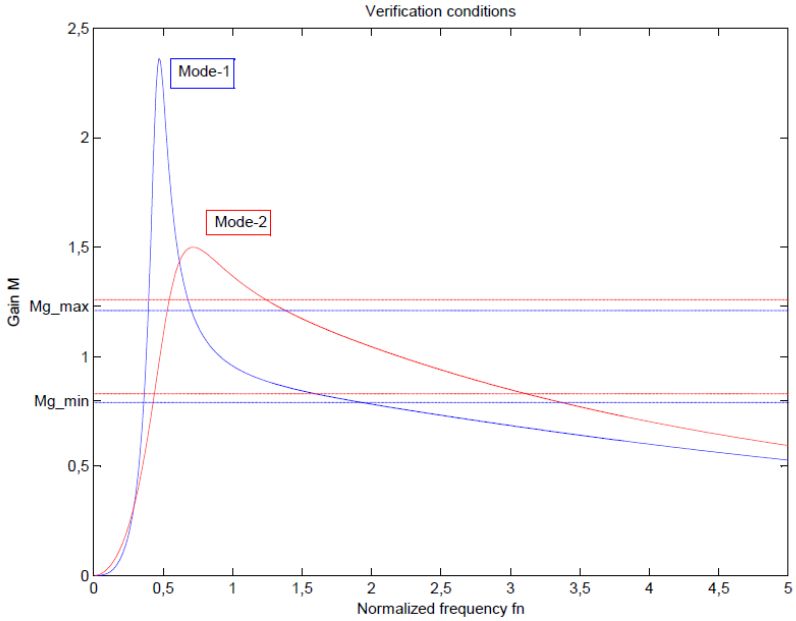

Figure 3.48 Verification conditions g = 1

- **Second resonant capacitance**

$$C_{r2} = g \cdot C_{r1} = 4.44\ \mu F$$

- **Dead time**

$$t_{dead} \geq n \cdot C_{eq} \cdot f_{sw} \cdot L_m = 1.76\ \ ns$$

A minimum dead time needs to be defined to avoid short-circuits and to assure ZVS.

For more information about CLLC designing process consult Annex 2.

3.4.2 Simulation analysis and evaluation

In this section ZVS condition, output response and no load condition simulations (ANSYS Simplorer) are presented to prove the designing.

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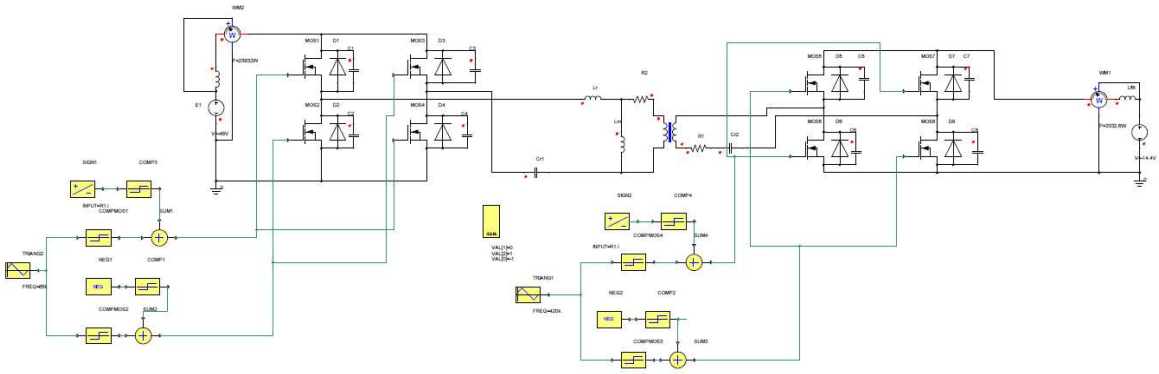

Figure 3.49 Simulated Full-Bridge CLLC Resonant Converter

3.4.2.1 ZVS condition

ZVS condition will be showed in forward and reverse mode.

- **Forward mode**

As seen in Figure 3.50, ZVS is achieved when the converter works at Mode-1.

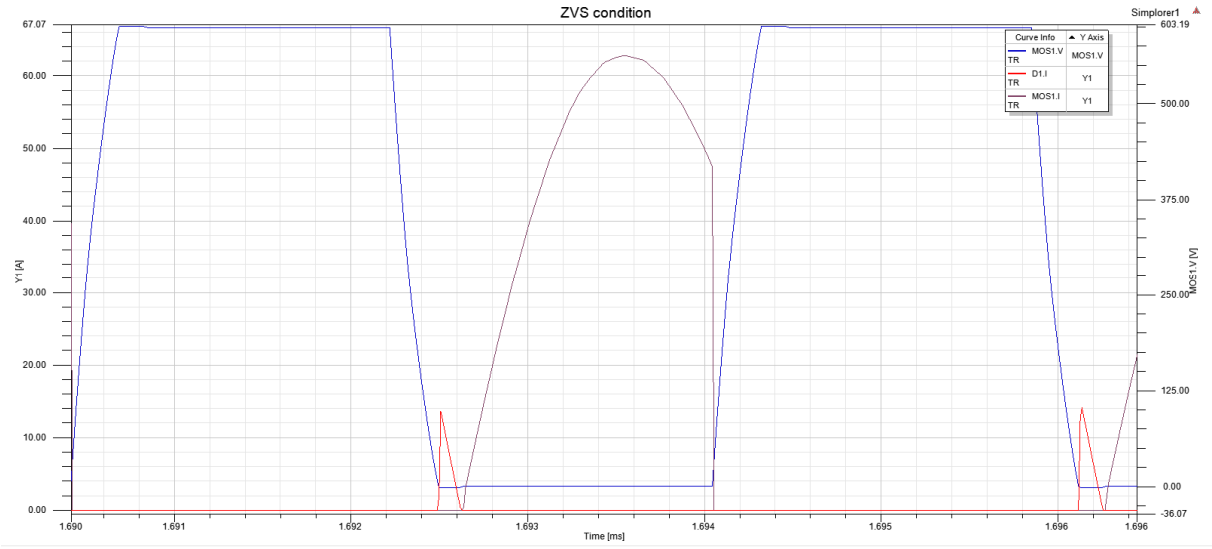

Figure 3.50 ZVS condition for forward mode at 360 V

- **Reverse mode**

ZVS is almost completely achieved when the converter works at Mode-2 as seen in Figure 3.51.

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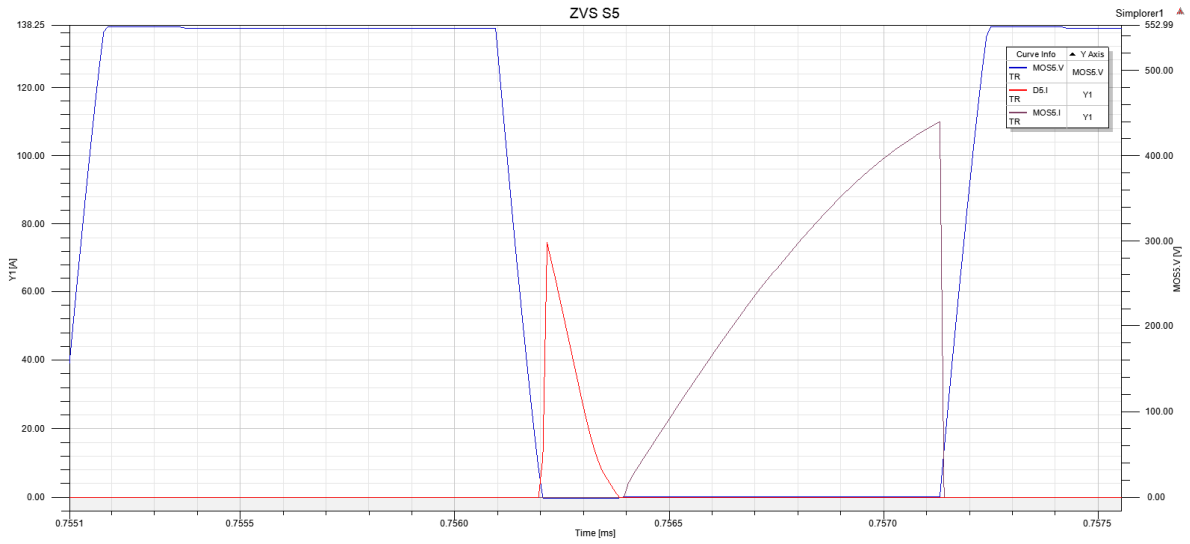

Figure 3.51 ZVS condition for reverse mode at 550 V

3.4.2.2LLC converter response

In Figure 3.52 is possible to see how the converter controls the output-power (purple) when output-voltage (red) variation is produced in reverse mode and in forward mode (Figure 3.53). Output inductance filters are used to make clearer the output power graph.

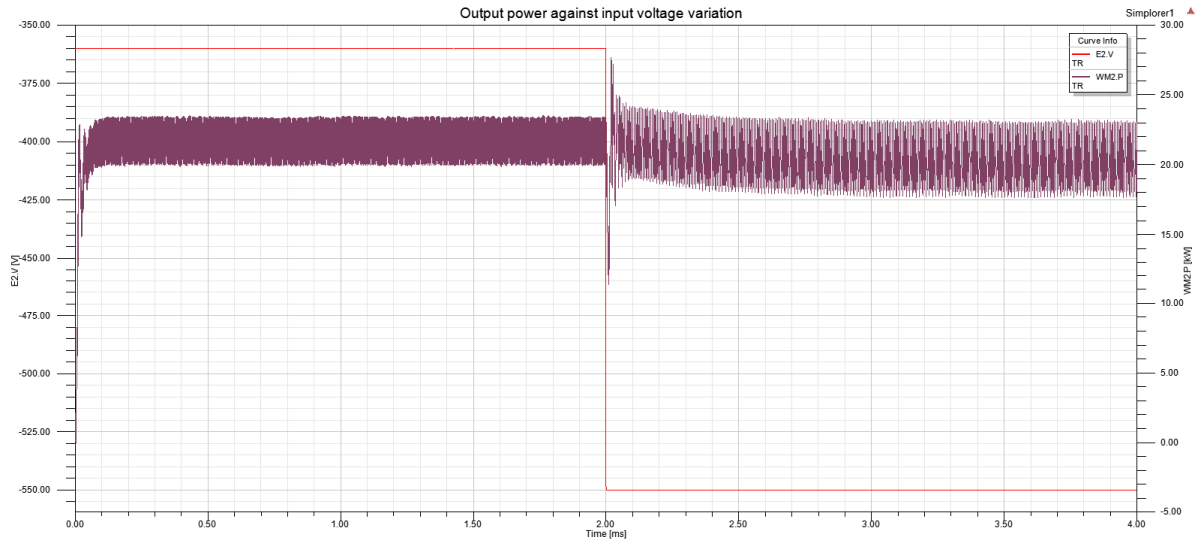

Figure 3.52 Output power against output voltage variation reverse mode

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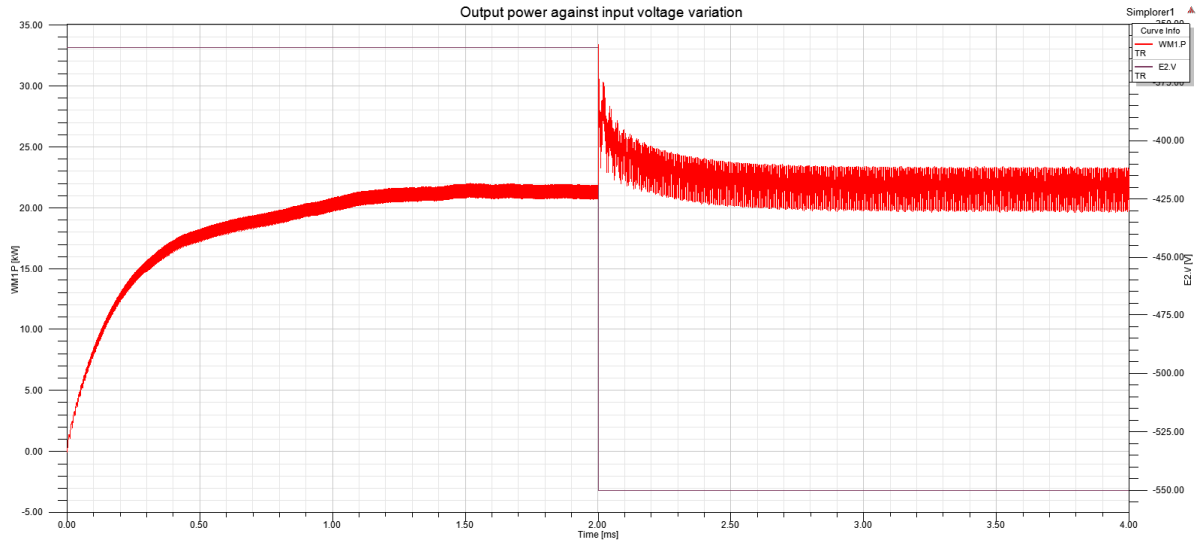

Figure 3.53 Output power against output voltage variation forward mode

A close-control can be a solution to avoid that the converter spends time re-controlling the output power. Because of a feed-forward control with a look-up table has been used.

ZCS in the secondary side is not achieved because synchronous rectification is not properly attained. To remove the output inductance filter is considered a possible solution to facilitate the normal switching of the MOSFETs.

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4 GALVANIC INSULATION FOR STANDARD EV ONBOARD CHARGER HARDWARE DESIGN

In this chapter, the hardware design procedure for a prototype resonant converter is presented. A galvanic insulation for a standard EV Onboard charger converter in Full-Bridge topology is designed. The resonant parameters have been studied in the previous chapters; however, other properties as isolation or temperature values are also important.

4.1 Introduction

A high level block diagram of the proposed circuit is shown in Figure 4.1. The input voltage block is connected to the full-bridge with a parallel capacitor. Between the transformer (electric isolation is represented with discontinuous line) and the full-bridge, the LLC resonant tank is placed. After that a full-bridge rectification and a low pass filter are connected to the load. The MOSFETs are controlled with four isolated drivers. Two voltage sensors (input and output voltage) and a current sensor are placed to provide measurements to the microcontroller. It is also connected with CAN and USB communication.

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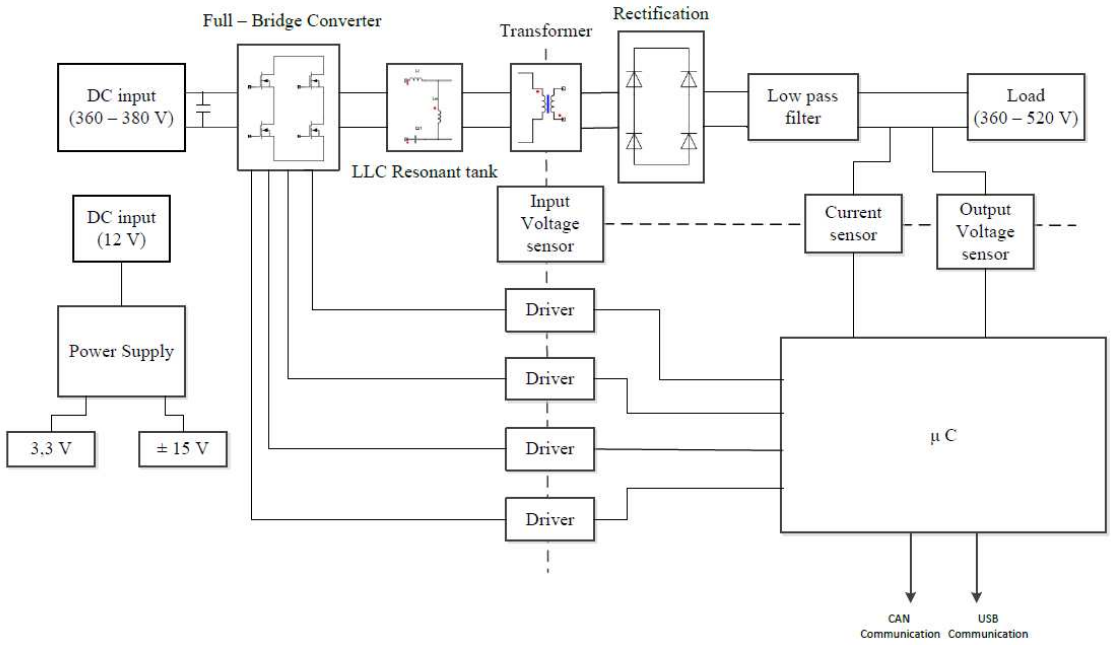

Figure 4.1 High level LLC converter block diagram

The converter can be logically divided into two sections, the high power side and the auxiliary control circuits.

4.2 High Power side

The specifications and main parameters of the converter are specified as follows:

- P_0: 3600 W
- V_{in}: 360 – 380 V
- V_{out}: 360 – 520 V
- I_0: 8.1 A
- f_{sw}: 150 kHz

The high power side is formed by the active parts, the transformer and the additional passive parts.

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4.2.1 Active parts: Power semiconductors

Power semiconductors are always essential in converters. Devices information are presented here.

- **Switches**

  As explained in previous chapters, MOSFETs are suitable for resonant converter to achieve ZVS. Low power loss is one of the principle goals of the resonant converters and CoolMOS MOSFETs from Infineon are used because of their switching properties.
  After analyzing the simulation results, IPP60R099C6 with PG-TO220 package is selected.
  The key performance parameters define the MOSFET characteristics:

  - $V_{DS\ (Tj,max)} = 650$ V
  - $R_{DS(on),max} = 0{,}099\ \Omega$
  - $Q_{g,typ} = 119$ nC
  - $I_{D,pulse} = 112$ A
  - $V_{GS(th)} = 2{,}5 – 3{,}5$ V
  - $C_{oss} = 154$ pF

- **Rectifier diodes**

  A full-bridge topology is selected for the rectifier. Simulation results present the normal current and voltage values and silicon carbide technology is selected with STPSC10TH13TI from STMicroelectronics. It is a power Schottky diode with a 650 V rating and TO-220 package.
  A device summary is presented:

  - $I_{F(AV)} = 10$ A
  - $V_{RRM} = 650$ V
  - $T_{j(max)} = 175$ °C
  - $V_{F(25\ °C)} = 1{,}56$ V

  Because of the very low reverse-recovery losses of SiC schottky technology, these diodes

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are very well-suiting for high frequency applications.

4.2.2 Transformer

The transformer is an important element for the tank circuit parameters and its design is decisive for a properly response. This section provides the details of how to calculate the transformer; however, some parameters such as turn ratio have already been calculated.

4.2.2.1 Transformer parameters

To calculate the transformers primary and secondary turns, ETD – 49 datasheet, maximum duty-cycle, switching frequency and input-voltage are required.

$$N_p = \frac{V_{in\,min} \cdot D_{max}}{2 \cdot \Delta B \cdot A_e \cdot F_{min}} \approx 23$$

$$N_s = \frac{N_s}{n} \approx 29$$

$$L_r = 25.4\ \mu H$$

$$L_m = 63.5\ \mu H$$

4.2.2.2 Transformer inductances

In this case, the resonant and the magnetizing inductance are the important parameters. They are integrated into the transformer, no external. It is needed to take advantage of transformer characteristics and adapt transformer inductances to theoretical inductances.

Open circuit and short circuit tests are useful to know more about transformer parameters. In this case, the tests are focused on inductance analysis, and different topologies for the windings are studied (Figure 4.2) to manage transformer inductances.

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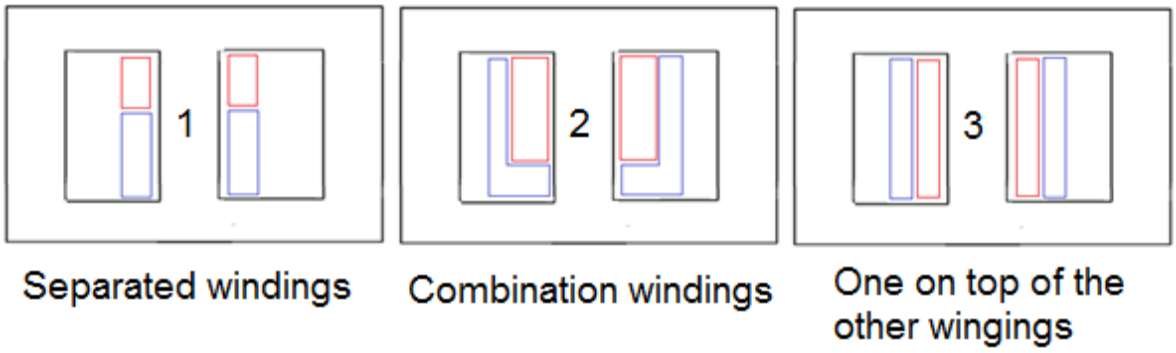

Figure 4.2 Winding models

The primary and the secondary are placed separated with some space between them in the first model. The second model is a mix of the others. Because in one part they are separated in the same level and in other part they are above each other. In the third model, the secondary winding is placed on top of the primary winding.

The variation graphs of the inductances depending on the models and for different Air gaps are presented here (for more detailed data, check Annex 3).

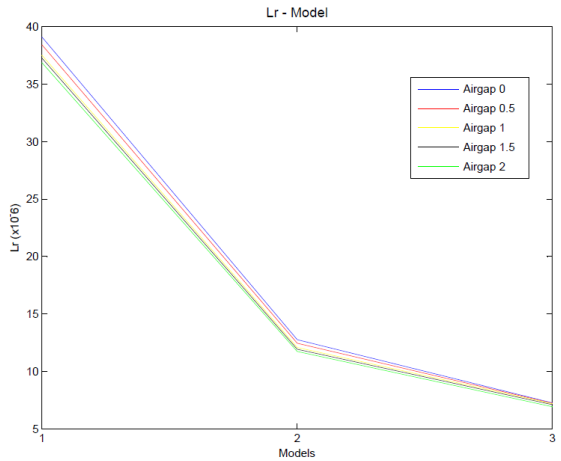

Figure 4.3 Lr value against different winding models topology for different air gaps

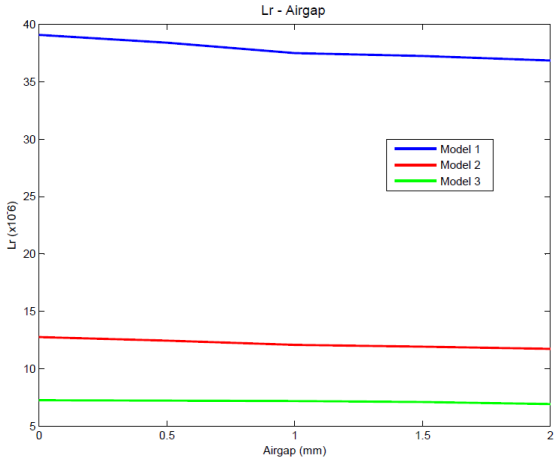

Figure 4.4 Lr value against air gap variation

It is seen in Figure 4.3 how the resonant inductance is higher for model 1 and how it decreases for model 2 (combination of model 1 and model 3) until minimum value of model 3. The values of resonant inductances do not vary significantly with the different air gaps, since

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all the lines are almost horizontal in Figure 4.4.

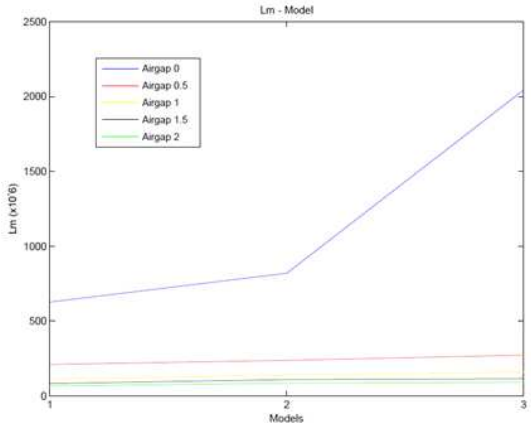

Figure 4.5 Lm value against different winding models topology for different air gaps

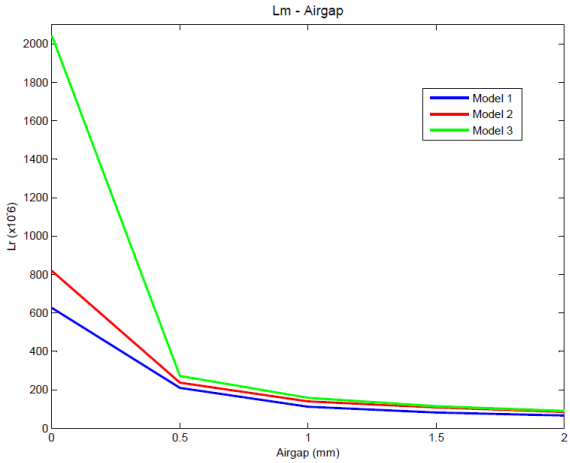

Figure 4.6 Lm value against air gap variation

The magnetizing inductances are almost constant for the three models except with no Air gap as seen in Figure 4.5. With no Air gap the minimum value is model 1 and model 2 the maximum. The high growth of the magnetizing inductance is produced between 0 and 0.5 mm Air gap (Figure 4.6).

4.2.2.3 Manufactured transformer

Considering the previous chapter, the transformer is built with separated primary and secondary windings (model 1) and 1 mm air-gap.

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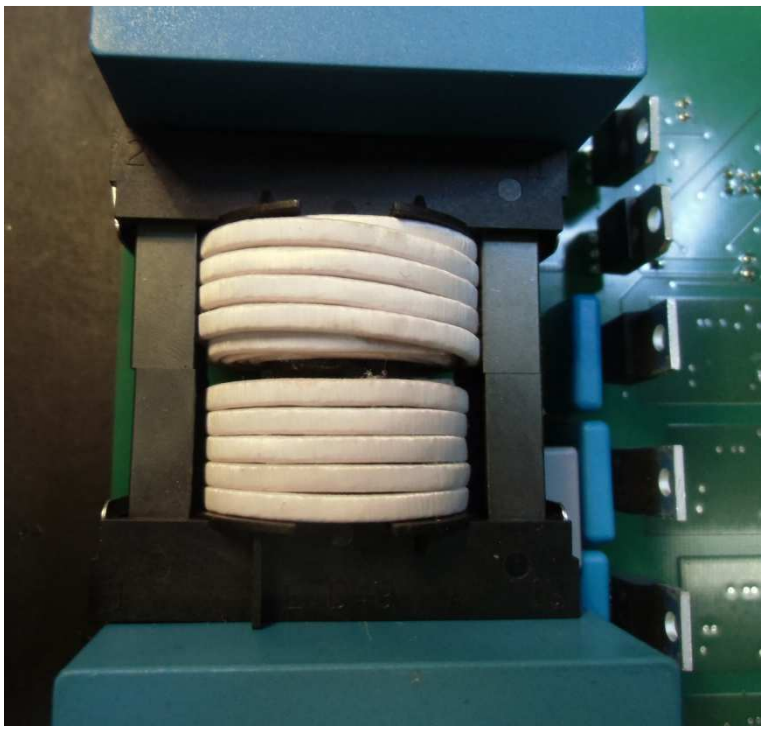

Figure 4.7 Transformer for galvanic insulation for standard EV Onboard charger

After the transformer construction, the inductances are measured and compared to the first theoretical values.

$$L_r = 36.3\ \mu H \rightarrow\ 25.4\ \mu H$$

$$L_m = 98.1\ \mu H \rightarrow\ 63.5\ \mu H$$

The resonant inductance is similar; however, the magnetizing is a bit different and a re-design process with the new values is implemented. The theoretical response is guaranteed and the new simulation ensures proper behavior.

To check the optimal behavior of the transformer, an experimental gain curve is obtained. A sweep of the frequency range is created with a waveform generator and the input and output-voltage are measured with an oscilloscope. The resonant capacitor (47 nF) is also added to simulate as much as possible the LLC resonant tank.

In Figure 4.8 is possible to see how the transformer has an experimental gain curve similar to the theoretical gain curve.

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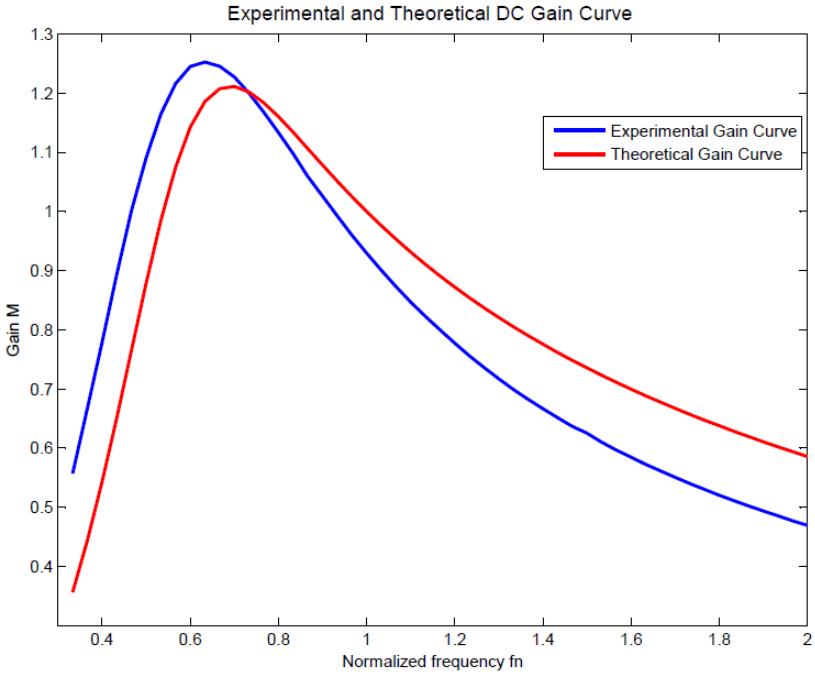

Figure 4.8 Comparative of experimental and theoretical gain curve of the transformer

4.2.3 Additional passive parts

Passive elements are always located in high power side.

For the resonant capacitor and the MOSFETs parallel capacitors, polypropylene (PP) capacitors from Wima are placed. For the resonant capacitor is used a 0.047 µF (FKP1G024705D00) and 2200 pF (FKP1G012204B00) for the MOSFETs parallel capacitors.

For the input and output capacitors, a Metalized Polypropylene film (MKPB32678G6256K00) capacitors from EPCOS are placed.

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4.3 Control side

The control side is formed of different circuits. Each one is explained in this chapter and identified with a color code in the printed board (Figure 4.9).

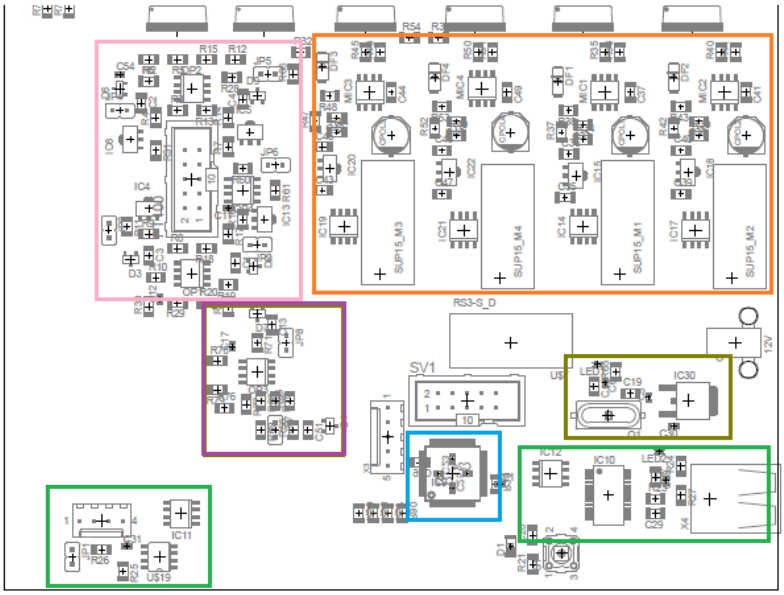

Figure 4.9 Control Side of the printed board

4.3.1 MOSFETs Drivers

Drivers are required for the MOSFETs because of the high voltage and switching frequency. A driver circuit allows to supply enough current for a proper MOSFET transition and adequate isolation is required.

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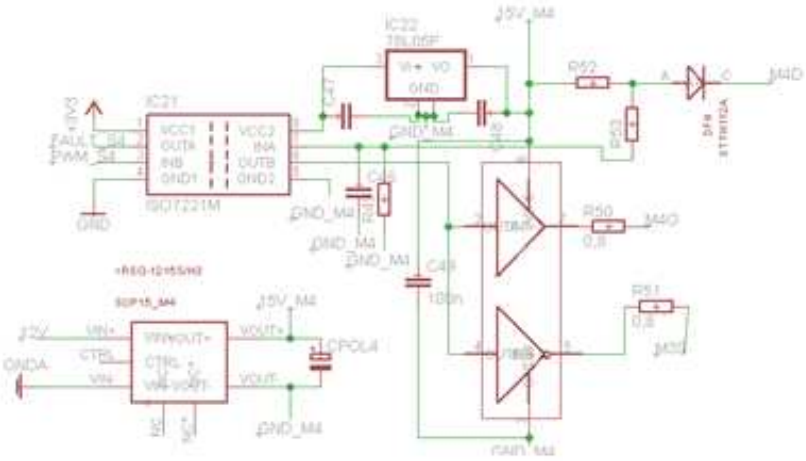

Figure 4.10 MOSFET driver schematic circuit

Figure 4.10 shows how the MIC4128 is used to supply the isolated 15 V to the MOSFETs. The LM78L05F, in Fixed Output Regulation topology, is connected to guarantee the supply to the ISO7221M which allows the circuit to detect short-circuits through the diode (STTH112A), the capacitors and the resistors connection.

4.3.2 Microcontroller

A DSP-based digital control scheme (dsPIC33FJ64GS606) is proposed to generate the driving signals for the MOSFETs under 50% duty cycle and to control the fault signals in case of short-circuit.

USB communication and CAN bus circuits are also added to guarantee the control of the microcontroller.

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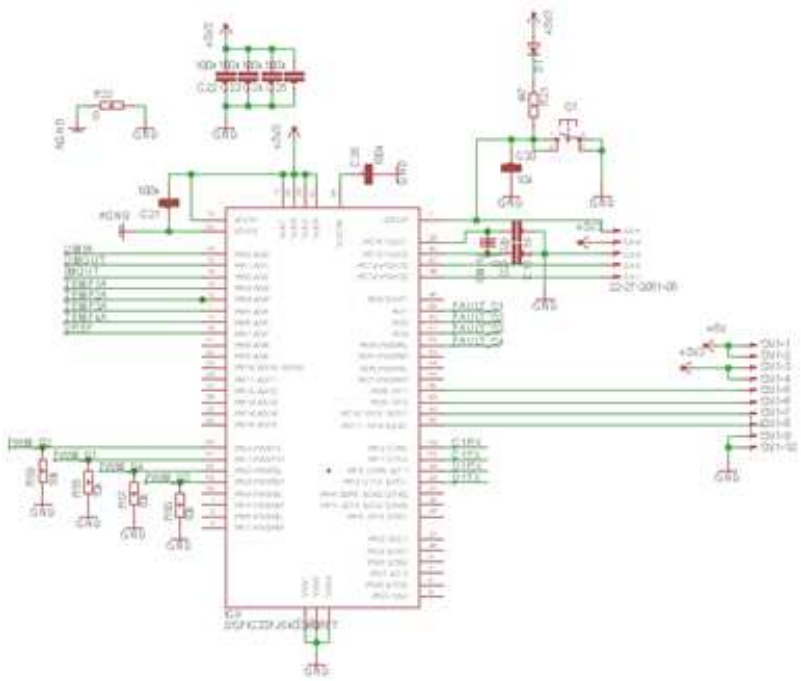

Figure 4.11 Microcontroller schematic circuit

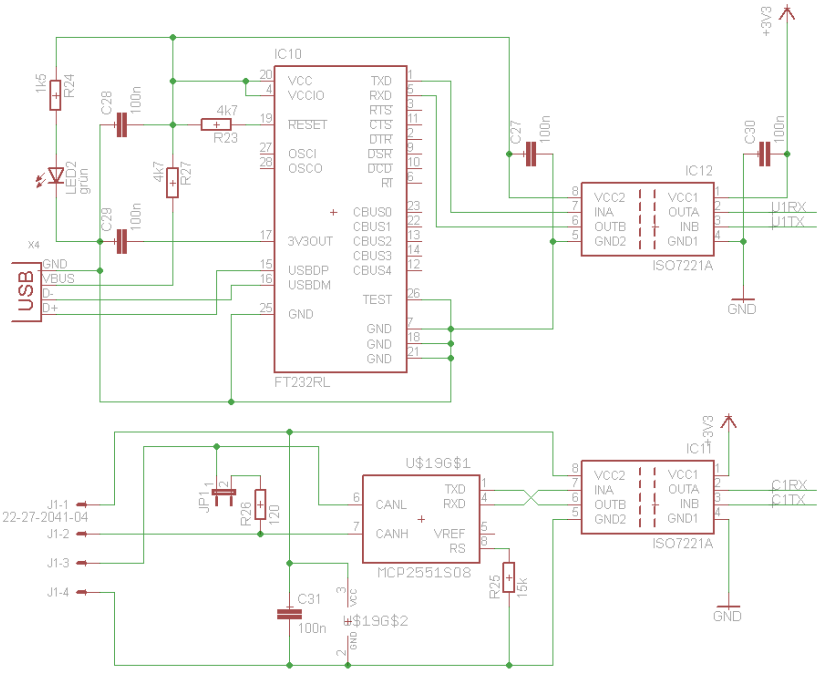

Figure 4.12 USB communication and CAN bus circuit

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4.3.3 Voltage measurement

An operational amplifier is used as differential amplifier for the input and output voltage measurements to reduce the voltage amplitude within the microcontroller input range.

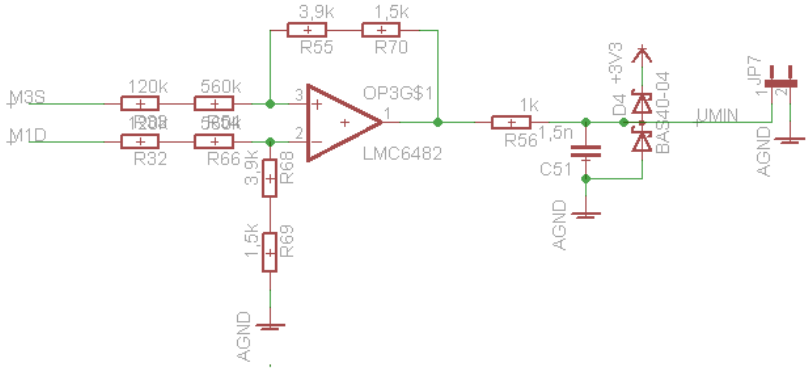

Figure 4.13 Voltage measurement schematic circuit

Resistors are calculated to hold the high voltage (max. 520 V) and to adapt it to the microcontroller input range.

4.3.4 Temperature measurement

Temperature sensors are also needed to guarantee MOSFETs security. A circuit with a fixed current (LM317L), a variable resistor (PT-100) and a reference voltage is integrated to control this critical parameter.

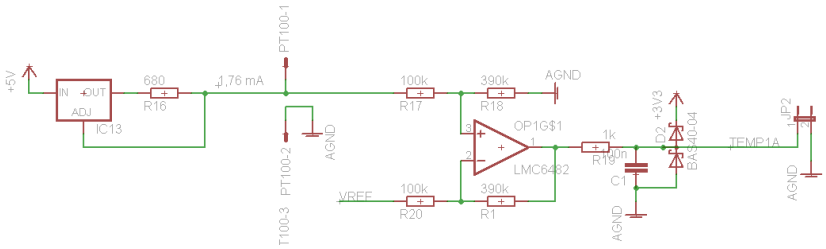

Figure 4.14 Temperature measurement schematic circuit

A forced ventilation system is set up to cool the power elements.

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4.3.5 Control Voltage

The supply for the control circuits is obtained through an isolated conversion (3,3 V and 5 V – RSO) from a common voltage (12 V) in vehicle applications.

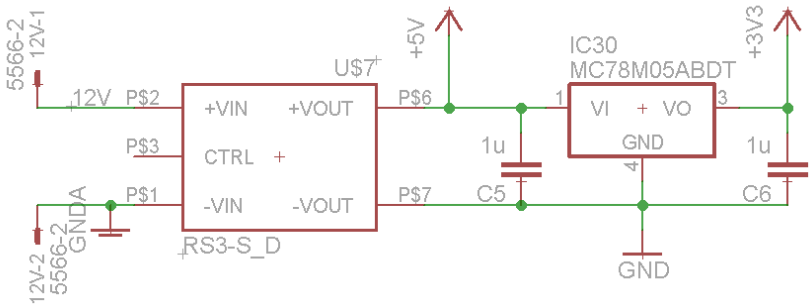

Figure 4.15 Control voltage schematic circuit

For more detailed information about the control circuits, Annex 4 can be consulted.

4.4 Circuit design

For the printed board design Eagle Software and libraries have been used. Figure 4.16 shows the printed circuit. The control side elements have been placed on the top layer (Figure 4.17) and the high power elements in the bottom layer (Figure 4.18). Due to forced ventilation system to cool the power elements is required.

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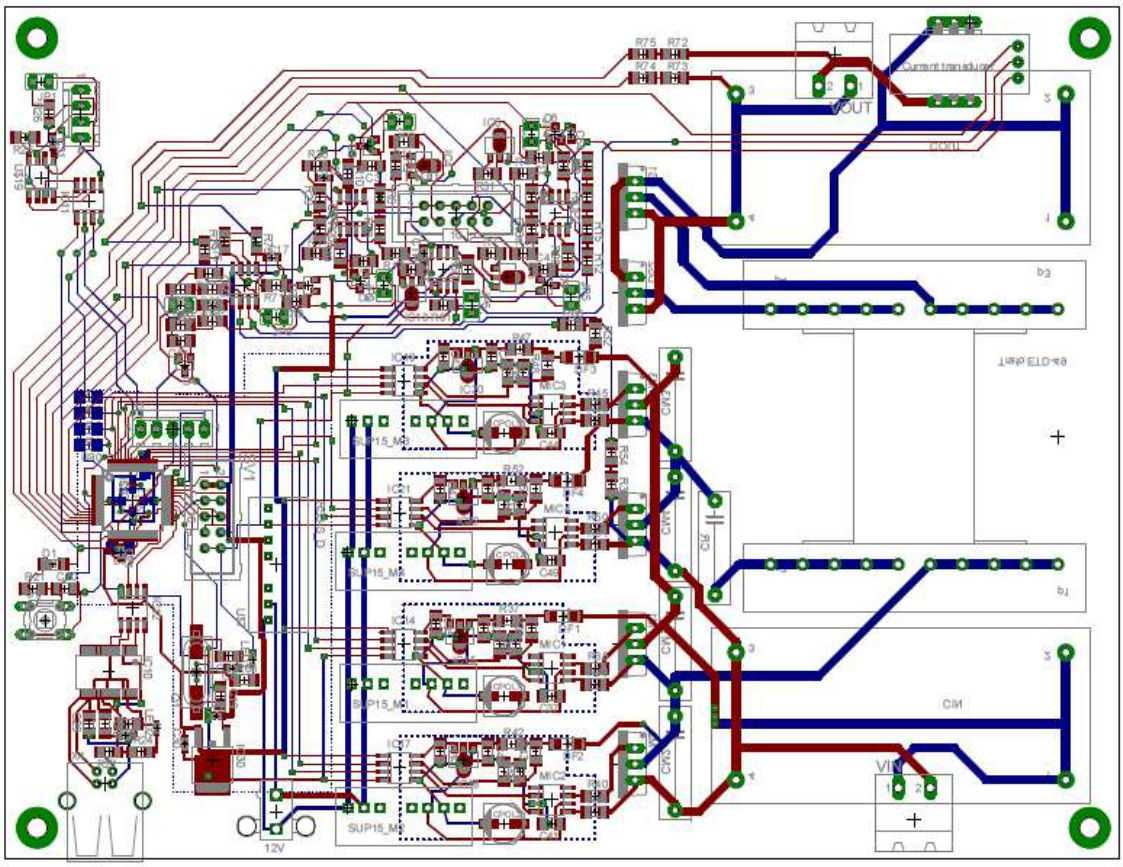

Figure 4.16 Printed board for LLC converter

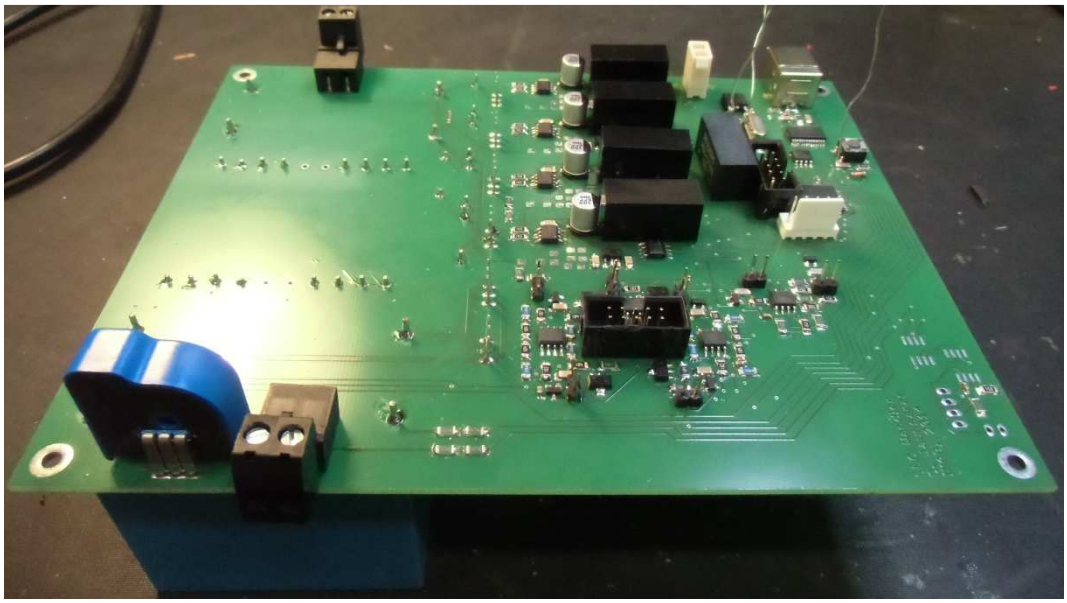

Figure 4.17 Top layer of Galvanic insulation for a standard EV Onboard charger

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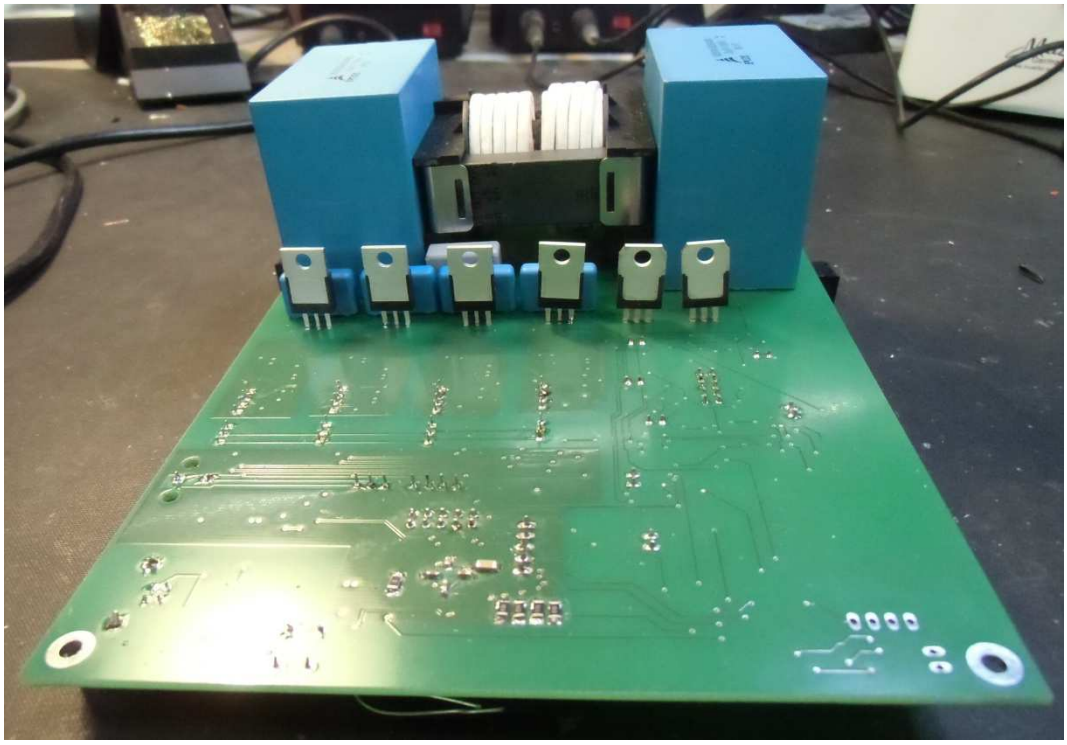

Figure 4.18 Bottom layer of Galvanic insulation for a standard EV Onboard charger

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5 Conclusions

The increasing of electric power in automobiles requires larger number of applications where DC-DC converters are used. To reduce the size of power supplies, resonant power converters are receiving renewed interest.

In this thesis, principle resonant converter topologies have been studied with their response and characteristics.

No voltage regulation for no load condition is the main disadvantage of Series resonant converter (SRC). This is achieved by Parallel resonant converter (PRC). However, the constant current in PRC makes the power losses high for applications with no constant load. Series Parallel resonant converter (SPRC) is a combination of SRC and PRC. In spite of SPRC achieves both previous main advantages, the power losses are still high. With LLC resonant converters these problems are solved and high efficiency or simpler design is achieved. Nevertheless, bidirectional applications cannot be designed optimally with normal LLC and another converter with similar characteristics is developed. CLLC resonant converters work in both directions but the design process is more complicated.

The presented design process for LLC converter considers different parameters, such as resonant frequencies (f_0 and f_1), maximum and minimum gain (M_{g_max} and M_{g_min}) or transformer turn ratio. Furthermore, proper values for inductance ratio (L_n) to guarantee no load response and quality factor (Q_e) to assure ZVS are calculated.

The CLLC design process is more complicated since more parameters have to be considered. The two gain curves for both directions must be as similar as possible and it is achieved with a proper capacitance ratio (g).

Four automotive applications are designed and simulated. *EV auxiliary power supply* and *Galvanic Insulation for standard EV Onboard charger* are unidirectional and LLC topology

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is employed. CLLC topology is used for bidirectional applications as *EV auxiliary power supply for MILD HEV* and *Galvanic Insulation for EV fast charger with optimal "Vehicle to grid" feature.*

Main characteristics and behavior of resonant converters as ZVS or output voltage regulation are achieved for LLC designs. In spite of it, a deep study to the simulation model would be interesting to avoid the noise in the MOSFETs parallel diodes during the peak current.
ZVS and output voltage regulation are also achieved in bidirectional designs. However, *EV auxiliary power supply for MILD HEV* model must be redesigned to guarantee ZVS in reverse mode. In addition, synchronous rectification must be also checked to ensure ZCS in the secondary side.

A feed-forward control with a look-up table previously obtained has been employed in the simulations. It causes that the converter spends a time re-controlling the output; design a close-control can be a solution to avoid it.

For the hardware implementation *Galvanic Insulation for standard EV Onboard charger* converter is selected. Isolation for the MOSFETs drivers and voltage supplies as well as for the voltage, current and temperature measurements is considered essential.

To demonstrate converter low power losses through experimental measurements will be interesting to show the main resonant converter characteristic.

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A Annex

A.1 LLC RESONANT CONVERTER DESIGNING GUIDE

This guide is a step by step tool for designing LLC resonant converter parameters. Calculations are in Excel and Matlab.

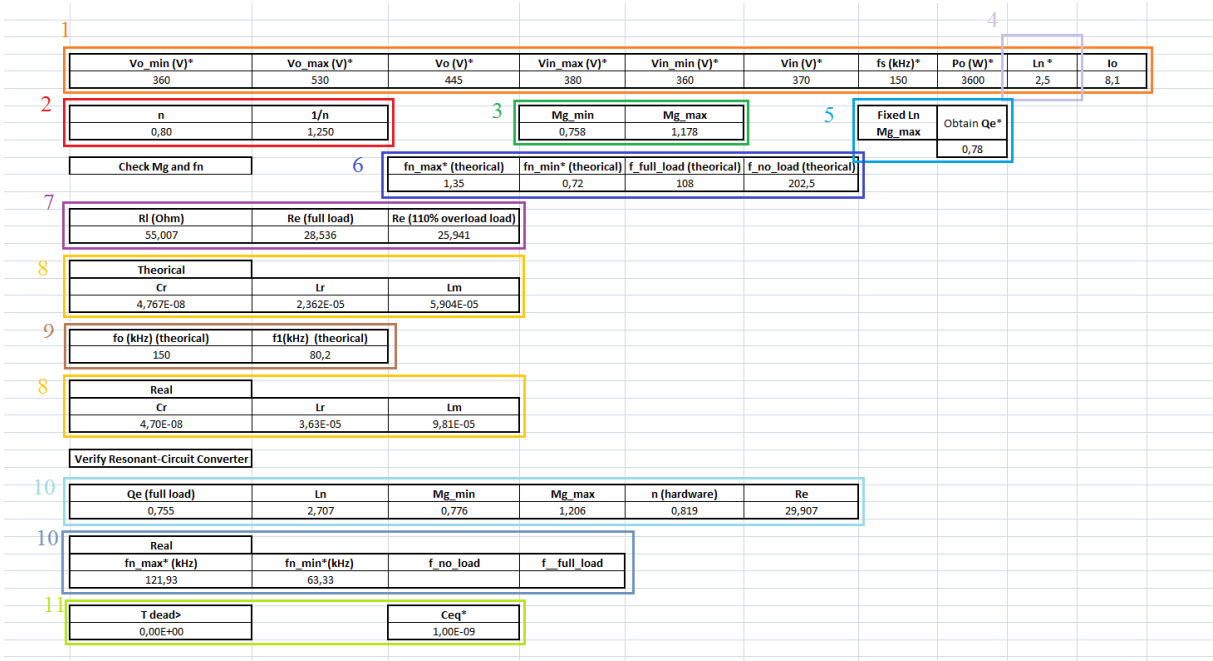

Figure A.1. 1 Helping Excel image

Each step is linked with Figure A.1. 1 Helping Excel image through colour code.

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A.1.1 Define working conditions

- Vo_min*[1]: Minimun output-voltage
- Vo_max*: Maximum output-voltage
- Vin_min*: Minimun input-voltage
- Vin_max*: Minimun input-voltage
- Fs: Switching frequency
- Po: Output-power
- I_o: Output-current

A.1.2 Transformer turn ratio, n

Also, 1/n is calculated (Ansys Simplorer transformer ratio is used as 1/n).

A.1.3 Gain, Mg

A.1.4 Inductance ratio, Ln* and Quality factor, Qe

Different applications may require the selection of unique values for Ln and Qe to achieve an optimal design. However, LLC converters have some things in common that may be used to guide the selection.

For some applications is essential to work in different load conditions, and no load (Qe = 0) is a critical operation point for high input voltage. It is a good point to select first Ln value. With initial_Ln_value.m MAtlab file, different Ln values are tested to obtain optimal initial one, Figure A.1. 2 Initial Ln = 2 value with Qe = 0**.**

[1] Symbol * means this value is an „input“ and has be full-fit by the design

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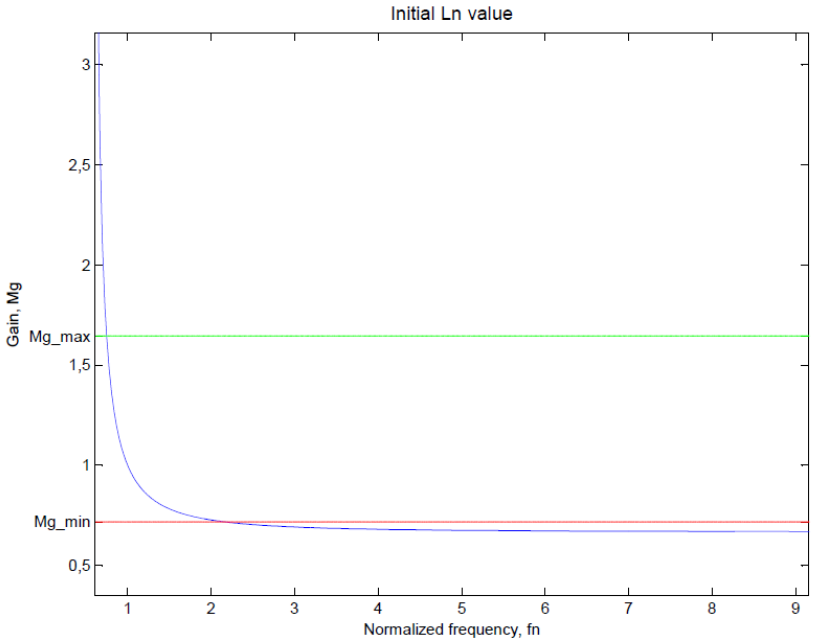

Figure A.1. 2 Initial Ln = 2 value with Qe = 0

```
clear all
Ln=2;
fn=[0.01:0.01:10];
Qe=[0];
Mg=zeros(length(fn),length(Qe));
Mg_max=1.64583;
Mg_min=0.71818;

for j=1:length(Qe)
    for k=1:length(fn)
        Mg(k,j)=abs((Ln*fn(k)^2)/(((Ln+1)*fn(k)^2-1)+((fn(k)^2-1)*fn(k)*Qe(j)*Ln)*i));
    end
end
plot(fn,Mg)
hold on;
plot(fn,Mg_max,'g')
hold on;
plot(fn,Mg_min,'r')
```

Figure A.1. 3 Matlab code

In this file Ln, Mg_max and Mg_min value have to be changed (red square Figure A.1. 3).

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A.1.5 Quality factor, Qe

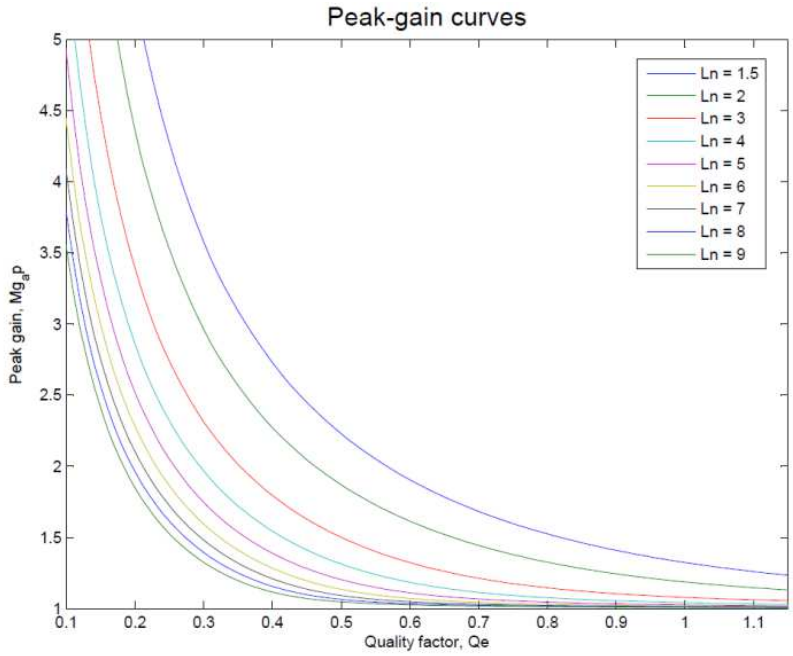

Figure A.1. 4 Mg_ap image for different Ln

Figure A.1. 4 is used to calculate Qe. However, graphically is not exactly enough and *Qe_calculation.m* MATLAB file is used.

```
clear all
Ln=5;
fn=[0.01:0.1:10];
Qe=[0.15:0.01:2];
Mg=zeros(length(fn),length(Qe));

for j=1:length(Qe)
    for k=1:length(fn)
        Mg(k,j)=abs((Ln*fn(k)^2)/(((Ln+1)*fn(k)^2-1)+((fn(k)^2-1)*fn(k)*Qe(j)*Ln)*i));
    end
end

for j=1:length(Qe)
    m(j)=max(Mg(:,j));
end
plot(Qe,m)
Qe
m

```

Figure A.1. 5 Matlab Code

In this file only Ln value has to be changed (red square **Figure A.1. 5)**.

Mg_ap graph and every Qe and Mg_ap values are shown. With your Mg_max value enter to Mg_ap table (Figure A.1. 6) and find his position in the table (For example, Mg_max =

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1.057 -> position 58 - 59).

```
m =

  Columns 1 through 13

    3.2838    3.0788    2.8978    2.7370    2.5930    2.4635    2.3462    2.2396    2.1423    2.0531    1.9710    1.8952    1.8250

  Columns 14 through 26

    1.7599    1.6992    1.6426    1.6052    1.5785    1.5523    1.5265    1.5013    1.4767    1.4525    1.4289    1.4059    1.3833

  Columns 27 through 39

    1.3613    1.3398    1.3188    1.2983    1.2782    1.2587    1.2396    1.2210    1.2028    1.1920    1.1830    1.1741    1.1652

  Columns 40 through 52

    1.1563    1.1475    1.1387    1.1300    1.1213    1.1127    1.1041    1.0998    1.0958    1.0918    1.0878    1.0838    1.0798

  Columns 53 through 65                                  Position 58 - 59

    1.0757    1.0716    1.0675    1.0634    1.0593    1.0572    1.0556    1.0541    1.0525    1.0509    1.0493    1.0477    1.0461

  Columns 66 through 78

    1.0445    1.0428    1.0411    1.0395    1.0378    1.0361    1.0344    1.0327    1.0309    1.0292    1.0274    1.0269    1.0266

  Columns 79 through 91

    1.0262    1.0259    1.0255    1.0251    1.0248    1.0244    1.0240    1.0236    1.0232    1.0229    1.0225    1.0221    1.0217

  Columns 92 through 104

    1.0213    1.0209    1.0205    1.0200    1.0196    1.0192    1.0188    1.0184    1.0179    1.0175    1.0171    1.0166    1.0162

  Columns 105 through 117

    1.0158    1.0153    1.0149    1.0144    1.0139    1.0135    1.0130    1.0126    1.0121    1.0116    1.0111    1.0107    1.0102

  Columns 118 through 130

    1.0097    1.0092    1.0087    1.0082    1.0077    1.0072    1.0067    1.0062    1.0057    1.0052    1.0047    1.0042    1.0037

  Columns 131 through 143

    1.0032    1.0026    1.0021    1.0016    1.0010    1.0005    1.0000    0.9994    0.9989    0.9983    0.9978    0.9972    0.9967

  Columns 144 through 156
```

Figure A.1. 6 Matlab Mg_ap table

With this position in Qe table (Figure A.1. 7), Qe value is obtaned interpolating if it is necessary (Qe = 0.7202 for Mg_max = 1.057).

```
Qe =

  Columns 1 through 13

    0.1500    0.1600    0.1700    0.1800    0.1900    0.2000    0.2100    0.2200    0.2300    0.2400    0.2500    0.2600    0.2700

  Columns 14 through 26

    0.2800    0.2900    0.3000    0.3100    0.3200    0.3300    0.3400    0.3500    0.3600    0.3700    0.3800    0.3900    0.4000

  Columns 27 through 39

    0.4100    0.4200    0.4300    0.4400    0.4500    0.4600    0.4700    0.4800    0.4900    0.5000    0.5100    0.5200    0.5300

  Columns 40 through 52

    0.5400    0.5500    0.5600    0.5700    0.5800    0.5900    0.6000    0.6100    0.6200    0.6300    0.6400    0.6500    0.6600

  Columns 53 through 65                                  Position 58 - 59

    0.6700    0.6800    0.6900    0.7000    0.7100    0.7200    0.7300    0.7400    0.7500    0.7600    0.7700    0.7800    0.7900

  Columns 66 through 78

    0.8000    0.8100    0.8200    0.8300    0.8400    0.8500    0.8600    0.8700    0.8800    0.8900    0.9000    0.9100    0.9200

  Columns 79 through 91

    0.9300    0.9400    0.9500    0.9600    0.9700    0.9800    0.9900    1.0000    1.0100    1.0200    1.0300    1.0400    1.0500

  Columns 92 through 104

    1.0600    1.0700    1.0800    1.0900    1.1000    1.1100    1.1200    1.1300    1.1400    1.1500    1.1600    1.1700    1.1800

  Columns 105 through 117

    1.1900    1.2000    1.2100    1.2200    1.2300    1.2400    1.2500    1.2600    1.2700    1.2800    1.2900    1.3000    1.3100

  Columns 118 through 130
```

Figure A.1. 7 Matlab Qe table

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A.1.6 Obtain fn and check ZVS condition

In this (Matlab file *verification_ZVS_condition.m*) file Ln, Qe, Mg_max and Mg_min value must be changed (red square Figure A.1. 8).

```
clear all
Ln=5;
fn=[0.01:0.01:10];
Qe=0.7202;
Mg=zeros(length(fn),length(Qe));
Mg_max=1.057;
Mg_min=0.75;

for j=1:length(Qe)
    for k=1:length(fn)
        Mg(k,j)=abs((Ln*fn(k)^2)/(((Ln+1)*fn(k)^2-1)+((fn(k)^2-1)*fn(k)*Qe(j)*Ln)*i));
    end
end
plot(fn,Mg)
hold on;
plot(fn,Mg_max,'g')
hold on;
plot(fn,Mg_min,'r')

```

Figure A.1. 8 Matlab Code

The program creates a graphic which allows to obtain fn_max and fn_min (graphically) and to ensure ZVS (Figure A.1. 9).

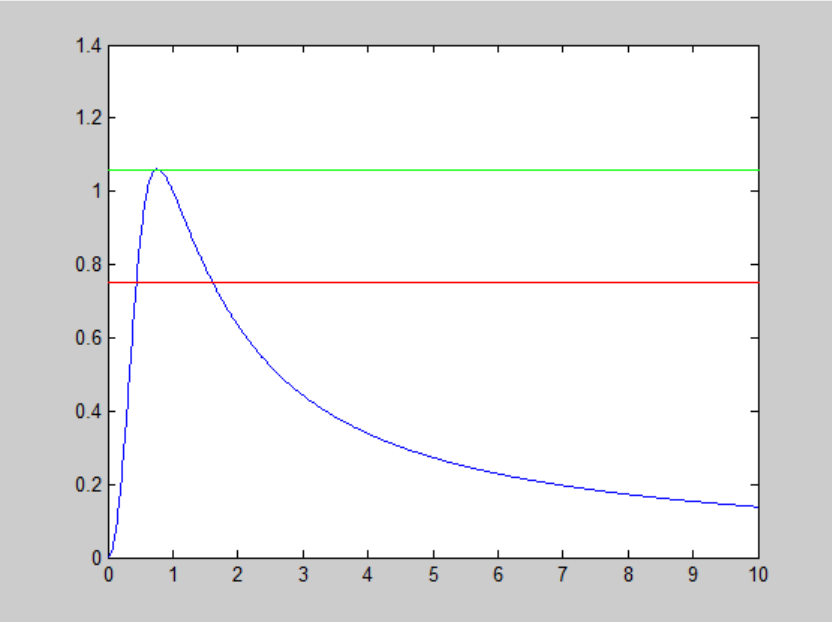

Figure A.1. 9 Matlab Graph

If one verification is not accomplished, process starts again and new values are needed.

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A.1.7 Load resistant (Rl) and equivalent load resistant (Re)

Sometimes it is necessary to guarantee a property behavior when an overload current appears.

A.1.8 Resonant parameters

Real values for components are standard, and real and theoretical can be a bit different.

A.1.9 Resonant frequencies, f1, f0

A.1.10 Verify resonant-circuit converter

Ln, Qe, Mg_min, Mg_max, n and Re are calculated with real values.

A new graph (Matlab file *verification_real_condition.m*) with all the real values to guarantee properly resonant conditions is created.

In this file (Figure A.1. 10) Qe, Ln, Mg_max and Mg_min are changed.

```
clear all
Ln=5;
fn=[0.01:0.01:10];
Qe=[0.7202  0.729];
Mg=zeros(length(fn),length(Qe));
Mg_max=1.057;
Mg_min=0.75;

for j=1:length(Qe)
    for k=1:length(fn)
        Mg(k,j)=abs((Ln*fn(k)^2)/(((Ln+1)*fn(k)^2-1)+((fn(k)^2-1)*fn(k)*Qe(j)*Ln)*i));
    end
end
plot(fn,Mg)
hold on;
plot(fn,Mg_max,'g')
hold on;
plot(fn,Mg_min,'r')
```

Figure A.1. 10 Matlab Code

This graph allows checking a properly resonant behavior, to obtain real fn_max and fn_min

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values.

If this verification is not accomplished, new values for the resonant components are needed.

A.1.11 Dead time, Tdead

Ceq is needed to calculate Tdead.

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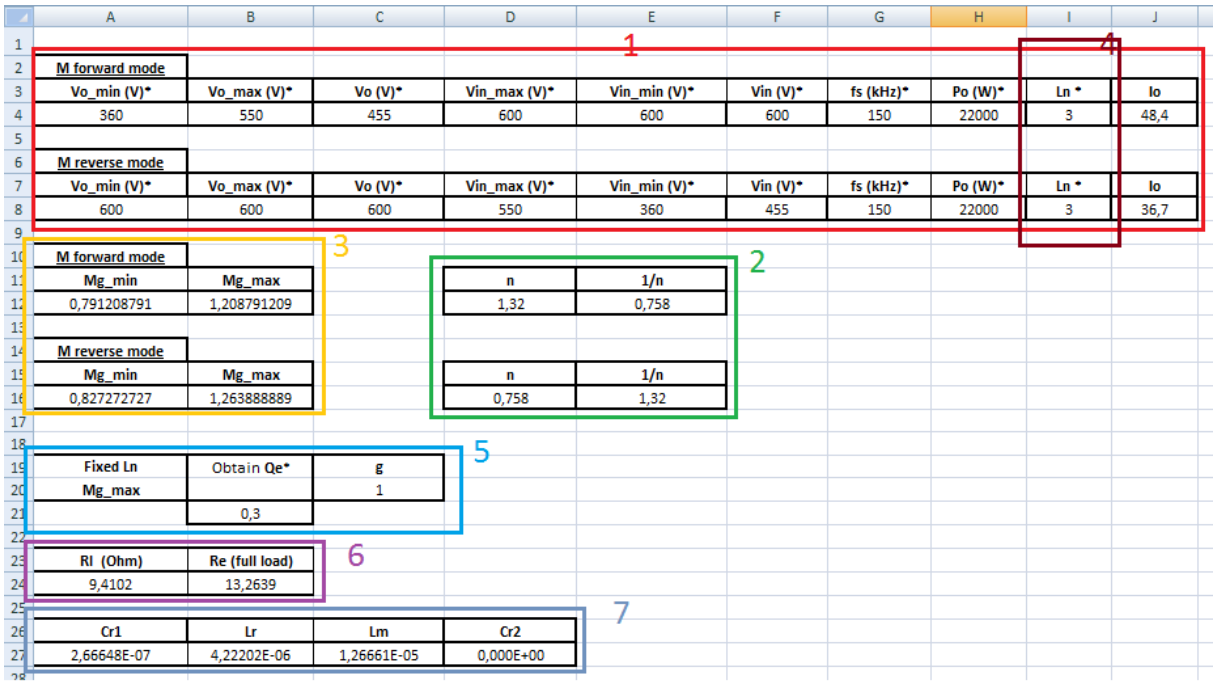
A.2 CLLC RESONANT CONVERTER DESIGNING GUIDE

This guide is a step by step tool for designing CLLC resonant converter parameters. Calculations are in Excel and Matlab.



M forward mode									
Vo_min (V)*	Vo_max (V)*	Vo (V)*	Vin_max (V)*	Vin_min (V)*	Vin (V)*	fs (kHz)*	Po (W)*	Ln *	lo
360	550	455	600	600	600	150	22000	3	48,4
M reverse mode									
Vo_min (V)*	Vo_max (V)*	Vo (V)*	Vin_max (V)*	Vin_min (V)*	Vin (V)*	fs (kHz)*	Po (W)*	Ln *	lo
600	600	600	550	360	455	150	22000	3	36,7

M forward mode	
Mg_min	Mg_max
0,791208791	1,208791209
M reverse mode	
Mg_min	Mg_max
0,827272727	1,263888889

n	1/n
1,32	0,758
n	1/n
0,758	1,32

Fixed Ln	Obtain Qe*	g
Mg_max		1
	0,3	

Rl (Ohm)	Re (full load)
9,4102	13,2639

Cr1	Lr	Lm	Cr2
2,66648E-07	4,22202E-06	1,26661E-05	0,000E+00

Figure A.2 1 Helping Excel image

Each step is linked with Figure A.2 1 Helping Excel image through colour code.

A.2.1 Define working conditions for both modes

- Vo_min*[2]: Minimun output-voltage
- Vo_max*: Maximum output-voltage
- Vin_min*: Minimun input-voltage
- Vin_max*: Minimun input-voltage

[2] Symbol * means this value is an „input“ and has be full-fit by the design

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- Fs: Switching frequency
- Po: Output-power
- I_o: Output-current

A.2.2 Transformer turn ratio, n

Also, 1/n is calculated (Ansys Simplorer transformer ratio is used as 1/n).

A.2.3 Gain, Mg

A.2.4 Inductance ratio, Ln*

Different applications may require the selection of unique values for Ln and Qe to achieve an optimal design. However, CLLC converters have some things in common that may be used to guide the selection.

For some applications is essential to work in different load conditions, and no load (Qe = 0) is a critical operation point for high input voltage. It is a good point to select first Ln value. With initial_Ln_value.m MAtlab file, different Ln values are tested to obtain optimal initial one in Figure A.2 1.

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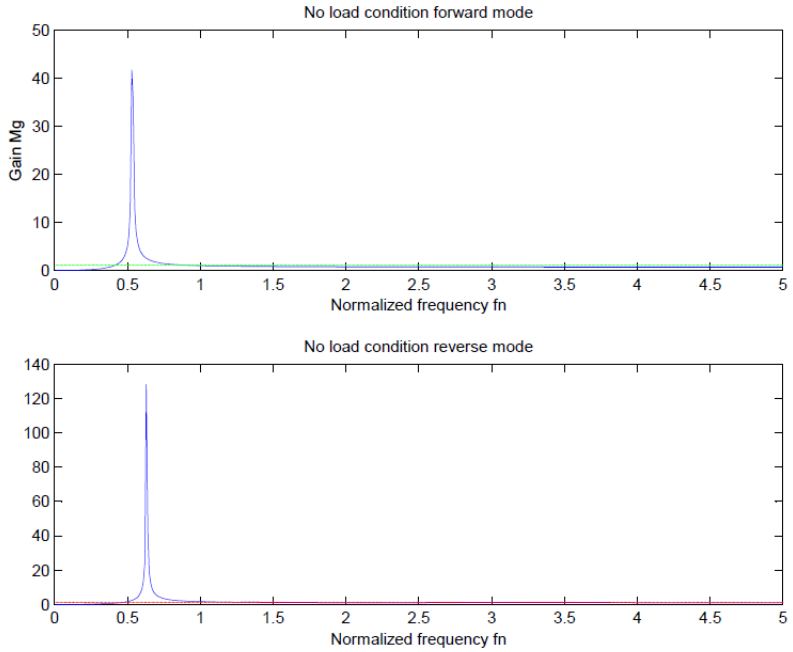

Figure A.2 2 Initial Ln = 2.5 value with Qe = 0

```
clear all
Ln=2.5;
fn=[0.01:0.01:5];
Qe=[0];
gx=1;
Mg=zeros(length(fn),length(Qe));
Mg_min_mode1=1.1;
Mg_min_mode2=1.2;

for j=1:length(Qe)
    for k=1:length(fn)
        Mg4(k,j)=abs(1/((1/Ln+1-1/(Ln*(fn(k))^2))-(Qe(j)*((1/fn(k))-fn(k))+Qe(j)*(1+Ln)/(gx*Ln*fn(k))-Qe(j)/(gx*Ln*(fn(k))^3))*i));
    end
end

for j=1:length(Qe)
    for k=1:length(fn)
        Mg11(k,j)=abs(1/((1-1/(Ln*(fn(k))^2))-(Qe(j)*(1/fn(k)-fn(k))+Qe(j)*(1+Ln*gx)/(Ln*fn(k))-Qe(j)*gx/(Ln*(fn(k))^2))*i));
    end
end

subplot(2,1,1)
plot(fn,Mg4)
hold on;
plot(fn,Mg_min_mode1,'g')
title('No load condition forward mode')
xlabel('Normalized frequency fn')
ylabel('Gain Mg')
subplot(2,1,2)
plot(fn,Mg11)
hold on;
plot(fn,Mg_min_mode2,'r')
title('No load condition reverse mode')
xlabel('Normalized frequency fn')
ylabal('Gain Mg')
```

Figure A.2 3 Matlab code

In this file Ln, gx, Mg_max_mode1 and Mg_max_mode2 value have to be changed (red square Figure A.2 3).

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A.2.5 Quality factor, Qe and g

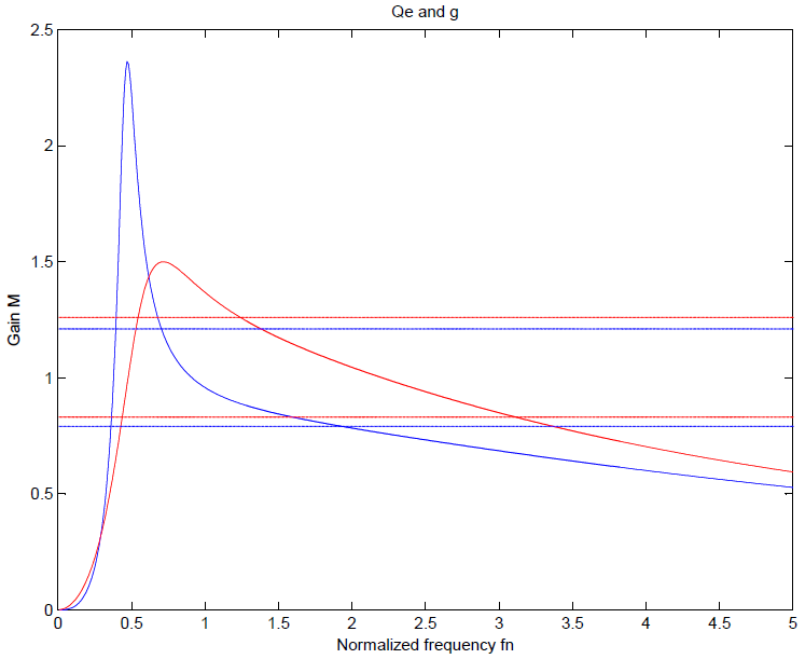

Figure A.2 4 Curves for Qe and g

Figure A.2 4 is used to calculate Qe and g. Different values of Qe and g are tried looking for the combination that guarantied designing requirements in Qe_g.m Matlab file.

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```
clear all
Ln=3;
fn=[0.01:0.01:5];
Qe=[0.3];
gx=1;
Mg4=zeros(length(fn),length(Qe));
Mg4_max=1.21;
Mg4_min=0.79;
Mg11_max=1.26;
Mg11_min=0.83;

for j=1:length(Qe)
    for k=1:length(fn)
        Mg4(k,j)=abs(1/((1/Ln+1-1/(Ln*(fn(k))^2))-(Qe(j)*((1/fn(k))-fn(k))+Qe(j)*(1+Ln)/(gx*Ln*fn(k))-Qe(j)/(gx*Ln*(fn(k))^3))*i));
    end
end

Mg11=zeros(length(fn),length(Qe));
for j=1:length(Qe)
    for k=1:length(fn)
        Mg11(k,j)=abs(1/((1-1/(Ln*(fn(k))^2))-(Qe(j)*(1/fn(k)-fn(k))+Qe(j)*(1+Ln*gx)/(Ln*fn(k))-Qe(j)*gx/(Ln*(fn(k))^2))*i));
    end
end

plot(fn,Mg4,'b')
hold on;
plot(fn,Mg11,'r')
hold on;
plot(fn,Mg4_max,'b')
hold on;
plot(fn,Mg4_min,'b')
hold on;
plot(fn,Mg11_max,'r')
hold on;
plot(fn,Mg11_min,'r')
xlabel('Normalized frequency fn')
ylabel('Gain M')
title('Verification conditions')
```

Figure A.2 5 Matlab Code

In this file Qe, Ln, Mg4_max, Mg11_max, Mg4_max and Mg11_max are changed (red square Figure A.2 5).

Figure A.2 4 can also be used to check ZVS condition.

A.2.6 Load resistant (Rl) and equivalent load resistant (Re)

Sometimes it is necessary to guarantee a property behavior when an overload current appears.

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A.2.7 Resonant parameters

Resonant parameters are obtained

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A.3 INDUCTANCE ANALYSIS FOR TRANSFORMERS

For resonant applications the transformer parameters are very important, especially inductance. In this chapter, an analysis of transformer inductance is done trying to optimize the resonant converter building process presented previously.

A.3.1 Theoretical summary

Electrical Power Transformer is a static device which transforms electrical energy from one circuit to another without any direct electrical connection and with the help of mutual induction between two windings.

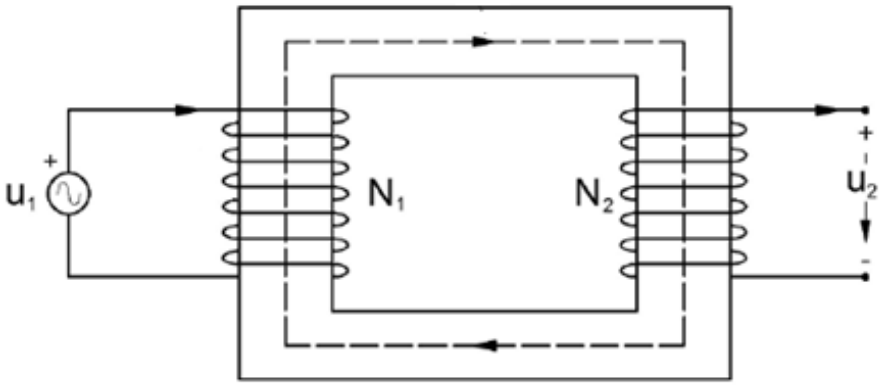

Figure A.3 1 Electrical transformer

The equivalent transformer circuit is very useful to understand the transformer behavior. It is possible to build an equivalent circuit that takes care about transformer characteristics.

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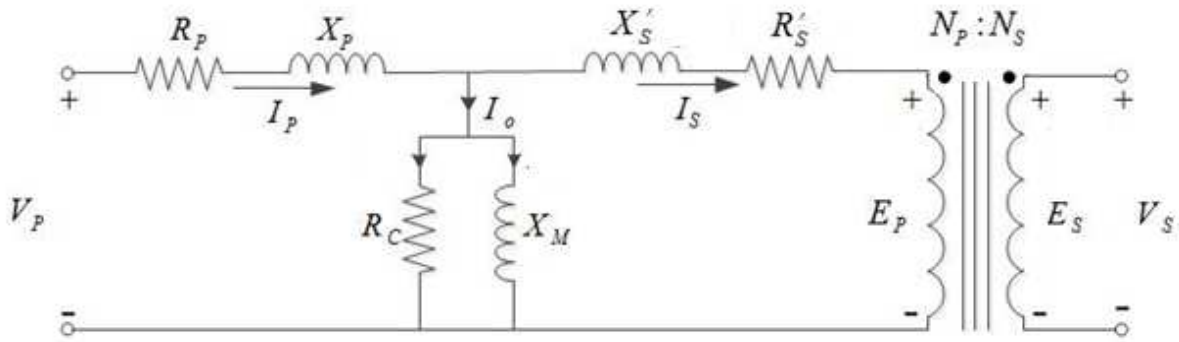

Figure A.3 2 Exact equivalent transfomer circuit

Open circuit test and short circuit test are useful to know more about transformer parameters. In this case, the tests are focused on inductance analysis.

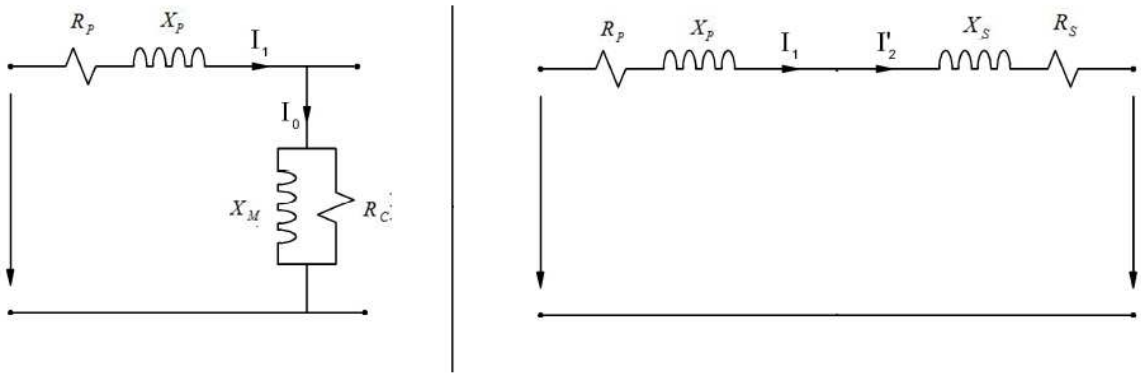

Figure A.3 3 a) Open circuit test equivalent circuit. 3b) Short circuit test equivalent circuit

A.3.2 Winding model

The three winding models, used in this analysis, are presented looking for different inductance values in Figure 4.2.

Depending on the winding distribution the values of the inductances are different.

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A.3.3 Analysis

A.3.4.1 Transformer details

The transformer details, used in this analysis, are presented:

- ETD – 49
- n ≈ 0.8
- Np = 23
- Ns = 29
- S = 2.5 mm^2
- Isolated

A.3.4.2 Results

The results obtained through experimental measurement are presented.

- Model 1

Table 1 Inductance values for model 1

Airgap (mm)	Loc_p	Lcc_p	Loc_s	Lcc_s	n	Lr	Lm	Ln
0	665,8	39,07	1039,7	67,07	0,800	39,07	626,73	16,04
0,5	248,2	38,4	413,2	64,03	0,775	38,4	209,8	5,46
1	149,78	37,49	251,9	63	0,771	37,49	112,29	3,00
1,5	119,05	37,24	194,91	60,95	0,782	37,24	81,81	2,20
2	102,71	36,85	162,32	58,22	0,795	36,85	65,86	1,79

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- Model 2

Table 2 Inductance values for model 2

Airgap	Loc_p	Lcc_p	Loc_s	Lcc_s	n	Lr	Lm	Ln
0	2051	7,26	3268	11,39	0,792	7,26	2043,74	281,51
0,5	279,8	7,22	452,6	11,64	0,786	7,22	272,58	37,75
1	165,7	7,19	271,7	11,66	0,781	7,19	158,51	22,05
1,5	121,94	7,1	201,8	11,66	0,777	7,1	114,84	16,17
2	97,35	6,93	162,55	11,64	0,774	6,93	90,42	13,05

- Model 3

Table 3 Inductance values for model 3

Airgap (mm)	Loc_p	Lcc_p	Loc_s	Lcc_s	n	Lr	Lm	Ln
0	832,1	12,76	1257,5	18,78	0,813	12,76	819,34	64,21
0,5	249,9	12,45	384	18,93	0,807	12,45	237,45	19,07
1	151,91	12,08	238,9	18,97	0,797	12,08	139,83	11,58
1,5	120,23	11,93	191,34	18,94	0,793	11,93	108,3	9,08
2	96,9	11,73	155,73	18,77	0,789	11,73	85,17	7,26

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