ARISTOTLE UNIVERSITY OF THESSALONIKI
FACULTY OF PHYSICS
ELECTRONICS DEPARTMENT

FINAL PROJECT THESIS

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ANALYSIS AND DESIGN OF PFDs IN CADENCE

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Thanks Andriana Voulkidou for your help and time

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CHAPTER 1

INTRODUCTION

1.1 PRESENTATION

According to most of the actual Scientifics, nowadays, it is difficult to find a device as versatile as the PLL in the frequency world. It can be used, for example, as AM, FM and FSK demodulator; frequency conversion or signal regenerator.

It is also important to remind that behind an achievement as PLL can be considered in the IC world; there are always hidden minds and, also, hidden components. That is the case of the Phase Detector circuit.

Its improvement, in order to accommodate the latest technological advances such as high performance, high speed operating speed and low noise, is being considered over the last decades.

1.2 STUDY AREAS

This project will try to provide better understanding of Phase detectors, more specifically of the Phase Frequency Detectors; analysis some designs that presents very interesting properties.

The main tool of this study will be CADENCE Design Systems. It is the main IC software design and the most used by circuit designers.

1.3 GENERAL OBJETIVES

This study, which is summarized in this report, aims to show the characteristics and behavior of some PFD designs in order to improve some important aspects as the delay time and the power consumption in the classical model.

For this, CADENCE environment will be used, taking advantage of its potential and versatility in the design, implementation and analysis of IC circuits.

The aim of this thesis is to deepen the concept of the PFD, to know its basic performance and recognize their limitations in order to resolve them in future designs as the ones which are shown here. So, watching the properties of these new designs will be able to choose one or the other depending on the benefits and drawbacks of each.

CHAPTER 2

THEORICAL BASIS

2.1 PHASE LOCKED LOOPS

2.1.1 CONCEPT AND COMPONENTS

A Phase-Locked Loop (PLL) is a closed-loop circuit that compares its output phase with the phase of an incoming reference signal and adjusts itself until both are aligned, i.e., the PLL output's phase is "locked" to that of the input reference. It is composed by a phase detector (PD), a low-pass filter (LPF), and a voltage controlled oscillator (VCO).

The circuit compares the input signal phase and the oscillator output signal and adjusts the last one to maintain the phases matched. As it is known, the frequency is the derivate of phase. So, maintaining phases matched means maintaining matched frequencies.

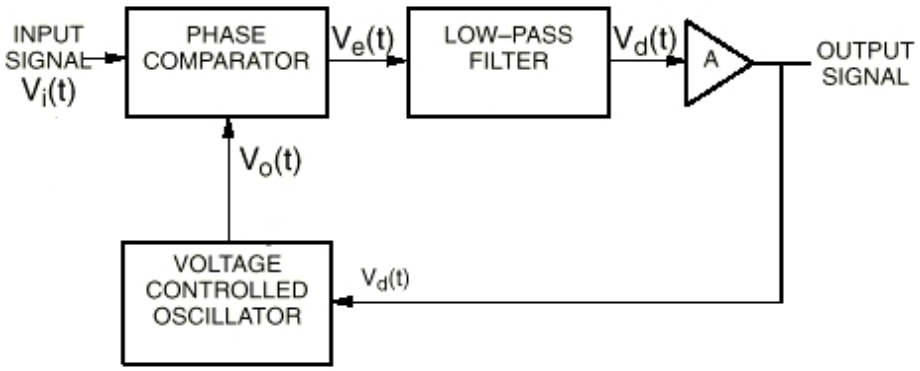


Fig.2.1 Basic PLL block diagram

When there is not input signal in the circuit, the $V_d(t)$ voltage that controls the VCO is zero. And its oscillation frequency is f_o (free oscillation frequency). In contrast, when there is an input signal in the circuit with frequency f_i, the phase detector device

compares the phase and frequency of this input signal with the $V_o(t)$ signal. This comparator generates an error voltage $V_e(t)$ which is proportional to the phase and frequency difference between the two signals. Then, this error voltage $V_e(t)$ after been filtered and (sometimes) amplified is applied to the VCO input. So, VCO frequency varies to reduce the difference between the frequencies f_o and f_i. Once the loop is locked (the phase difference between the output and the input signals is very close to zero) the frequency of the output signal is equal (or a multiple) of the input signal's frequency.

- **Phase Detector:** This dispositive has got two input signals: the reference input signal and the feedback from the VCO**.**

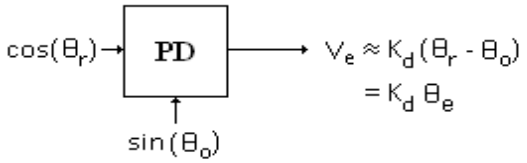


Fig.2.2 Phase detector

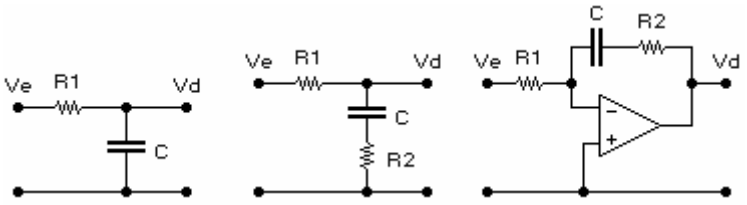
An ideal phase detector (PD) produces an output signal whose dc value is linearly proportional to the difference between the phases of the two periodic inputs. Typically, the width pulse is equal to the time difference between consecutive zero crossings of the two inputs.

There are several types of phase detectors in the two main categories of analog and digital environment, depending on the kind of application. Most of the analog phase detectors are just analog multipliers: their output voltage is proportional to the multiplication of the two input voltages. And their main advantage is that they can be used in a large frequency range. In the other hand, the most popular and simplest in the digital world is the XOR gate.

These models and other ones will be detailed later on.

- **Low pass filter:** It receives the error voltage signal Ve(t) and suppresses high-frequency components in it, allowing the dc value to control the VCO frequency.

  It has the important function to eliminate noise and high-frequency components (including harmonic frequency components). The most common designs in PLL applications are shown in Fig. 2.3.



$$F_A(s) = \frac{1}{1+sT_1} \qquad F_B(s) = \frac{1+sT_2}{1+s(T_1+T_2)} \qquad F_C(s) = \frac{1+sT_2}{sT_1}$$

Where $T_1=R_1C$ and $T_2=R_2C$.

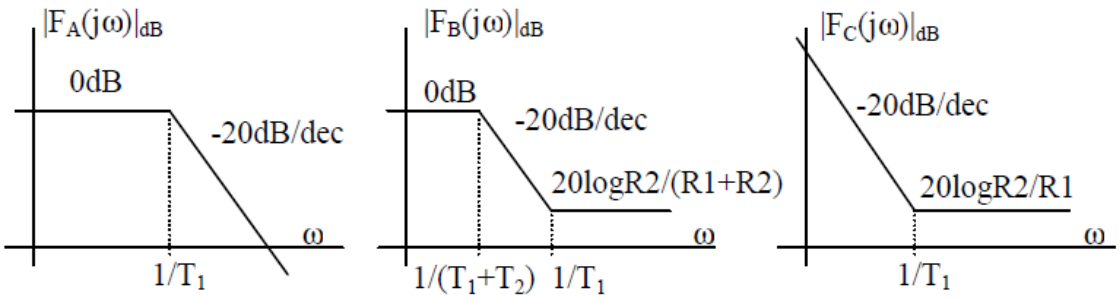


Fig.2.3 Most common LPF designs in PLL circuits

- **Voltage controlled oscillator:** It is an electronic oscillator designed to be controlled in oscillation frequency by a voltage input. The frequency of oscillation is varied by the applied DC voltage; being proportional to this input voltage.

  When the input voltage is zero, the VCO output signal will have a frequency called "free oscillation frequency" and when the input signal changes, the output frequency increases or decreases proportionality. It has an integrator function for the phase input signal.

It is typically build with varicap diodes and crystal quartz. They are very sensitive to weather conditions. Fig.2.4 shows its operation through some waveforms.

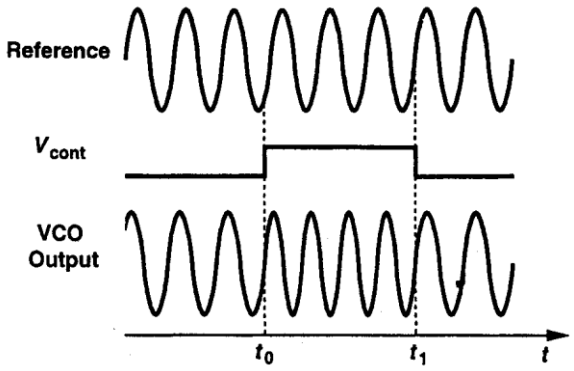


Fig.2.4 VCO output wave

Next fig.2.5 and fig.2.6 shows the waveforms of the different components in a PLL. The first one illustrates a typical situation where the two input signals have the same frequency but a small phase difference between them. So, the PD generates a signal according to this phase difference. Besides, the LPF avoids the high frequency components in the PD output and generates the dc voltage that controls the VCO.

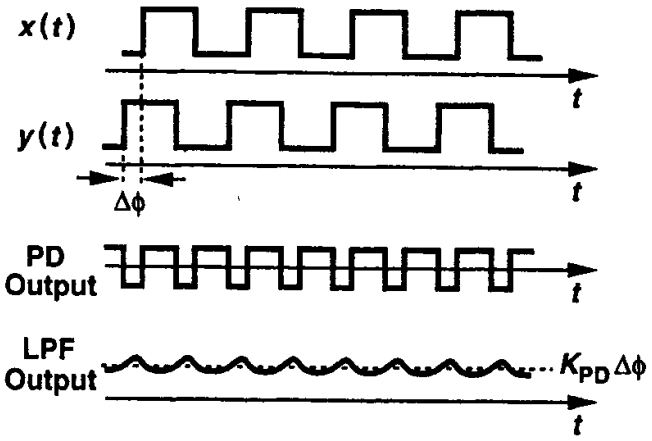


Fig.2.5 PLL operation

Fig.2.6 shows the PLL behavior in the situation where there is a frequency change when it is already locked.

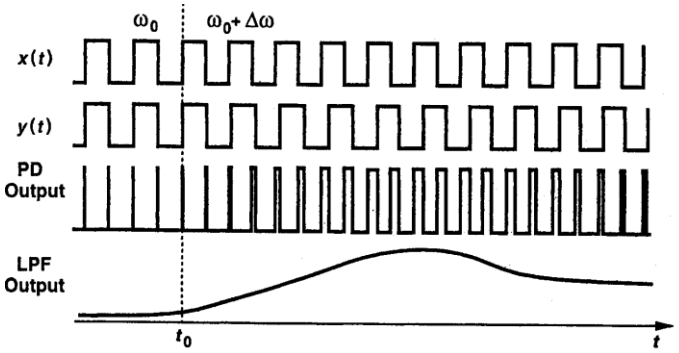


Fig.2.6 Response of a PLL to a small frequency step

2.1.2 HISTORY OF PLLS

Historically, earliest research towards what became known as the phase-locked loop goes back to 1932, when British researchers developed an alternative to Edwin Armstrong's super heterodyne receiver, the Homodyne or direct-conversion receiver. The technique was described in 1932, in a paper by Henri de Bellescize, in the French journal *L'Onde Électrique*. Besides, in analog television receivers since at least the late 1930s, phase-locked-loop horizontal and vertical sweep circuits are locked to synchronization pulses in the broadcast signal. When Signetics introduced a line of monolithic integrated circuits that were complete phase-locked loop systems on a chip in 1969, applications for the technique multiplied. A few years later RCA introduced the "CD4046" CMOS Micropower Phase-Locked Loop, which became a popular integrated circuit.

2.2 PHASE DETECTOR AND PHASE/FREQUENCY DETECTOR

2.2.1 PHASE DETECTOR (PD)

- Ideal phase detector: an ideal phase detector (PD) produces an output signal whose dc value is linearity proportional to the difference between the phases **(Δϕ)** of the two periodic inputs.

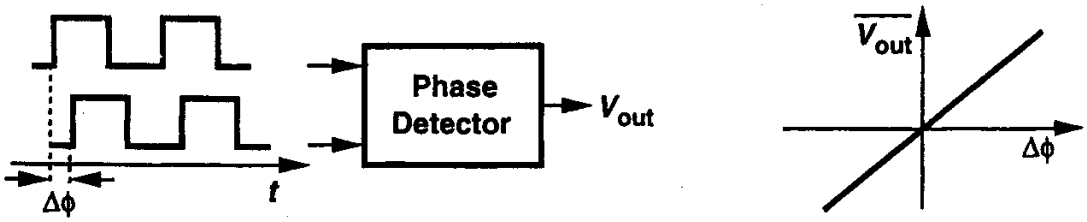


Fig.2.7 Characteristic of an ideal PD

Typically, PD generates an output pulse whose width is equal to the time difference between the consecutive zero crossing of the two inputs. Since the two inputs are not equal, the phase difference exhibits a "beat" behavior with an average value of zero.

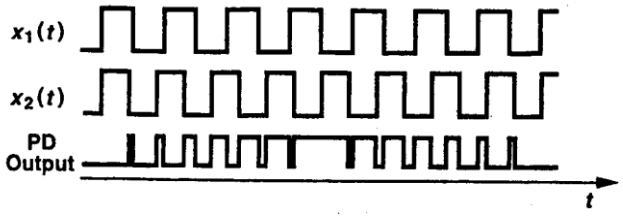


Fig.2.8 Input and output waveforms of a PD

- Real phase detector: The implementation described above is not possible to be realized in practice. If, for example, the difference between the two frequencies of the two input signals is constant, the phase error which increases in time will produce an increasing DC voltage in the output of the detector. And this is not possible because of the transistors saturation. So, really, the real phase detector has not got a lineal characteristic and usually its phase error detector range is finite.

    - Analog phase detector: it is an analog multiplier. Its characteristic is shown in fig.2.9.

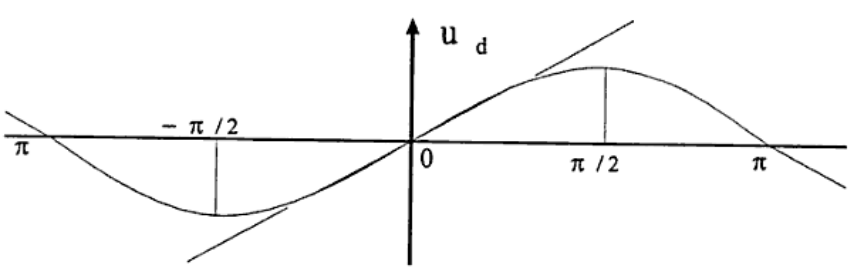
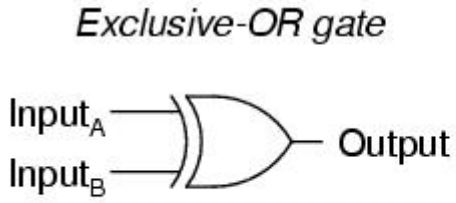


Fig.2.9 Characteristic of an analog phase detector

As it is shown in the above figure, when the phase error is small (smaller than 60º) this phase detector could be considered as an ideal one. Besides, when the phase error is smaller than 90º, the output voltage increases when the phase error increases while this relation is not linear, at least the phase detector works. But, in contrast, when the phase error is bigger than 90º, the output voltage decreases; so, this means a malfunction.

- Digital phase detector: Its output is a rectangular signal whose average value is proportional to the phase error.

The simplest implementation of this kind of detectors is an X-OR digital gate; whose inputs are the reference signal and the VCO output.



A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

Fig.2.10 XOR gate phase detector and operation

In Fig. 2.11 the XOR phase detector characteristic is shown. According to it, this phase detector is perfectly linear: its output voltage is exactly proportional to the phase error. But, if the phase error is greater than 180º the characteristic loses its linearity and the output voltage is not proportional to this error anymore.

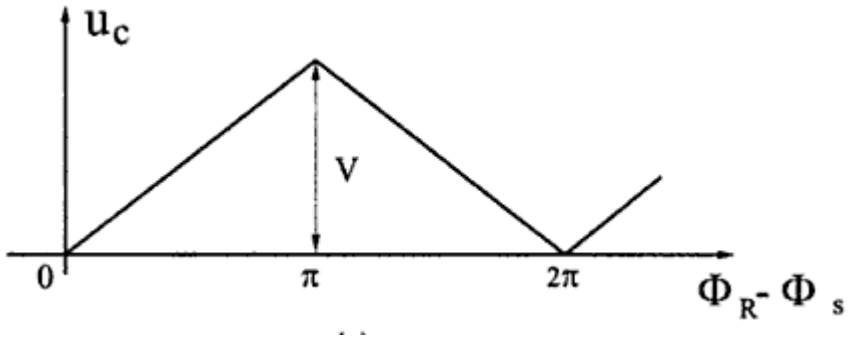


Fig.2.11 XOR phase detector characteristic

Commonly, this characteristic is lightly modified to distinguish between positive and negative phase differences. The definitive characteristic is shown in fig.2.12.

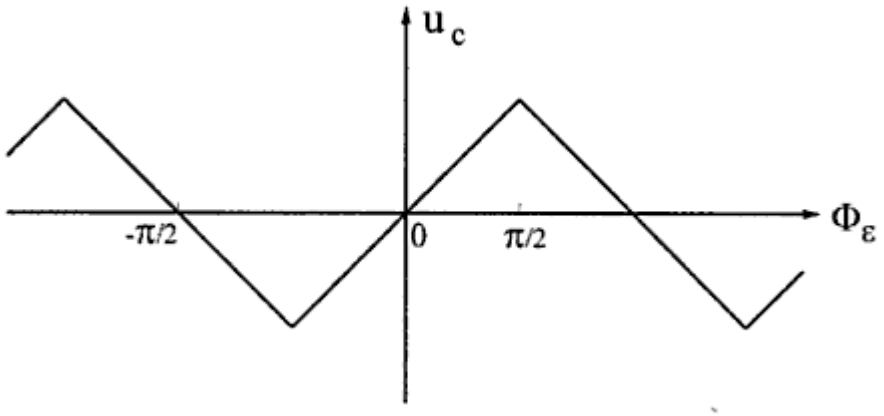


Fig.2.12 Popular XOR phase detector characteristic

Thus, this digital phase detector has the same operation range than the analog one but it has the advantage that it is more linear in it.

View this XOR implementation, it is important to say that there are other structures also used as the BJ bistable whose linear range is the maximum one, 360º.

2.2.2 PHASE FREQUENCY DETECTOR (PFD)

These special detectors are allowed to detect both phase and frequency difference proves extremely useful because it significantly increases the acquisition range and lock speed of PLLs.

Unlike multipliers and XORs, sequential phase/frequency detectors (PFDs) generate two outputs that are not complementary. The operation of a typical PFD is illustrated in Fig.2.13.

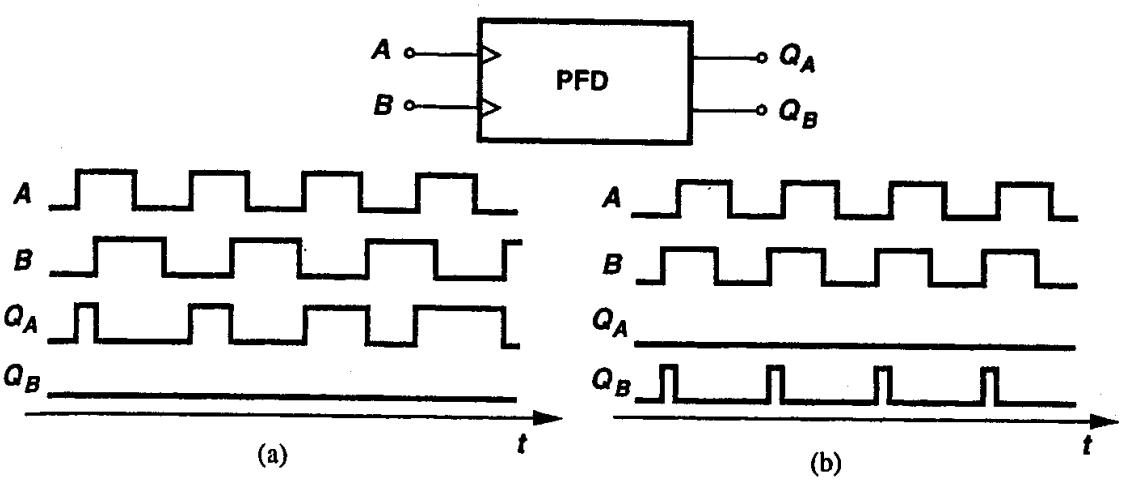


Fig.2.13 Operation of a typical PFD

It works as follows: If the frequency of input A is greater than that of input B, then the PFD produces positive pulses at Q_A, while Q_B remains zero. Conversely, if frequency in input B is greater than in A, positive pulses appear at Q_B while Q_A=0. If both frequencies are equal, then the circuit generates pulses at either Q_A and Q_B with a width equal to the phase difference between the two inputs. Thus, the average value Q_A-Q_B is an indication of the frequency or phase difference between A and B. The outputs Q_A and Q_B will be called UP and DOWN signal, respectively.

This basic PFD is also called “three states PFD”. That is why it can be understood also as a three state machine as follows:

	STATE 0	STATE I	STATE II	NO ALLOWED STATE
Q_A (UP)	0	1	0	1

Q_B (DOWN)	0	0	1	1

The circuit can change state only on the rising transitions of A and B. Fig. 2.14 shows a state diagram summarizing the operation: If the PFD is in state 0, a transition on A takes in to state I. In this situation, if a transition occurs on B, the PFD returns to state 0. Similarly between state 0 and state II.

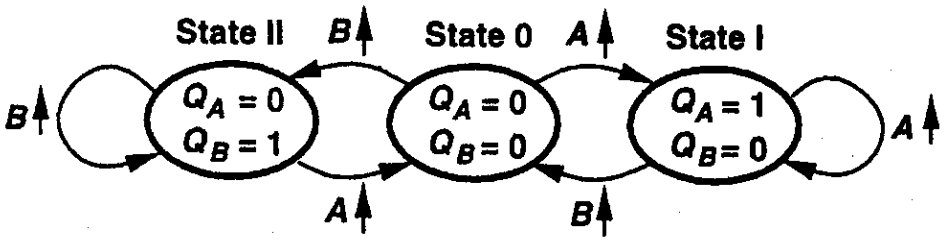


Fig.2.14 State diagram of a PFD

According to all of this, in case that Fref is a little bit higher than Fvco, the subtraction UP-DOWN will be positive. And, the control signal that arrives at the VCO system, will force it to increase its output frequency. In contrast, if Fvco is higher than Fref, this subtraction will be negative and it will produce the contrary effect.

The most popular implementation of the above PFD is shown in Fig. 2.15. It is formed by two D-FF and an AND gate. Each D-FF is activated by the CK signal where the input PFD signals are (ref and VCO). That way, as the D input of the D-FF is always "1", the Q (output of the D-FF) will be up at the moment of a positive rising edge in the CK input (in the PFD inputs, respectively).

When the two outputs of the two D-FF are in the "high" state (state not allowed), they will be reset by the reset signal generated by the AND gate output whose inputs are Up and Dn. In this moment, both outputs become down again.

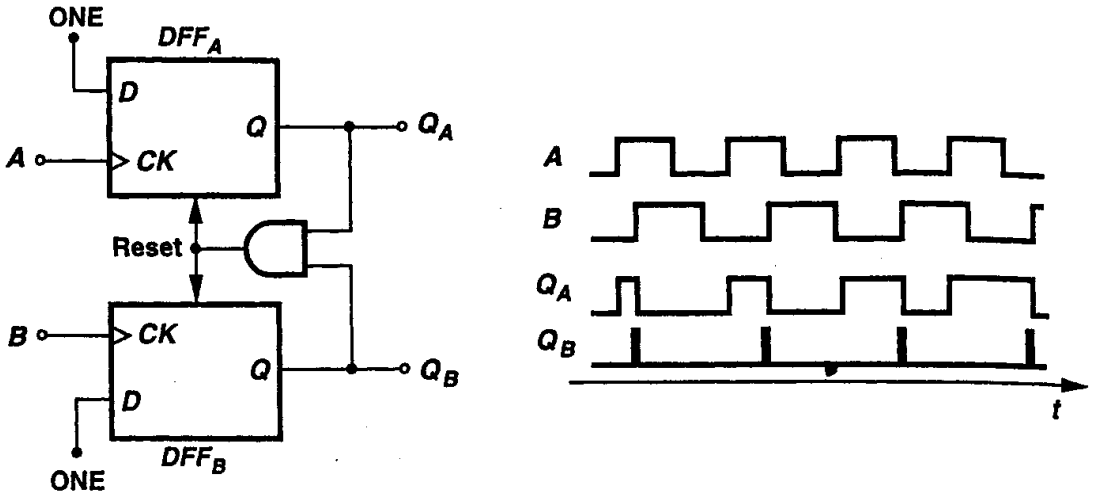


Fig.2.15 PFD implementation

Besides, the Fig. 2.16 shows the input-output characteristic of the PFD.

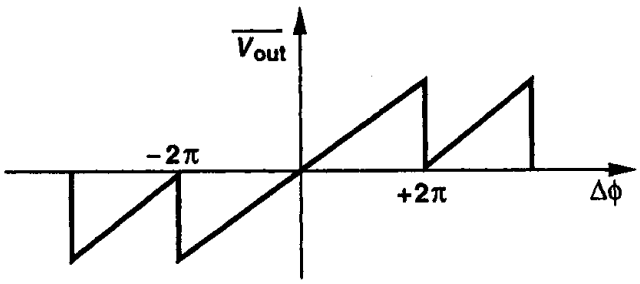


Fig.2.16 PFD characteristic

- The use of the Charge Pump (CP): It is a circuit whose aim is to convert to DC the PFD output voltage. Next figure (fig. 2.17) illustrates this circuit.

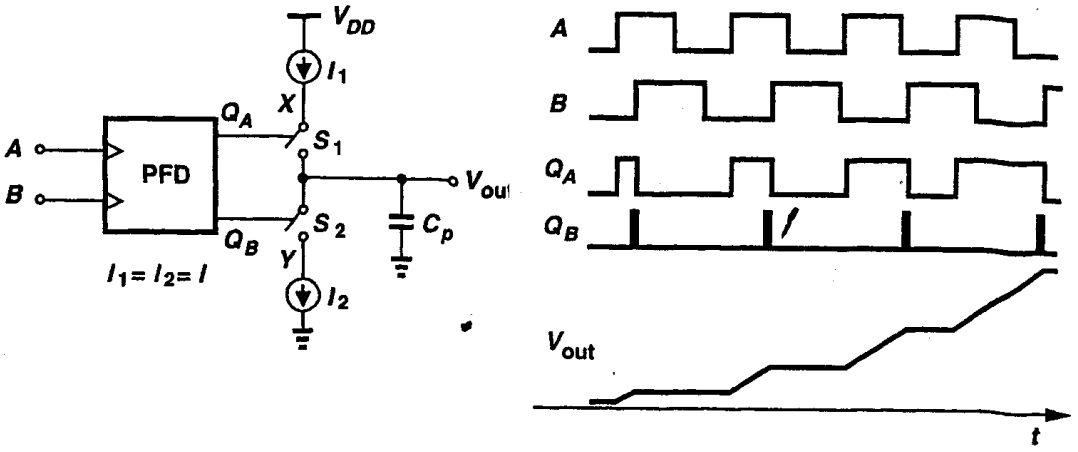


Fig.2.17 PFD and charge pump circuit

It consists of two switched current sources (S_1 with I_1 and S_2 with I_2) driving a capacitor (Cp). Its operation depends on the state of the PFD: in state 0, both switches remain opened. So, the capacitor voltage does not change from its last value, V_{out}. In state I, where A leads B, S_1 closes and I_1 source charges Cp. In state II, S_2 closes and I_2 removes charge from Cp.

This circuit is widely used in PLLs where there are PFDs. So, instead of a PD and a LPF, these PLLS called Charge-pump PLLs (CPPLLs), presents a PFD and a CP. This new model has the advantage that the capture range is now only limited by the VCO output frequency range and that the static phase error is zero if mismatches and offsets are negligible.

Next figure 2.18 shows the mentioned circuit.

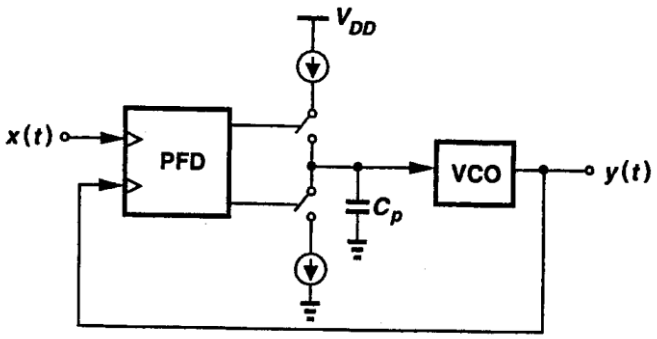


Fig.2.18 Charge-pump PLL

- Problems in the conventional PFD: To improve the operating speed of PFD, both the pulse width and the propagation delay of reset signal need to be reduced. In the previous design, the reset signal is structurally affected by the DFF delay. To improve the operating speed of PFD, both the pulse width and the propagation delay of the reset signal need to be reduced.

  According to that, the way to decrease the width pulse and the delay of the reset signal (and so, increase the speed of operation) is to reduce these two delays, avoiding its dependence with the DFF device.

Below, two different methods to achieve this goal are presented:

- **PFD with dynamic CMOS logic**

  This improvement attempt consists on redesign the D-FF device using dynamic logic instead static one. Dynamic CMOS logic circuits are constructed with small transistor number and also, reduce parasitic node capacitance compared with static CMOS logic.

  This new design could be over twice as fast as with static logic. It uses only fast N transistors, and is amenable to transistor sizing optimizations. Static logic is slower because it has twice the loading, higher thresholds, and actually uses slow P transistors to compute things.

  In it, propagation delay and pulse width of the reset signal are shorter than in the conventional one and it can improve the frequency limit of the PFD. The only disadvantage of the dynamic CMOS circuit is its high power consumption.

- **Feedforward-reset design**

  A new design of the PFD will be presented in the next chapter, and it will be analyzed step by step.

CHAPTER 3

FEEDFORWARD-RESET PFD

3.1 DESIGN

This new PFD model is described in "Phase Detectors/Phase Frequency Detectors for High Performance PLLs" article; by Hiroyasu Y, Kenji T. and Kenichi N. And its goal is to avoid de bad effect of the D-FF in the PFD behavior and, so, to use it in more exigent applications.

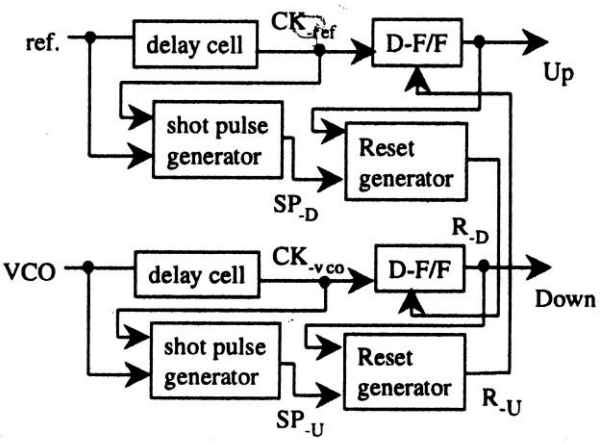


Fig. 3.1 Feedforward reset PFD

Its improvement consists of removing the dependence that the reset signal has with the D-FF. That way, the D-FF delay will not affect the width and the delay of this signal and a higher operation speed will be achieved.

3.2 COMPONENTS

This parallel and symmetrical configuration is composed by several blocks (which are duplicated for each input signal: ref and VCO) that are described below:

- *Delay cell*: it takes the input signal and gives it a delay. Its output is called "CK-ref" or "CK-vco", respectively. It could be implemented by some inverters (even number for not invert the signal), as in the conventional one.

This way, the delayed input signals are obtained and they will be in D-FF input, respectively.

It is possible to control the introduced delay by the method of logical effort. It is a straightforward technique used to estimate delay in a CMOS circuit. Used properly, it can aid in selection of gates for a given function and sizing gates to achieve the minimum delay possible for a circuit. Delay is expressed in terms of a basic delay unit, $\tau = 3RC$, the delay of an inverter driving an identical inverter with no parasitic capacitance.

Really, the delay can be done by many ways (for example, all logic gates introduce some delay) but the use of the inverters gives to the circuit simplicity and it does not need too much circuitry.

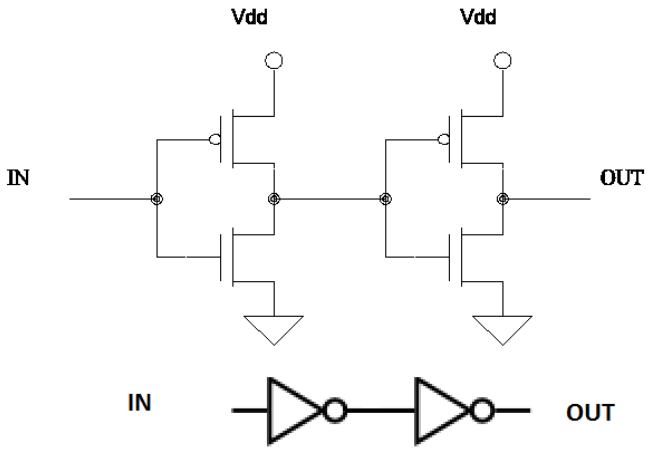


Fig.3.2 Delay cell

After, in the simulation, some problems with them will be appointed.

- *Shot pulse generator:* it generates a pulse that will activate the "reset generator". It has two input signals: the original input signal (ref and VCO in each branch) and the delayed by the delay cell input signal.

  It will produce a pulse at the same time as the one of its inputs will be active first, so, the ref or the VCO signal, respectively. The second input, the delayed ref or VCO signal, determinates de width of the pulse.

- *Reset generator:* it is implemented as an OR gate whose inputs are the D-FF output signal and the "shot pulse generator" output. So, at the output of this item we will have the reset signal that will reset the other input signal D-FF output. This signal will start at the same time as the ref or VCO signal because of the OR gate operation which is shown in the following fig.3.3.

  So, reset signal will be active always that one of the OR inputs will be active. That way, the dependence that the signal had with the D-FF delay in the classical model of a PFD is avoided.

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1

Fig.3.3 OR logic gate operation

- *D-FF:* As it is known, it conserves the value of the D input in its Q output while the clock signal is active. In the design of this new PFD it is only described with one input, so, the delayed PFD input signal will act as the clock signal (CLK) of the D-FF. And D input in the D-FF will be a constant "1" signal.

  That way, at the output of it, Up and Down signals will be CKref and CKvco, respectively, according to the reset signal described before.

  This reset signal, when it will be active, will deactivate D-FF signal, resetting the D-FF dispositive. Then, the outputs will be active again until a new up (or down, depending on the D-FF) rising edge in the input will active the output again.

  Besides, the fact that one reset signal is introduced in the other D-FF, allows a kind of synchronism between the two PFD outputs: Up and Down.

  The following figure illustrates the D-FF operation.

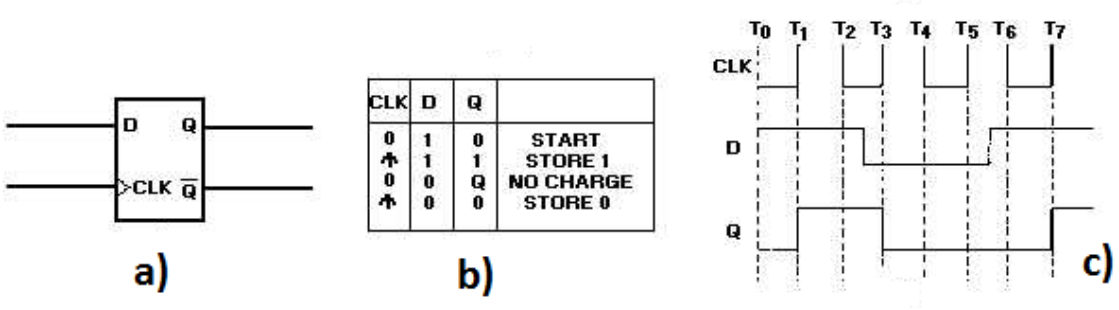


Fig.3.4 a) D-FF standard symbol. b) Truth table c) Timing diagram

The D-FF used in this study is the one that is shown in figure 3.5. It operates as follow: When both CLK and RST are low, node 1 will be connected to VDD through M8, M4. At the raising edge CLK, the node 2 will be connected to ground through M3, M2. Since node 1 is connected to VDD that will turn off M6 keeping node 2 from charging high. As RST signal charges up, node 1 will be connected to the ground through M27, which will lead to pull up node 2 and it will become high due to switching M6 on. Transistor M8 job is to prevent a short circuit in the M5, M8amd M27 path. When CLK is low and RST is high a large current will low this path so M8 is placed there to prevent this current and lower the power consumption of the D flip-flop. Since we are getting flipped value of Q, an inverter has been added at the end of the circuit to flip the value and get a correct value of Q. The two D-FFs have the same design, one of them will control the UP output of the PDF and the other will control the DOWN output.

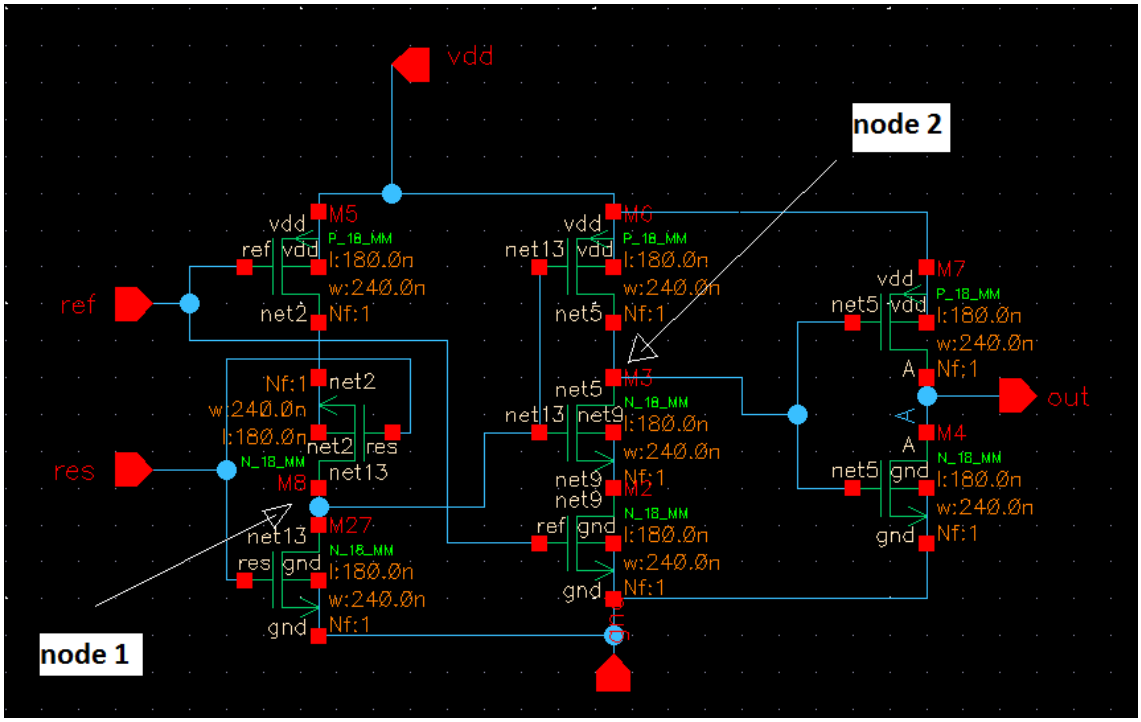


Fig.3.5 D-FF circuit

3.3 CONCLUSIONS

As a conventional PFD, the three valid states will be:

a) Up and Dn down (V constant, loop locked);

b) Up high, Dn down (V will increase to become locked);

c) Up down, Dn high (V will decrease to become locked);

According to all described above, the essential difference with the conventional one is the reset generation. In the classic model, it is made by the AND output of the D-FF outputs; in contrast, now the reset signal is directly built from the input signal and the D-FF output. So, that way the D-FF delay does not affect the reset signal delay.

Besides, the result of changing the AND gate by the OR gate, reduces the total reset signal delay but also increase the width of the reset pulse. Anyway, this effect can be controlled by the pulse width of the input signals and also by the "delay cell" and the "shot pulse generator".

Chapter 4

Simulations and results

After the theorist study of each design, it is necessary to verify the properties of which boast. The parameters that will be analyzed are the ones that describe the operation of this kind of circuits: transient response, periodic noise, the delay time/reset time and the power consumption.

For the simulations in CADENCE the used technology is UMC_180 CMOS.

The two input signals are two pulse ones with the following parameters:

	Period	**pw**	**td**	**tf**	**tr**	**Val0**	**Val1**
Fref	2u	1u	0	100p	100p	0V	1.8V

Fvco	1.8u	0.9u	80n	100p	100p	0V	1.8V

Bellow, the analysis parameters from which the two main designs will be compared are briefly described:

- Transient Response: It is the response of a system to a change from equilibrium. In this case, the input signals, that active the circuit, are some periodic succession of pulses and this causes some variations in the outputs of the circuit. In the following simulations the duration is 10us.

- Noise: In this analyze, the noise produced by the components of the circuit will be shown in its output nodes. It consist on a "*pss" (periodic steady state)* and a "*pnoise"(periodic noise analysis)* simulations and from them, the output noise will the plotted in a range of frequencies.

- Delay time and reset time: These parameters are usually the bottleneck in the PFD designs. These circuits are called to be as faster as possible. So, the delay time and the reset time must be the shorter the better. The delay time is measured as the difference in time between the input signal and the output one (in the half maximum voltage value) that ideally would be zero but it depends on the circuit structure so it is difficult to reduce. Besides, in the basics designs of PFD, the reset time is the reset pulse width also in the medium voltage value. Both of them should be as short as possible.

- Current - Power consumption: To measure the power consumption of a circuit, it is necessary to know the voltage value and the average current value in a period. It must be measured in the supply voltage node. According to that, to obtain the average current its wave must be integrated in a period. After, it must be divided by the period length. Then, P=VI. The power is expensive, so it is interesting to work with low power consumption designs.

First, one by one, and after making a comparison between all of them; their operation will be discussed.

4.1 THREE STATES PFD

4.1.1 BASIC PFD

As it was described above, it is composed by two D-FF and an AND logic gate. Each D-FF has got eight CMOS transistors and the AND gate has got six ones. So, this design consists of 22 transistors.

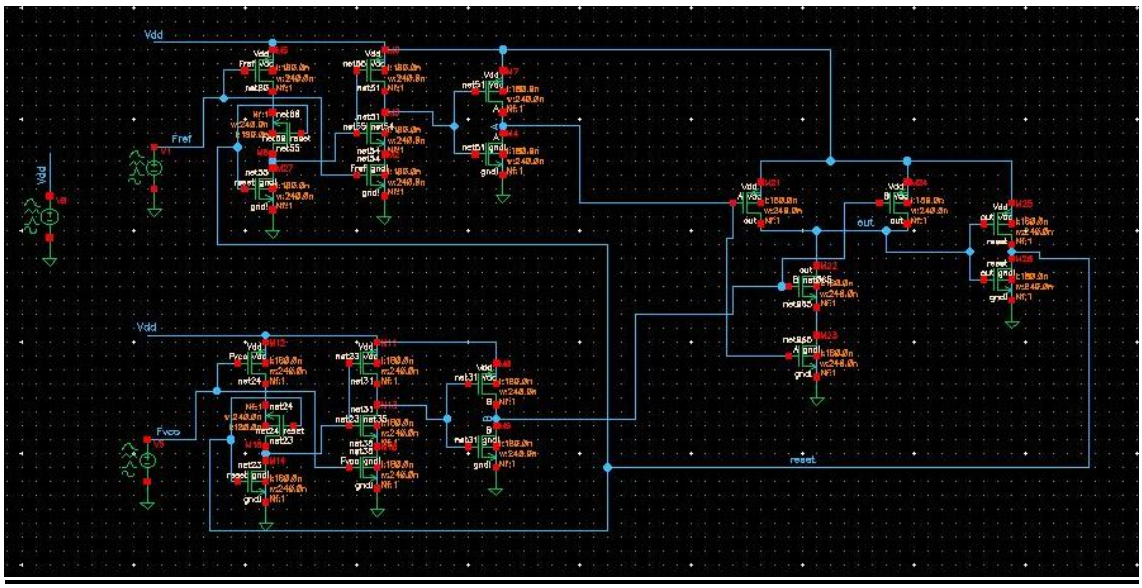


Fig.4.1 Basic PFD schematic

4.1.1.1 Transient Response

Realizing the transient simulation, the obtained waves are illustrated in fig.4.2. As it is shown on it, the input signals (Fref and Fvco) have different frequency and phase. Besides, the A signal (which is the D-FF output whose input is Fref) follows Fref input until the reset signal is activated. The same happens with B signal (which is the D-FF output whose input is Fvco) and Fvco. Moreover, reset signal (which is the AND gate output) is active only when both A and B are up.

It is observable, also, that as it is said in previous chapters, when Fref presents an instantaneous frequency higher that Fvco, A (“up signal”) increases its value, maintaining B (“down signal”) zero. Additionally, when both Fref and Fvco have the same frequency, both A (“up”) and B (“down”) signals become zero.

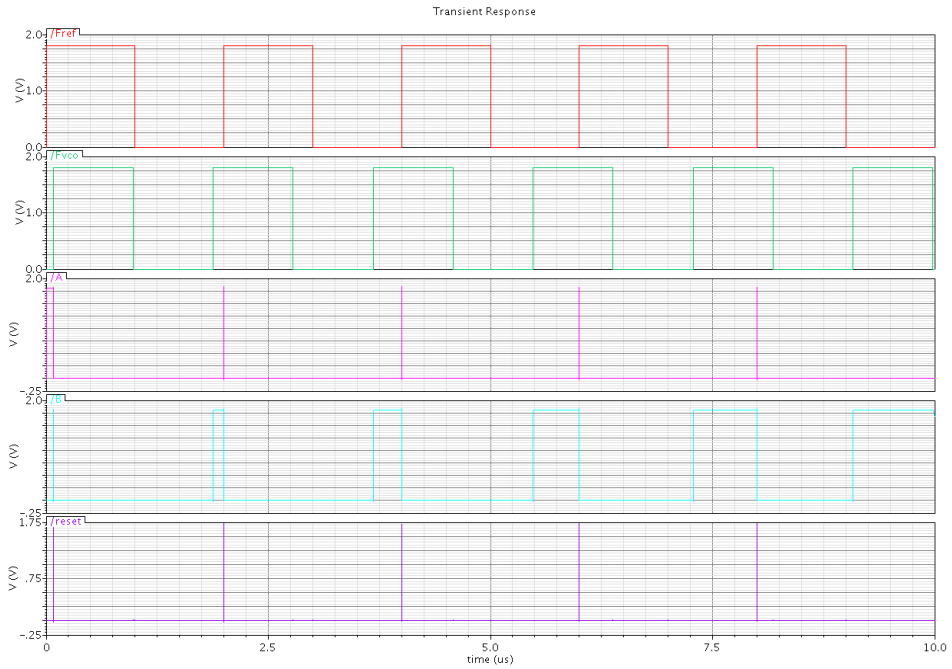


Fig.4.2 Transient response in a basic PFD

4.1.1.2 Noise

Realizing the noise simulation, the obtained wave is illustrated in fig.4.3. Due the symmetry of the circuit, both periodic noise responses in the Up and Down nodes are the same.

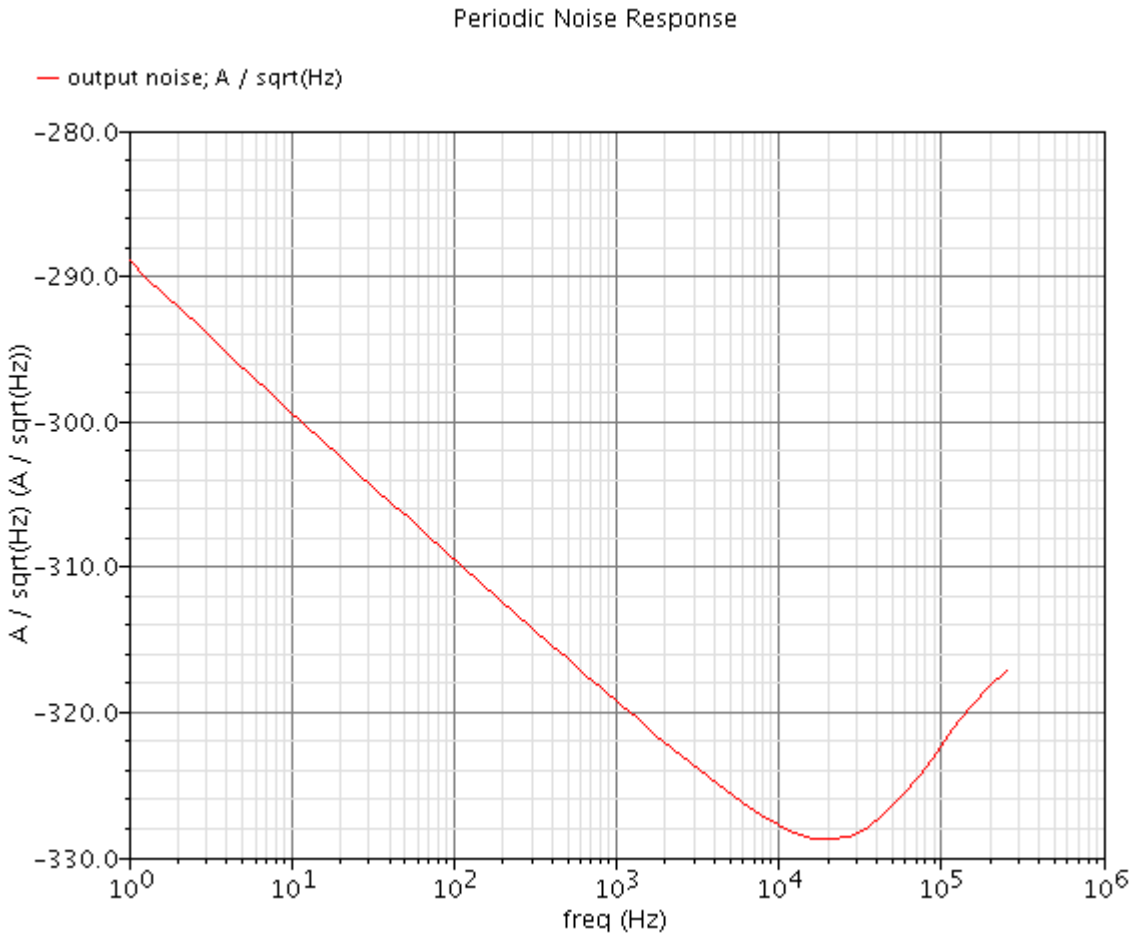


Fig.4.3 Periodic noise response in a Basic PFD in one output

4.1.1.3 Delay time and reset time

Looking at the basic PFD design, it is clear that de delay between the input signal and the output one will the de D-FF delay. In an ideal situation in which neither the transistors, nor cables nor any device presented in the circuit have delay, both input and output signals would be simultaneous.

Besides, the reset signal should act immediately when both Up and Down signals are active at the same time. However, it is not that way because these two signals must be processed by the AND gate. This reset time is the AND gate delay.

- Delay time between Up output and Fref input:

Fig.4.4 shows the delay between the Fref signal pulse and an Up signal one. Measuring this time difference in 0.9V, the obtained value is 88,9pseg.

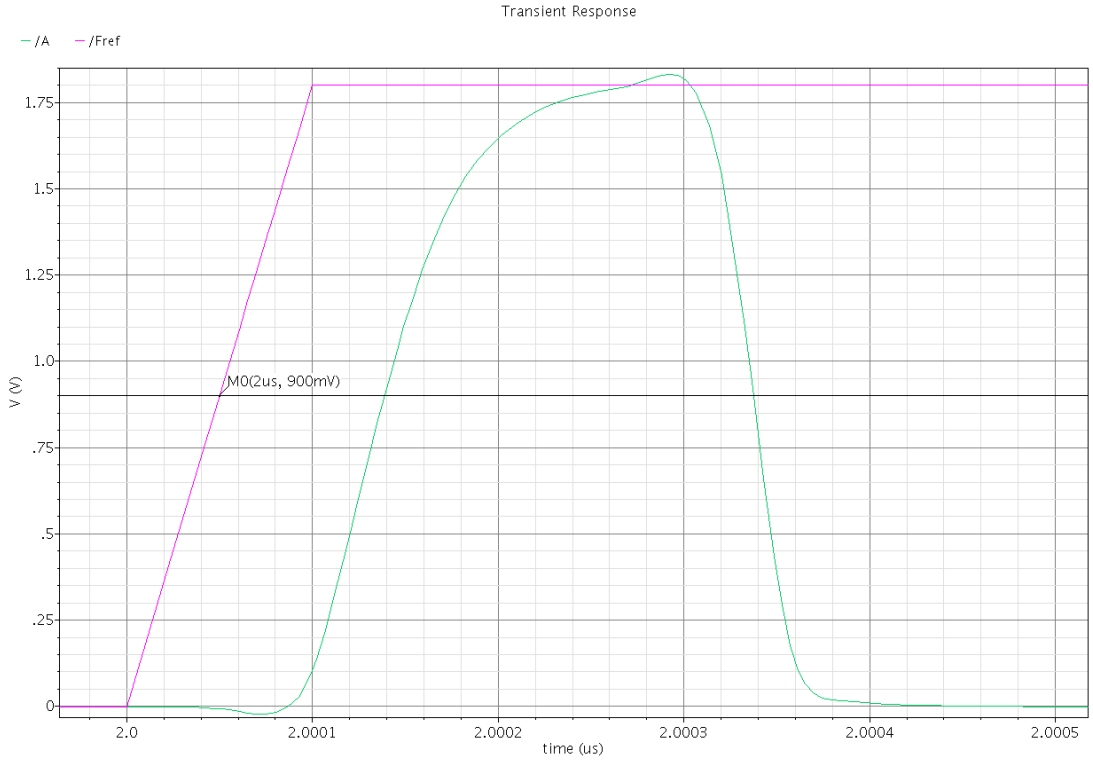


Fig.4.4 Delay time between Fref and Up signal in a Basic PFD

- Delay time between Down output and Fvco input:

Fig.4.5 shows the delay between the Fvco signal pulse and a Down signal one. Measuring this time difference in 0.9V, the obtained value is 86pseg.

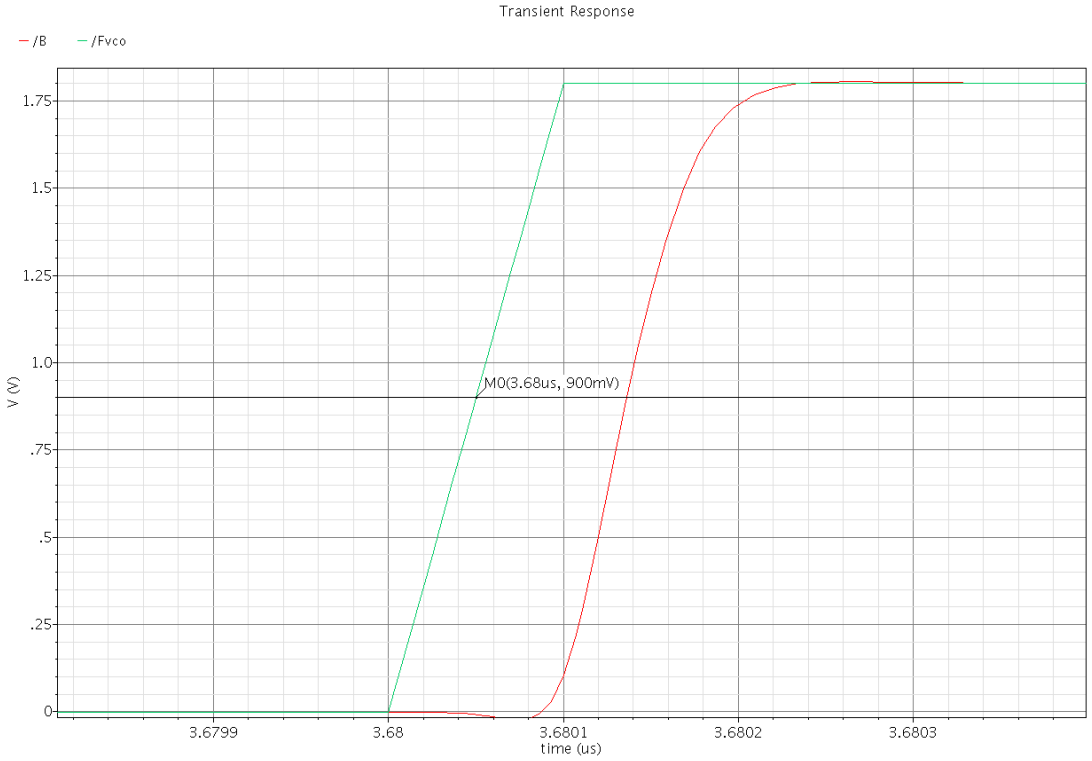


Fig.4.5 Delay time between Fvco and Down signal in a Basic PFD

- Reset time:

  Fig.4.6 shows the reset pulse width. Measuring this time difference in 0.9V, the obtained value is 151,4pseg.

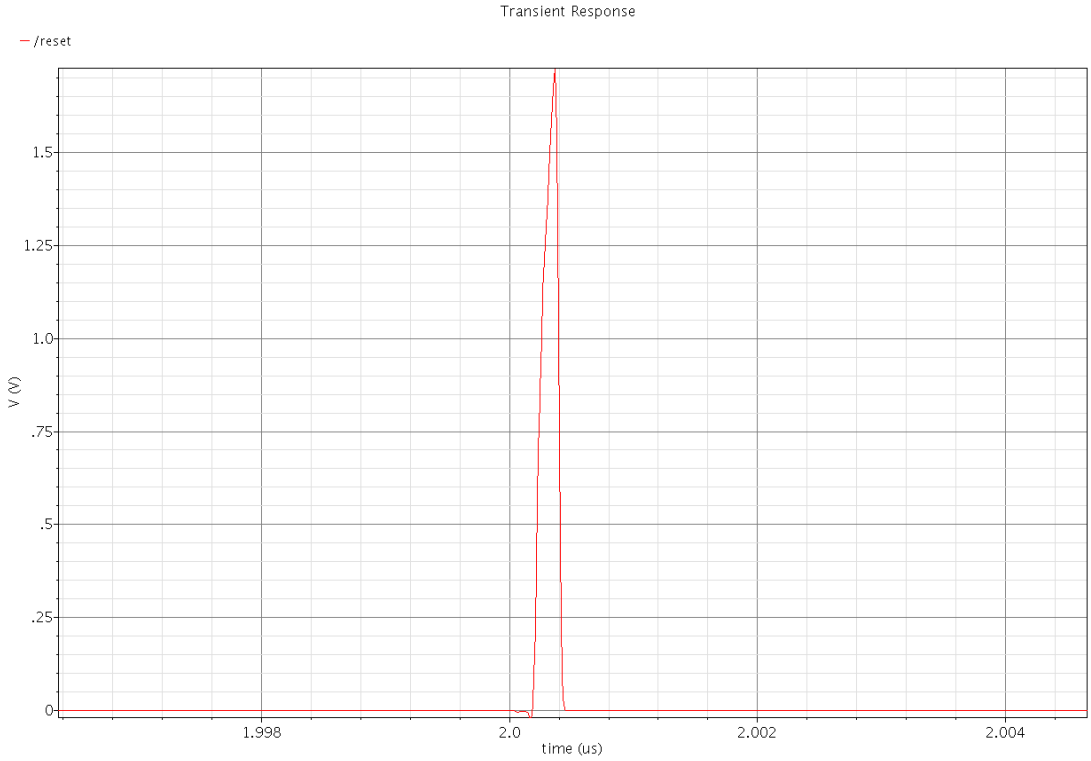


Fig.4.6 Reset signal pulse in the basic PFD

As it was expected, both delay times between the inputs ant the outputs are almost the same. Besides, the reset signal (AND gate delay) is lower than these values (D-FF delay).

4.1.1.4 Current and power consumption

Next fig. 4.7 shows the current in the Vdd node. Taking a period of this signal and integrating its value; dividing by the length of this period, the average current is obtained. Then, multiplying by the Vdd voltage value, the power consumption is obtained.

So, I= (38.99e-15)/2u=19.495e-9 A.

P=1.8V*19.495.5e-9A=0.035uW

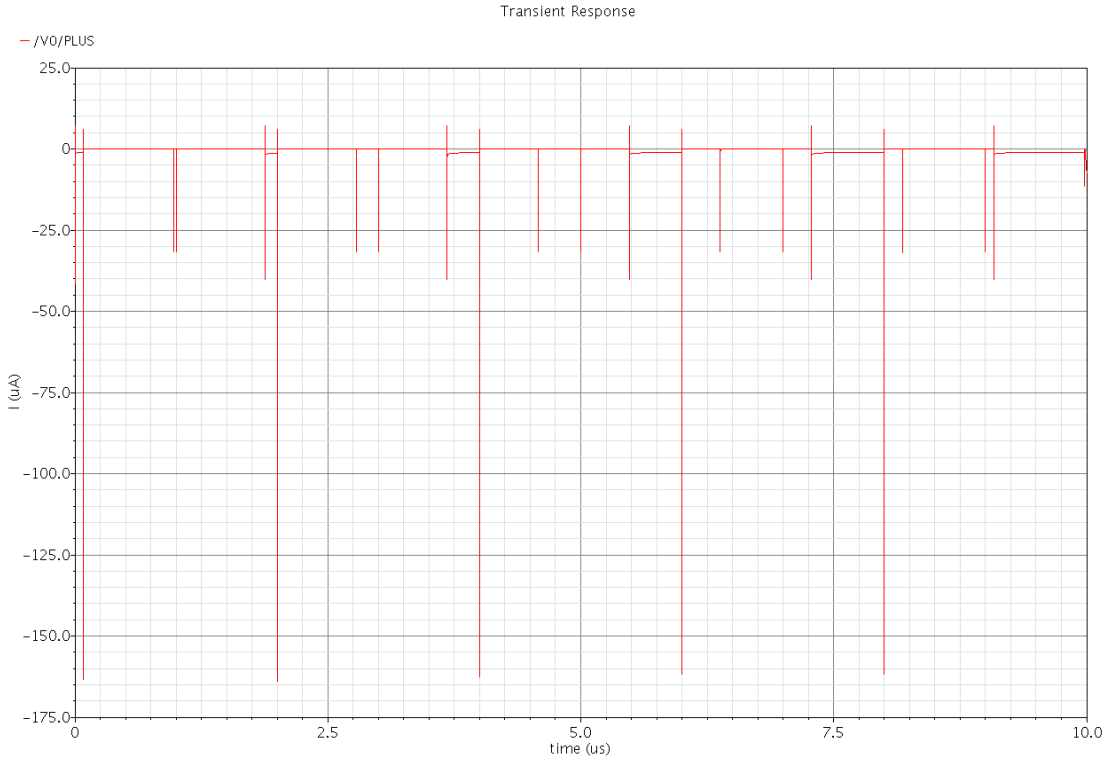


Fig.4.7 Current in Vdd node in a Basic PFD

5.1.2 BASIC PFD WITH EXTRA DELAY

There is a controversy regarding the reset time. As it is shown in fig. 4.2, the UP width pulse depends on the reset signal width pulse. On the one hand, it is convenient to reduce the width of the reset pulse in order to increase the circuit speed and also for not loosing during this active time in the reset any rising edge in the input signals; maintaining it as brief as possible to ensure a good performance in the design. On the other hand, a very brief width pulse in the output signals can produce problems in the operation of the charge pump.

So, it is necessary to find a compromise to reconcile these two inverse effects. Therefore, another design of the basic PFD is proposed in fig.4.8. The only difference compared with the previous one is the incorporation of two extra inverters at the output of the AND gate. This way, the width of the reset signal will be increased but at the same time it is the way to make sure a good operation of the charge pump.

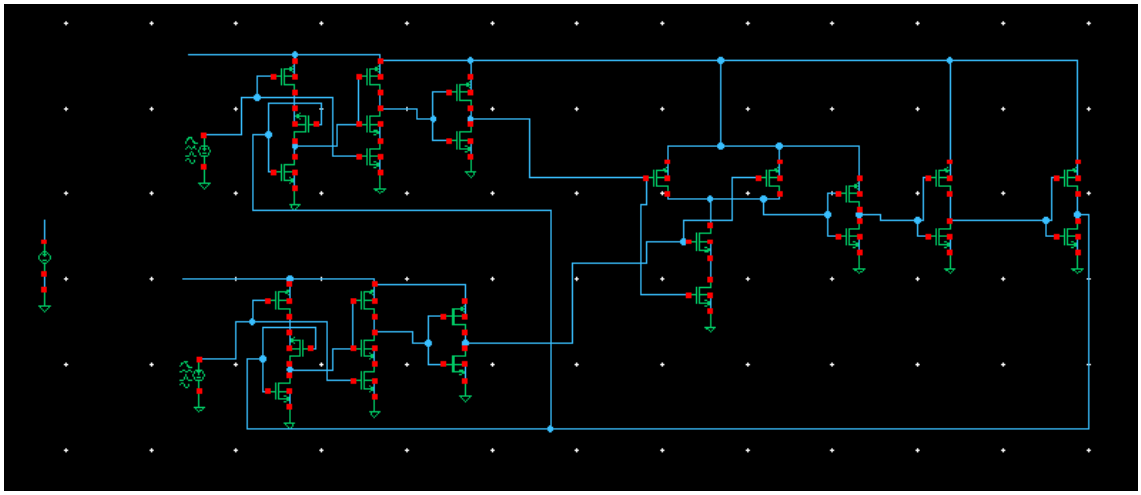


Fig.4.8 Basic PFD schematic with extra delay

4.1.2.1 Transient Response

Realizing the transient simulation, the obtained waves are illustrated in fig.4.9. The operation of this design is essentially the same as the previous one.

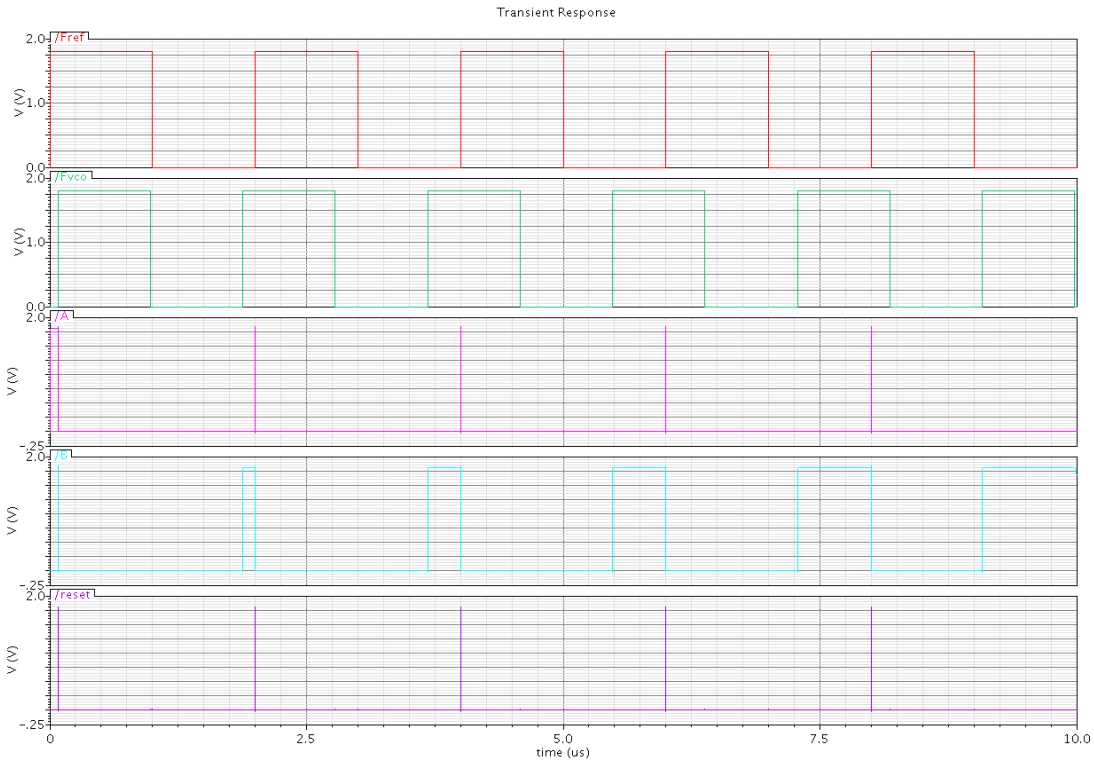


Fig. 4.9 Basic PFD with extra delay transient response

4.1.2.2 Noise

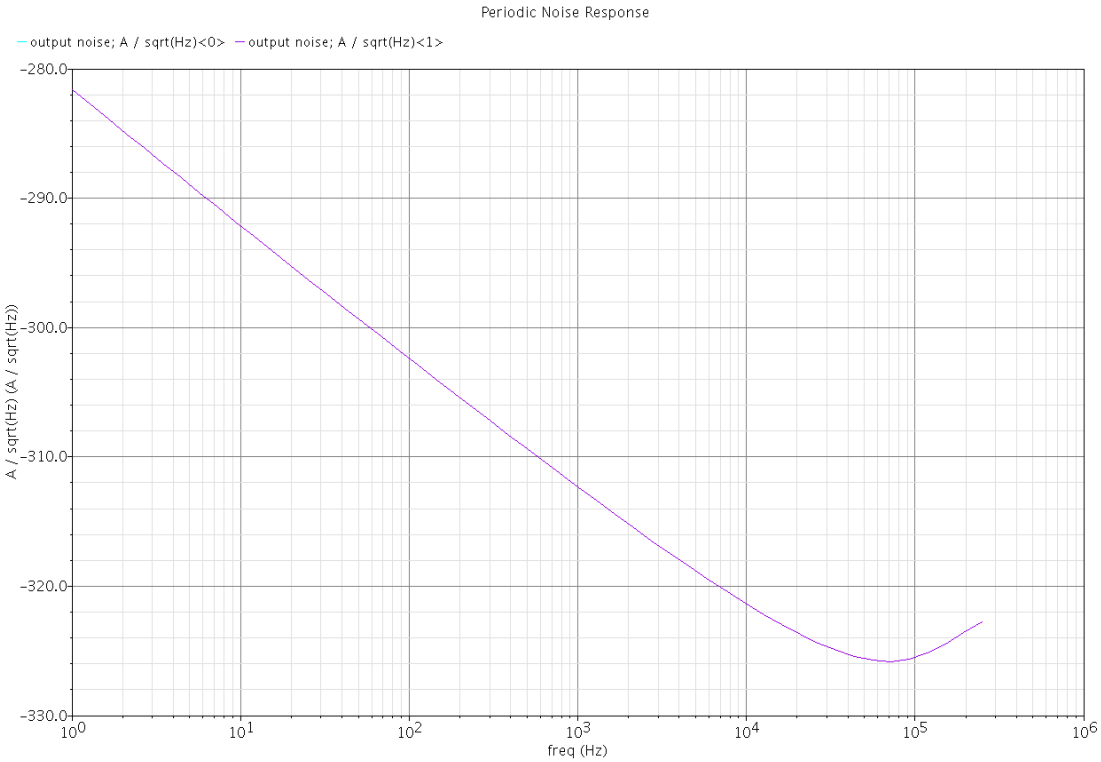


Fig.4.10 Periodic noise response in a Basic PFD with extra delay in one output

Due to the incorporation of the two inverter devices, the noise suffers an increase.

4.1.2.3 Delay time and reset time

The delay time between the input and the output signals will be the same as in the previous design, only the reset signal will be increased because of the include of the two inverters. Now, the reset signal will not be defined as the AND gate delay but as the AND gate delay and the two inverters delay. So, it will be bigger.

- Delay time between Up output and Fref input:

Fig.4.11 shows the delay between the Fref signal pulse and an Up signal one. Measuring this time difference in 0.9V, the obtained value is 88,9pseg.

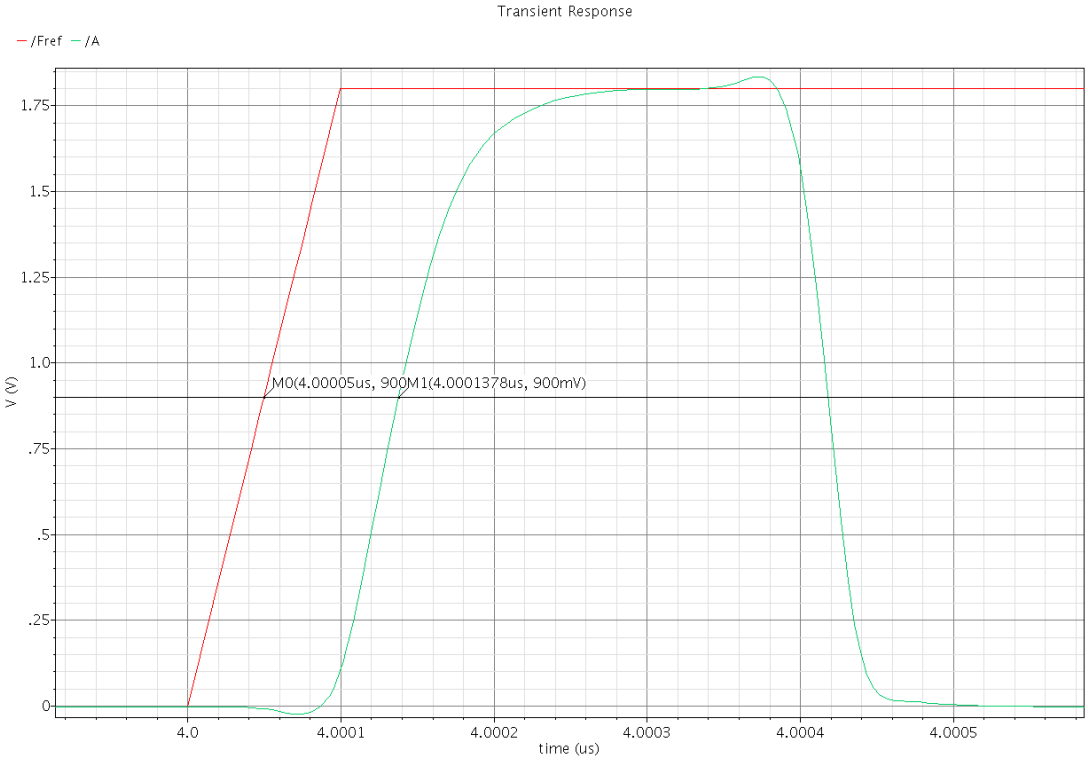


Fig.4.11 Delay time between Fref and Up signal in a Basic PFD

- Delay time between Down output and Fvco input:

Fig.4.12 shows the delay between the Fvco signal pulse and a Down signal one. Measuring this time difference in 0.9V, the obtained value is 86pseg.

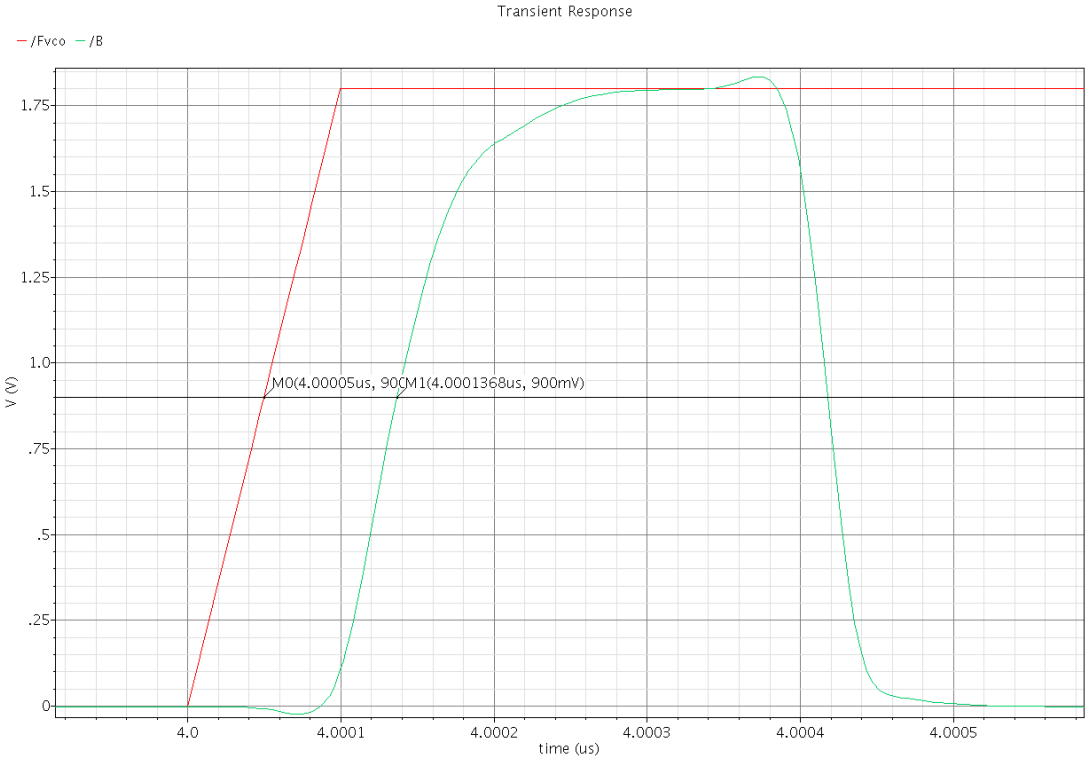


Fig.4.12 Delay time between Fvco and Down signal in a Basic PFD with extra delay

-Reset time:

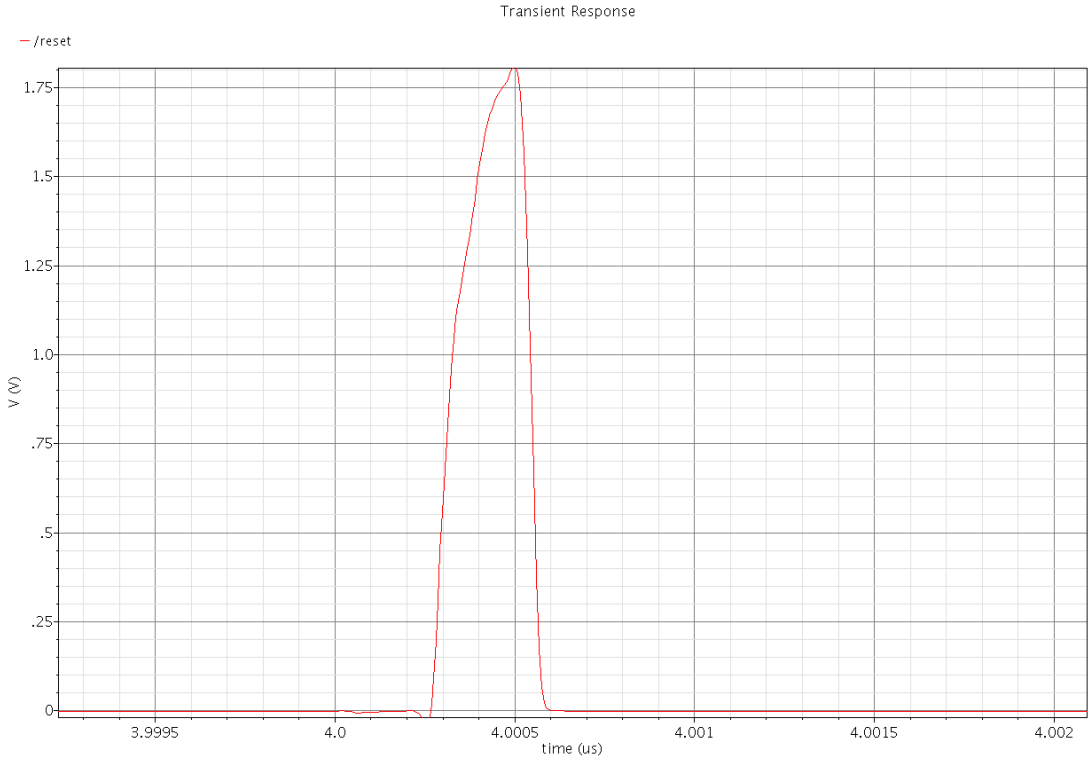


Fig.4.13 Basic PFD (with extra delay) reset time

As it was supposed to be, the reset time has been increased thanks to the inclusion of the two inverters. The reset time value is equivalent to the AND gate and the two inverters delay. Its value is 227ps.

4.1.2.4 Current and power consumption

Next fig. 4.14 shows the current in the Vdd node. Taking a period of this signal and integrating its value; dividing by the length of this period, the average current is obtained. Then, multiplying by the Vdd voltage value, the power consumption is obtained.

So, I= (48.77e-15)/2u=24.38e-9 A.

P=1.8V*24.38e-9= 4.38e-8w=0.0438uW

Of course, the inclusion of the two inverter devises involves an increase in the power consumption.

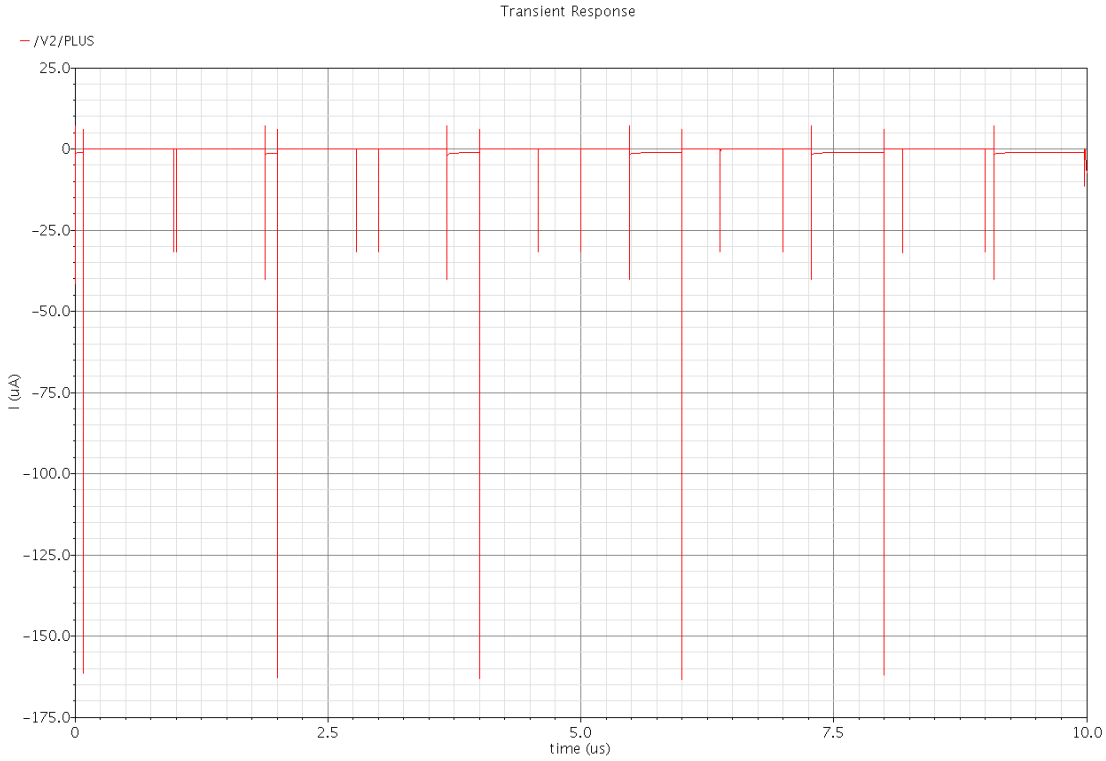


Fig.4.14 Basic PFD with extra delay current in Vdd node

4.2 FEEDFORWARD RESET PFD

Addressing the need of reducing the reset time, the Feedforward reset PFD, which was presented in previous chapters; will be implemented and simulated. As it was already described, it is composed by two D-FF, two delay cells, two shot pulse generators and two reset generators. In total, the design has 40 CMOS transistors.

Next fig.4.15 shows the schematic of this PFD design.

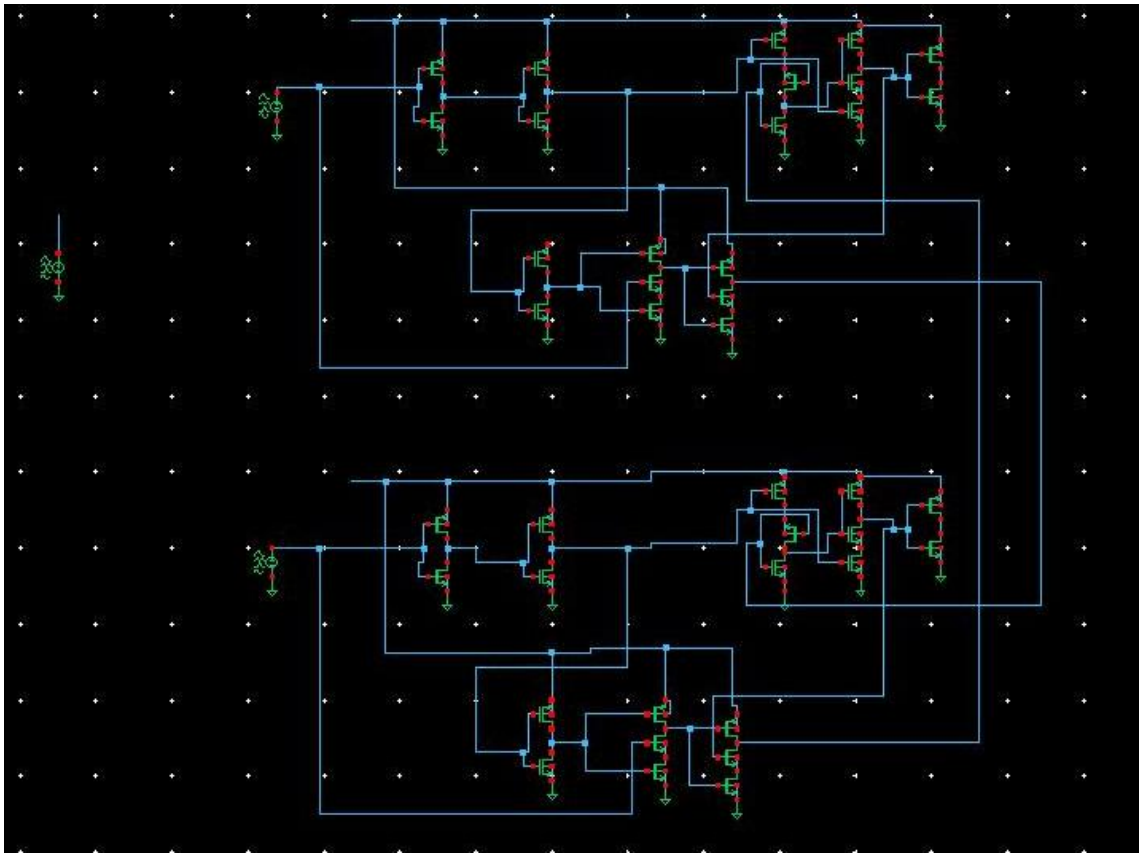


Fig.4.15 Feedforward reset PFD schematic

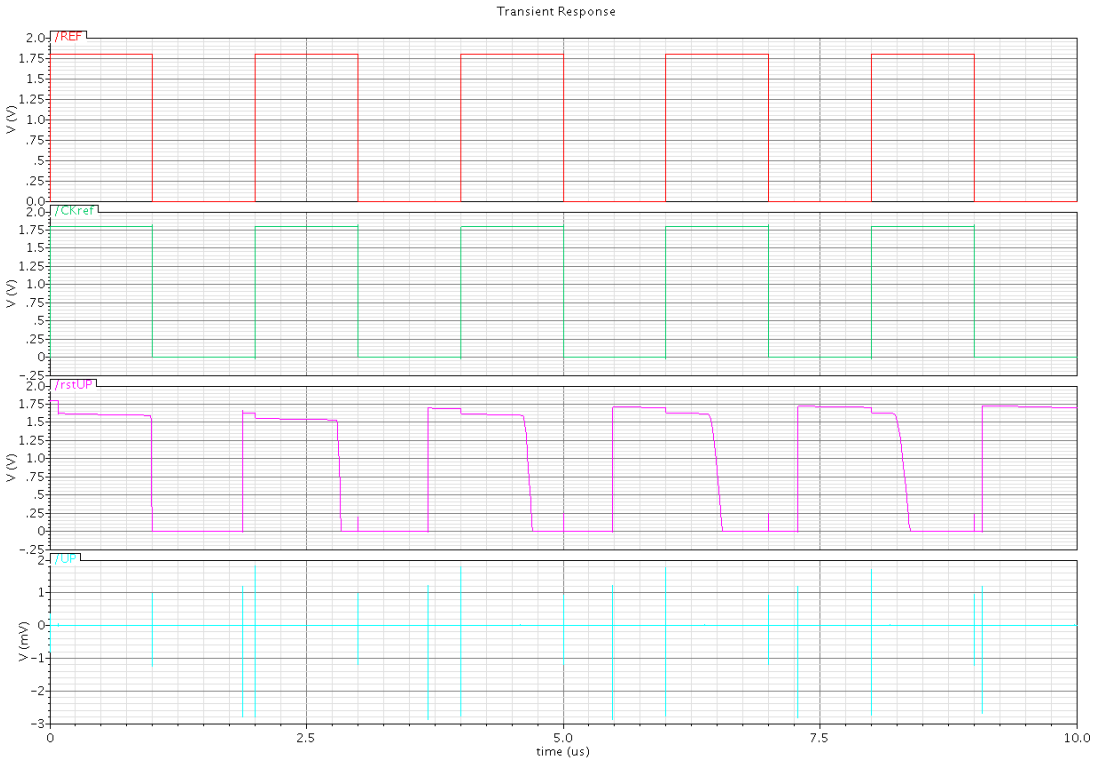
4.2.1 TRANSIENT RESPONSE AND PROBLEM

Looking at the following fig. 4.16, it is easy to observe that the circuit does not work properly. It is due to the way of working of the delay cell. As it is said before, it is composed by two inverter circuits that produce in the input cell a delay on it. But, as it is shown bellow, the delay between Fref and CKref or Fvco and CKvco is so tiny that the reset generator does not work as it should do.

So, the alternatives is to put more inverter circuits in these cell to increase the delay between the original input signals and the D-FFs inputs which increases the number of transistors and make the schematic more complicated.

Alternatively, the following simulations will be done with some external sources with the same frequency of Fref and Fvco, respectively; but adding to their delay, other extra one. It is a practical way to face the problem acting as the delay cell should do.

Anyway, in the real world, fabricants offer delay cells for all king of devises.



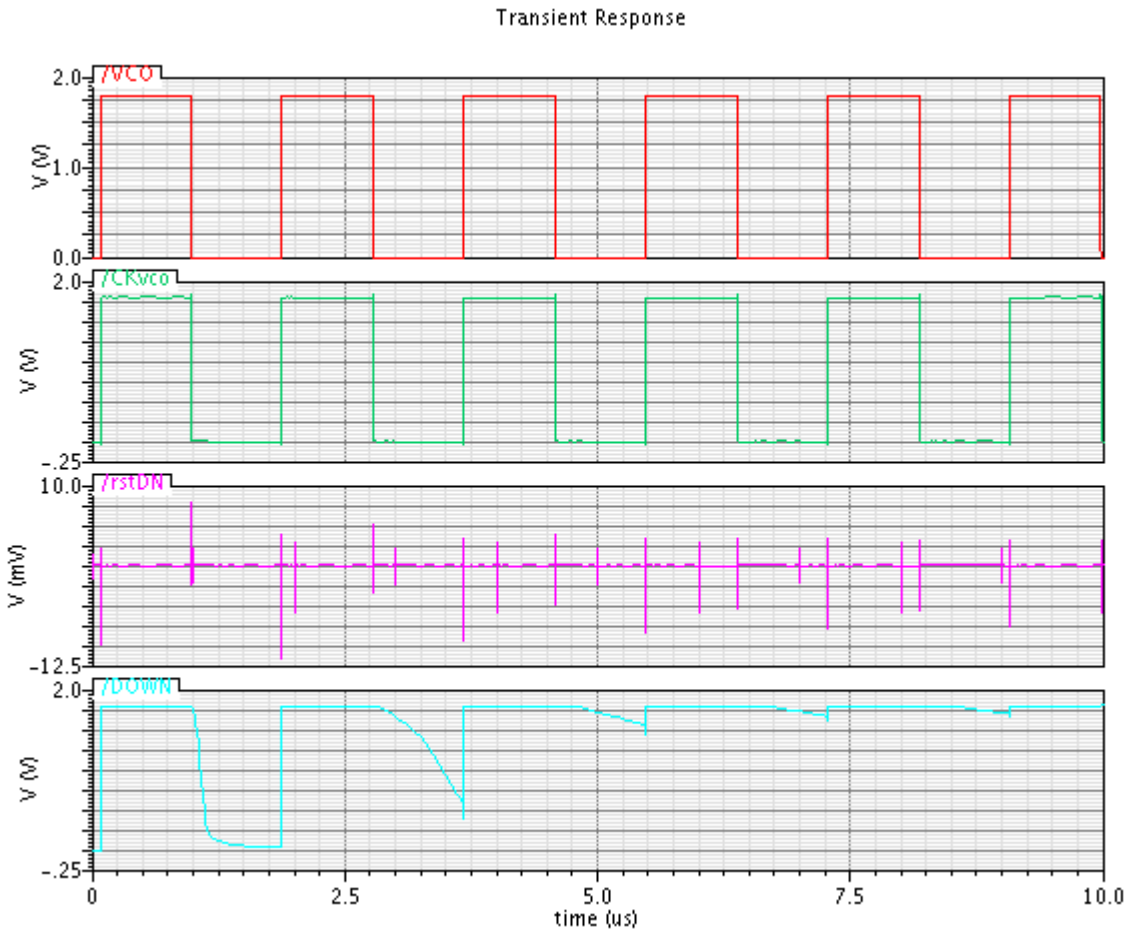


Fig.4.16 Feedforward reset PFD transient response

4.2.2 ALTERNATIVE DESIGN: FEEDFORWARD RESET PFD WITH EXTERNAL DELAY CELL

As it was described below, instead of the delay cell composed of two inverters, some external voltage sources are uses to generate the CKref and the CKvco signals.

	Period	pw	td	tf	tr	Val0	Val1
CKref	2u	1u	200n	100p	100p	0V	1.8V
CKvco	1.8u	0.9u	280n	100p	100p	0V	1.8V

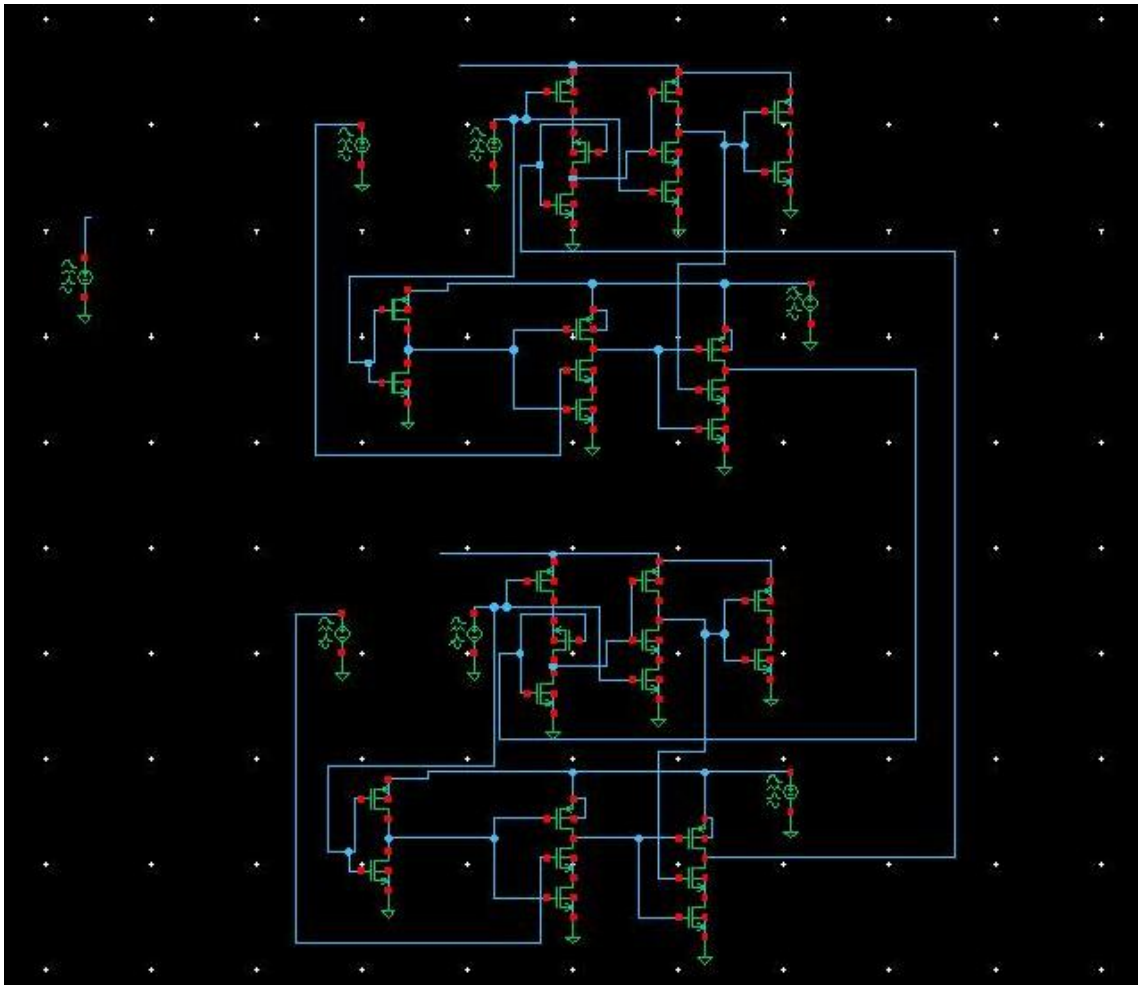


Fig.4.17 Feedback reset PFD with external delay cell schematic

4.2.2.1 Transient Response

The following fig.4.18 illustrates the transient response of the described design. The fact that there are two reset signals intersecting in the two circuit branches guarantees certain synchronicity between them.

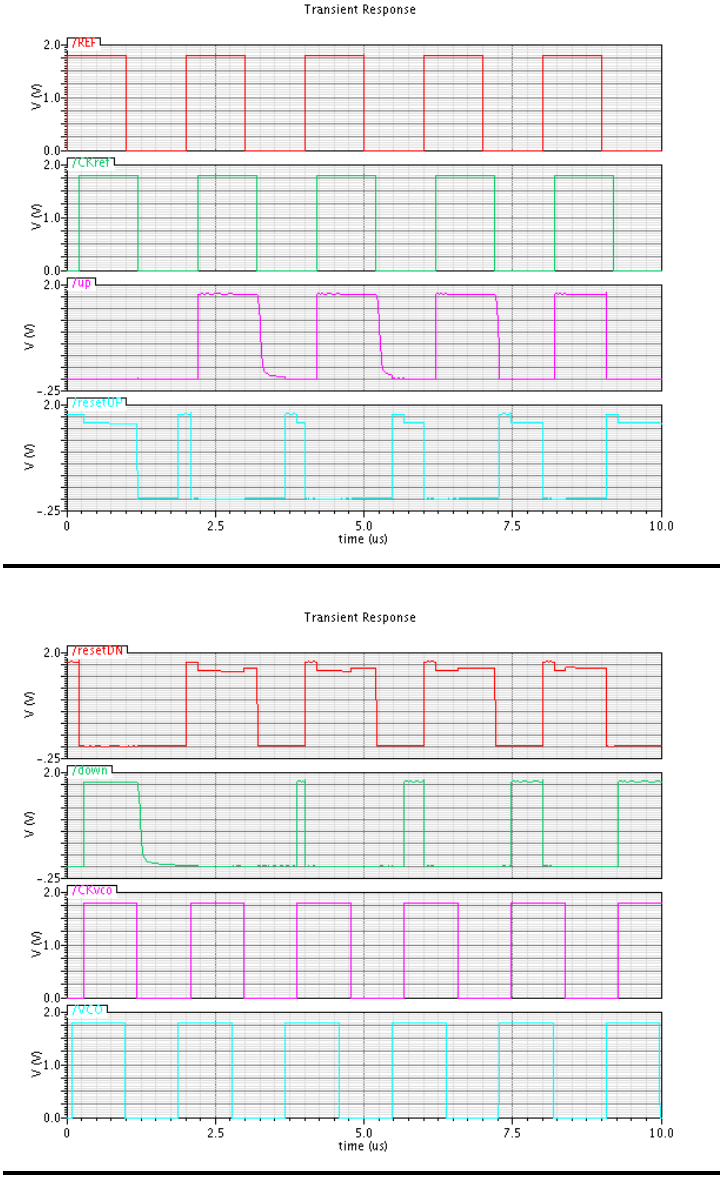


Fig.4.18 FR-PFD transient response

4.2.2.2 Noise

Realizing the noise simulation, the obtained wave is illustrated in fig.4.19. To measure the noise, both inputs have the same frequency one of the outputs is zero.

This design presents more noise in the output node. This is due to the increase of devices in it, comparing to the basic topology. Each device introduces noise and also the cables.

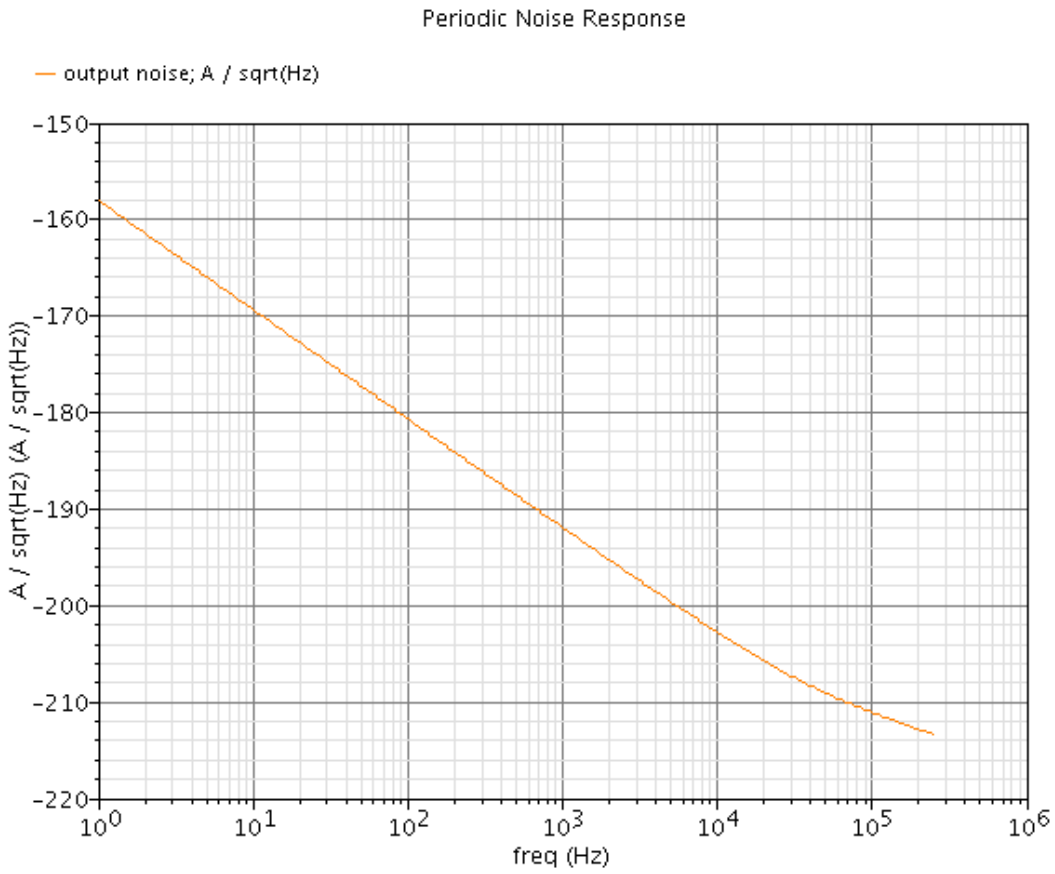


Fig.4.19 FR-PFD periodic noise response

4.2.2.3 Delay time

Looking at the design, it is clear that de delay between the input (CKref and CKvco) signals and the output ones will the de D-FF delay. In an ideal situation in which neither the transistors, nor cables nor any device presented in the circuit have delay, both input and output signals would be simultaneous.

- Delay time between Up output and CKref input:

Fig.4.20 shows the delay between the CKref signal pulse and an Up signal one. Measuring this time difference in 0.9V, the obtained value is 79,7pseg.

As it is supposed, this value is practically the same as the ones in the previous designs. The used DFF is the same so, its delay too.

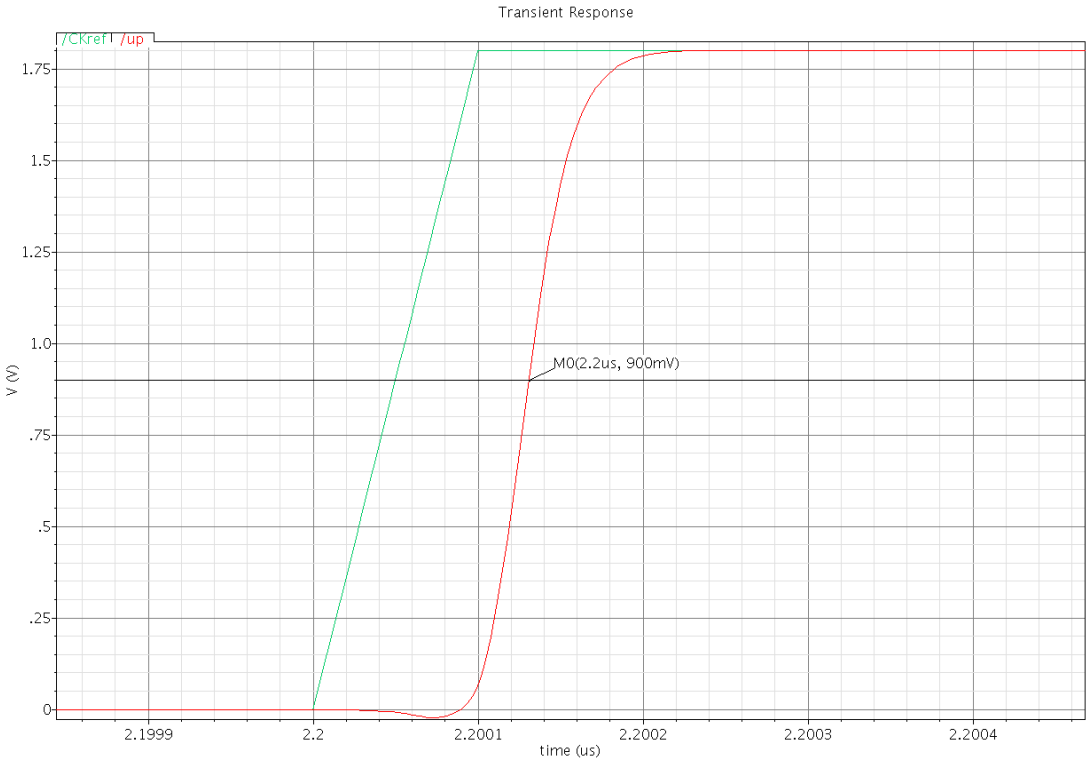


Fig.4.20 Delay time between CKref and Up signal in a FR-PFD

-Delay time between Down output and CKvco input:

Fig.4.21 shows the delay between the Fvco signal pulse and a Down signal one. Measuring this time difference in 0.9V, the obtained value is 79.3pseg.

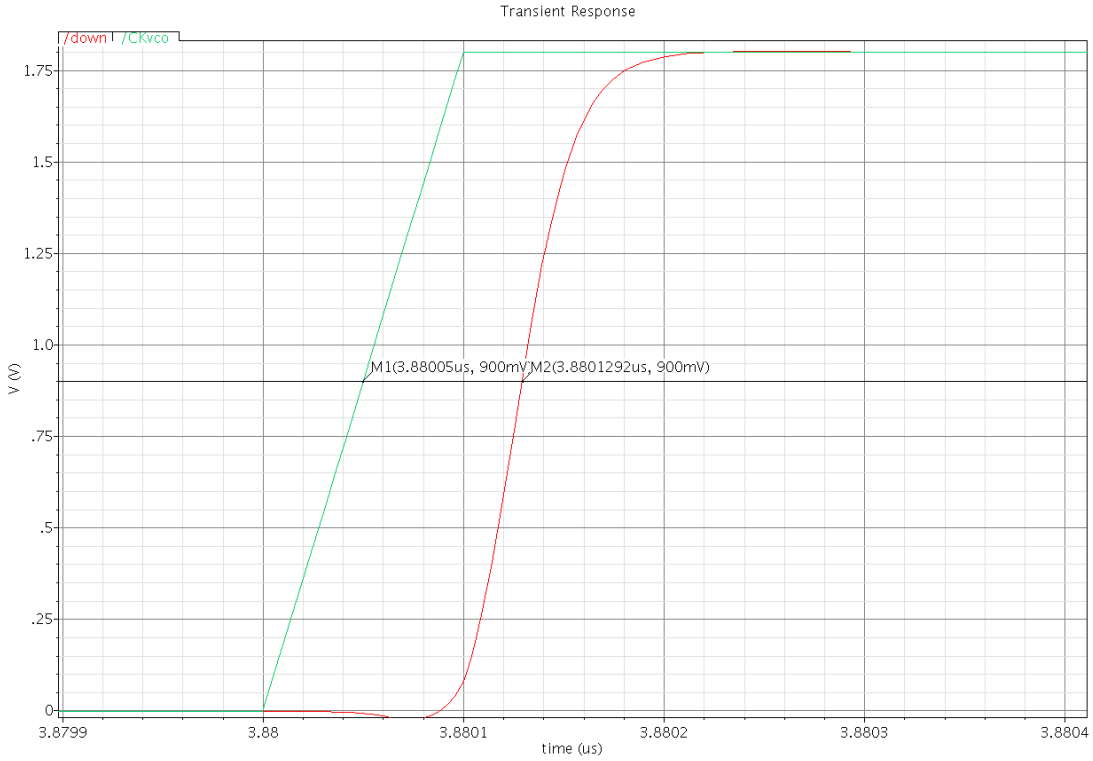


Fig.4.21 Delay time between CKvco and Up signal in a FR-PFD

4.2.2.4 Current

Next fig. 4.22 shows the current in the Vdd node. Taking a period of this signal and integrating its value; dividing by the length of this period, the average current is obtained. Then, multiplying by the Vdd voltage value, the power consumption is obtained.

So, I= (21.86e-12)/2u=10.93e-6 A.

P=1.8V*10.93e-6A=19.674uW

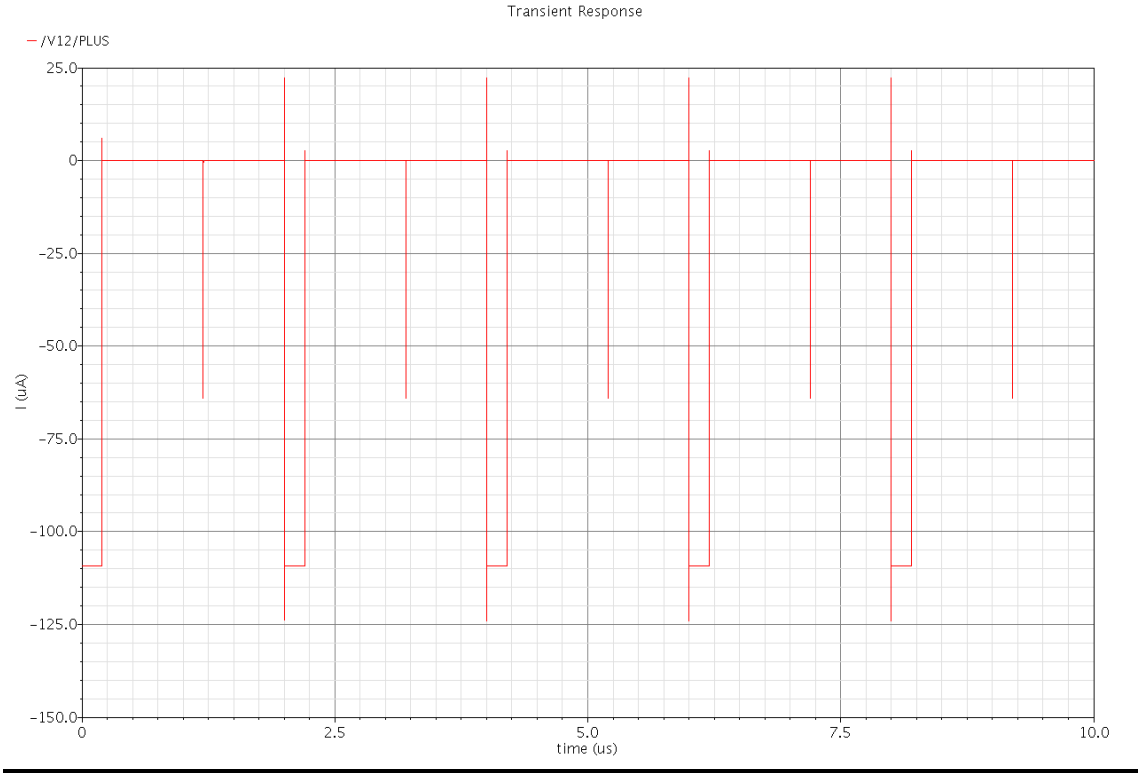


Fig.4.22 FR-PFD current in Vdd node

4.3 COMPARATIONS BETWEEN THE TWO DESIGNS

All the results that were detailed before are summarized in the following table. As it can be seen in it, the main advantage of the Feedforward reset PFD design is the independence of its reset generation, who does not depend on the DFF delay.

Apart from that, the design is much more complicated than the basic one. It includes 40 transistors that increase the noise, the current and the power consumption, and so, its price. As it is said in previous chapters, this disadvantage can be solved partially by using dynamic CMOS logic instead of the static one.

In the next chapter, these main designs will be simulated adding in its topology the parasitic capacitance effect, which means another added disadvantage in their operation.

Anyway, the feedforward reset PFD design offers a high speed reset signal but ads too much complicity in the circuit.

	Basic PFD	Basic PFD extra delay	Feedforward reset PFD
Delay time UP	88.9ps	88.9ps	79.7ps
Delay time DN	86ps	86ps	79.3ps
Reset time	151.4ps	227ps	
Current	38.99e-15A	48.77e-15A	21.86e-12A
Power consum.	0.035uW	0.0438uW	19.674uW

Chapter 5

Layout-Parasitic capacitances

Due to the simulator problems, it was not possible to apply the CDR to this layour design and so, not possible also to simulate it. So, in order to study the effects of the parasitic capacitances in the PFD designs descrived, other transistor level simulations will be done but this time considering the presence of these noideal effects: considering a capacitance in all the nodes of the circuit with a certain value.

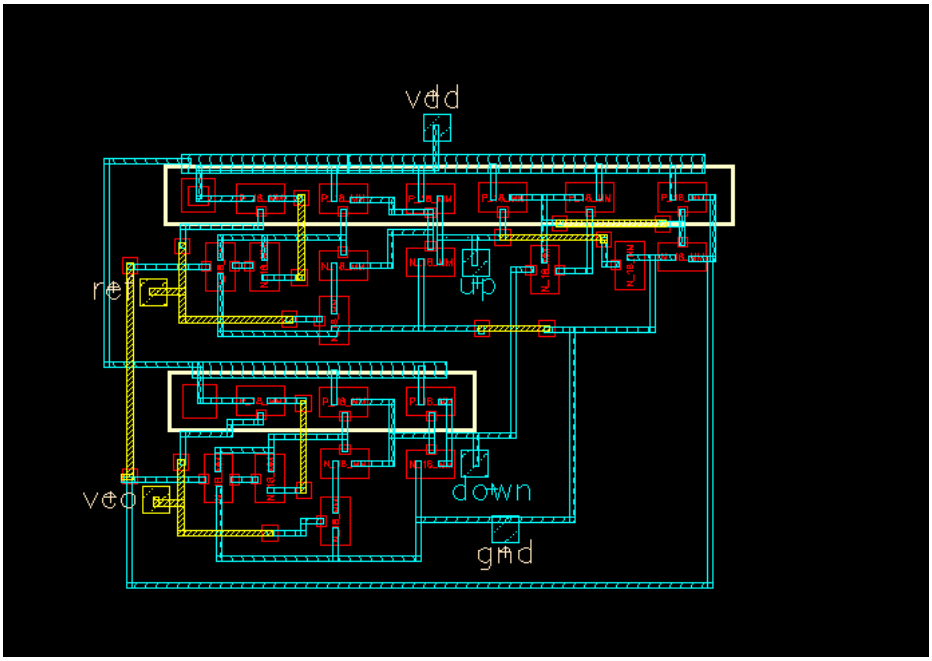


Fig. 5.1 Basic PFD layout

The propose of this new study in to make a comparation between the operation of each PFD design with (noideal) and without (ideal) the parasitic effects. And, besides, compare the Basic PFD and the Feedforward reset PFD behaviours with this effect.

As it is known, in electrical circuits, parasitic capacitance is the unavoidable and usually unwanted capacitance that exists between the parts of an electronic component or circuit simply because of their proximity to each other. All actual circuit elements such as inductors, diodes, and transistors have internal capacitance, which can cause their

behavior to depart from that of 'ideal' circuit elements. In addition, parasitic capacitance can exist between closely spaced conductors, such as wires or printed circuit board traces. The parasitic capacitance between the base and collector of transistors and other active devices is the major factor limiting their high frequency performance.

5.1 BASIC PFD WITH PARASITIC EFFECTS

- Transient response

Next fig. 5.2 shows the transient response of the Basic PFD when the parasitic effects are considered. As it is illustred in it, the waves forms are a little bit rounder than in the ideal situation and it means a bad linearity behaviour in the design.

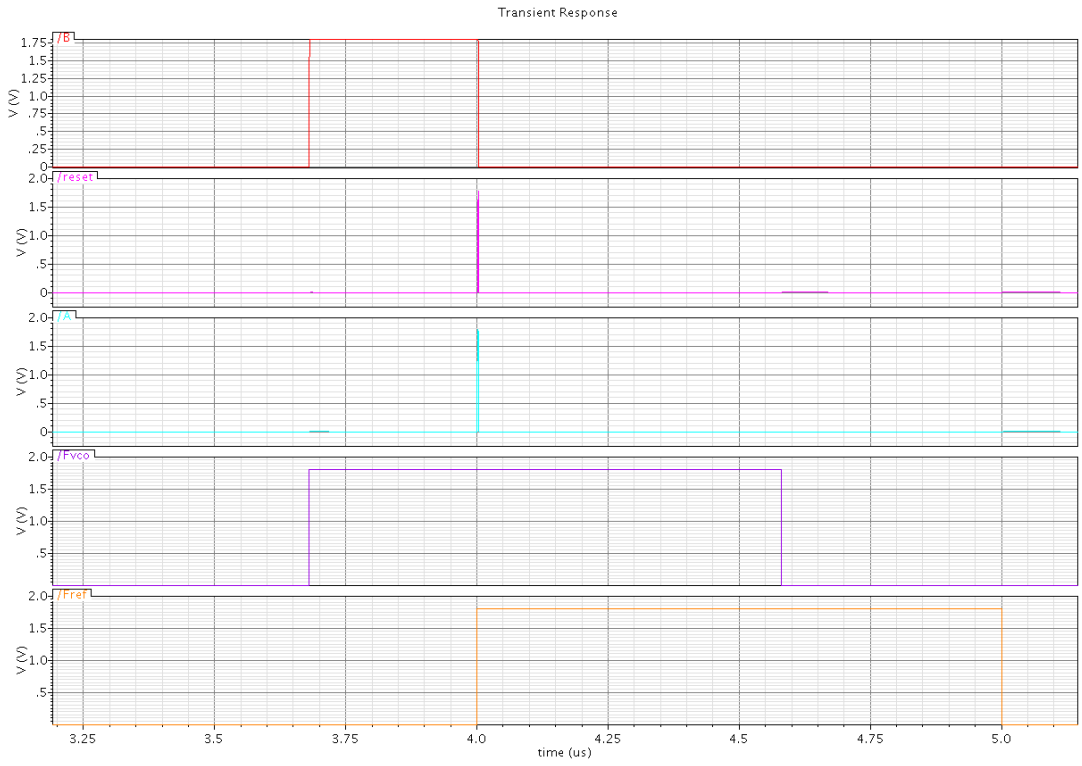


Fig.5.2 Basic PFD transient response with parasitic effects

- Delay times

- Between Fref and Up signals:

  As it is said before, the delay time between Fref and Up signal measures the DFF delay. The study considering the parasitic effects, consists of “adding” in a

simbolic way some capacitances in each node of the circuit. This fact supposes an increase of the D-FF propagation delay as it is traduced in the results.

The value of this delay is 606ps.

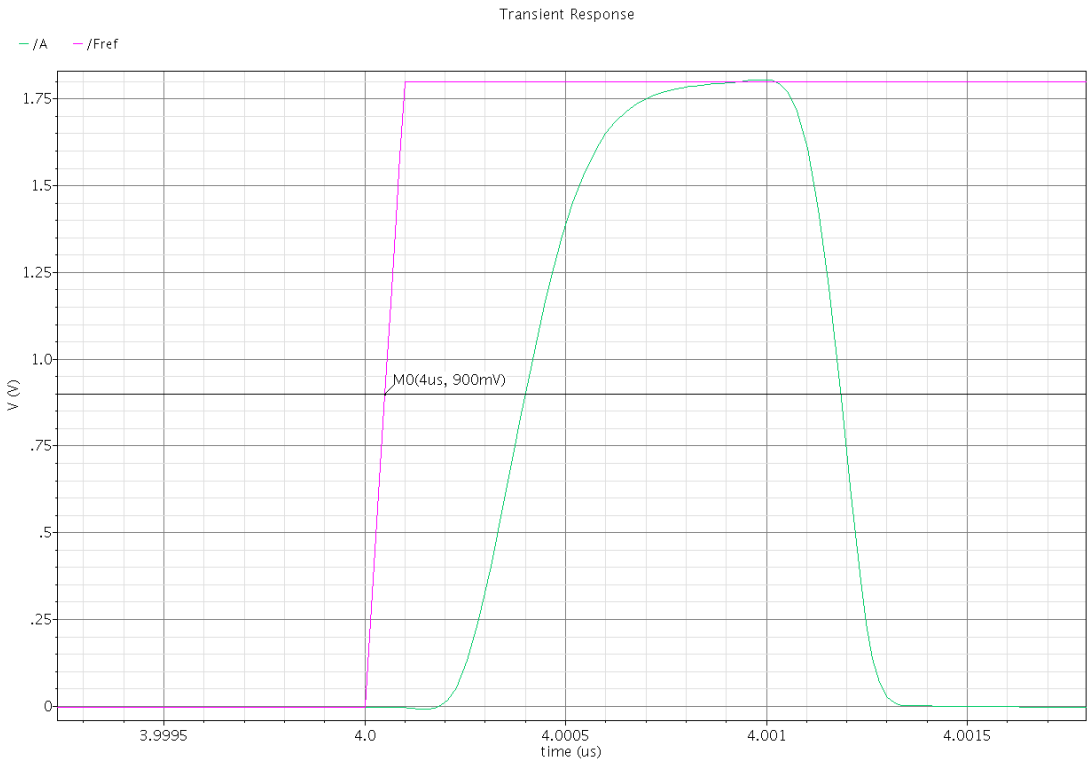


Fig.5.3 Fref-Up delay in the B-PFD with parasitic effects

- Between Fvco and Down signals:

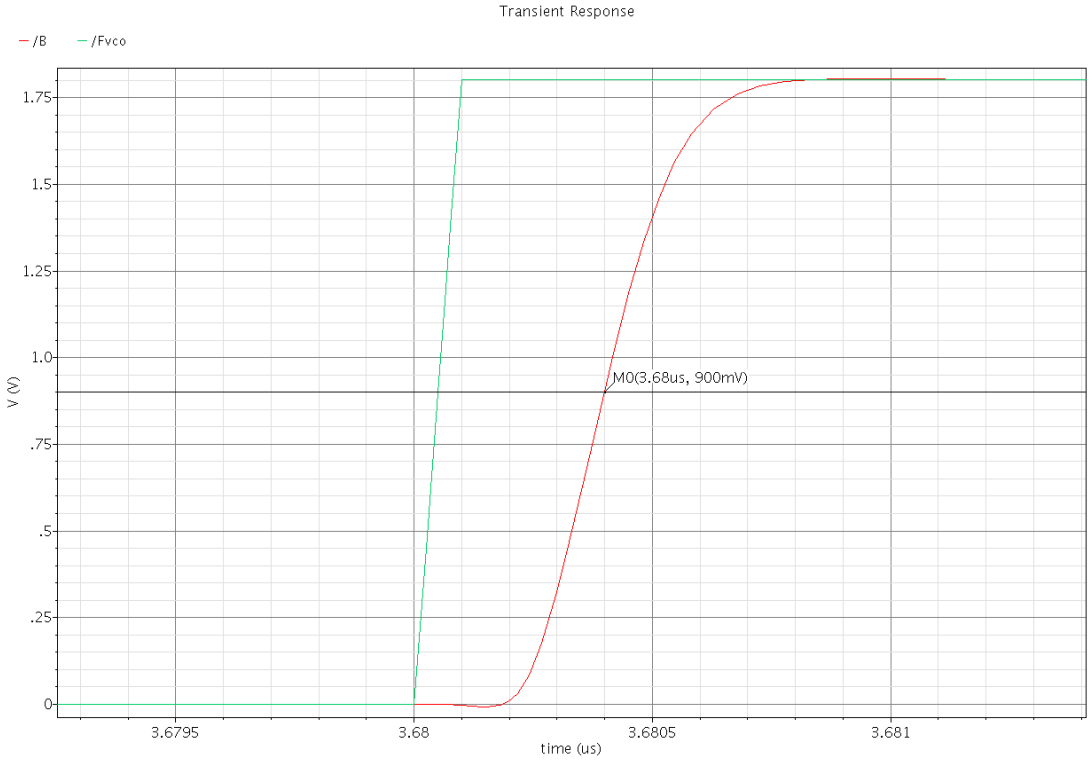


Fig.5.4 Fvco-Down delay in the B-PFD with parasitic effects

As the DFF is the same in both branches, the delay time is the same. The value of this delay is 605ps.

- Reset time

The reset signal suffers a lot the parasitic effect. The capacitances added in each node affect its width as it is illustred in fig.5.5. Now, the reset width value is 1010ps.

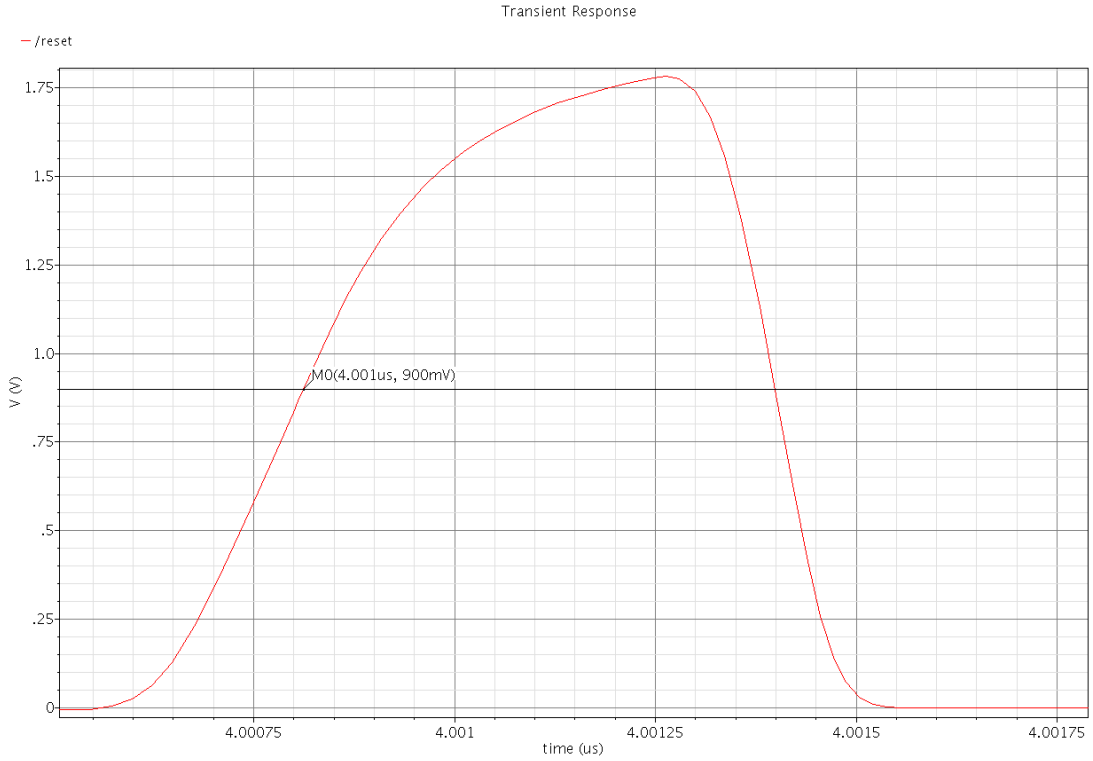


Fig.5.5 Reset time in the B-PFD with parasitic effects

- Current-Power consumption

As it is obvious, the addition of the new capacitances in every node involves an increase in the current that it is traduced as an increase in the power consumption by the circuit. Calculing the average current in a period (2us) of signal and after, obtaining the power consumption value, the results are as follows:

I=291.5e-15A → I/T=1.45e-7 → **P=VI=1.8*1.45e-7=0.26uW**

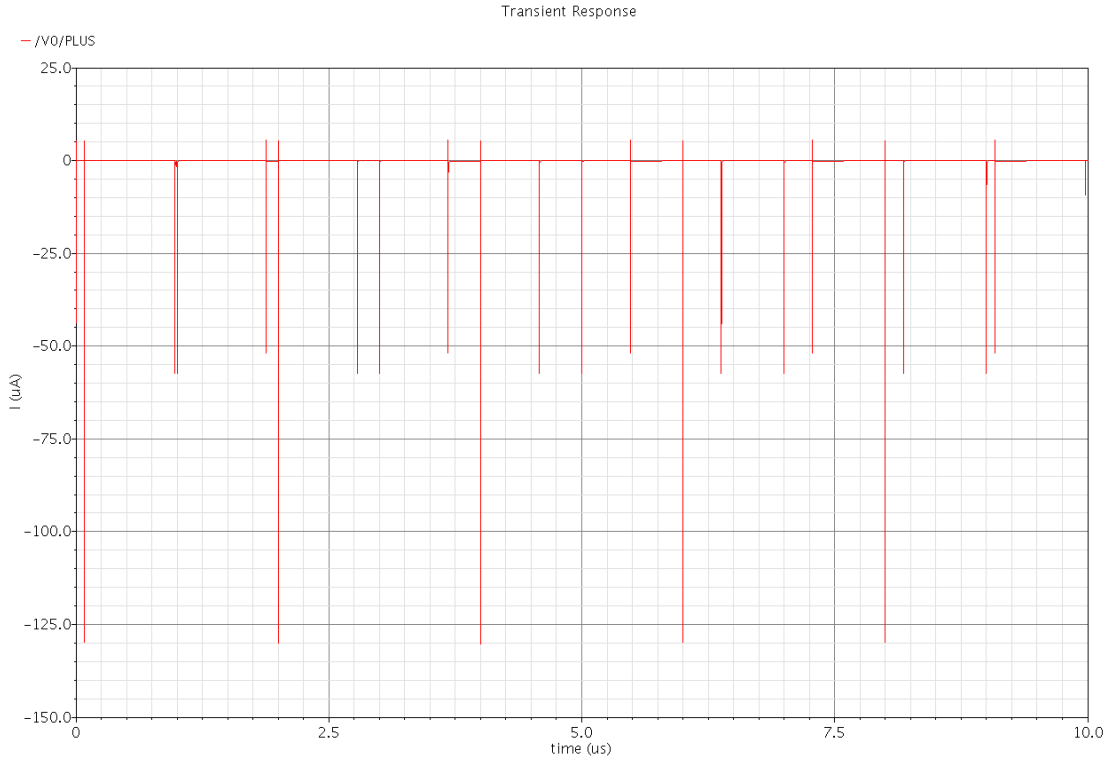


Fig.5.6 B-PFD current with parasitic effects

5.2 FEEDFORWARD RESET PFD WITH PARASITIC EFFECTS

- Transient response

Next fig.5.7 shows the transient response of the Feedforward reset PFD when the parasitic effects are considered. As it is illustred in it, the waves forms are a little bit rounder than in the ideal situation and also the reset signals suffers a notable widening. All these effects mean a bad linearity behaviour in the design.

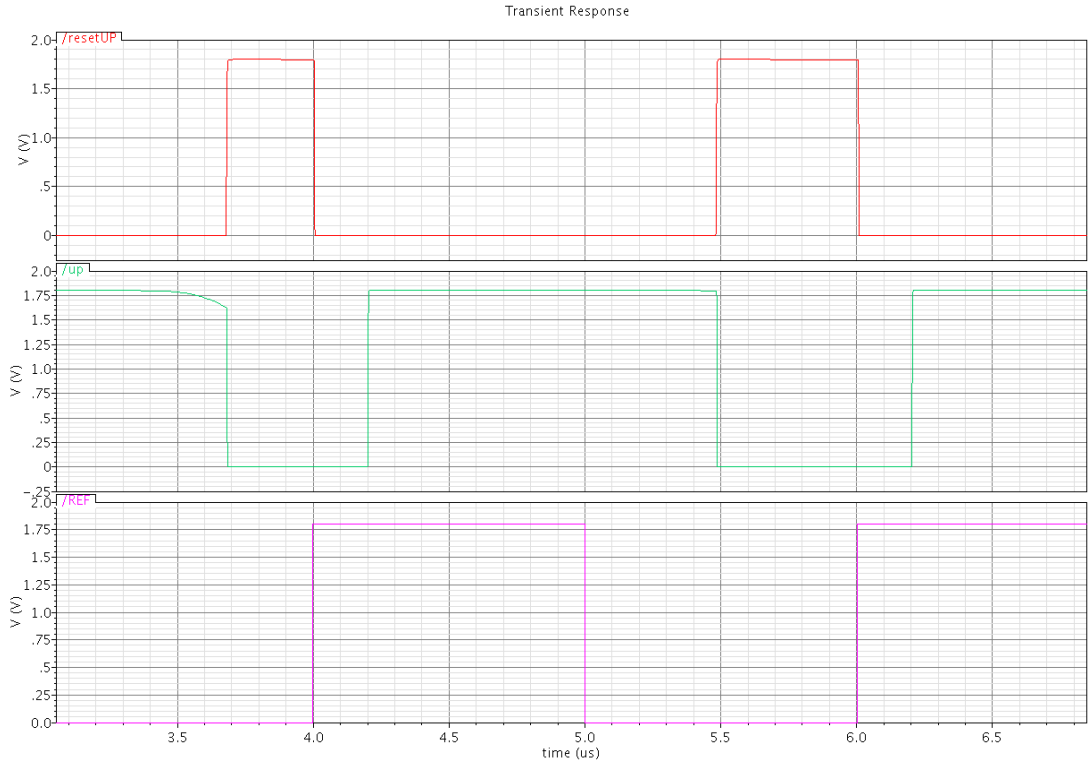


Fig.5.7 FR-PFD transiet response with parasitic effects

- Delay times

- Between CKref and Up signals:

  As it is said before, the delay time between CKref and Up signal measures the DFF delay. The study considering the parasitic effects, consists of "adding" in a simbolic way some capacitances in each node of the circuit. This fact supposes an increase of the D-FF propagation delay as it is traduced in the results.

  The value of this delay is 602ps.

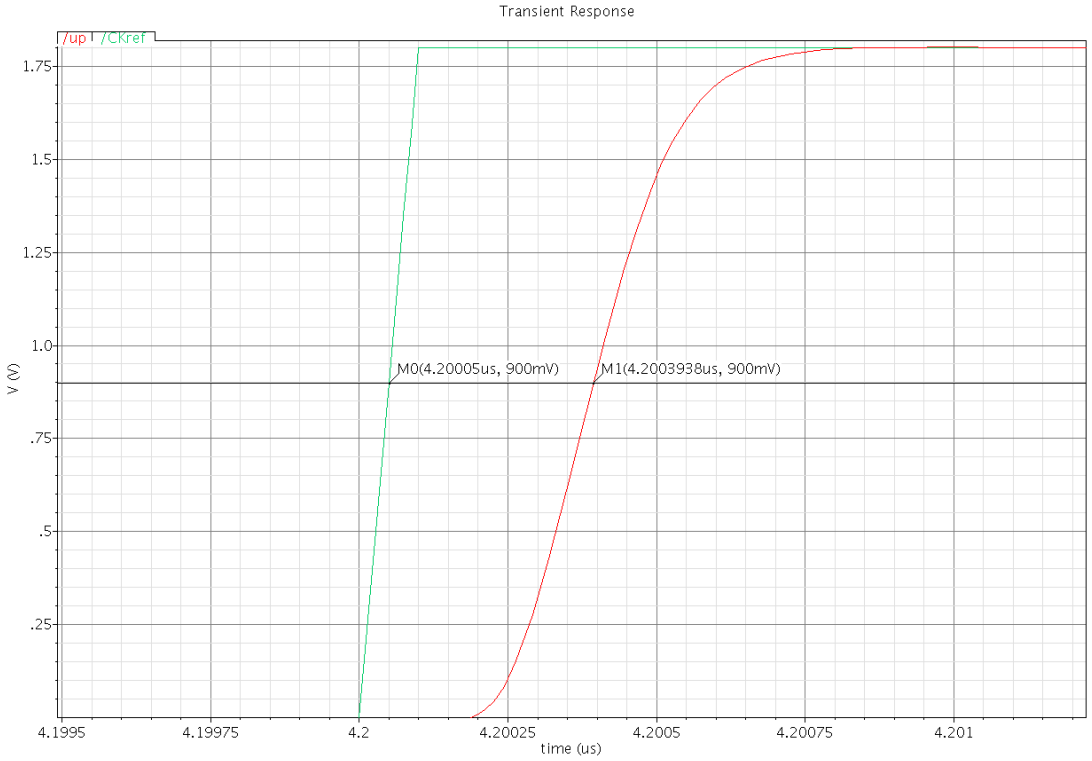


Fig.5.8 CKref-Up delay in the FR-PFD with parasitic effects

- Between CKvco and Down signals:

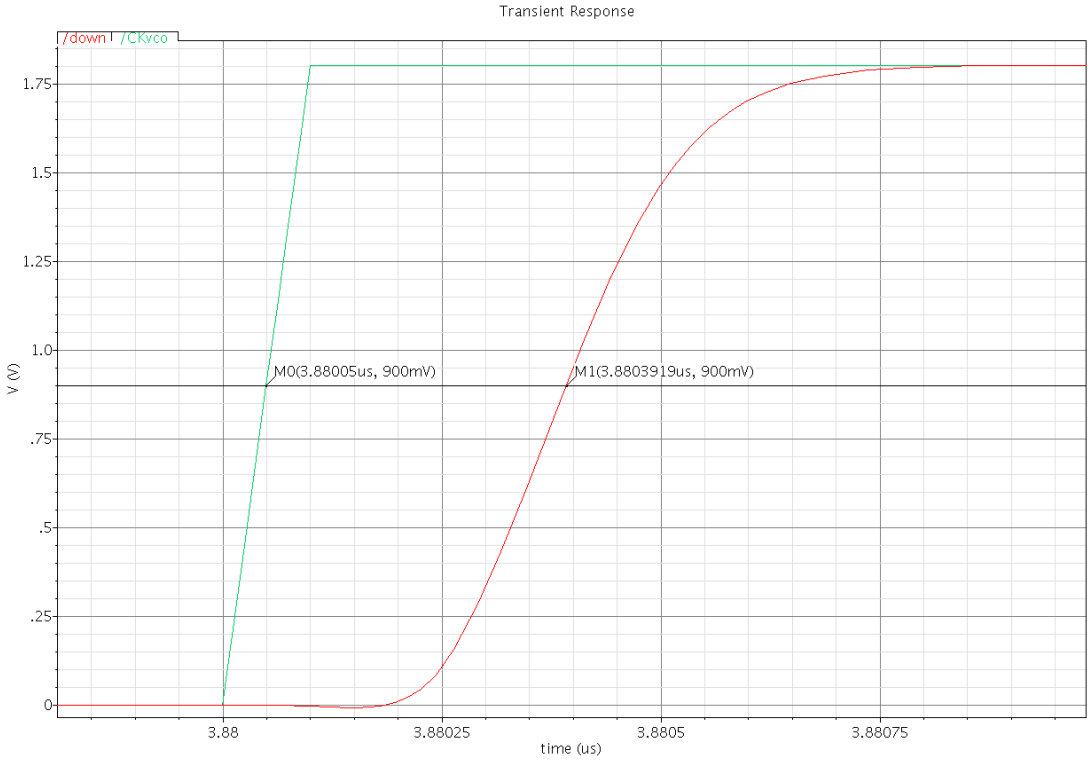


Fig.5.9 CKvco-Down delay in the FR-PFD with parasitic effects

As the DFF is the same in both branches, the delay time is the same. The value of this delay is 599ps.

- Current-Power consumption

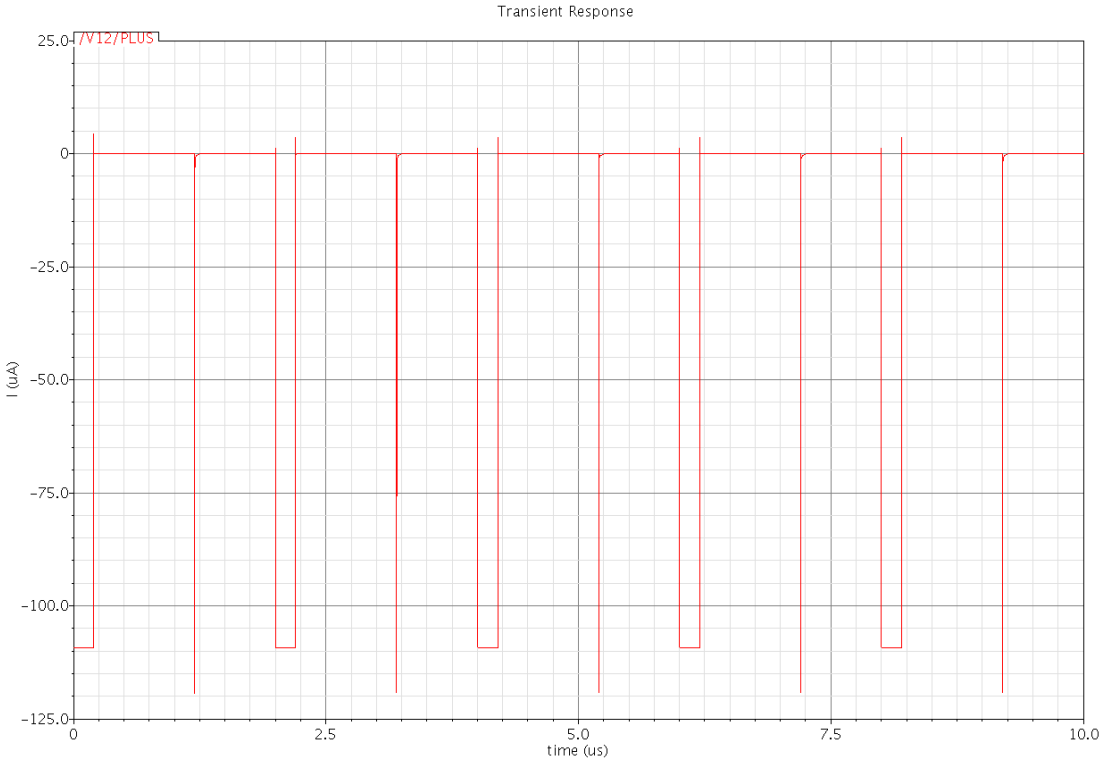


Fig.5.10 FR-PFD current with parasitic effects

The value of the integral of the I signal in the Vdd node in a period is -21.188e-12A. Dividind this value by the period length (2us), the following value is obatained: 10.944e-6A. To obtain the power consumption, P=IV and as the Vdd voltage value is 1.8V, the result is: **P=10.944uA*1.8V=19.7uW**.

5.3 COMPARATIONS

Next table shows briefly the previous simulation results. Values in black correspond to the noideal simulations where parasitic capacitances are considered. Besides, values in grey correspond to the ideal simulations with no parasitic effects made in Chaper 4.

	Basic PFD		Feedforward reset PFD	
Delay time UP	606ps	88.9ps	602ps	79.7ps
Delay time DW	605ps	86ps	599ps	79.3ps

Reset time	1010ps 151.4ps	
Current	291.5e-15A 38.99e-15A	49.01e-12A 21.86e-12A
Power consum.	0.26uW 0.0395uW	19.7uW 19.674uW

As it is detailed here, all the delay times increases because of the presence of the parasitic capacitances. Also, its effect involves a huge increase in the power consumption in both designs.

Comparing the behavior of both models in the real situation of parasitic presence, the Feedforward reset PFD suffers less in the power consumption. Besides, while the reset signal in the basic design suffers a huge increase, in the new design it remains immune.

APPENDIX A

LTSPICE SIMULATIONS

Before can work with CADENCE software, I tried to analyze the behaviors of the circuits simulating them in LTSpice tool. SPICE is an English acronym for Simulation Program with Integrated Circuits Emphasis (Simulation Program with emphasis on integrated circuits). It was developed by the University of California, Berkeley in 1975 by Donald Pederson. It is an international standard which aims to simulate analog electronic circuits composed of resistors, capacitors, diodes, transistors, etc.

For these simulations I used the models that I had in my university courses:

.model n_30 nmos level=2 vto=0.9 kp=57e-6 gamma=0.3 phi=0.7 lambda=0.05 cgso=1.8e-10 cgdo=1.8e-10 cj=7e-5 mj=0.5 cjsw=3.9e-10 mjsw=0.33 js=0.001 tox=4.25e-8 nfs=1e11 Id=2.2e-7 ucrit=10000 rsh=25 af=1 kf=2.3e-27

.model p_30 pmos level=2 vto=-0.9 kp=17e-6 gamma=0.5 phi=0.69 lambda=0.04 cgso=2.8e-10 cgdo=2.8e-10 cj=33e-5 mj=0.5 cjsw=4.4e-10 mjsw=0.33 js=0.001 tox=4.25e-8 nfs=1e11 Id=3.5e-7 ucrit=10000 rsh=45 af=1 kf=7.2e-29

In the absence of data, all the transistors have the same dimensions: length (L)=1um and width(W)=4um.

In all the simulation the VDD will be a DC voltage source of 1.8V. And the Fref and Fvco have the following properties:

	Function	V(1)	V(0)	Tdelay	Trise	Tfall	Ton	Tperiod	Ncycles
Fref	PULSE	1.8V	0V	0s	1e-8s	1e-8s	1e-6s	2e-6s	10
Fvco	PULSE	1.8V	0V	8e-8s	1e-8s	1e-8s	1e-6s	2e-6s	10

1. Basic PFD

Remaining, it is composed by two D-FF and and an AND gate.

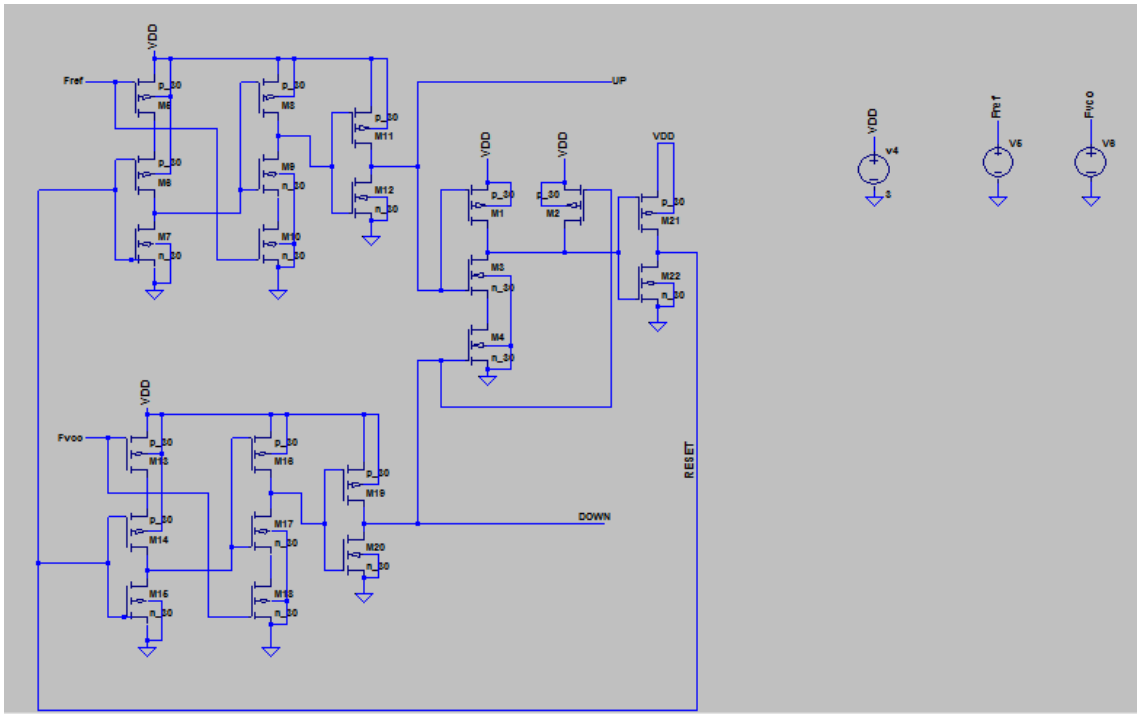


Fig.A.1 Basic PFD LTSpice schematic

- **Transient response**

The waveforms plotted in Fig. A.2 are the transient response: **.trans 0 10u**

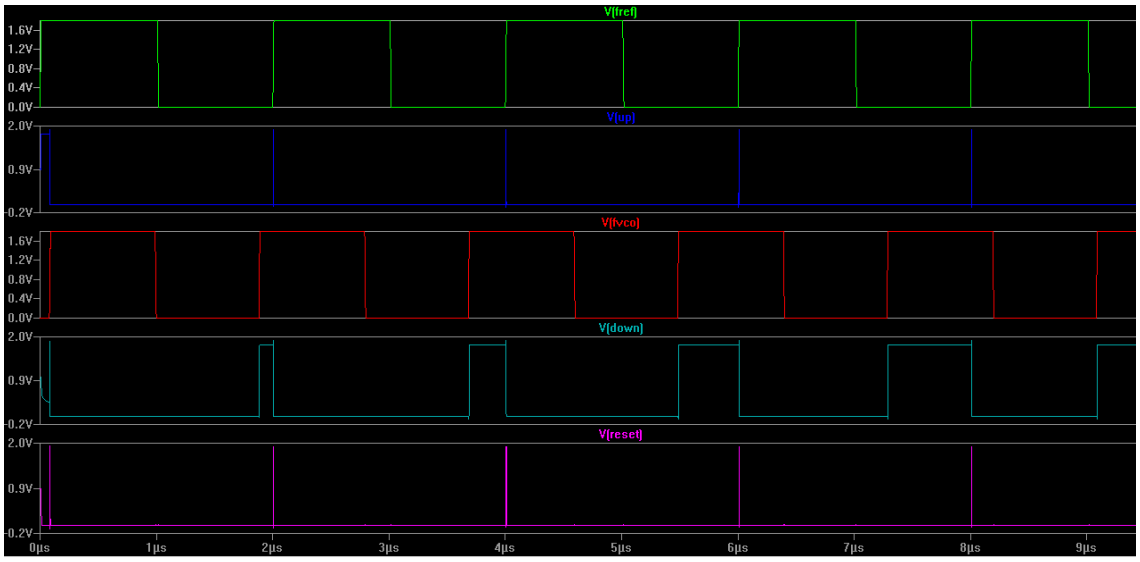


Fig.A.2 Basic PFD LTSpice transient response

- **Delay time**

  It is measured as the delay between the input signals Fref and Fvco and the output ones, Up and Down, respectively; in the middle of the maximum voltage value.

  - Delay between Fref and Up signals:

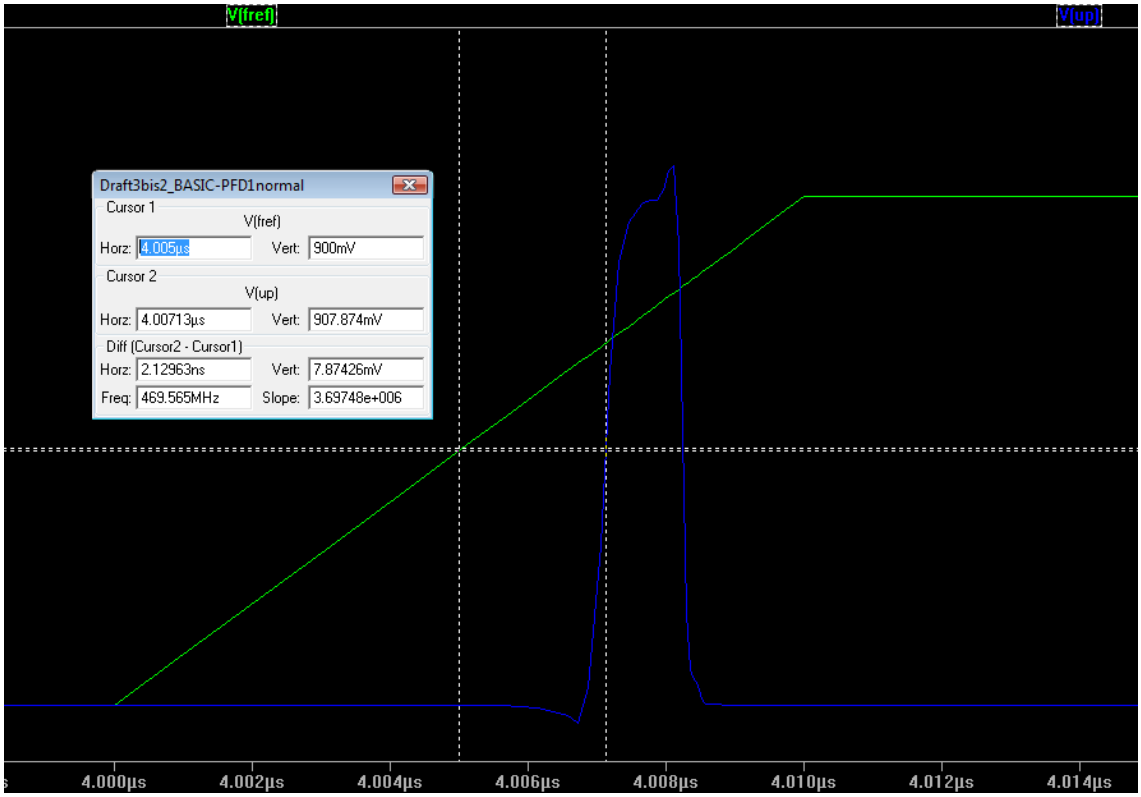


Fig.A.3 LTSpice delay time between Fref and UP signal in Basic PFD

According to the graphic, the delay is 2.130ns.

  - Delay between Fvco and Down signals:

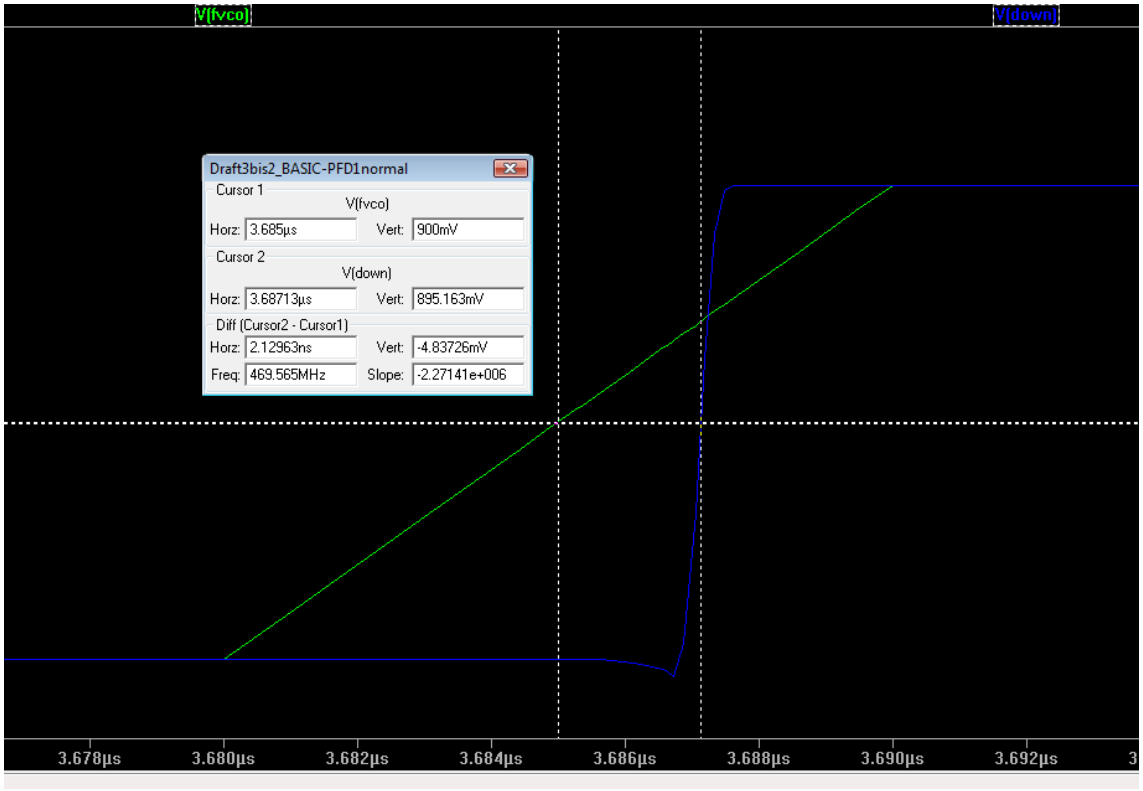


Fig.A.4 LTSpice delay time between Fvco and DOWN signal in Basic PFD

According to the graphic, the delay time is 2.130ns.

- **Reset time**

  It is measured as the reset signal width in the middle of its maximum voltage value.

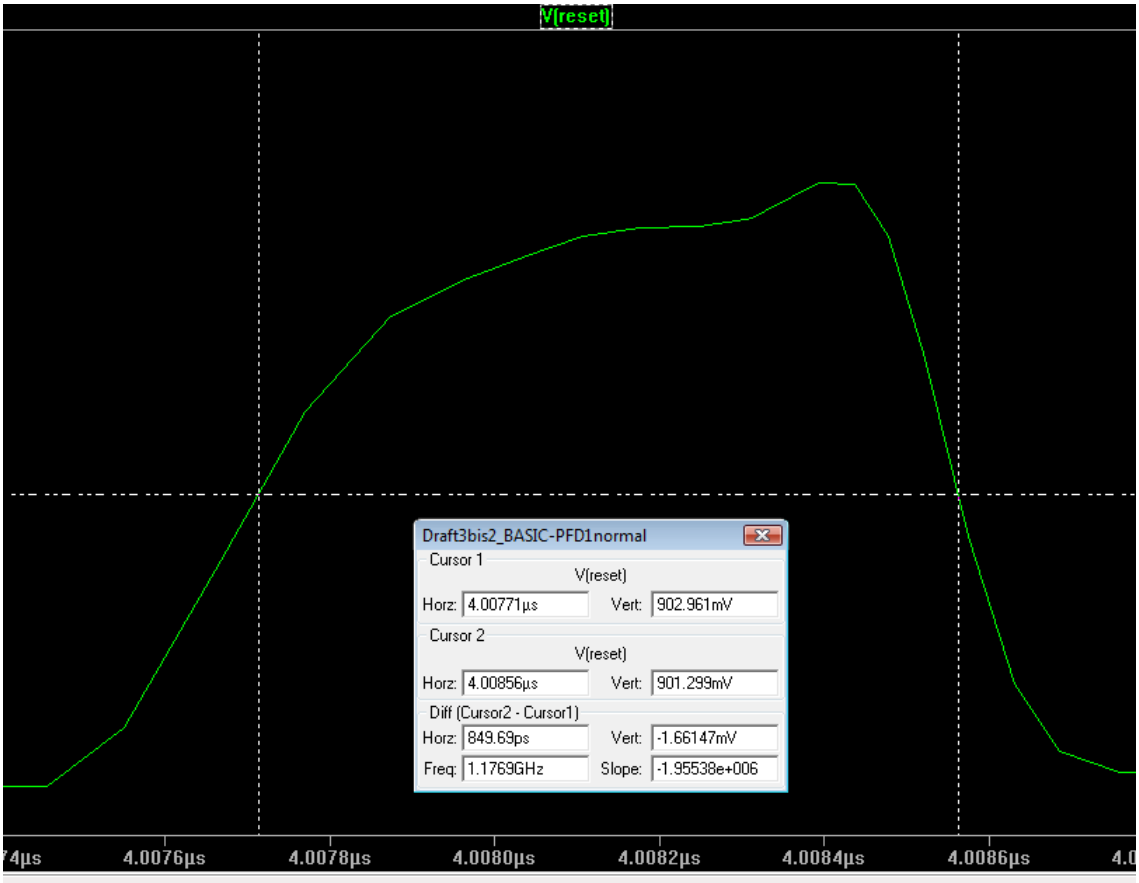


Fig.A.5 LTSpice reset time in Basic PFD

The reset time is 849.69ps.

- **Power consumption – current**

From the simulator, the average current in a period is obtained (which is the integral in a period of the current, divided by the period length). So, multiplying this value to the Vdd voltage, the power consumption is derived.

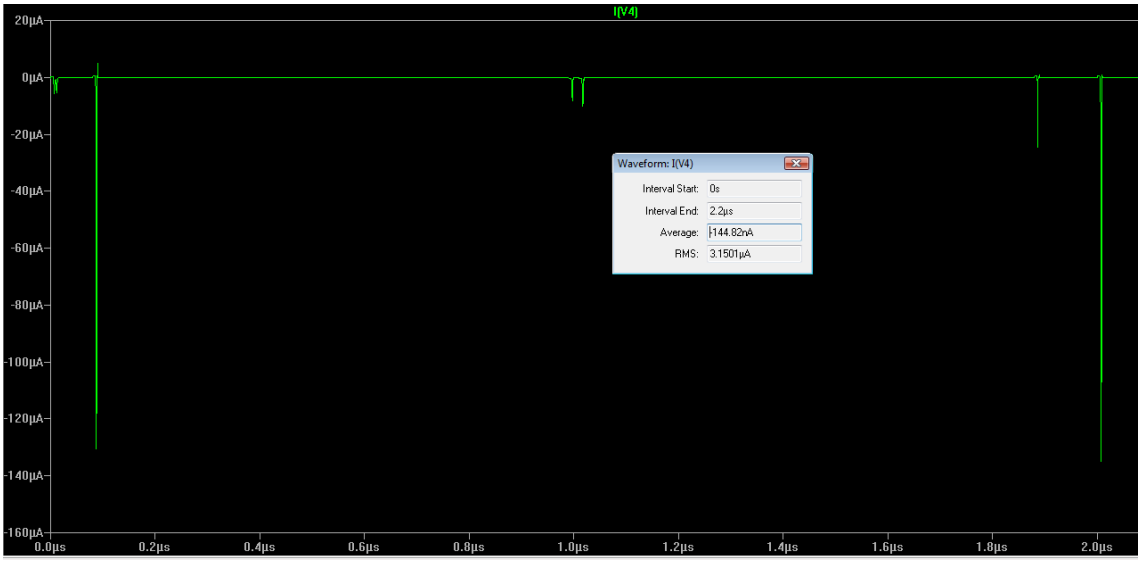


Fig.A.6 LTSpice average current in a Basic PFD

The power consumption will be: P=VI=1.8V*144.82nA=2.61e-7A=0.261uW.

2. FEEDFORWARD RESET PFD

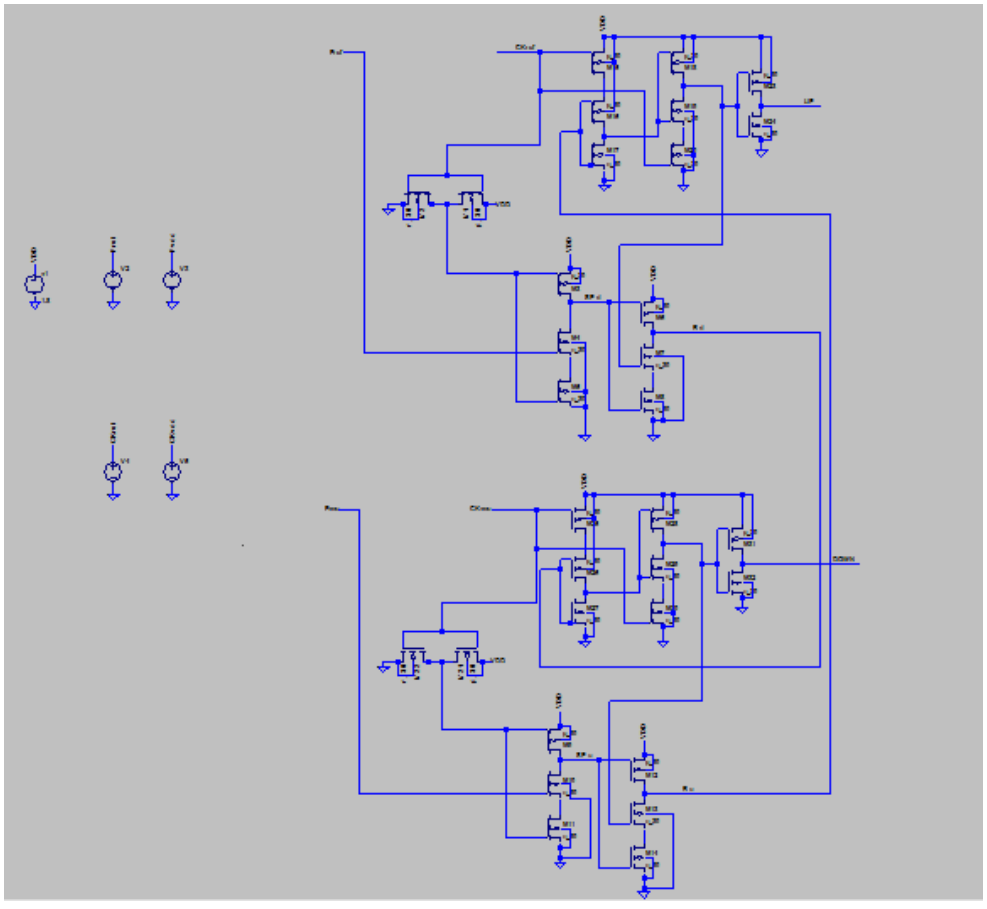


Fig. A.7 Feedforward reset PFD LTSpice schematic

- **Transient response**

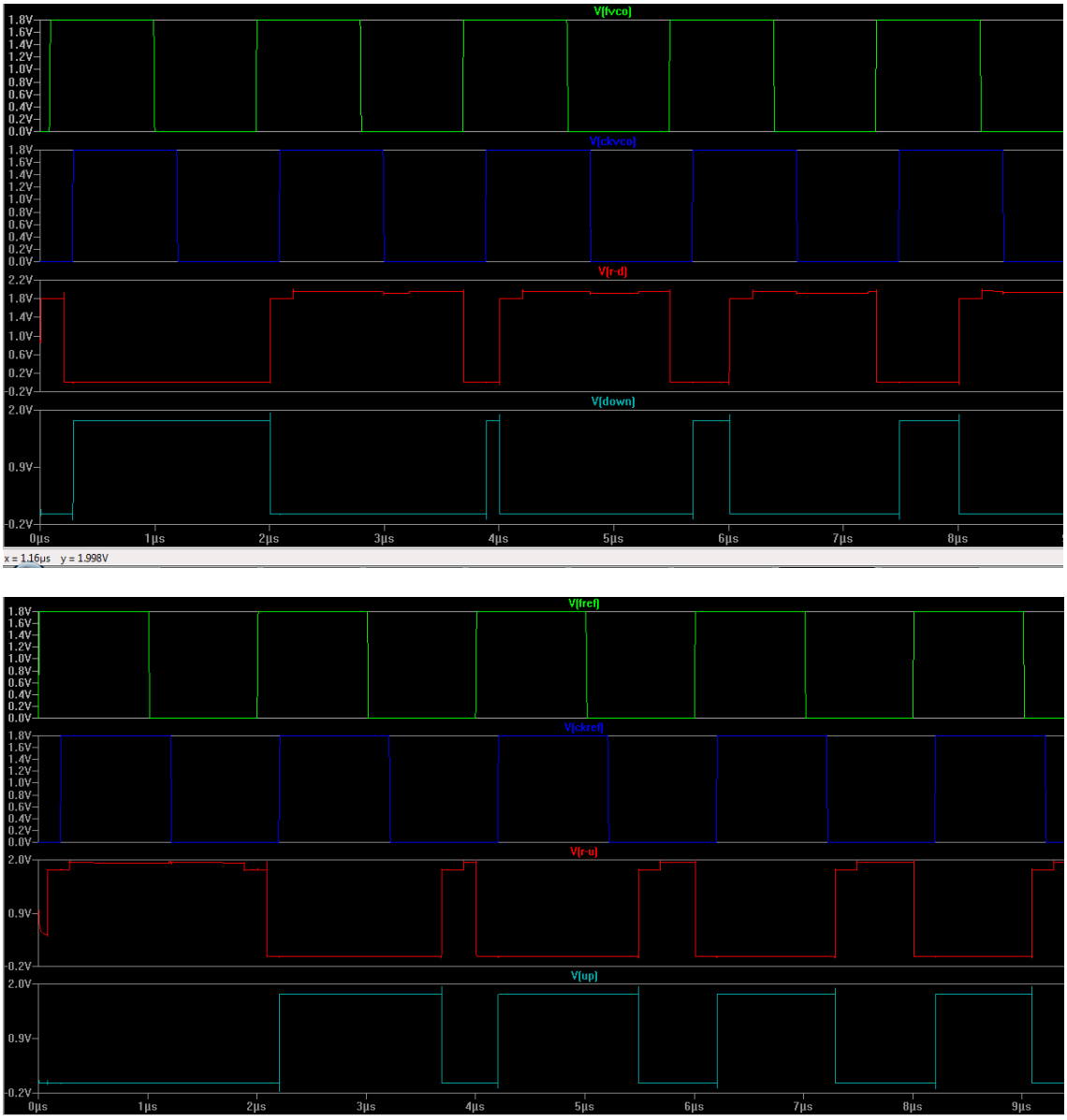


Fig. A.8 Feedforward reset PFD LTSpice transient response

- **Delay time**

It is measured as the delay between the input signals Fref and Fvco and the output ones, Up and Down, respectively; in the middle of the maximum voltage value.

- Delay between CKref and Up signals:

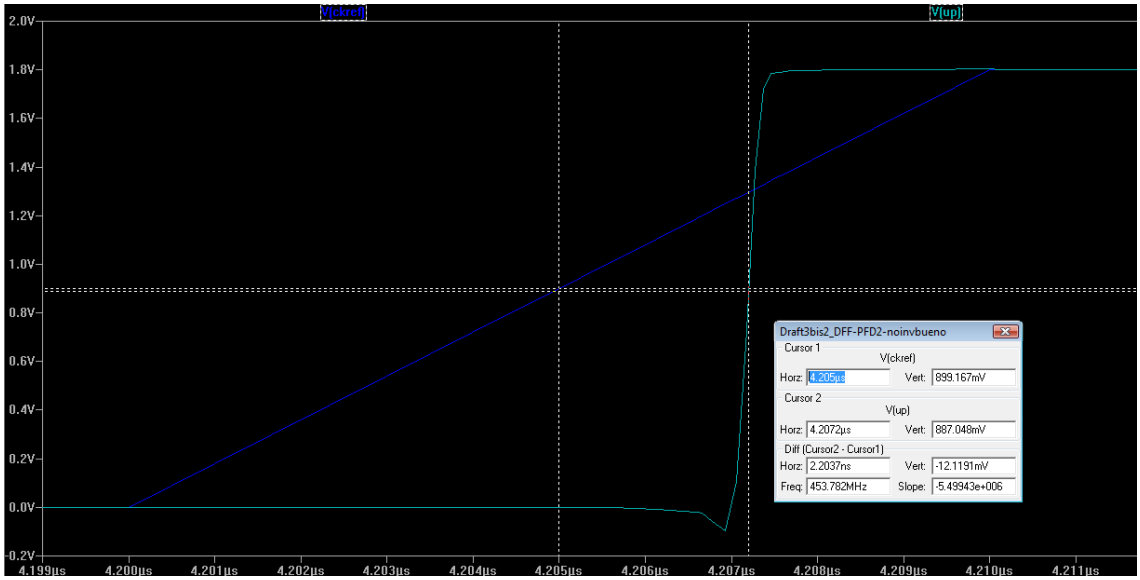


Fig.A.9 LTSpice delay time between CKref and UP signal in FR-PFD

According to the graphic, the delay is 2.204ns.

- Delay between CKvco and Down signals:

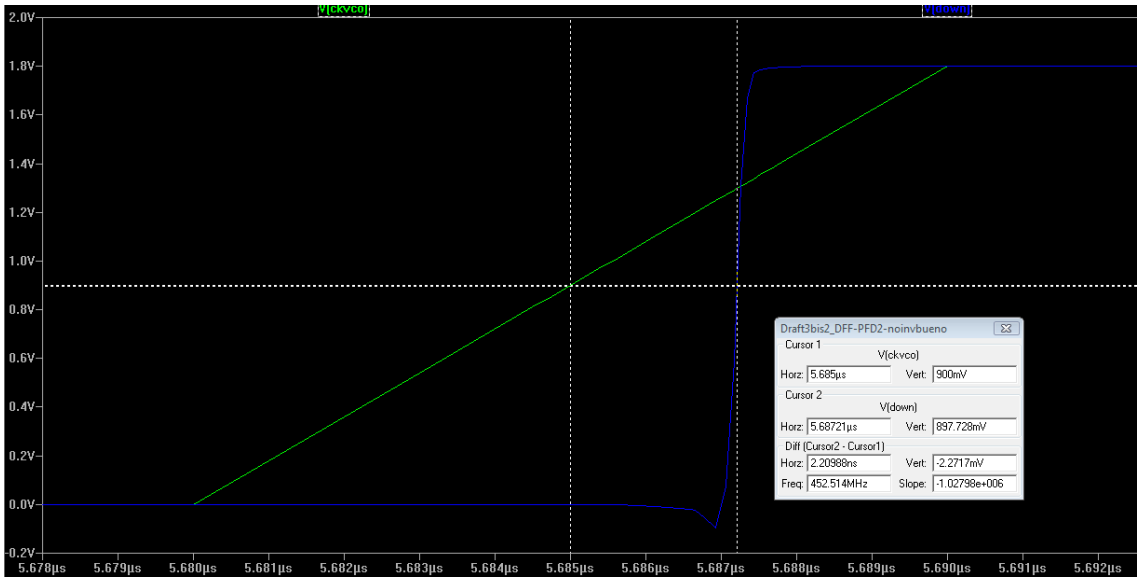


Fig.A.10 LTSpice delay time between CKvco and DOWN signal in FD-PFD

According to the graphic, the delay is 2.210ns.

- **Power consumption – current**

  From the simulator, the average current in a period is obtained (which is the integral in a period of the current, divided by the period length). So, multiplying this value to the Vdd voltage, the power consumption is derived.

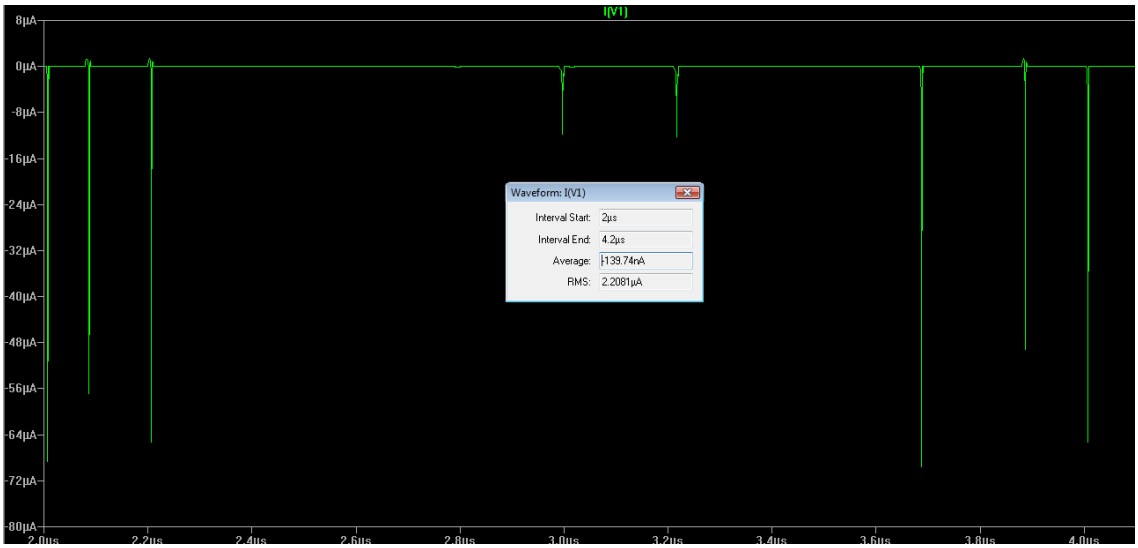


Fig.A.11 LTSpice average current in a FR-PFD

The power consumption will be: P=VI=1.8V*139.74nA=2.51e-7A=0.251uW.

APPENDIX B

Analysis of previous related publications

Article A1

A simple CMOS PFD for High Speed Applications

The design of a good PFD design means play with some PFD parameters that sometimes are opposite to get this good design. In general, the main characteristics that are sought are:

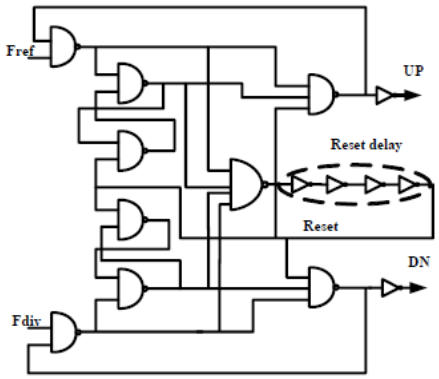
- Its application in high speed designs: this typically involves high power consumption. To obtain that, the method is to redesign the D-FF using some high speed logic families.
- Low power consumption, which limits the speed of operation.
- High maximum operation frequency: so, it means reduce the circuit delay and the number of transistors and their size. The maximum operation frequency is defined as the shortest period with correct UP and DN signals together with the inputs have the same frequency and 90º phase difference. It increases with the voltage supply (that should be as low as possible).´
- Free dead zone

The ideal PFD design has free dead zone, the highest maximum frequency of operation with the lowest power consumption. But that is not easy to obtain. Later, some designs will be compared:

- **Conventional PFD**

  The conventional PFD design has several disadvantages. When it is used in high frequency applications, this leads to high power consumption. Besides, its speed is limited because its maximum operation frequency is inversely proportional to the reset pulse width and to the transistors number and size. In this design 48 transistor are used.

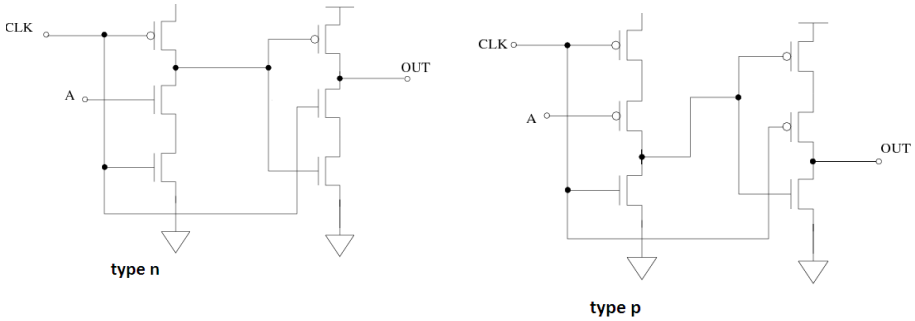
In addition to this, this configuration suffers from dead zone effect. The simplest method to reduce it is to introduce several inverters in the Reset signal. But this damages the maximum frequency of operation that, as it is known; it depends on the reset signal delay. If this delay increases, the maximum frequency decreases.



- **Modified pre-charge PFD (MPt-PFD)**

One way to increase the operation speed without suffering damages is to use a specific dynamic logic family, as TSPC (True Single Phase Clock), which performs the flip flop operation with little power and at high speeds.

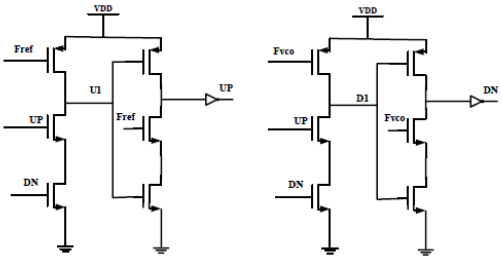
The TSPC logic is “n-p” logic, since of each gate exists the n-version and the p-version. The main advantage of the TSPC logic is the presence of a single clock, since for its internal structure it is not necessary the presence of the clock negated. This family has shown good characteristics in term of speed, area occupancy and power dissipation. It has got also some disadvantages as a complicated distribution of the CLK signal and also, the huge evaluation time difference between the P-logic (very slow) and the N-logic.



Apart from that, every dynamic logic needs of a pre-charge (or pre-discharge) transistor to lead to a known state some pre-charged nodes. This is done during the working phase known as pre-charge phase or memory phase; during another working phase, the evaluation phase the output has a stable value.

As advantage, comparing to the conventional PFD design, it does not suffer the dead zone effect. Besides, it presents the highest maximum frequency of operation. But, due to the use of 16 of transistors; its power consumption is still high.

The following scheme is the modified TSPC pre-charge PFD which is presented. It uses 16 transistors using an n-type modified TSPC circuit. It is called MPT-PFD.

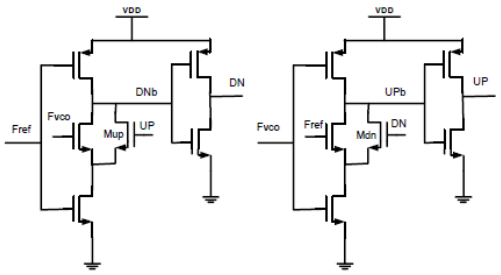


- **Falling Edge PFD (FE-PFD)**

Edge Triggered D flip flops are often implemented in integrated high speed operations using dynamic logic. This means that the digital output is stored on parasitic device capacitance while the device is not transitioning. This design of dynamic flip flops also enable simple resetting since the reset

operation can be performed by simply discharging one or more internal nodes.

The proposed design is shown below. It is composed by 12 transistors, so, that means less power consumption.

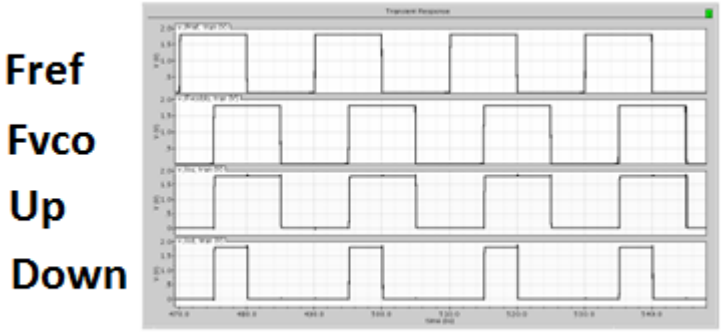


Simplifying, this structure works like that:

UP and DN signals trigger because of the falling edge of F_{vco} and F_{REF}, respectively.

-UP and DN output signals will be high when both F_{REF} and F_{vco} are high.

-UP and DN output signals will be down when both F_{REF} and F_{vco} are down.



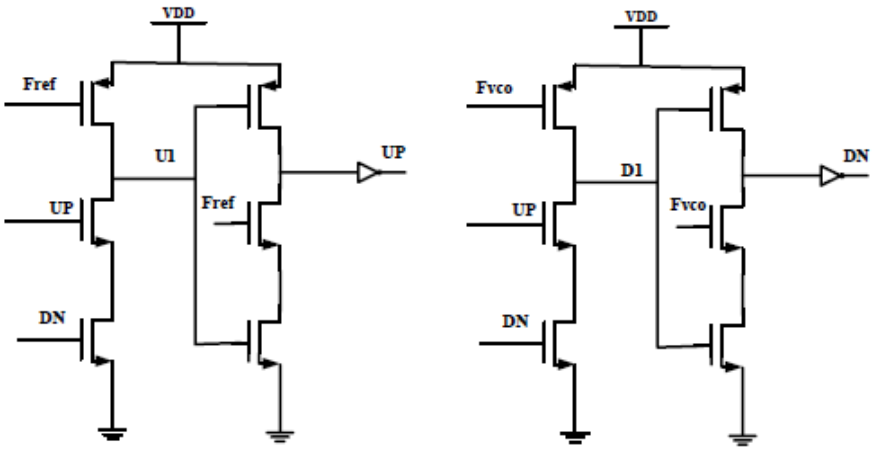
So, the difference in pulse width between UP and DN is equal to the phase difference between the input frequencies.

Besides, looking at the frequency characteristics, the difference between the output signals duty cycle will determinate which output signal will be active, so, if the V in the capacitor of the charge pump must be increased (so, increasing the Fvco) or decreased (so, decreasing the Fvco).

In summary, the Falling Edge PFD design presents the following properties: free dead zone, the lowest power consumption (thanks to the only 12 transistors in use) and a higher maximum operation frequency than the conventional PFD design but lower than the MPt-PFD.

- **Simulaciones**

Figure 2: Modified Pre-Charge Type PFD (MPT-PFD) circuit architecture.



The simulated circuit is like as follows and it is fed with two input signals that have the following properties:

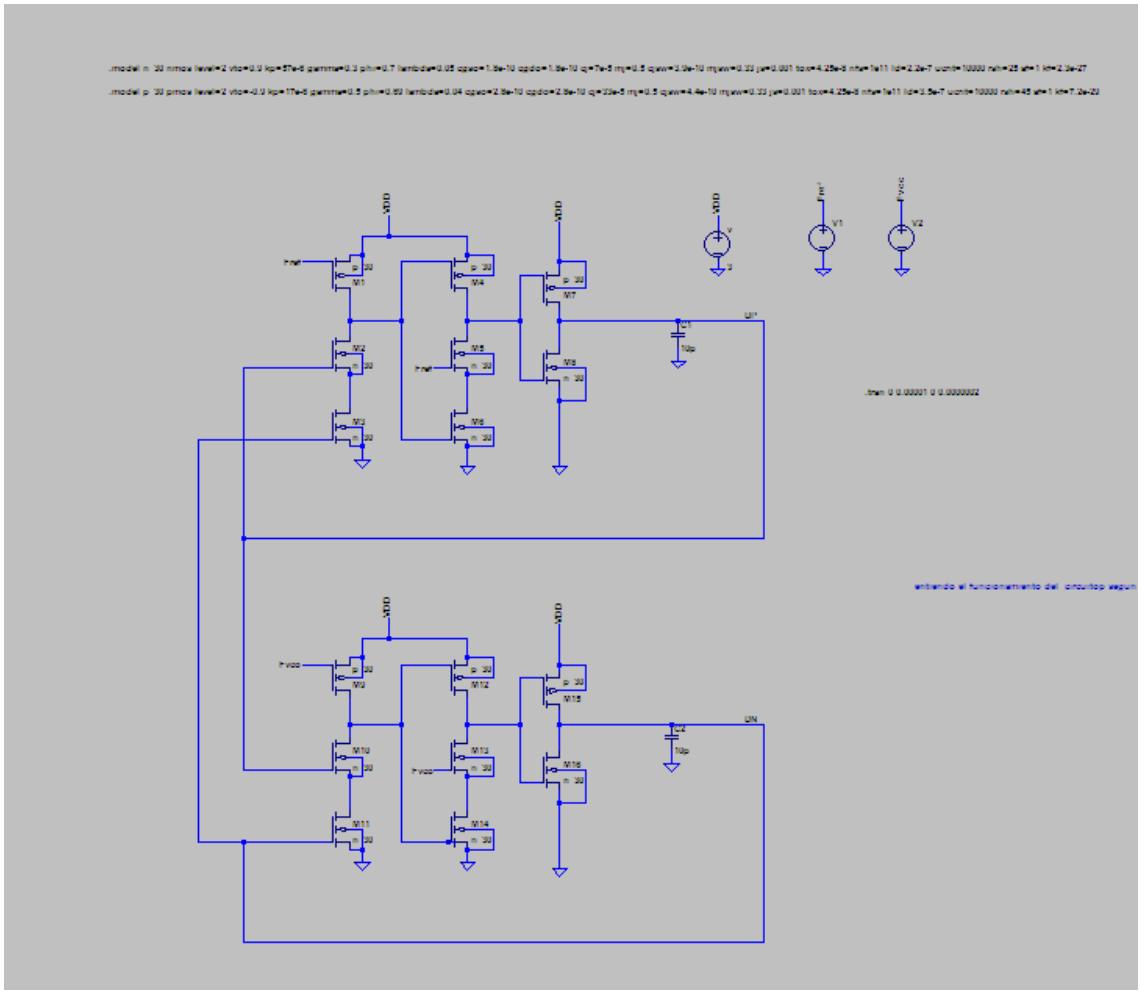
	V1 (V)	V2 (V)	Tdelay (s)	Trise (s)	Tfall (s)	Ton (s)	Tperiod (s)	Ncycles
Fref signal (500 KHz)	0	3	0	1e-12	1e-12	1e-6	2e-6	10
Fvco signal (550 KHz)	0	3	5e-7	1e-12	1e-12	9e-7	1.82e-6	10

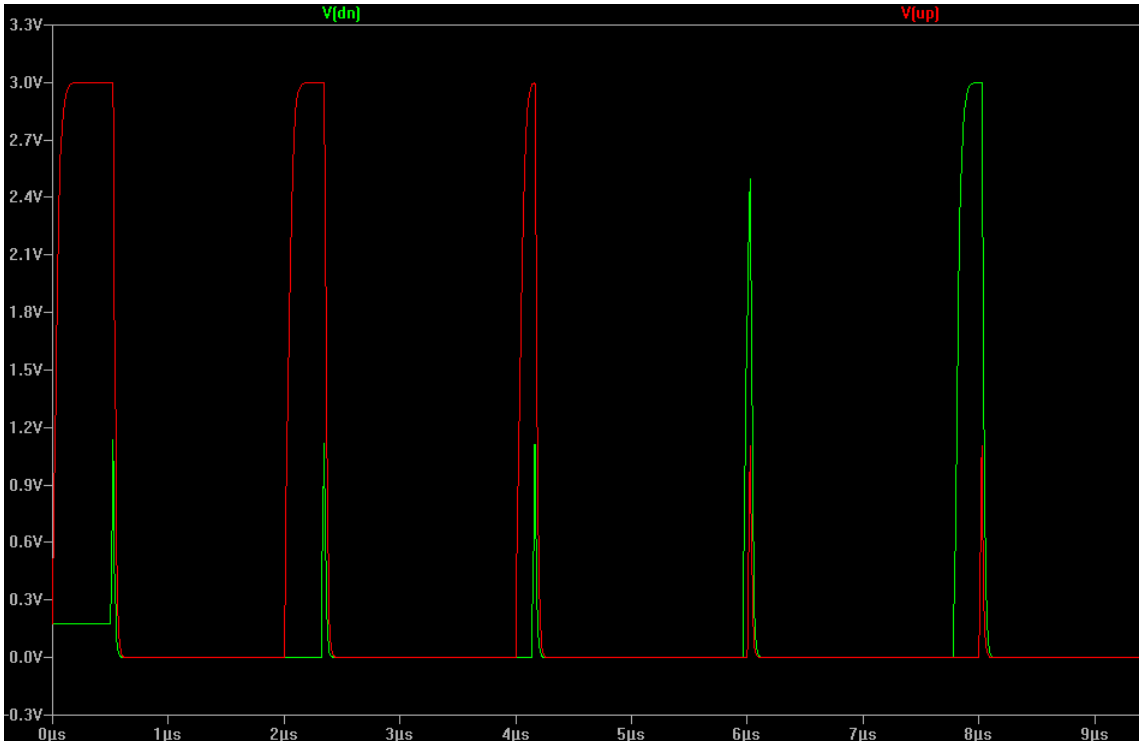
-VDD is a constant voltage source of 3V

-The size of all the transistors is L=1um and W=4um

-The simulation consists on a time-domain transient simulation with Tstop=1e-5 seg; Time to start saving data=0 seg and Maximum time step=2e-7 seg.

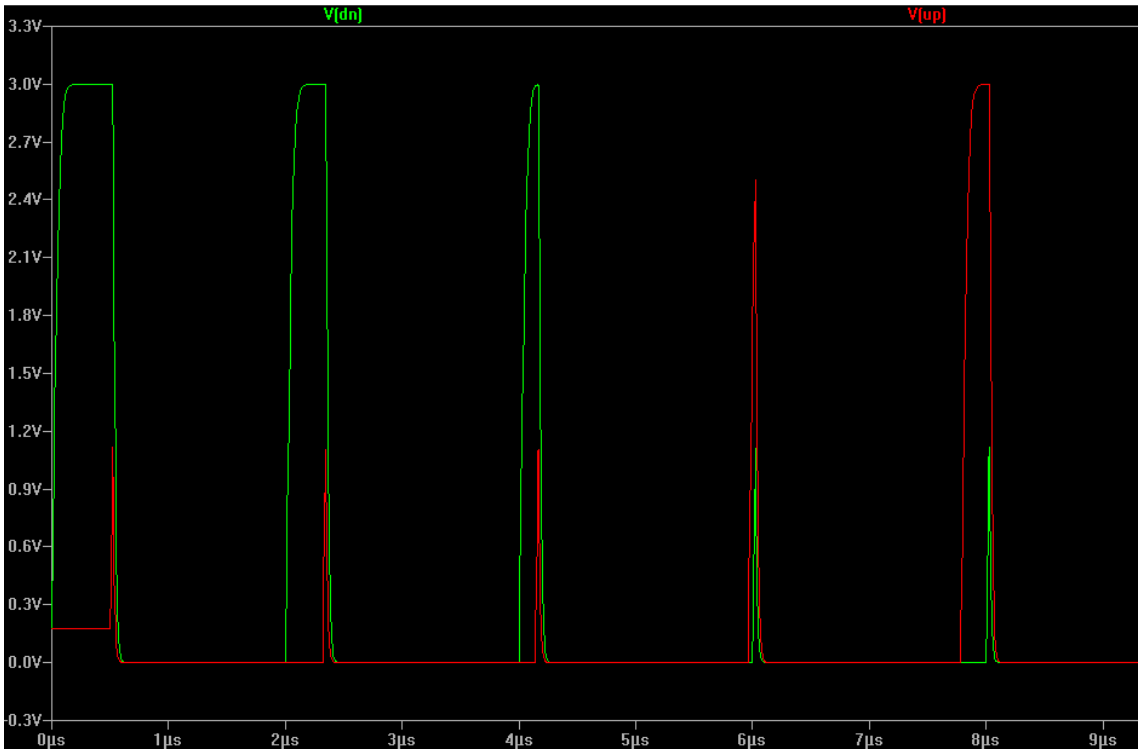
According to all that, we obtain the graphics bellow:





In it, we can see that the first pulse width of the UP signal is the phase difference between the two input signals.

If the input signals are interchanged: Fref=550KHz and Fvco=500KHz, changing also the rest of the parameters that are shown in the table, we obtain the following output:



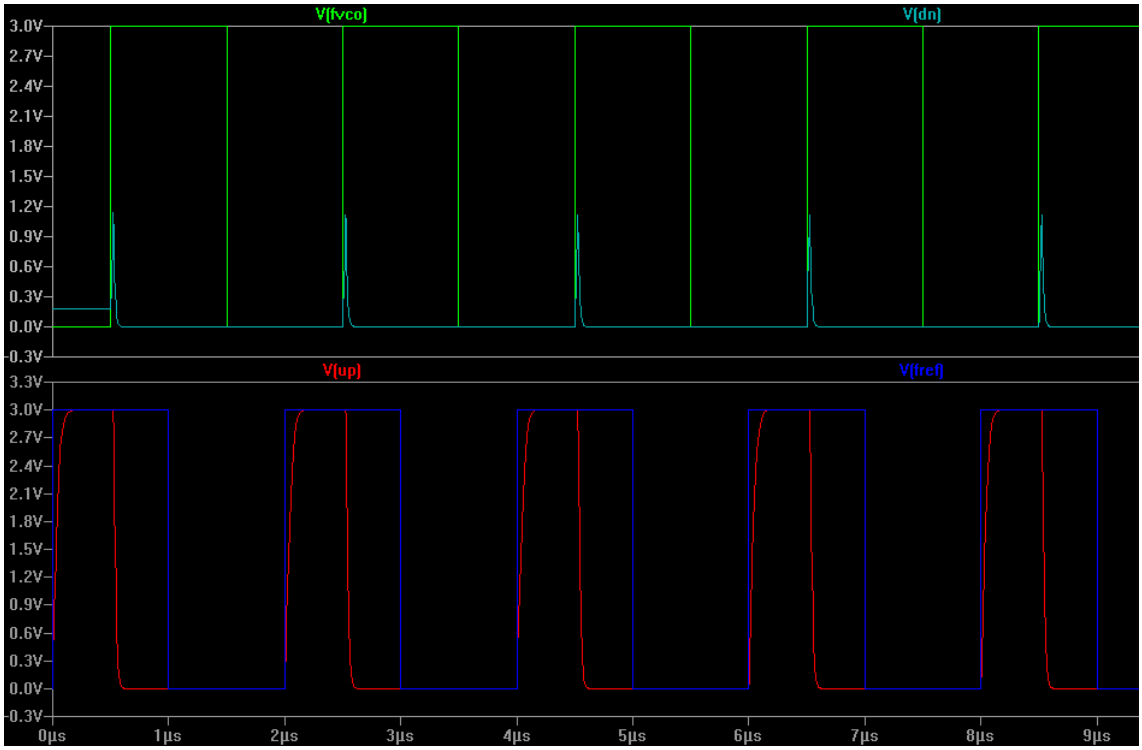
Now, the signal whose first pulse width shows the difference phase between Fref and Fvco is DOWN (DN) signal.

These values coincide with the theoretical values.

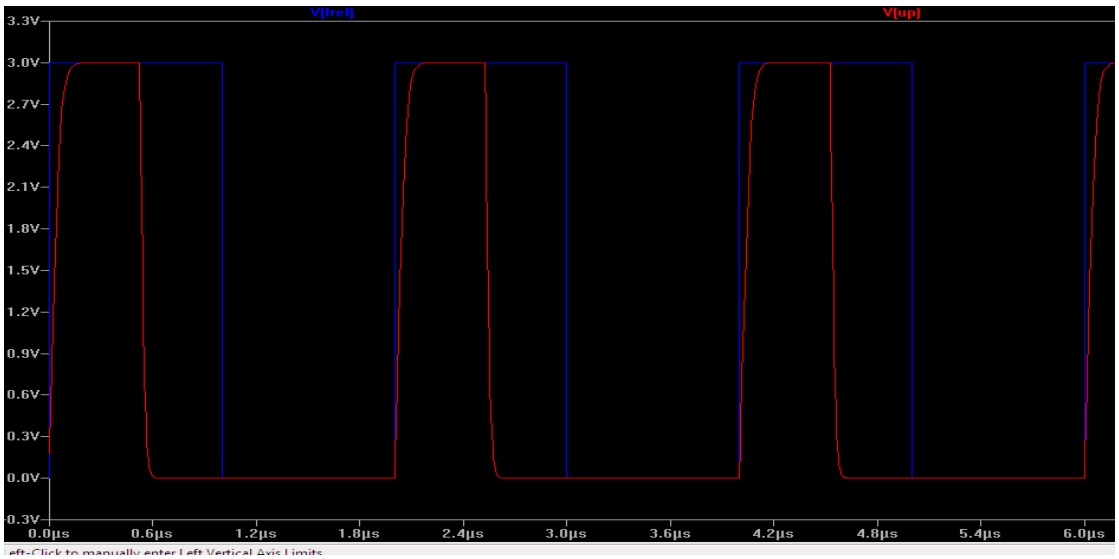
To analyze the results in a better way, I re-simulated the circuit introducing two input signals with the same frequency but a delay between them.

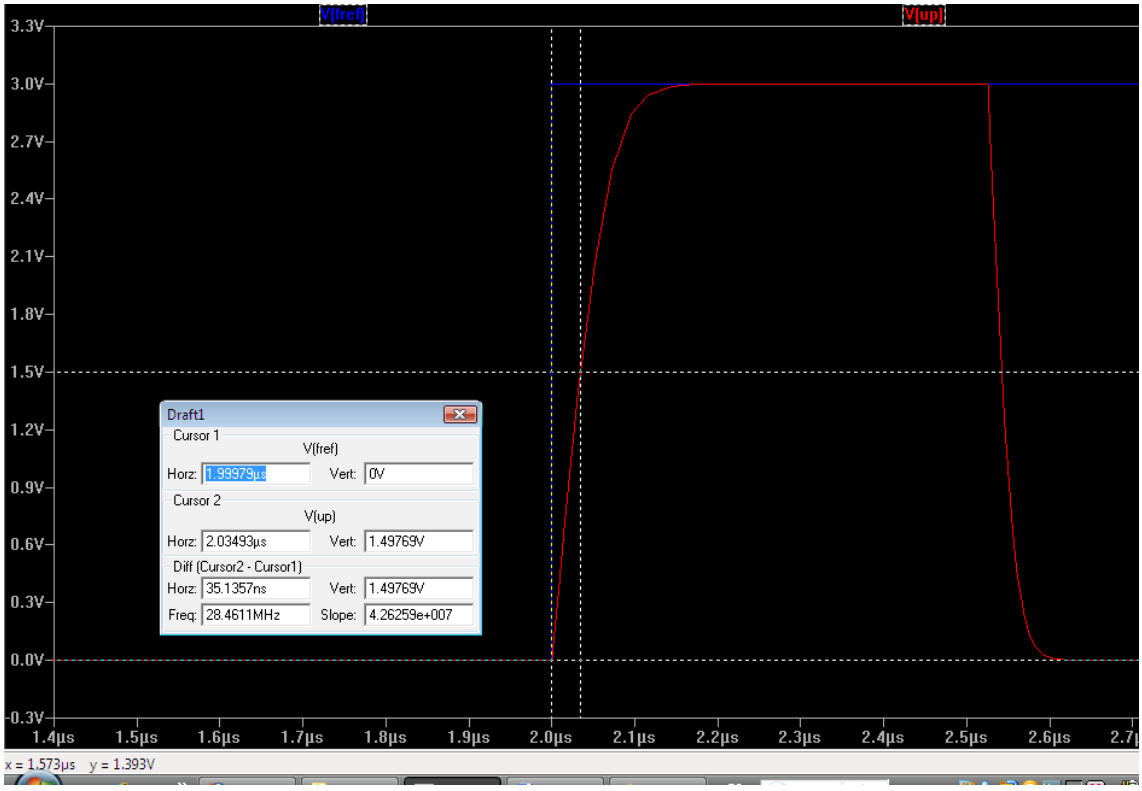
	V1 (V)	V2 (V)	Tdelay (s)	Trise (s)	Tfall (s)	Ton (s)	Tperiod (s)	Ncycles
Fref signal (500 KHz)	0	3	0	1e-12	1e-12	1e-6	2e-6	10
Fvco signal (500 KHz)	0	3	5e-7	1e-12	1e-12	1e-6	2e-6	10

The results are like that:



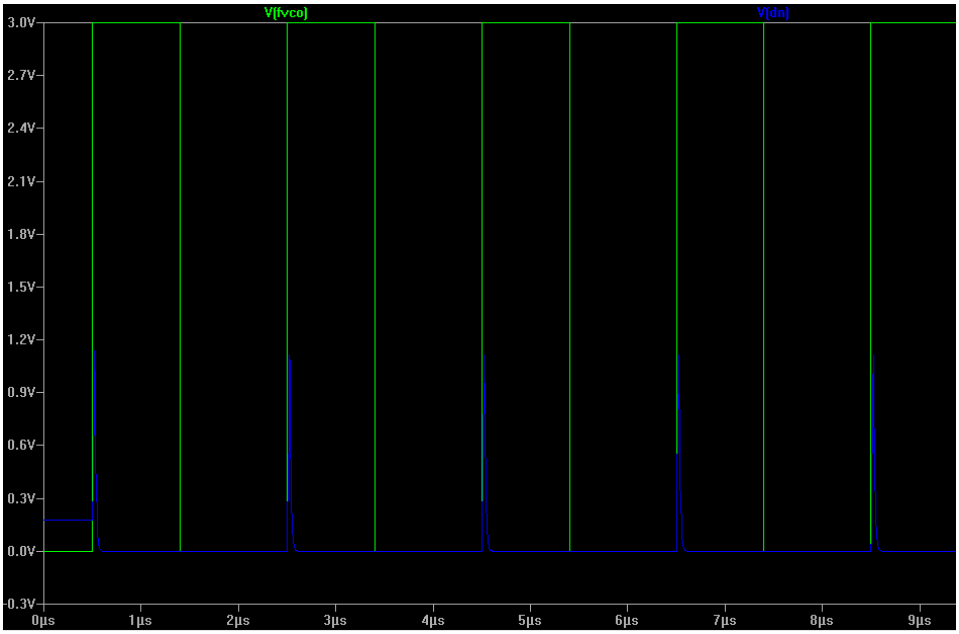
Measuring:

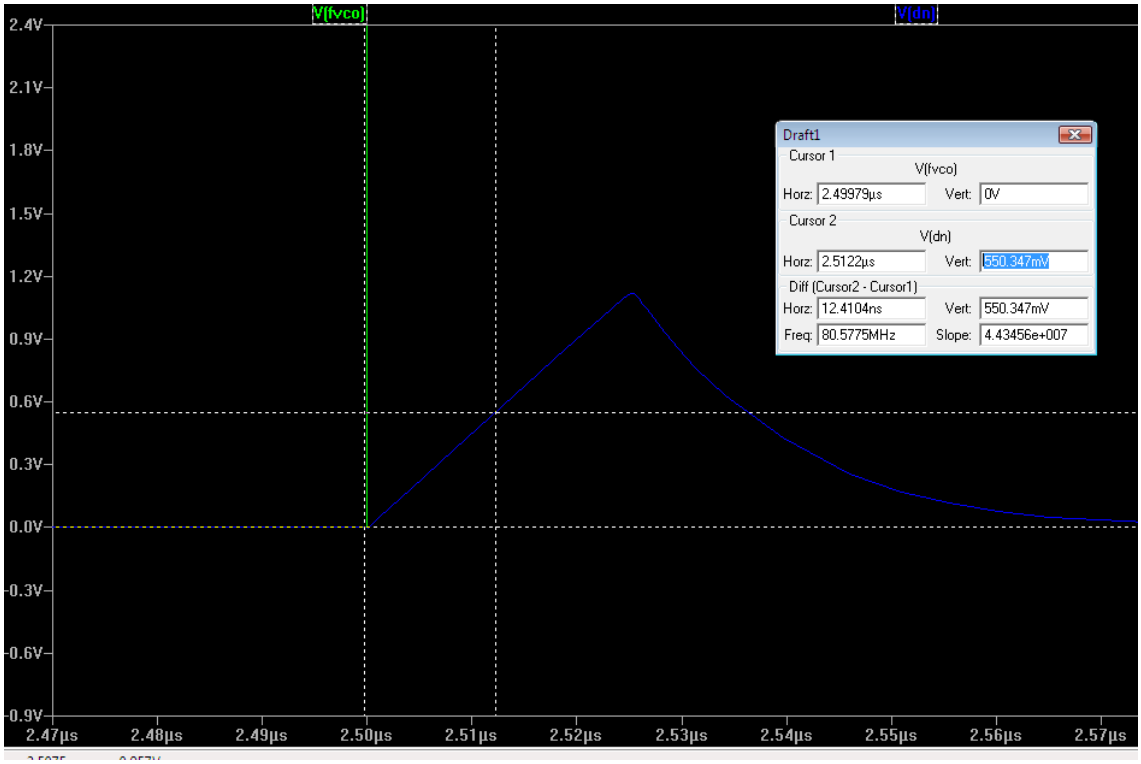




So, the time difference in the middle voltage value between the Fref and the Up pulses is 35.1357ns.

Looking at the Fvco-DN pair of signals:





So, the time difference in the middle voltage value between the Fvco and the Dn pulses is 12.4104ns.

Article B1

Phase detectors for PLL-based high-speed data recovery

The new proposed PFD is used in PLLs to recover high-frequency clocks to integrated NRZ pseudo-random sequences. It has a simple architecture, removing the state machine.

Traditionally, phase detectors used to this application include a state machine with a nonlinear operator to generate energy at the speed of the data; but their performance degrades rapidly at high frequencies due to flip-flop which forms the state machine.

The general structure of the proposed PD is shown below:

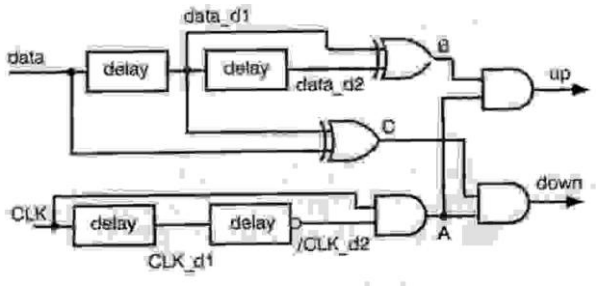


Fig.1

Conventional PD uses a single-phase clock and multi-phased data signals. In contrast, this new design taps has multi-phase clock signals and the data sequence. Thus, it gives simplicity and achieves high-speed operation. The way to create multi-phase signals (CLK_d1 and CLK_d2) is to delay the clock signal (CLK).

This structure could be still simplified in PLLs with ring-oscillator type VCO. In that situation, the two delay stages to generate CLK_d1 and CLK_d2 signals would not be necessary because they could be obtained from the VCO. This idea is shown in the following figure:

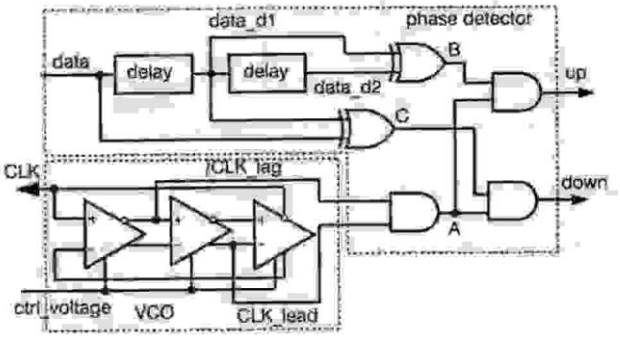


Fig.2

Comparing both structures: “CLK_d1” in Fig.1 is similar to “CLK” in Fig.2. “CLK” in Fig.1 is similar to “CLK_lead” in Fig.2. “/CLK_d2” is similar to “/CLK_lag” in Fig.2.

Furthermore, if the number of stages of the oscillator is even and bigger than 4, the AND gate can be removed since that signal is generated directly to the VCO output. Next figure shows that idea:

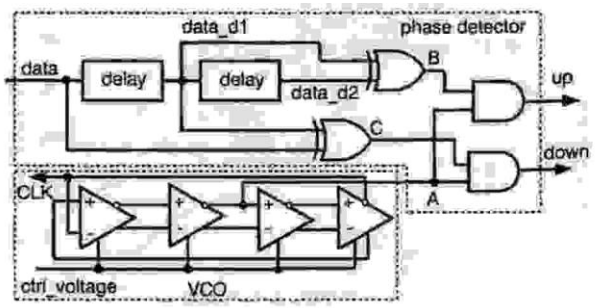


Fig.3

This new PD design can be used for both clock recovery and random signals and allows working at higher speeds tan conventional ones.

Article B2

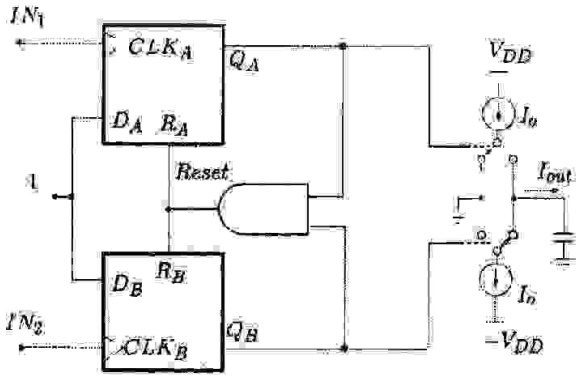
A modular Phase-Frequency Detector design with ±2Nπ linear range of operation

Objet: increasing the linear range of operation in a PFD/CP (charge pump)

This new design gives a modular extension range of -2Nπ to 2Nπ, where N is an integer, order of the PFD/CP. This new range improves frequency acquisition time. Besides, the improvement of frequency acquisition of single-loop PLLs requires an extended linear range of operation for PFDs and, also, it is a way to avoid some kinds of noises.

- A conventional structure of a PFD/CP is shown:

PFD consists of 2 D-flip-flops and an AND gate. And the CP is made of 2 current sources I_o, 2 switches and a capacitor. The current sources charge or discharge the capacitor according to the flip-flop output (Q_A and Q_B).



Finite state machine: when the phase difference between the input signals IN_1 and IN_2 is within ±2Nπ, I_{out} (in average) is proportional to this phase difference. For input phase differences larger than 2π, the output current is not linear. Talking about times, the time that the state machine spends in the state 1 is equal to the time difference between IN_1 signal rising edge and IN_2 *rising edge*. And, thus, the amount of charge to the capacitor is proportional to this time.

As it is said before, if the input phase difference is larger than 2π, the linearity disappears. The way to make it larger is to increase the number of states of the PFD in

order to know the exact difference between the number of rising edges of IN_1 and the number of rising edges of IN_2. This difference is the frequency difference between IN_1 and IN_2. Due to the CP elements, this frequency difference is integrated, so at the end, it provides the phase difference between IN_1 and IN_2.

- The new design: (2N D-flip-flops and N charge pumps)

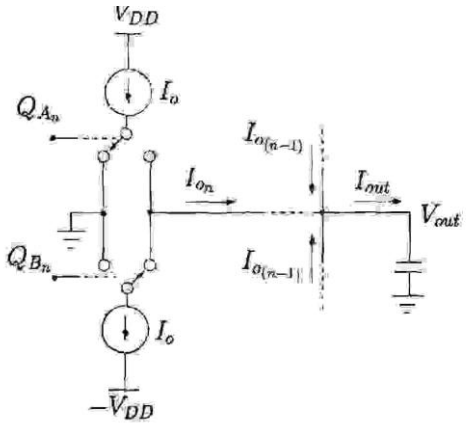
The new state machine has 2N+1 states. This new state machine works like that: if the phase difference between the input signals IN_1 and IN_2 is between $2\pi(k-1)$ and $2\pi k$; k is ≥ 0 and $\leq N$; then, the state is +k in the time interval from the rising edges between signals IN_1 and IN_2. On the other hand, if the phase difference between IN_1 and IN_2 is between $-2\pi k$ and $-2\pi(k-1)$, the machine is in the state –k in the time interval from the rising edges between IN_1 and IN_2.

D represents the input signal to the D-FF, according to:

$$D_{An} = \begin{cases} 1, & n = 0 \\ Q_{An-1}, & 1 \leq n \leq N-1 \end{cases}$$

$$D_{Bn} = \begin{cases} 1, & n = 0 \\ Q_{Bn-1}, & 1 \leq n \leq N-1, \end{cases}$$

So, the new CP circuit is like that:



For example, according with those details, a PFD/CP with range of linearity of $\pm 4\pi$ (N=2) should be like that:

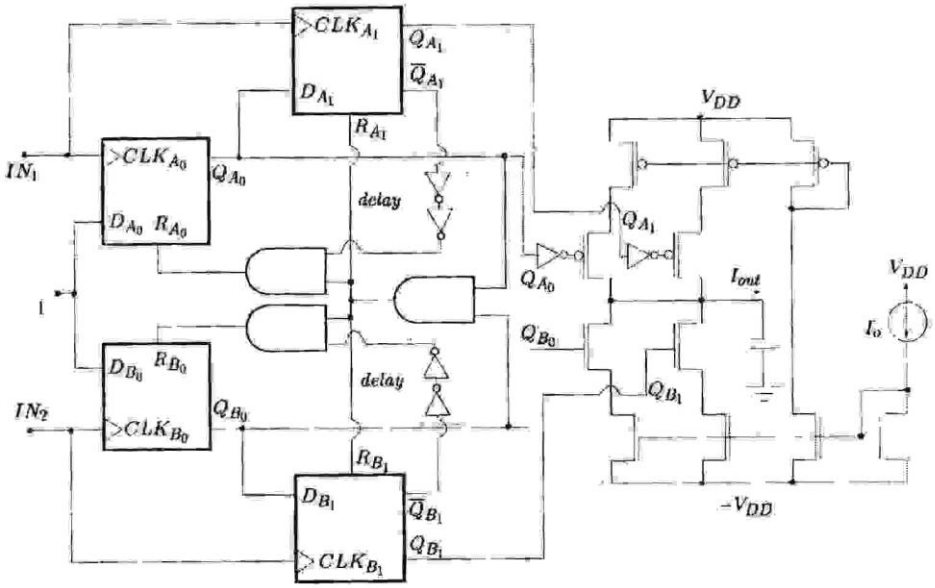
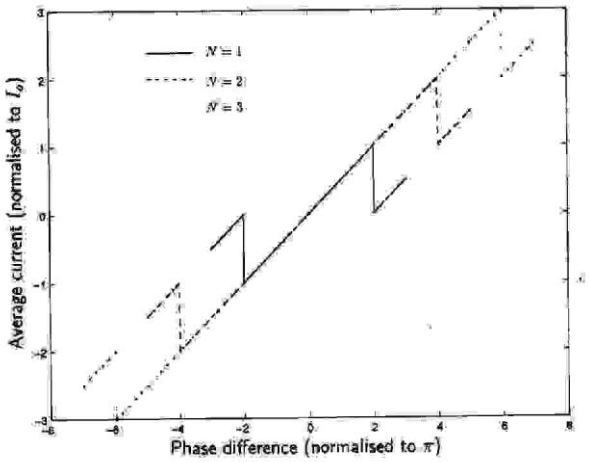


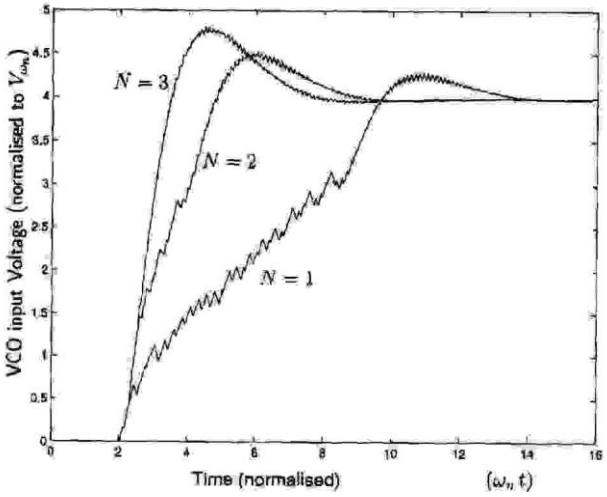
Figure 4. Schematic diagram of a PFD/CP combination with range of linearity of $\pm 2N\pi$. $N = 2$.

Note that the use of inverts is to avoid critical races that could appear between the various reset signals.

As the aim of this new design is to increase the range of linearity, the next figure shows the simulated average output current I_{out} normalized to I_o versus the input signals phase difference normalized to π. The conventional one (N=1), N=2 and N=3 can be compared in it and it is easy to see that actually, the bigger N the larger linearity range:



Such an increase of the linearity range improves the acquisition frequency time as it is shown in the next figure. In it, the transient VCO input voltage (normalized to $V_{\omega c}$) when the input signal is a frequency step of $4\omega_c$ is shown versus the acquisition time. Looking at the figure, the acquisition time is reduced by about 40% in N=2 design and 50% in N=3 design, comparing with the conventional design (N=1):

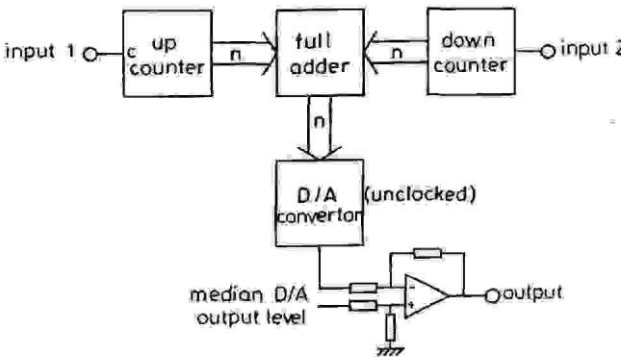


Article B3

Performance of phase-locked loop frequency synthesizer using accumulative phase detector

A new phase detector design is presented, which is capable of linear operation over an arbitrary wide operating range. It is constructed with a pair of n-bit counters. Its linear operating range is between $-(2^n-1)\pi$ to $+(2^n-1)\pi$. This kind of design provides several benefits. First, the linear range of behavior could be modified according to the application; so, cycle slips can be avoided and that allows an analytical treatment of transient behavior. Second, this design involves an important increase in acquisition speed most of the times.

Next figure shows the outline design of the accumulative PFD:

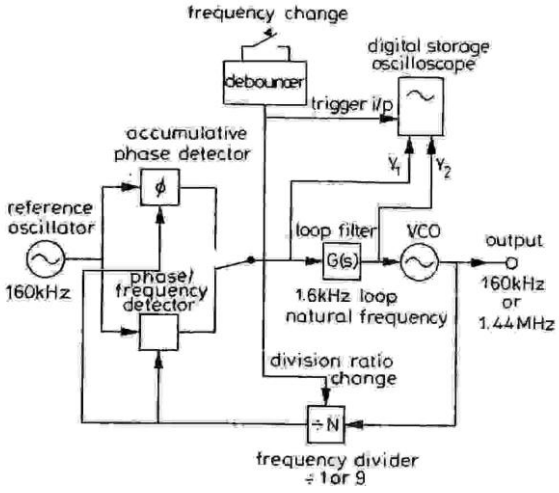


As it is shown, each input is clocked by a counter: rising edges from input1 by the up counter and rising edges from input2 by the down counter. The outputs of these two counters will be summed and converted to an analogical signal thanks to the D/A converter.

If the two inputs have the same frequency, the counters count at the same rate. And, if it exists, the phase difference between the two input signals could add some duty cycle. If the frequency of the input2 increases, the counter of this input will be faster than the other counter; and the overall output declines reflecting the accumulative difference phase between the two signals. After the D/A convertor, there is a differential amplifier which provides a DC offset that gives a symmetrical swing around zero volts.

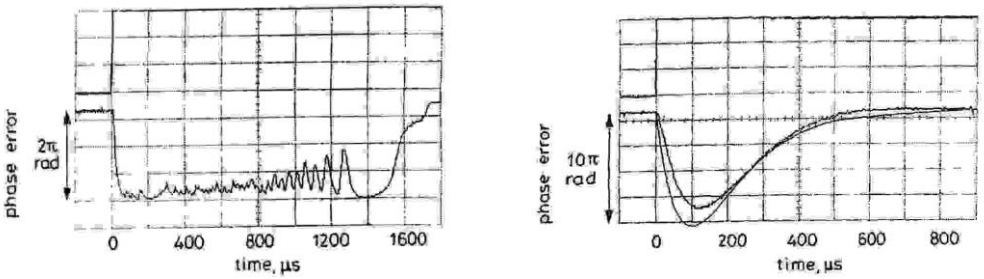
An accumulative phase detector as this one, using n-bit counters has an operating range of $\pm(2^n-1)\pi$ radians, and the n factor will be chosen depending on the application. This wider operating range provides a linear character to the design and that guarantees no cycle slips and phase continuity. To really guarantee no cycle slips, it is important to support S/N ratios high and to use a low noise design in D/A converter and the following analog circuit.

To make sure of this design works and meets expectations, an experimental PLL circuit has been constructed where the new design could be compared with the traditional phase/frequency detector. The PLL circuit is shown below:

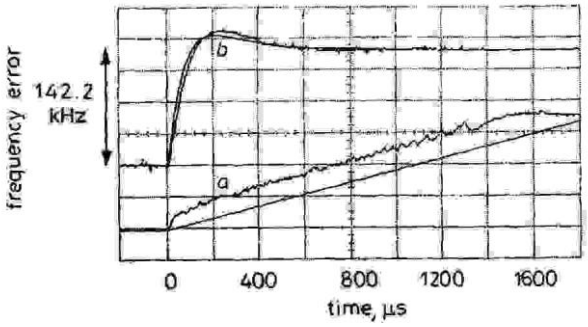


After the simulation, the phase and the frequency error of the PLL with the traditional PFD and with the accumulative PD (with 4-bit counters) have been compared.

Next two figures show the measured phase error transient obtained with a PFD and with the new accumulative PD (filtered, to appreciate it better). In the first one, this error reaches 2π in around 50µs and thereafter, the loop suffers some cycle slips until around 1700µs, when the system becomes stable. In contrast, with the accumulative PFD (filtered), the peak phase error is around 9π rad. Now, the system becomes stable in 600µs, a third part of the same system using the traditional PFD.



The following figure shows the measured frequency error transient obtained with a PFD and with the new accumulative PD after being filtered. Again, the tuning time with the accumulative PD is the third part.



The use of this accumulative PD is beneficial when there is a frequency change of 15% or more. In this case, cycle slipping could appear and it could be avoided with the accumulative phase detector.

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