A Novel Design Method for Phase-Locked Loops of any Order and Type

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***Abstract*—In this paper a novel approach to the design of PLLs is presented, which can be used regardless of their Order and Type. The method stems from the fact that high-frequency poles in the loop filter determine filtering properties of the PLL, while zero-pole (at the origin) pairs determine its Type and thus the loop control dynamics.**

***Index Terms*— Phase-Locked Loops, Loop Filters, Modulators, Frequency Sinthesizers, Feedback Systems.**

I. Introduction

PHASE LOCKED LOOPS are generally designed by a combination of linear techniques, phase plane plots, rule of thumb and iterative simulations [1-3]. Some computational tools, intended to automate the process, are also available. In the case of low order PLLs, design methods are easy and well documented, but their extension to higher orders is still a topic of interest among researchers. Being a quite mature topic, it cannot be affirmed that a general method for designing PLLs is available. We can identify some reasons for this unfortunate situation. On one side most designs are based on particular circuit implementations, remarkably Charge Pump topologies. The particularization to circuital parameters quite often buries a more general vision. On the other side there is a widely extended misconception that associates the complexity of the design with the PLL order, leaving aside the Type, i.e. where the poles-zeroes are located. Finally, some parameters used such as damping and natural frequency, which strictly speaking are defined for second order PLLs, are questionable for higher orders and may become meaningless

In this paper we propose an alternative procedure for the design of any kind of PLL, regardless of the their order or type. The method is quite general, while at the same time allows for an intuitive insight into the system operation. To this end, we have kept the number of parameters used to the minimum and worked on their ratios. For a given implementation, such parameters can be mapped onto the corresponding electrical parameters. The design method is based on a general model for PLLs presented by the authors in [4]. Here, we will only concentrate in the practical aspects arising from the model. Since we are assuming a linear, continuous-time model, the validity of the results for sampled PLLs (e.g. Charge Pump) is limited to well know operating ranges [1]

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II. General Approach

In short, a typical design for a PLL begins with the selection of a simple Loop Filter (LF) according to the general requirements of the application, and the implementation constraints. Then, its components are selected to achieve a given specifications in terms of phase noise bandwidth, transient behavior, lock-in range, with a given stability margin. Since this is done for low order PLLs (three at most), and the design space is limited, some kind of trade-off is necessary. Then, if necessary, additional poles and/or zeros are added, increasing the PLL order, to increase the stability margin and/or reduce high frequency phase noise. A paradigm would be a typical Charge Pump PLL of order 3 and type II. With two integrators in the loop, Loop Transfer Function (LTF) has a single zero and three poles, which are calculated to meet the specifications, and by choosing a desired phase margin [5-6]. Another alternative is to design the Loop Transfer Function as a whole to meet a classical approximation [7]. Either way the addition of extra pole(s) to filter out phase noise, may substantially modify the expected PLL behavior, and thus the design procedure has to be modified [5].

In contrast, our design procedure starts by only taking care first of the PLL bandwidth, the desired high frequency roll-off, and also the transient behavior. Loop filter can be of any order, but always low-pass with (preferably) no zeroes, leading to a Loop Transfer Function with no zeroes too. Loop Filter order determines the slope of high frequency roll-off and well known Approximation Theory for filters can be used to decide the shape and parameters (bandwidth, transient) of the LTF. This procedure leads to the design of a Type I PLL of any order. Once this has been accomplished, we can now take care of the dynamics of the PLL in terms of its ability to track frequency step variations (hold-in range), frequency ramps, and so on, while keeping a negligible phase error. This can be done in practice by adding to the Loop Filter Transfer Function factors of the form:

$$(\omega_a + s)/s \tag{1}$$

Where they obviously represents a pole at the origin and a zero at ω_a. Filter gain at frequencies well beyond the zero is not substantially modified. Every factor of this kind adds an integration to the loop and thus increases the Type in one and so too with the Order. In the next sections we will see how the

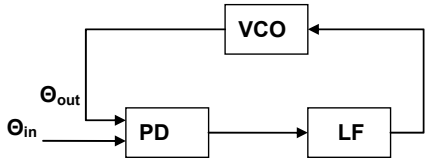

Fig. 1. Phase-Locked Loop Block Diagram

increase in the Type can be done without significantly affecting the specifications obtained in the first design step.

Before exploring all the possibilities this scheme gives, and analyzing some particular examples, we will first see how it reflects in the transfer functions describing the PLL. We show in Figure 1 a typical block diagram, representing the model of a PLL, including a Phase Detector (PD), a Loop Filter and a Voltage Controlled Oscillator (VCO). VCO is usually modeled by an integrator, accounting for the fact that phase is the integral of instantaneous frequency, with sensitivity K_V rads/Volt. As for the Phase Detector, its model depends on the implementation (multiplier, digital, etc.), but it is usually approximated by the phase difference within a limited range, scaled by a gain K_P. Since K_V and K_P show up as a product in all equations, we define the constant $K_{PV} = K_P.K_V$. We assume for the filter a transfer function $LF_I(s)$ with no zeroes and no poles at the origin, and unity DC gain. Conventionally defined transfer functions for the PLL are:

Loop Gain (LG):

$$G_I(s) = \frac{K_{PV}}{s} LF_I(s) \tag{2}$$

Loop Transfer Function (LTF)

$$H_I(s) = \frac{G_I(s)}{1+G_I(s)} = \frac{1}{1+s/\left(K_{PV} LF_I(s)\right)} \tag{3}$$

Under the conditions described in the previous paragraph, $H_I(s)$ can be always written as in the following way:

$$H_I(s) = \frac{H_N}{H_D(s)} \tag{4}$$

Where H_N is a constant equal to the independent term of $H_D(s)$ such that DC gain is unity. The order of the denominator determines the high frequency roll-off for the noise TF. When the additional pole-zero pair, as in exp. (1) is introduced in the Loop Filter expression (4) becomes

$$H_{II}(s) = \frac{\omega_a H_N + s H_N}{\omega_a H_N + s H_D(s)} \tag{5}$$

It is then analytically apparent that if ω_a is kept small, H_{II} can be approximated by H_I. In the same way, if an additional pole (at the origin) and zero (at ω_b) are introduced, the new expression for the Loop Transfer Function is:

$$H_{III}(s) = \frac{\omega_a\omega_b H_N + s(\omega_a+\omega_b)H_N + s^2 H_N}{\omega_a\omega_b H_N + s(\omega_a+\omega_b)H_N + s^2 H_D(s)} \tag{6}$$

Where we must impose a similar condition on ω_b to keep H_{III} close to H_{II} and H_I. In practice, by inspecting expressions (4) to (6) it is easy to see that low- and high-frequency performance will be similar but some additional peaking, and phase response modifications, can be expected in mid-frequencies due to the increase in the number of poles and zeroes. Figure 2 is an example of such behavior. What it is clear is that the Type of the PLL has increased from I to III, and thus its capability to track different kinds of frequency variations [8,9]. To which extent this can be done without affecting the remaining characteristics of the PLL will be analyzed in the next sections, in terms of ω_a(or ω_b)/K_{PV} ratios. The generalization of expression (6) to higher types is straightforward though, as mentioned before, does not have much practical interest. We note that regularity in the expressions for the different PLL Types (exp (4) to (6)) has been so far overlooked and thus not exploited.

Tables I to III include all of the transfer functions that result from the application of the procedure proposed, starting from a Type I-Order one PLL (table I), a Type I-Order two (table II), and finally a Type I-Order three (table III). Since filtering properties of the PLL depend on the difference between order an type, each table corresponds to a given high frequency roll-off, i.e., roll-off = –6dB/oct (Order–Type+1). The tables can be easily extended to higher order and/or types, but the ones shown include all cases of practical interest. In the next section we will detail the design procedure for one of such case

TYPE / ORDER	I /1	II / 2	III /3
$G(s)$	$\frac{K_{PV}}{s}$	$\frac{K_{PV}.\omega_a}{s^2}\left(1+s/\omega_a\right)$	$\frac{K_{PV}.\omega_a.\omega_b}{s^3}\left(1+s/\omega_a\right)\left(1+s/\omega_b\right)$
$H(s)$	$\frac{1}{1+s/K_{PV}}$	$\frac{K_{PV}\omega_a + K_{PV}s}{K_{PV}\omega_a + K_{PV}s + s^2}$	$\frac{K_{PV}\omega_a\omega_b + K_{PV}(\omega_a+\omega_b)s + K_{PV}s^2}{K_{PV}\omega_a\omega_b + K_{PV}(\omega_a+\omega_b)s + K_{PV}s^2 + s^3}$
$K/\omega_n/\xi$	K_{PV}/K_{PV}/--	$K_{PV}/\sqrt{K_{PV}\omega_a}/\frac{1}{2}\sqrt{\frac{K_{PV}}{\omega_a}}$	Non Aplicable

TABLE I- Type n–Order n PLLs

TYPE / ORDER	I / 2	II /3	III / 4
G(s)	$\frac{K_{PV}}{s}\frac{1}{1+s/\omega_p}$	$\frac{K_{PV}.\omega_a}{s^2}\frac{1+s/\omega_a}{1+s/\omega_p}$	$\frac{K_{PV}.\omega_a.\omega_b}{s^3}\frac{(1+s/\omega_a)(1+s/\omega_b)}{1+s/\omega_p}$
H(s)	$\frac{K_{PV}.\omega_p}{K_{PV}\omega_p+\omega_p.s+s^2}$	$\frac{K_{PV}\omega_a\omega_p+K_{PV}\omega_p s}{K_{PV}\omega_a\omega_p+K_{PV}\omega_p s+\omega_p s^2+s^3}$	$\frac{K_{PV}\omega_a\omega_b\omega_p+K_{PV}\omega_p(\omega_a+\omega_b)s+K_{PV}\omega_p s^2}{K_{PV}\omega_a\omega_b\omega_p+K_{PV}\omega_p(\omega_a+\omega_b)s+K_{PV}\omega_p s^2+\omega_p s^3+s^4}$
$K/\omega_n/\xi$	$K_{PV}/\sqrt{K_{PV}\omega_p}/\frac{1}{2}\sqrt{\frac{\omega_p}{K_{PV}}}$	N/A	N/A

TABLE II- Type n–Order n+1 PLLs

TYPE / ORDER	I/3	II / 4
G(s)	$\frac{K_{PV}}{s}\frac{1}{(1+s/\omega_{p1})(1+s/\omega_{p2})}$	$\frac{K_{PV}.\omega_a}{s^2}\frac{1+s/\omega_a}{(1+s/\omega_{p1})(1+s/\omega_{p2})}$
H(s)	$\frac{K_{PV}\omega_{p1}\omega_{p2}}{K_{PV}\omega_{p1}\omega_{p2}+\omega_{p1}\omega_{p2}.s+(\omega_{p1}+\omega_{p2})s^2+s^3}$	$\frac{K_{PV}\omega_a\omega_{p1}\omega_{p2}+K_{PV}\omega_{p1}\omega_{p2}s}{K_{PV}\omega_a\omega_{p1}\omega_{p2}+K_{PV}\omega_{p1}\omega_{p2}s+\omega_{p1}\omega_{p2}s^2+(\omega_{p1}+\omega_{p2})s^3+s^4}$
TYPE / ORDER	*III /5*	
G(s)	$\frac{K_{PV}.\omega_a\omega_b}{s^3}\frac{(1+s/\omega_a)(1+s/\omega_b)}{(1+s/\omega_{p1})(1+s/\omega_{p2})}$	
H(s)	$\frac{K_{PV}\omega_a\omega_b\omega_{p1}\omega_{p2}+K_{PV}(\omega_a+\omega_b)\omega_{p1}\omega_{p2}s+K_{PV}\omega_{p1}\omega_{p2}s^2}{K_{PV}\omega_a\omega_b\omega_{p1}\omega_{p2}+K_{PV}(\omega_a+\omega_b)\omega_{p1}\omega_{p2}s+K_{PV}\omega_{p1}\omega_{p2}s^2+\omega_{p1}\omega_{p2}s^3+(\omega_{p1}+\omega_{p2})s^4+s^5}$	

TABLE III- Type n–Order n+2 PLLs

III. DESIGN EXAMPLES

Let us assume that we are looking for a steep frequency roll off (-12 dB/oct) beyond PLL bandwidth, the latter being a fraction of PLL Free Running Frequency (FRF), say 10%. This kind of requirements are found in many frequency synthesizers for wireless transceivers [5,6,10]. But imagine that, with the same specifications, we need the PLL to be capable to follow both frequency steps and also frequency ramps which are beyond its hold-in capabilities, due to its bandwidth limitations. These call for a high type PLL [11,12].

The roll-off specification leads us to a Type N-Order N+1 PLL (table II). Then, we begin our design assuming a Type I. LTF, shown in table I, does not contain zeroes and thus we can decide the kind of approximation (Bessel, Butterworth ,…) or any in between, or equivalently choose damping factor and bandwidth. Since we are dealing with a second order function, performance in terms of settling time, overshoot, etc, are well known [1-3]. Let us suppose a Butterworth response ($\xi=\sqrt{2}$). It is easy to calculate that this is achieved if:

$$\omega_p = 2K_{PV} \tag{7}$$

From where 3dB frequency is calculated as:

$$\omega_{3dB} = \sqrt{2}K_{PV} \tag{8}$$

At this point it is important to note that as the ratio ω_p/K_{PV} increases (damping increases), 3dB bandwidth gets closer to K_{PV} . Actually, and since this kind of solutions are preferable, K_{PV} becomes a better parameter to estimate bandwidth than natural frequency. This affirmation is also true, as we will see, for any kind of PLL, particularly for higher orders and types, where natural frequency becomes a meaningless parameter. By the way, the use of K_{PV} as a better estimator for bandwidth has been also suggested in recent literature [1,4,13].

Selection of K_{PV} according to bandwidth also determines acquisition and hold-in ranges. However these constraints are avoided if we jump to a Type II, 3rd order, as described in the previous section. The resulting transfer functions are shown in second column of table II. Zero value has to be selected small enough so as not to significantly affect the LTF shape. Unavoidably, a peaking will show up, accompanied by a reduction in the phase margin and higher overshoot. Taking K_{PV} as a reference, we can analyze how such parameters vary for different ω_a/K_{PV} ratios. Figure 2 shows new LTF for a ratio of 0.1 (dotted), which exhibits a peaking below 1dB. In table IV, second row, we show the evolution of the phase margin as the ratio decreases. These values, peaking and phase margin can be approximated to a very good degree of accuracy by the following empirically obtained relationships:

$$PM \approx PM_o - 60 \cdot \frac{\omega_a}{k_{PV}} \tag{9}$$

$$Peaking \approx 9 \cdot \frac{\omega_a}{k_{PV}} \quad (10)$$

Where PM_o corresponds to the phase margin of the second order, Type I PLL. For a Butterworth approximation this value is approximately 66º .

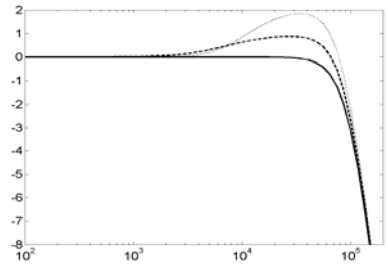

Fig. 2. LTF for 2nd (Butterworth), 3rd and 4th order PLLs.

ω_a/K_{PV}	1/10	3/20	1/5	1/4	3/10	7/20	2/5	9/20	1/2
3rd ord	59	56	53	50	47	45	42	40	37
4th ord	58	47	40	35	30	25	20	15	10

TABLE IV. Phase Margins for 3rd and 4th order PLLs

We can give now an step forward by increasing the Type-Order of the PLL by the addition of another pole-zero pair. We already know that the new zero, at ω_b, has to be small enough so as not to substantially modify the original PLL response with regard to bandwidth and transient characteristics, while at the same time making it capable to follow frequency ramps. Figure 2 and table IV also show the resulting peaking and phase margins, respectively, when making $\omega_b=\omega_a$. Peaking, with respect to Type II-order 3 is practically doubled, while phase margin reduces at a higher pace, according to the approximation:

$$PM \approx PM_o - 110 \cdot \frac{\omega_a}{k_{PV}} \quad (11)$$

Anyway, we can conclude that, even for ω_a/K_{PV} ratios that can be considered high (1/5), phase margin is wide and peaking could be tolerated in many applications.

Let us now imagine that we start with tighter specifications with respect to high frequency roll off, say -18 dB/oct. This calls for a Type N, order N+2 PLL (table III). The design process is similar to the one described before. Starting with the simplest case, a Type I, and choosing K_{PV} as a first estimation for bandwidth, we must decide the approximation for LTF. A Butterworth approximation, as in the previous case, would be now of the form:

$$H(s) = \frac{8.K_{PV}^3}{8.K_{PV\,p2}^3 + 8.K_{PV}^2.s + 4.K_{PV}s^2 + s^3} \quad (12)$$

From where ω_{p1} and ω_{p2} can be easily calculated:

$$\omega_{p1}\omega_{p2} = 8K_{PV} \quad (13)$$

$$\omega_{p1} + \omega_{p2} = 4K_{PV} \quad (14)$$

And 3dB bandwidth would be exactly $\omega_{3dB}=2K_{PV}$. For a Bessel approximation denominator coefficients in (12) would be {15,15,6,1}, and $\omega_{3dB}=1.75K_{PV}$. There are a number of non standard options for the coefficients that also render a monotonic low-pass response: {16,16,8,1}, {20,20,9,1} and {25,25,10,1}. Modifications of equations (13) and (14) are straightforward. A better estimation for 3dB bandwidth would be in these latter cases $\omega_{3dB}\approx 1.6K_{PV}$.

The extension of the above design to Type II (4th order) and type III (5th order), can be done by introducing ω_a and ω_b. A similar analysis as the one shown for the Type n-Order n+1, shows that expressions (9) to (11) are still good approximations for peaking values and *PM* (Note that PM_o is now 61º for the Butterworth approximation, and factor 9 in expression (10) should be 10 instead).
It goes without saying that the case of Type n, Order n is much simpler than the other two developed here an is not included for the sake of brevity.

IV. Simulation Results

A Simulink model, which allows for an evaluation of the PLL for any Order and Type, has been implemented. Phase Detector is modeled as a perfect analog multiplier, while VCO is assumed ideal. We will proceed by first designing for a Type I PLLs (regardless of the order) and then appraise how it is affected when "upgraded" to Type II and Type III.

We will begin with the design and analysis of a Type n-Order n+1 PLL, which exhibits a –12dB/oct roll-off at high frequencies. Type I is thus of 2nd order and we have chosen for it the parameters shown in Table V that give a PLL bandwidth around 15% of the FRF. Damping factor is 0.707 that corresponds to a LTF with maximally flat (Butterworth) response

VCO		*PD*	*LF1*
$K_v=10^4$	$FRF=10^5$	$K_P=2$	$\omega_p=4.10^4$

Damping Factor	Natural Frequency	3 dB Bandwidth	Hold-in Range	Lock-in Range
$\xi=1/\sqrt{2}$	$\omega_n=\sqrt{2}.K_{PV}$ 2.10^4	$\omega_{3dB}=\sqrt{2}.$ K_{PV}	~10%*FRF*	~8%*FRF*

TABLE V. PLL parameters (frequencies in rads/sec)

We have used as test signal a sinusoid whose initial frequency is 10^5 Krad/sec (*FRF* + 5%, which is within acquisition range), stays stationary for 5 milliseconds, and then follows successive intervals of ramp-ups and constant frequency of 5 milliseconds duration each. Under these conditions, in the upper trace of Figure 3 we show LF output. As could be expected, after a lightly under-damped response, PLL is able to track while input frequency (within lock-in range) is steady, but lose track when it goes beyond

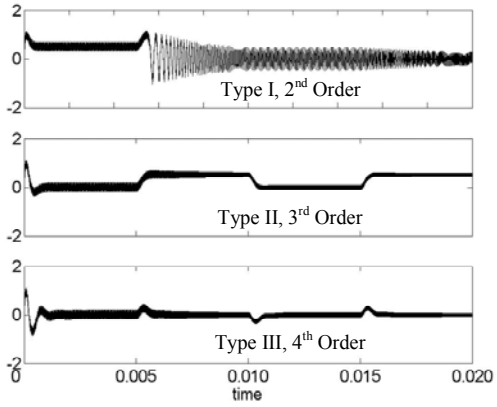

Fig. 3. Phase Errors for Type n-order n+1 PLL

hold-in range. Note that a phase error is always present since it is a Type I PLL. To avoid this limitation, we can successively introduce in the LF additional zero-pole pairs, converting the PLL into a type II (3rd order) and Type III (4th order). Frequencies ω_a and ω_b have been chosen equal and only five times lower than K_{PV}. The response under these conditions are also shown in Figure 3. In the middle curve, we can see that the PLL remains always locked, as predicted for a Type II, exhibiting a zero phase error while input frequency is constant, but with a DC phase error for linear frequency variations (velocity error).

In the lower curve, type III, it is apparent how mean phase error tends to vanish after each transient, regardless whether input signal has constant frequency or it is a ramp. Analysis of the transients shows an increase in the overshoot with the order. This is to be expected since ratios K_{PV}/ω_a, K_{PV}/ω_b are only five, leading to appreciable peaking in the LTF.

A similar analysis has been carried out with PLLs of Type n-Order n+2 where phase noise is filtered at a rate of -18 dB/octave. To make the comparison with the previous case fair, we have also started with a Butterworth response for the Type I, which is now of third order. K_P and K_V are as in table IV, and ω_{p1} and ω_{p2} are calculated to achieve such Butterworth response (see section III for details). Under similar simulations conditions, resulting phase errors are shown in Figure 4.

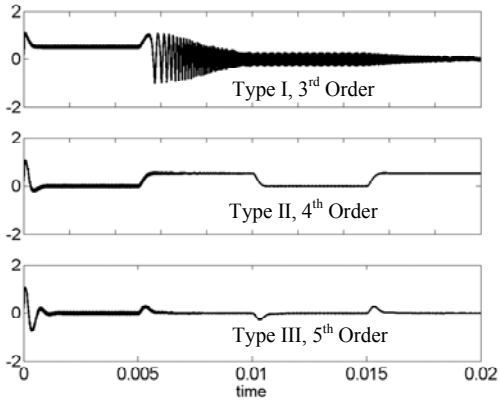

Fig. 4. Phase Errors for Type n-Order n+2 PLL

It is really noteworthy how close Figure 3 and 4 are, the main difference being the lower ripple in signals in Figure 4, as a consequence of the additional -6dB/octave in the phase transfer function. This supports the affirmation in [1] that Type characterizes a PLL more than Order. We note that in this class of PLL, we are dealing with a Type III-5th order PLL, which has been found to be stable.. Note that 5th order PLLs are extremely rare to find [15]. With this method, its design is readily accomplished

V. Summary and Conclusion

According to the analysis presented in this paper, a design flow for a PLL would be as follows.

1) Start with a Type I PLL where the order should be chosen to achieve the desired high frequency roll-off.

2) LTF, which does not include zeroes, can be approximated by a monotonic response (Bessel, Butterworth,..) where K_{PV} should be chosen so that desired bandwidth, ω_{3dB} is around 1.5 to 2 times K_{PV}. High frequency pole(s) are then determined from K_{PV} and Phase Margin (PM_o) is determined too.

3) Add pole-zero pair(s) to LF as needed to achieve Type II or Type III operation. Zero positions, ω_a and ω_b, have to be such that $\omega_a(=\omega_b)/K_{PV} \ll 1$. PM drops, and peaking raises approximately, according to expressions (9) and (11).

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