High-order PLL Design with Constant Phase Margin

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***Abstract*—In this paper we describe a novel procedure to design high-type high-order Phase Locked Loops (PLLs) from lower order prototypes, preserving a prescribed Phase Margin (*PM*). The method builds on a model recently proposed by the authors, and is supported by extensive simulations and experimental results, giving up to a type-III fifth-order PLL with a commercial circuit.**

1. INTRODUCTION

High-order, and thus high-type PLLs are sometimes required in applications where extra phase noise filtering or operation in wide frequency ranges, for instance, are mandatory design conditions [1,2]. However such designs are difficult, and stability of the resulting PLL is not easy to guarantee. From an analytical point of view, even linear equations describing PLL behaviour assuming stationary response are difficult to analyze and interpret; typical parameters of the second order case (natural frequency, damping, gain) become useless for higher orders since they do not result straightforwardly from the transfer functions.

Recently, authors proposed an alternative model for analog PLLs, which make both analysis and design tasks easier [3,4]. Parameters introduced have a more meaningful interpretation in terms of the resulting physical behaviour, giving at the same time clearer design equations, particularly for high-order high-type cases [5]. The reason for that is that such more complicated PLLs are seen as natural "upgrades" of the simple and thus well known second (or even third-order) cases.

In this paper we will work further on this idea showing how higher order PLLs can be designed from lower order ones preserving a prescribed phase margin. To this end, we will first obtain a general expression, based on the model parameters, which approximates phase margin for any kind of sensible PLLs. The method is supported on simulations and experimental results with a popular commercially available circuit, resulting in a type-III fifth-order PLL, which we believe is the first ever reported. An original procedure to measure phase margin is also described.

We note that in [6] a type-II fourth-order design from a third-order is elaborated, also with the constrain to preserve phase margin, but the procedure is much less intuitive and restricted to this particular situation and circuit implementation.

2. PM APPROXIMATION

Phase Margin (*PM*) is routinely used in feedback systems, and thus also in PLLs, to measure stability. Therefore when a lower order PLL is designed with a prescribed Phase Margin and there is a need to improve or modify other PLL parameters, it is important to keep Phase Pargin constant. In this section we will obtain an approximate expression for the PM of PLLs.

The transfer function of a feedback systems can be written as:

$$H(s) = \frac{G(s)}{1+G(s)} \tag{1}$$

where *G(s)* is the Open Loop Gain. For a PLL, and assuming the ideal models for Phase Detector (*PD*) and *VCO*, it takes the following form:

$$G(s) = \frac{K_{VCO} \cdot K_{PD} \cdot LF(s)}{s} \tag{2}$$

The Loop Filter, *LF,* which mid-frequency gain is assumed unity, may contain poles at the origin, and the same number of zeroes to compensate them. Thus, its transfer function can be written as, [3,5]:

$$LF(s) = \frac{\prod_{i=1}^{N} \omega_{zi} \cdot (1 + s/\omega_{zi})}{s^N \prod_{j=1}^{M} (1 + s/\omega_{pj})} \tag{3}$$

where ω_{zi} and ω_{pj} are the zeroes and the high-frequency poles of the filter, respectively. Thus, using (2) and (3) the general form for *G(s)* becomes:

$$G(s) = \frac{K_{VCO} \cdot K_{PD} \cdot \prod_{i=1}^{N} \frac{\omega_{zi}}{s} \cdot (1 + s/\omega_{zi})}{s \prod_{j=1}^{M} (1 + s/\omega_{pj})} \tag{4}$$

Operating with the expression above,

$$G(s) = \frac{K_{VCO} \cdot K_{PD} \cdot \prod_{i=1}^{N} (1 + \omega_{zi} / s)}{s \prod_{j=1}^{M} (1 + s / \omega_{pj})} \quad (5)$$

from which it is easy to extract the contribution of each factor to the overall phase. The pole at the origin adds $-\pi/2$ radians to the phase. The gain components K_{VCO} and K_{PD} obviously do not affect the phase. The remaining components (in brackets) are complex terms. Thus, the phase response of $G(j\omega)$, is as follows:

$$\angle G(j\omega) = -\frac{\pi}{2} - \left(\sum_{i=1}^{M} \arctan\left(\frac{\omega_{zi}}{\omega} \right) + \sum_{j=1}^{N} \arctan\left(\frac{\omega}{\omega_{pj}} \right) \right) \quad (6)$$

To obtain the *PM*, we need to know the frequency at which the loop gain magnitude is unity, which we will call ω_0 (unity gain frequency) and then

$$PM = \frac{\pi}{2} - \left(\sum_{i=1}^{M} \arctan\left(\frac{\omega_{zi}}{\omega_0} \right) + \sum_{j=1}^{N} \arctan\left(\frac{\omega_0}{\omega_{pj}} \right) \right) \quad (7)$$

Unity gain frequency can be easily calculated for third or lower order PLLs, but this is not the case for higher order ones. However, we have shown in [3] that for most practical designs. i.e.

$$\omega_{zi} << \omega_0 << \omega_{pj} \quad (8)$$

the following approximation works well:

$$K = K_{PD} K_{VCO} \approx \omega_0 \quad (9)$$

which can be also approximated by the PLL bandwidth. This approximation is implicitly accepted and used by Gardner and Wolaver [1,2], and key in our model in [3,4,5].

Under the same assumptions given by exp. (8), the following approximation holds

$$\arctan(x) \approx x \quad (10)$$

resulting in the following *PM* approximation:

$$PM \approx \frac{\pi}{2} - \alpha \left(\sum_{i=1}^{M} \frac{\omega_{zi}}{K} + \sum_{j=1}^{N} \frac{K}{\omega_{pj}} \right) \quad (11)$$

Constant α, close to unity, has been introduced in order to compensate for the errors owed to the approximations, mainly the shift between ω_0 and K. After extensive simulations of different open-loop transfer functions for a variety of types and orders, the value of α that better fits the actual *PM* values is 0.925 radians or equivalently 53 degrees. So, the final expression for the approximated *PM*, expressed in degrees, is:

$$\boxed{PM \approx 90 - 53 \left(\sum_{i=1}^{M} \frac{\omega_{zi}}{K} + \sum_{j=1}^{N} \frac{K}{\omega_{pj}} \right)} \quad (12)$$

which can be seen as a generalization of the expression given in [5]. In Fig. 1 we show a comparison between simulated *PM* values and approximated ones for a type-II third-order PLL. The *PM* is represented versus the frequency of the zero ω_z and normalized with respect to K. The different curves correspond to different values of the pole ω_p. The simulated *PM* values have been obtained using Simulink.

It can be observed that the approximated values are very similar to the simulated ones, the error being always beyond 3 degrees. For higher order loops representation is not so easy because of the additional number of parameters. However, the maximum error found for the type-III fifth order PLL is lower than 4 degrees.

3. HIGH-ORDER PLL DESIGN WITH PRESCRIBED PHASE MARGIN

Examples of high-order PLL designs are scarce in literature. In [6] an interesting approach is developed to design a third-order PLL calculating gain-crossover frequency that maximizes the *PM*. Once it is accomplished, another high frequency pole is added to design a fourth-order loop, still of type II. In order to keep constant both *PM* and unity gain-crossover frequency, original poles and zeroes locations have to be predistorted. Design equations are given.

The design method proposed here has some similarities with the previous one, in the sense that it starts from the design of a lower order PLL. However, our approach is much more general in the sense that it is useful for any order and type, and is independent on the circuit implementation. Just for comparison purposes, let us start with a type II third-order PLL , whose loop filter can be expressed as:

$$LF_{3rd}(s) = \frac{\omega_z \cdot (1 + s / \omega_z)}{s \cdot (1 + s / \omega_p)} \quad (13)$$

Once the PLL bandwidth (which we approximate by K) and the *PM* have been defined, the corresponding type II third-order form of the expression (12) can be used to obtain the pole and zero frequencies. It is obvious that the solution is not unique. However, condition (8) must be beard in mind, and other design conditions may be met: ω_z relates to the ability to respond to frequency hops (velocity error), and ω_p has to do with the selectivity of the whole PLL as a phase noise filter. Any of those (or more) factors can be used to define one of the parameters.

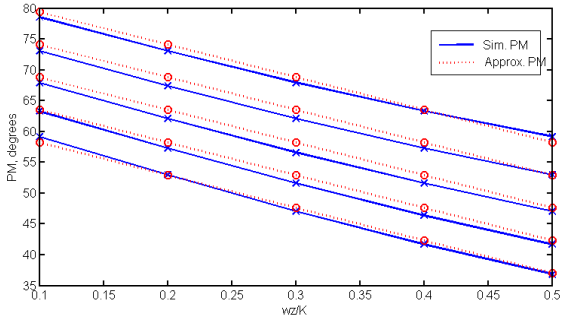

Figure 1. Type II third-order PM simulation and approximation for different zero and pole values.

When design specifications are more demanding (for example, a steeper high-frequency roll-off or a ramp-like frequency tracking,) the order and/or the type of the PLL must be increased. With classical design methods it is difficult to deal with high order filters due to its stability problems. With our method, however, the stability is not an issue since the *PM* is maintained constant through the level-up process.

Adding another zero or pole to the current device, while preserving phase margin, requires a shift in the original pole/zero locations, according to general expression (12). Following with Brennan´s example, *PM* particularizes for a type-II forth-order PLL as follows.

$$PM \approx 90 - 53 \cdot \left(\frac{\omega_z}{K} + \frac{K}{\omega_{p1}} + \frac{K}{\omega_{p2}} \right) \qquad (14)$$

The extension to a type-III and up to fifth-order is straightforward. More complicated designs are possible but not practical. In the following sections we will demonstrate this approach with an example.

4. DESIGN EXAMPLE AND EXPERIMENTAL RESULTS

The following example shows three different design specifications (i.e. three different *PM* values) in which the method presented here has been applied. In the three cases we start from a type-II third-order design. Then, another high frequency pole is added to form a type-II fourth-order one and, finally, a low frequency zero is added to achieve a type-III fifth-order PLL. It will be obvious that *PM* approximation (12) works better in some cases than others, mainly depending on how well conditions (8) are fulfilled.

We have implemented a PLL model on Simulink to first validate our procedure, and then prototypes are implemented and measured. The test circuit makes use of a commercial version of the popular 4046, which contains a Phase Detector and a programmable Voltage Controlled Oscillator. The Loop Filter is external to the monolithic PLL and its *RC*-Active implementation for the type-II third-order PLL is shown in Fig. 2a. This implementation is not optimum but allows an easy tuning, since all poles an zeroes are decoupled. Resistor R_{DC} is included in order to ensure a *DC* feedback path for the op-amp though it causes a low frequency error: poles are no longer at origin. The transfer function of the filter, neglecting the effect produced by R_{DC}, is:

$$LF_{3rd}(s) = \frac{(1 + sC_1R_2)}{sC_1R_1(1 + sC_PR_P)} \qquad (15)$$

To achieve the type-II forth-order PLL a buffered passive *RC* low pass filter is added, and thus implementing the type-III fifth-order PLL, requires an active-*RC* stage implementing a pole-zero pair (pole at the origin.) This is shown in Fig. 2b and Fig. 2c respectively.

The overall transfer function is as follows:

$$LF_{5th}(s) = \frac{(1 + sC_1R_2)(1 + sC_1R_4)}{s^2C_1^2R_1R_3(1 + sC_PR_{P1})(1 + sC_PR_{P2})} \qquad (16)$$

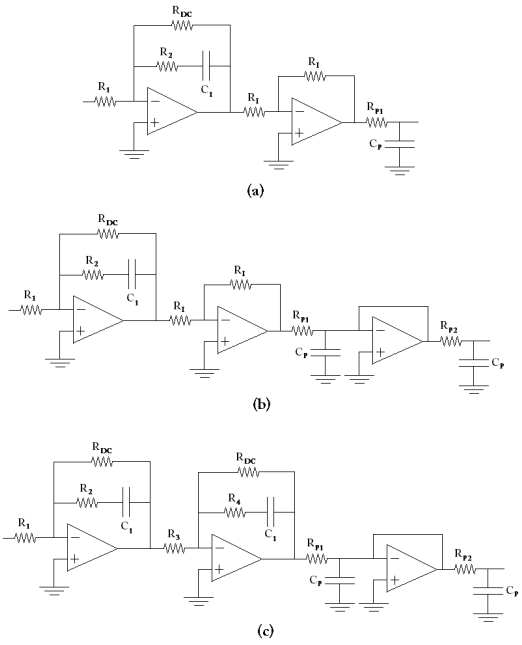

Figure 2. Loop filter implementations for II-3, II-4 and III-5 PLLs

By comparing the filter transfer functions with the general expression (3), it is easy to see that (16) shows up a mid-frequency gain different from unity that does not appear in the general one. This value must be included in the definition of *K*, as an additional factor $K = K_{PD}K_{VCO}K_{LF}$. For the type-II third-order and fourth-order PLLs this factor is $K_{LF}=R_2/R_1$; while for the other type-III fifth-order it is $K_{LF}= R_2*R_4/(R_1*R_3)$.

Regarding the monolithic PLL (SN74LV4046AN from Texas Instruments) and out of the three possible selectable outputs, the *XOR* gate, with a voltage mode output, has been selected as Phase Detector. The device has been tuned properly to achieve the following design parameters: Free Running Frequency (*FRF*)=*272 KHz*, K_{VCO}=*286 KHz/V*, K_{PD}=*0.6366 V/Hz*. Applying the typical analysis equations of the loop [1], and assuming a desired loop gain of *K=20 KHz*, the Loop Filter has to be tuned such that K_{LF}=*0.1099*.

All of the component tolerances and the residual low frequency pole have been introduced in the simulator in order to have a more realistic model for the loop. As we said before, all of the simulations of the loop transfer functions have been carried out with Matlab-Simulink.

The Loop Filter parameters from the three design examples are collected in Table 1. All frequency values are normalized with respect to loop gain *K*. The three design cases correspond to more or less favourable situations in terms of how well approximations (8), driving to the *PM* expression (12), are fulfilled. The *PM* values are different too, but in any case are kept within reasonable values [7].

In Table 2 we show the resulting *PM* obtained in both the simulated model and the experimental circuits under test. We note that approximation values for II-3, II-4 and III-5 are not exactly equal since tolerance in component values make it

difficult to preserve exactly the same *PM* value. However, what is relevant to remark here is that approximate expression works very well in the sense that it is able to predict *PM* value, allowing for the design of *PM* invariant PLLs, regardless of the order and type, and for any practical design condition.

As a by-side result of our work, we have demonstrated the proper operation of very complex analog PLLs (III-5), which are to the best of our knowledge the first experimental results reported.

At this point, it could be of interest to describe how Phase Pargin has been measured in actual circuits, since this is not described in literature. The main difficulty comes from the fact that *PM* has to be measured at low frequencies while the PLL is working (with the loop closed) at much higher frequencies. In [8], this is solved by breaking up the loop and inserting another element (a resistor in the easiest case or a passive widget.) Then, the input and output signals needed to estimate the frequency response are taken from both terminals of that device. The problem with this method is that this additional element unavoidably modifies the PLL operation.

We have developed another method that does not require external elements in the loop. Looking at the Open Loop transfer function expression (2), it is easy to consider the loop as the series connection of the Loop Filter and the nonlinear components (*VCO* and *PD*). At the gain-crossover frequency, the magnitude of *G(s)* is unity (0*dBs*):

$$\left|G(j\omega_0)\right| = \left|\frac{K_{VCO}\cdot K_{PD}}{j\omega_0}\right|\cdot\left|LF(j\omega_0)\right| = 1 \qquad (17)$$

So,

$$\left|LF(j\omega_0)\right| = \left|\frac{j\omega_0}{K_{VCO}\cdot K_{PD}}\right| \qquad (18)$$

TABLE I. ZERO AND POLE FREQUENCIES FOR THE DESIGN EXAMPLES

	II3		*II4*			*III5*			
CASE	ω_Z	ω_P	ω_Z	ω_{P1}	ω_{P2}	ω_{Z1}	ω_{Z2}	ω_{P1}	ω_{P2}
More fav.	0.1	10	0.1	20	20	0.05	0.05	20	20
Intermediate	0.2	5	0.2	10	10	0.1	0.1	10	10
Less fav.	0.29	3.5	0.145	7	7	0.145	0.145	7	7

All the frequencies appear normalized by K

TABLE II. SIMULATED, MEASURED AND APPROXIMATED *PM* FOR THREE DESIGN CASES (DEGREES)

	SIMULATION			**MEASUR.**			**APPROX.**		
CASE	***II3***	***II4***	***III5***	***II3***	***II4***	***III5***	***II3***	***II4***	***III5***
More fav.	78,9	79,1	81,8	79,7	79,5	79,7	79,4	79,7	79,5
Intermediate	67,4	67,0	70,3	67,6	67,6	66,7	68,5	68,3	68,8
Less fav.	58,4	57,4	60,5	56,3	58,4	54,4	59,7	59,1	59,6

At unity gain-crossover frequency, the *LF* magnitude must be the exact inverse of the remaining of the loop response. Taking this into account, the measurement procedure can be split in two steps, for the two sections of the loop. First, the Loop Filter frequency response is routinely measured removing it from the PLL. As for the remainder of the PLL it can be only measured in close-loop mode, once the PLL is locked, we inject a sweeping sinusoidal signal through one of the Loop Filter ground connections and measure the *VCO* input and *PD* output signals to estimate its frequency response.

Particular care has to be taken with the external signal injected in the loop. As it is inserted in the *LF,* just before the *VCO* input, it definitely alters (i.e. modulates) the output frequency of the PLL. If the amplitude of the signal is too large, fluctuations produced in the frequency of the output signal may unlock the PLL. Therefore, non negligibly signal, due to the nonlinear behaviour of the PLL, may appear in the loop distorting the frequency response. On the other hand, if the amplitude is too small, the input and output signals required are too noisy degrading the quality of the obtained frequency response.

It remains nothing but comparing both magnitude responses, measure the phase contribution of each one at the crossing frequency and add these contributions to calculate the Open Loop phase at the *PM* frequency. Finally, subtracting (-180) degrees, the *PM* is obtained.

5. CONCLUSIONS

In this paper a high-order high-type PLL design method, built on the model proposed by Carlosena and Mánuel-Lázaro [3], has been presented. Starting from a low order design, desired order and type are achieved avoiding stability problems. This is accomplished by using an accurate *PM* approximation that allows a constant *PM* design process. Simulated and experimental results are presented to support the method. Furthermore, an experimental *PM* measuring procedure has been presented, and complex Type-III fifth-order PLLs have been designed and demonstrated to work properly.

Acknowledgements: This work has been supported in part by the Spanish Dirección General de Investigación and FEDER under grants TEC2007-67460-C03/01 and DPI2007-66615-C02-01

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