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On the Optimal Current Followers for Wide-Swing Current-Efficient Amplifiers

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***Abstract*— The design of various current followers for the implementation of OTAs with high slew rate and current efficiency is addressed. Two basic current follower topologies are compared, and modifications of both followers to improve these parameters are presented. As an application example, an enhanced recycling folded cascode OTA is proposed. Measurement results of the OTA fabricated in a 0.5 µm CMOS process show a 260% and 180% improvement in SR and GBW, respectively, for the same power consumption.**

***Keywords*— Current followers, Amplifiers, Analog integrated circuits, CMOS integrated circuits, Class AB circuits.**

I. Introduction

Mobile, portable and wearable electronic systems are becoming ubiquituous in all the scenarios of our daily life (4G/5G cellular radios, WLANs, WBANs, IoT devices, etc.). This unprecedent growth has led to a vivid interest in power efficient wireless electronic devices, due to the limited power available from small batteries (or in some scenarios from scavenged energy). Besides this demand for power efficiency, modern CMOS processes have witnessed an ongoing downscaling of the supply voltage and reduction of the intrinsic gain $g_m r_o$ of the transistors. Although this trend affects all the analog and digital system blocks, it is particularly significant for the design of amplifiers, which are a key element in the power budget of many systems nowadays [1].

In this scenario, cascode topologies are often required to achieve enough gain without requiring a large number of gain stages (which compromises stability and power consumption). The telescopic cascode amplifier [2] can improve gain versus the simple differential pair amplifier and at the same time it preserves a high current efficiency (CE) [3]. This factor is CE=I_{out}/I_{supply}, the ratio between the output current and the supply current. An optimal CE requires a direct path to convey the supply current to the output, without replicating internally the signal currents. This is done by both the simple differential pair and telescopic cascode amplifier. Unfortunately, this direct signal path requires a single branch from the supply rails to the output terminal, so that the input transistors reduce the signal swing available at the output. This fact has precluded the use of the telescopic cascode amplifier with the reduced supply voltages of modern CMOS technologies.

In order to overcome this problem, it is required to remove the input transistors from the output branch. To do so preserving at the same time the single-stage configuration of the amplifier, a current follower (CF) is needed which conveys the signal current generated at the differential pair to the output branch. This is shown in Fig. 1. The CF features a low impedance input (ideally a signal ground) to sense the input current without introducing low-frequency poles or zeros.

Two common implementations of the CF, namely, current mirror and common-gate amplifier, are shown in Figs. 2(b) and 2(c), respectively. When they are applied to the topology of Fig. 1, the well-known current mirror (CM) OTA and folded cascode (FC) OTA result. They basically preserve the gain and bandwidth of the telescopic cascode OTA and at the same time significantly increase the output range.

This paper focuses on the optimal design of current follower topologies required to achieve current-efficient amplifiers. As an application example, a novel class AB reclycling folded cascode (RFC) OTA is presented. The paper is organized as follows. Section II analyzes the advantages and shorcomings of the two current followers of Fig. 2. Modifications to these current followers to increase current efficiency and slew rate (SR) are discussed in Section III, and a RFC OTA using an efficient current follower is presented in Section IV. Simulation and measurement results of a test chip prototype containing the RFC OTA are presented in Section V. Finally, conclusions are drawn in Section VI.

II. Current Mirroring vs Current Folding

The use of current mirrors as current followers, illustrated by the wide-swing topology of Fig. 2(b), is a typical choice for OTAs, linear transconductors, CFOAs, current conveyors and several current-mode circuits. The main advantages are simplicity and the possibility to scale the output current by the current mirror ratio *K*. This improves the gain-bandwidth

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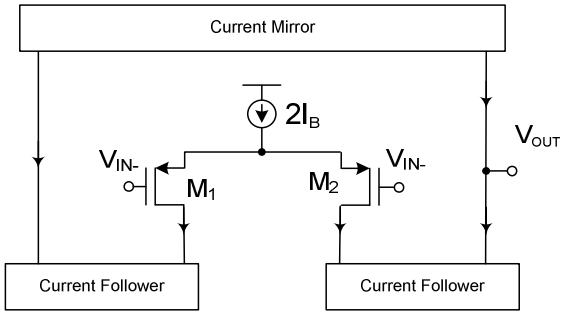


Fig. 1. Single-stage topology using current followers.

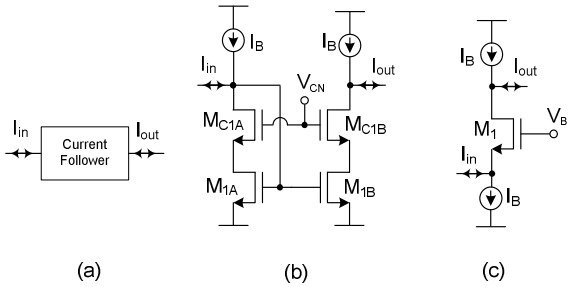


Fig. 2. Current follower implementation (a) basic diagram (b) with current mirror (c) with common-gate transistor.

product GBW of the amplifier by the same scale factor K. However, this choice also has some shortcomings: a) The current mirror introduces a pole $\omega_p \approx -g_{m1B}/(C_{gs1A}+C_{gs1B})$ and a zero $\omega_z \approx -(1+K)\omega_p$. This may become a serious shorcoming for wideband amplifiers, specially if large K ratios are required since they increase capacitance C_{gs1B}. This fact limits the maximum K value employed in practice. Moreover, a larger K also increases static power consumption as the scaling factor applies both to the signal current and the quiescent current. b) The current mirror replicates the signal current, leading to a CE<0.5 for K=1 since at least half of the signal current is wasted without reaching the output. Larger K values improve CE as the portion of total signal current not reaching the output decreases, but the maximum K value is limited as mentioned above. c) Accuracy of the current mirror relies on perfect matching between the current mirror transistors, which is not possible in practice due to geometric and parameteric variations. This degrades performance metrics such as linearity in open loop applications (e.g. transconductors). For instance, if a mismatch ΔV_{TH} in the threshold voltage exists in the current mirror transistors M_{1A} and M_{1B}, it is well known that the third order harmonic distortion component introduced by the current mirror is approximately [4]:

$$HD3 \cong \frac{\Delta V_{TH}}{8 g_m^2 \left(V_{GS}-V_{TH}\right)^3} i_{in}^3 \qquad (1)$$

with g_m and V_{GS} the transconductance and gate-source voltage of M_{1A} and M_{1B}, and i_{in} the AC input current.

In comparison, the current follower of Fig. 2(c) does not have any matching requirement between devices. The output current is exactly the inverted input current as long as the bias current sources in Fig. 2(c) remain signal-independent. The approximate expression for the third-order harmonic distortion becomes:

$$HD3 \cong \frac{1}{8 g_m^3 r_o \left(V_{GS}-V_{TH}\right)^2} i_{in}^3 \qquad (2)$$

where r_0 is the output resistance of the bias current source I_B. Comparing (1) and (2), the current follower of Fig. 2(c) leads to less HD3 as long as $\Delta V_{TH} > (V_{GS}-V_{TH})/(g_m r_0)$. This condition can be easily met in practice due to the low $V_{GS}-V_{TH}$ values used in modern low-voltage CMOS design. Concerning the second-order harmonic distortion term HD2, it is potentially lower when the current follower of Fig. 2(c) is used as in this case no matching condition is required between devices.

Another advantage of the current follower of Fig. 2(c) is that the pole introduced is $\omega_p \approx -g_{m1}/C_{gs1}$, which is at higher frequency than that of Fig. 2(b) for the same transistor dimensions and bias current, due to the lower intrinsic capacitance at the input. Moreover, in this case there is not need to replicate the signal current in order to convey it to the output, which potentially improves CE.

The main shortcoming of the current follower of Fig. 2(c) versus Fig. 2(b) is that current scaling cannot be carried out, so the current follower does not contribute to increasing the transconductance (and hence the GBW) of the amplifier.

A common disadvantage of both current followers in Fig. 2 is that the maximum signal current is limited by the bias current I_B. For the NMOS circuit in Fig. 2(b) the maximum current leaving the current mirror is I_B (a PMOS current mirror would lead to the same limitation for the current entering the mirror). In the current follower of Fig. 2(c), the maximum signal current entering the circuit is I_B. This fact leads to a tradeoff between SR and static power consumption, since the only way to improve SR is by increasing the bias current. In the next section, modifications to the current followers are discussed to improve SR and CE without increasing quiescent power consumption.

III. Power-Efficient Current Followers

In order to improve CE and SR in the current mirrors without the shortcomings of using a current mirror ratio K>1, the basic approach is employing a current mirror with K=1 (hence not scaling quiescent currents), but able to boost the output current for large input currents. A first implementation of this idea is shown in Fig. 3(b) [5]. In this case, the cascode bias voltage V_{CN2} at the output branch is chosen, as usually, to enforce that for the largest current expected transistor M_{1B} will remain in saturation. However, the cascode bias voltage V_{CN1} at the input branch is chosen so that in absence of input signal transistor M_{1A} is in the limit between triode and saturation regions. Using the simple MOS square law model and neglecting channel-length modulation and body effect, this value is $V_{CN1} = V_{TH}+V_{DS,sat1A}+V_{DS,sat1CA}$ with $V_{DS,satX}$ the minimum V_{DS} value in transistor M_X to operate in saturation. The quiescent behavior and small-signal performance are the same as with a conventional cascode current mirror. However, dynamic performance is improved as for large input currents, transistor

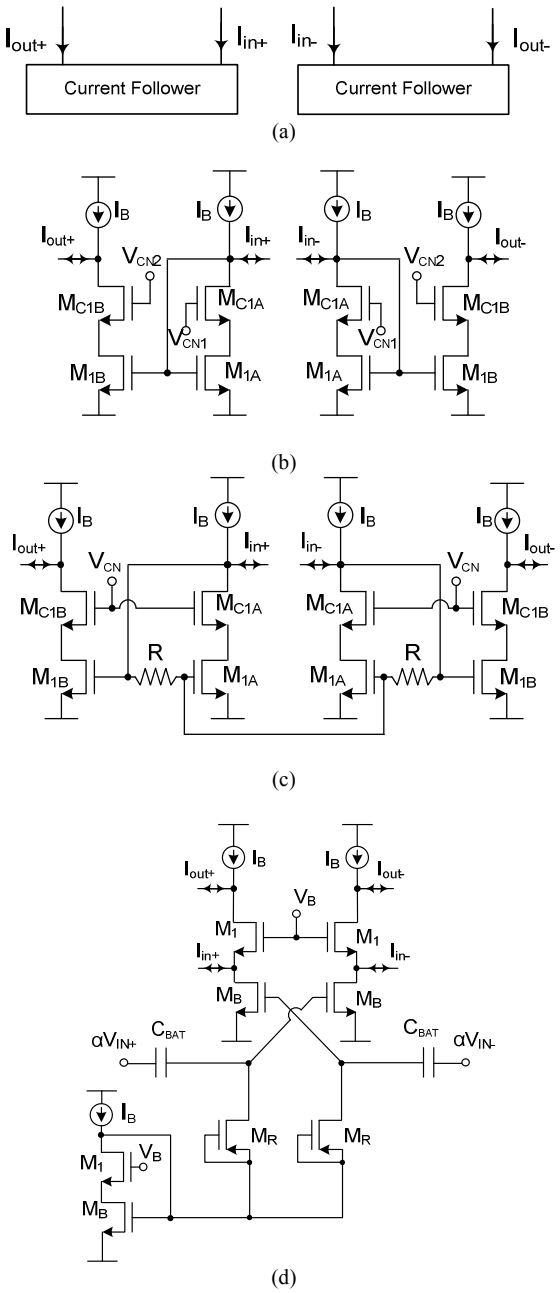


Fig. 3. Power efficient implementation of the current followers (a) Differential current follower (b) Implementation using transistors in the limit between saturation and ohmic region (c) Implementation using LCMFB. (d) Implementation using adaptive biasing.

M_{1A} enters triode region, yielding a large voltage increase at the gate of M_{1B} that boosts the output current.

An alternative approach is shown in Fig. 3(c). In this case the current mirrors are rearranged by connecting the gates of transistors M_{1A} and feeding the common-mode of the drain voltages of transistors M_{C1A} to the resulting common gate node by two matched resistors *R*. This technique, known as Local Common Mode Feedback (LCMFB) [6], allows further increase of the dynamic currents without scaling static currents. In absence of input signal, there is not voltage drop in the resistors, so the circuit acts as conventional current mirrors. However, when $I_{in+} > I_{in-}$, a voltage drop $\Delta V = R \cdot (I_{in+} - I_{in-})/2$ appears through each resistor. This voltage drop leads to a large output current I_{out+}. Analogously, for $I_{in+} < I_{in-}$, voltage drop ΔV is negative, leading to a large output current I_{out-}. Hence SR is improved without increasing quiescent currents. Moreover, LCMFB also increases small-signal performance thanks to the small-signal current gain provided by the LCMFB resistors and the AC small-signal ground at the common-gate of M_{1A}. However, resistors *R* increase the resistance at the input of the CF, decreasing phase margin. Hence a tradeoff between improvement of SR and stability exists in the choice of *R*.

Finally, an approach to improve dynamic performance in the CF of Fig. 2(c) is shown in Fig. 3(d). It is based on using an adaptive bias current source implemented using Quasi-Floating Gate (QFG) techniques [7], [8]. The gates of transistors M_B are connected to a scaled replica of the input voltages through capacitors C_{BAT}. High resistance devices are obtained by using the leakage resistance of minimum-size transistors M_R in cutoff region. In quiescent operation, C_{BAT} is an open circuit so no current flows across M_R. Hence the circuit acts as in Fig. 2(c) without input signal. The large resistive value of M_R avoids fast discharge of capacitors C_{BAT}, behaving as floating DC level shifters. Hence, when a large differential input voltage $V_{id}=V_{in+}-V_{in-}$ is applied, there is a decrease in the gate voltage of the left-hand side M_B and an increase in that of the right-hand side M_B. This way the output current increases, yielding a large SR.

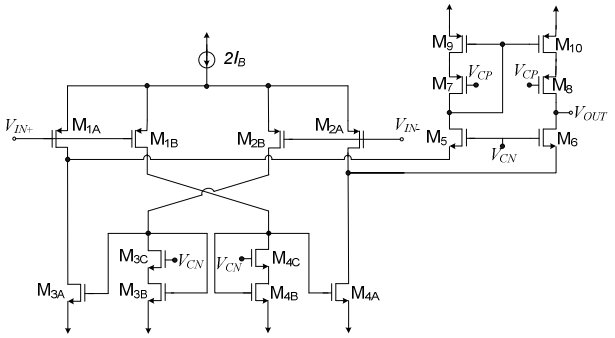
IV. Design Example

As an application example of the improved current followers just described, the circuit of Fig. 3(c) is applied to the design of an enhanced RFC OTA. Fig. 4(a) shows a conventional RFC OTA [1]. It is obtained by replacing the current sources at the folding stage of a FC OTA by active current mirrors, and reconnecting the differential pair transistors. This arrangement increases the transconductance, GBW and SR of the FC OTA for the same current consumption. Note also that the RFC OTA can be regarded as a three-current mirror OTA where an extra differential pair M_{1A} and M_{2A} is cross-connected to the folding nodes at the output branch. Fig. 4(b) shows the enhanced RFC OTA using LCMFB in the current mirrors that are employed as current followers, which further improves SR, GBW and CE.

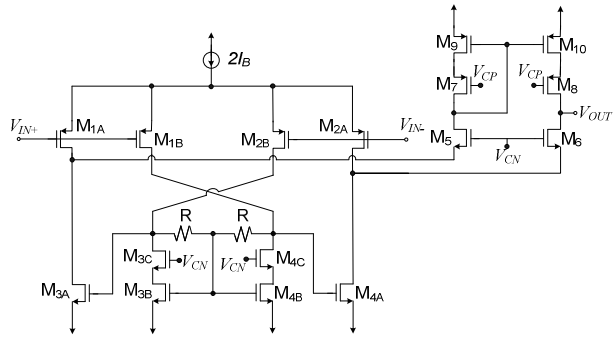
V. Simulation and Measurement Results

A test chip prototype containing the OTA of Fig. 4(b), as well as the RFC OTA of Fig. 4(a) and a FC OTA for comparison, was fabricated in a 0.5μm 2-poly n-well CMOS process. A microphotograph of the circuit of Fig. 4(b) is shown in Fig. 5. Table I shows the transistor sizes employed. Supply voltages were ±1 V, and the bias current was $2I_B$= 20 μA. Cascode bias voltages V_{CP} and V_{CN} were set to -0.2 V and 0 V, respectively. Two versions of the OTA of Fig. 4(b) were fabricated, one with *R*=10 kΩ and another one with *R*=20 kΩ.

The measured transient response of FC OTA and the OTAs of Fig. 4 connected as voltage followers is shown in Fig. 6. An



(a)



(b)

Fig. 4. (a) RFC OTA (b) Enhanced RFC OTA.

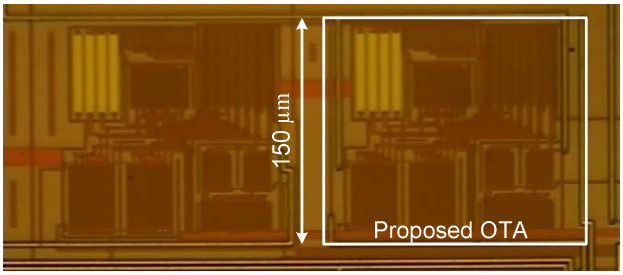


Fig. 5. Test chip microphotograph.

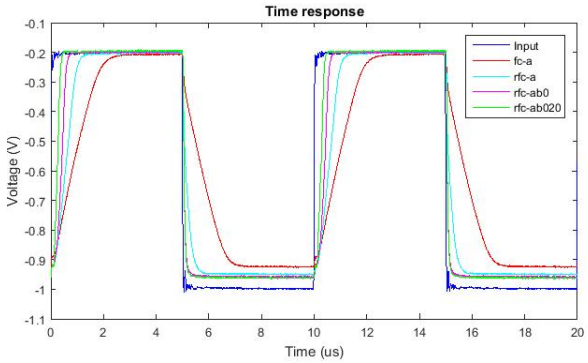


Fig. 6. Measured transient response of the FC OTA (fc-a), RFC OTA of Fig. 4(a) (rfc-a), RFC OTA of Fig. 4(b) with R=10 kΩ (rfc-ab0) and RFC OTA of Fig. 4(b) with R=20 kΩ (rfc-ab20).

external load of C_L = 47 pF was employed, which considering also the capacitance of the measurement setup leads to an overall estimated load capacitance of 70 pF. A 100 kHz 0.8 V periodic square wave with a -0.6 V DC component is employed as input signal. Note the improved SR achieved thanks to the enhanced CF of Fig. 3(c). The lack of compliance with the input at the lowest voltage is due to the voltage headroom required for the V_{DS} of M_{4A} and M_6.

Table II summarizes the main simulation and measurement results of the OTAs. Open-loop parameters correspond to simulations due to the large DC gain of the OTAs. Note the improved small-signal and large-signal performance for the same power consumption. The main drawbacks of the proposed OTA are a sligth degradation in phase margin and a small area increase due to the passive resistors R.

TABLE I - TRANSISTOR ASPECT RATIOS

Transistor	**W/L** (µm/µm)
M_{1A}-M_{2A}	190/0.6
M_{1B}-M_{2B}	190/0.6
M_{3A}-M_{4A}	180/0.6
M_{3B}-M_{4B}	60/0.6
M_{3C}-M_{4C}	60/0.6
M_5-M_6	120/0.6
M_7-M_8	200/0.6
M_9-M_{10}	200/0.6

TABLE II – SUMMARY OF MEASUREMENT RESULTS

Parameter	**FC OTA**	**Fig. 4(a)**	**Fig. 4(b), R=20kΩ**
CMOS process	0.5 µm	0.5 µm	0.5 µm
Supply voltage	±1 V	±1 V	±1 V
Capacitive load	70 pF	70 pF	70 pF
SR+	0.42 V/µs	0.80 V/µs	2.1 V/µs
SR-	-0.42 V/µs	-0.86 V/µs	-3.6 V/µs
THD @100kHz, 0.5V_{pp}	-35 dB	-42 dB	-47.7 dB
DC gain (*)	60.3 dB	68.8 dB	73.5 dB
PM (*)	88.6º	85.4º	75.9º
GBW (*)	692 kHz	1.36 MHz	2.43 MHz
CMRR @DC (*)	107 dB	116 dB	121 dB
PSRR+ @DC (*)	60 dB	69 dB	73 dB
PSRR-@DC (*)	93 dB	105 dB	110 dB
Eq. input noise @1MHz (*)	22 nV/√Hz	19 nV/√Hz	15 nV/√Hz
Power	80 µW	80 µW	80 µW
Area	0.022 mm^2	0.026 mm^2	0.028 mm^2

(*) Simulation

VI. CONCLUSION

The suitability of different current followers for the design of power-efficient OTAs is discussed. Modifications of conventional topologies to improve SR and CE have been presented. As a design example, an enhanced RFC OTA is proposed and the advantages versus the conventional RFC OTA are confirmed by simulations and measurement results of a test chip prototype.

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