

Multisampled-Capacitor-Voltage Active Damping for Parallel Interleaved Grid Connected Voltage Source Converters with LCL Filter

Javier Samanes, *Student Member, IEEE* and Eugenio Gubia, *Member, IEEE*
Public University of Navarre, Institute of Smart Cities
Campus de Arrosadia
Pamplona, Spain
Phone: +34 948168934
Email: javier.samanes@unavarra.es
URL: <http://http://www.unavarra.es/>

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Keywords

«Active damping», «Field Programmable Gate Array (FPGA)», «Frequency Domain Analysis», «Voltage Source Converter», «Converter Control».

Abstract

Parallel interleaved converters for high power renewable energy systems present stability issues at the LCL resonance frequency. A multisampled measurement and filtering strategy is proposed to stabilize the system based on the capacitor voltage derivative active damping, overcoming its limitations for low switching power converters. The effects of the delays on the stability of the active damping strategy would be analysed. The solution developed is robust against grid inductance variations, ensuring the fulfilment of the stringent harmonic grid codes.

Introduction

Grid-connected power converters are widely extended, as an interface for renewable energy generating systems. To limit the harmonic disturbances in the grid, stringent grid codes have been developed [1]. To fulfil those grid codes an LCL filter is commonly inserted at the output of the power converter [2].

Renewable energy generating systems, particularly wind turbines, are constantly incrementing their power ratings [3]. Low voltage generators are generally used in wind energy conversion systems, increasing the current handling requirements of the power converters. As the converter IGBT current is limited, the use of parallel power converters is a current trend in renewable energy systems. Moreover the filtering requirements can be reduced if advanced modulation techniques, such as interleaving, are applied [4], as the filter might be designed to attenuate higher order harmonics than the commutation frequency ones.

In renewable energy systems, efficiency and cost are key aspects. Active damping strategies are able to eliminate the stability issues related to the use of LCL filters, reducing the converter power losses, as the damping resistors, generally used to damp the resonance, can be eliminated. Furthermore, if the variable used to implement the active damping is already measured for control purposes, the overall

cost is reduced since no additional sensors are required and the resistors are eliminated. The capacitor current feedback active damping strategy is one of the most extended options [5], [6], but in general its implementation requires additional sensors, as the capacitor current measurement is not required in grid connected power converters. To avoid the use of additional sensors the use of filters in the control loop has been investigated [7], [8]. Some of the filter based approaches are not robust to grid inductance variations, or even though they stabilize the system, they do not help to meet the current harmonic grid codes [8]. The capacitor voltage active damping strategy is one of the most interesting options [9], as it is regularly measured for grid synchronization purposes. The lead-lag compensator applied to the capacitor voltage can be used to actively damp the system, but it is less robust to grid inductance variations [10], so the derivative of the capacitor voltage is a preferred solution. Its main drawbacks are noise amplification and the deformation of the derivative, due to the discretization, at frequencies close to the Nyquist frequency.

In this work the capacitor voltage active damping is studied for a system composed of two parallel interleaved power converters with an LCL filter connected to a low voltage network. The LCL resonance frequency is located close to the Nyquist frequency, resulting in an impossibility to properly implement the derivative, even with enhanced implementations, such as the proposed in [10]. To solve this problem, the derivative is programmed in a field programmable gate array (FPGA), already existing in many high power converters to implement complex digital filters in a more cost effective way than analog filtering. The FPGA is used to overcome the limitations in the sampling frequency of the converter control unit, normally set to twice the commutation frequency. The influence of the measurement filters will be analysed, usually not included in the active damping literature. The system stability is guaranteed against strong variations in the grid inductance, representing strong and weak grid operating conditions.

Three Phase Parallel Interleaved VSC

In wind power and photovoltaic systems the power converter is connected to the medium voltage grid through a step up transformer, so the transformer leakage inductance, L_{transf} , can be considered a part of the LCL filter, as shown in Fig. 1. L_g is the grid inductance at the point of common coupling (PCC) and depends on the grid at which the power converter is connected. L_{conv} is the converter inductance and C_f is the filter capacitor.

Each converter output current can be divided in the circulating current component, i_{Gc} , recirculated between both power converters, and the normal current component injected to the grid, i_{Gxn} , defined as half of the grid current [11]. In Fig. 1, for the system under study, independent inductances have been depicted even though interphase transformers can be used to limit the circulating currents and reduce the resulting LCL filter components [12]. L_{conv} , L_{transf} and C_f are set to attenuate the high

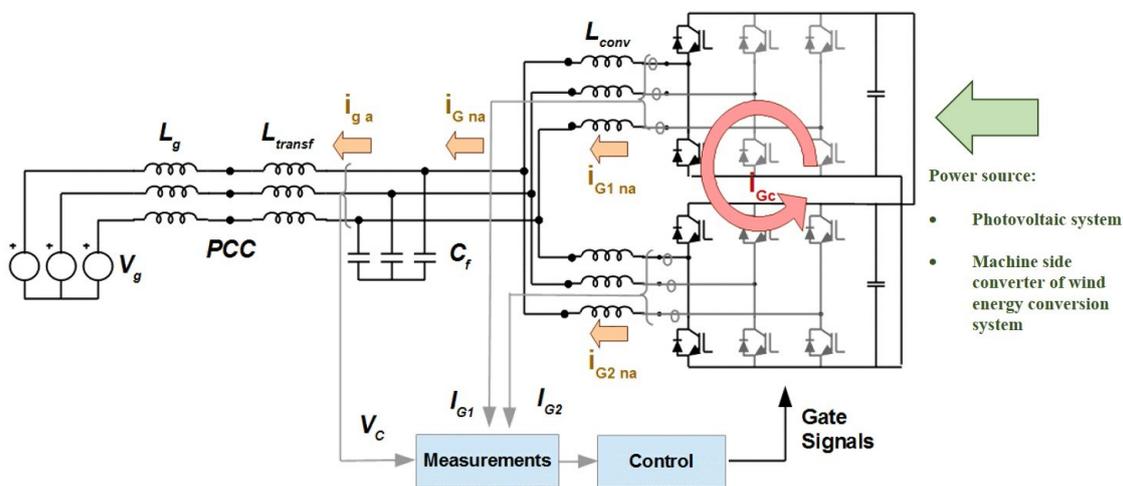


Fig. 1: System under study.

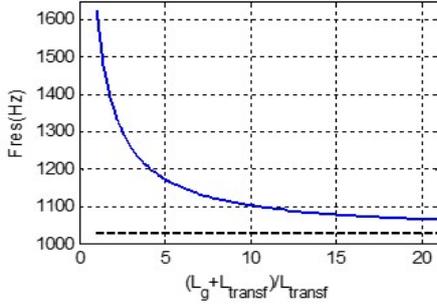


Fig. 2: Resonance frequency evolution as the grid inductance is increased.

Table I: System parameters

Parameter	Value	Parameter	Value
V_g	690 V	C_f	800 μF
P_{rated}	4 MW	F_{resmin}	1082 Hz
F_{comm}/F_{samp}	1950/3900 Hz	F_{resmax}	1600 Hz
$L_{conv}/L_{convout}$	60 $\mu\text{H}/30 \mu\text{H}$	F_{Ny}	1950 Hz
L_{transf}	20 H	F_{res}/F_{Ny}	0.83-0.53
L_g	1-250 μH	F_{FPGA}	117 kHz

frequency switching ripple. In an interleaved power converter formed by two parallel units, harmonics at the switching frequency are recirculated [13], designing the filter for the second harmonic family. The system parameters are presented in Table I for a 4 MW power converter, formed by the connection in parallel of two power converters.

The grid effective inductance varies as the power connected to the PCC is modified and from one location to the other, changing the filter resonance frequency [14]. Nevertheless, the variation is limited asymptotically when the grid inductance tends to infinity. Fig. 2 shows the variation of the filter resonance frequency for the parameters in Table I.

In these topologies, as shown in Table I, the commutation frequency is reduced to limit the power losses, and the resonance frequency is increased to reduce the cost of the LCL filter. As a result, the resonance frequency is close to the controller Nyquist frequency, commonly equal to the commutation frequency, due to the advantages of asymmetrical regular sampling [15], complicating the active damping of the resonance. The existence of the delays, mainly, PWM and computational delay, makes the system, with the undamped resonance, unstable [16].

In the existing literature, different active damping techniques have been proposed, but usually they are not applicable for systems where the resonance frequency is so close to the controller Nyquist frequency. Some active damping strategies can effectively stabilize the system when the resonance frequency is close to the Nyquist frequency [8], but this technique do not contribute to reduce the grid current harmonics at the resonance frequency. One of the most interesting active damping approaches is the capacitor voltage derivative active damping. Its application is limited for high resonance frequencies close to the Nyquist frequency [10], being the system under consideration an extreme case of proximity. In the following section an approach based on multisampling is implemented, offering a robust and cost-effective solution and contributing to a reduction of the current harmonics at the resonance frequency. The measurement filters are included in the stability analysis as they play a major role and are commonly neglected.

System Stability Analysis

Current control of the parallel interleaved power converters

The converter current is usually measured in order to control both the converter normal current component and the circulating current component. As represented in Fig. 3, the current normal component is controlled by means of a PI controller in the synchronous reference frame, setting the phase margin and the bandwidth to 60 degrees and 120 Hz. This control is implemented in the converter control unit (CCU), executed twice per commutation period. The FPGA runs at a higher speed, 117 kHz, being executed 30 times per CCU sampling time. Its main goal is the implementation of digital filters able to attenuate the switching ripple of the measurements, by programming complex filters in a cost effective approach, if compared with complex analog filters performing the same task. As depicted in Fig. 3, the outputs of the FPGA are the filtered measures, which are an input to the CCU, updated only twice per carrier frequency to avoid the issues related to oversampling [17]. The digital measurement filter implemented is a moving-average filter, having the frequency response plotted in Fig. 4, responsible of the

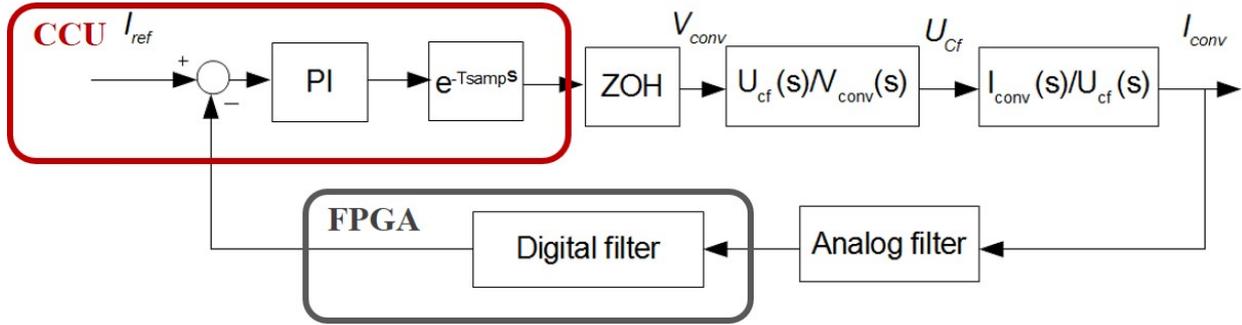


Fig. 3: Converter current loop showing the FPGA used for filtering purposes and the CCU where the controllers are implemented.

elimination of the commutation harmonics. The analog filter in Fig. 3 is a low pass filter with a cut-off frequency of 25 kHz.

In order to analyze the system stability all the current loop components must be modeled in the same domain. The continuous domain is chosen, due to the existence of different sampling times in the CCU and FPGA. The converter is modeled by a zero order hold (ZOH) and the computational delay by a pure sampling time delay [14].

The Nyquist stability criteria applied to the Bode diagram is used to assess the system stability for different grid inductance operating conditions. First of all, the stabilizing effect of the filters is studied.

Stabilizing effect of the filters used for the converter current measurement

The Bode plot of the open loop transfer function is depicted in Fig. 5 for a SCR of 1.5, equivalent to a grid inductance of $250 \mu\text{H}$, and for a SCR of 380, $1 \mu\text{H}$. In both cases the Bode diagram are plotted with the digital filter programmed in the FPGA and without such filter. It can be seen, for the low grid inductance case, how -180 degrees crossings are avoided at the resonance peak by the use of the moving average digital filter, meaning that there are not unstable poles in the closed loop transfer function. In contrast, for the high grid inductance values the digital filter is not able to introduce the required phase delay as to avoid the negative crossings. Moreover, in all the cases, the resonant magnitude peak is still important, even though in the strong grid case the system has been stabilized, requiring additional damping actions to fulfil the grid codes.

Multisampled-capacitor-voltage feedback active damping strategy

The capacitor voltage derivative feedback is able to damp the resonant peak, implementing a virtual resistor in parallel with the capacitor. As demonstrated in [18] for the grid current control, this equiva-

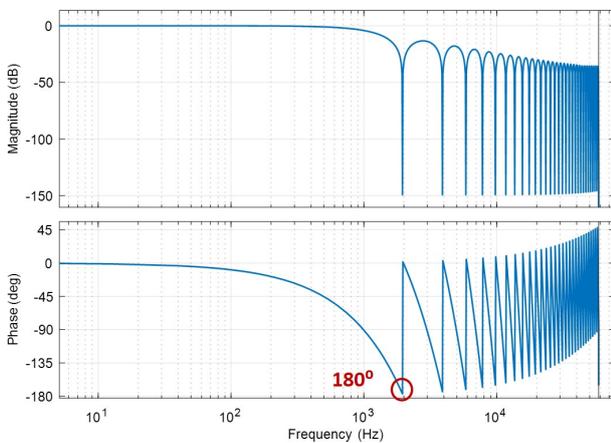


Fig. 4: Digital filter programmed in the FPGA.

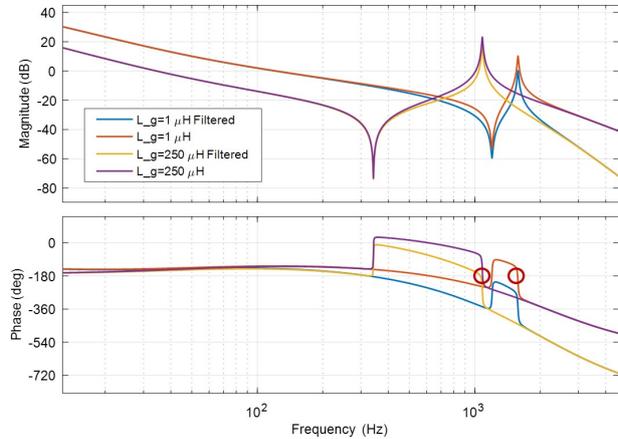


Fig. 5: Open loop Bode plots for different grid inductances.

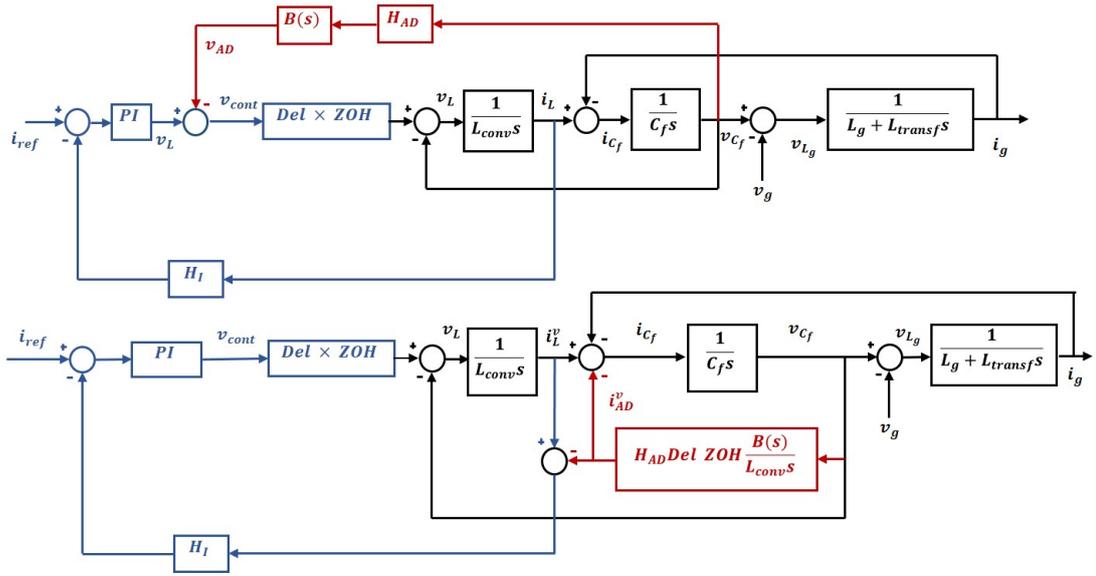


Fig. 6: Upper graph: block diagram representing the single phase equivalent model, the capacitor feedback active damping and the current control loop and lower graph: equivalent diagram representing the active damping as parallel admittance with the filter capacitor.

lence can be developed for the converter current control by operating with the block diagram presented in Fig. 6. In this way the impedance emulated, Z_{ad} , in parallel with the filter capacitor is given by (1), where Del is the computational delay, ZOH the zero order hold, H_{AD} the filter applied in the active damping feedback and $B(s)$ the transfer function used for the active damping of the filter resonance. The equivalent circuit derived from the block diagram is represented in Fig. 7. It is straight forward from Fig. 6 and (1) that, if $B(s) = K_{ad}s$ and the delays and filters are ignored, a virtual resistor would be implemented in parallel with the filter capacitor. Two concerns arise at this point; the digital implementation of the derivative and the effect of the delays in the emulated virtual impedance.

$$Z_{ad}(s) = \frac{L_{conv}s}{H_{AD}(s)Del(s)ZOH(s)B(s)} \quad (1)$$

The discrete implementation of the derivative is a key aspect of the strategy. It is known that the backward discretization of the derivative misshapes its frequency response close to the Nyquist frequency, as shown in Fig. 8. Even with an enhanced implementation of the derivative action, as proposed in [10] the system

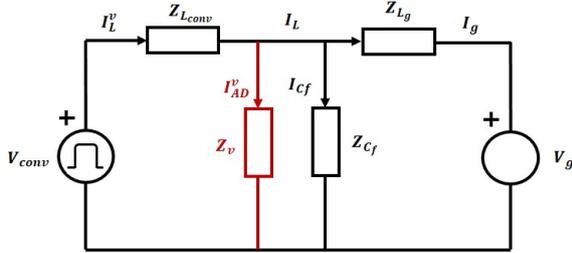


Fig. 7: Equivalent circuit of the LCL filter with the capacitor voltage feedback active damping.

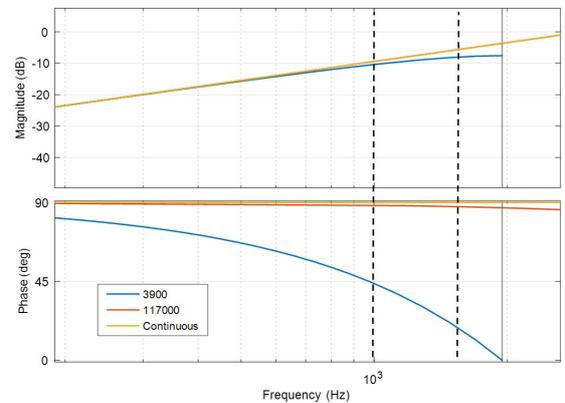


Fig. 8: Backward derivative discretization of the derivative at different sampling frequencies.

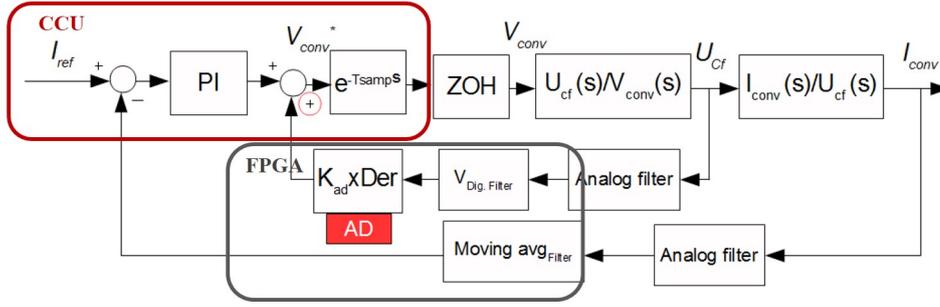


Fig. 9: Control loop including the active damping feedback programmed in the FPGA.

cannot be damped close to the Nyquist frequency. For this reason, the proposed solution for parallel interleaved converters is the implementation of a faster derivative in the existing FPGA, Fig. 8. With this approach, based on the oversampling performed in a faster digital system, an appropriate derivative is performed between the maximum and the minimum LCL resonant frequency in an almost costless solution for high power converters. A problem related to the implementation of the derivative in a faster controller is the amplification of high frequency noise. In the following, special attention is paid filtering solution applied in the derivative control path.

Even though the derivative action is properly implemented, it still suffers the effects of the delay. (2) shows the delays that affect the active damping, namely the ZOH, the computational delay and the filters used in the feedback path. If no filters are applied to the active damping feedback, the delay is equal to one and a half sample times, and thus the virtual resistance becomes a virtual impedance, whose real part can change its sign [18]. It must be reminded that the CCU is only updated twice per carrier cycle, to avoid the issues related to over sampling. The existing delays can be further increased by the filter applied to the voltage measurement, Fig. 9, compromising the stability of the active damping strategy. To analyse the effects of the delays on stability, in Fig. 10, it is depicted how the real part (the resistive part) of the virtual impedance changes its sign as the resonant frequency varies. In the first case, only the one and a half sample time delays are considered, proving that the stability can be guaranteed by performing a positive feedback as shown in Fig. 9. In the second case, the additional delay of the moving average filter, plotted in Fig. 4, is added proving that stability issues arise as the resonance frequency can be located between different signs of the virtual impedance real part. The stability cannot be guaranteed by simply modifying the feedback sign. For this reason, the delays introduced in the active damping control loop have to be reduced.

To solve this issue a modification of the moving average digital filter [19] is used instead of the classical moving average filter. In this way the introduction of an additional delay equal to a sample time is avoided. The new filter introduces less attenuation at higher frequencies, for this reason, a low pass second order Butterworth filter with a reduced effect in the phase at low frequencies is implemented. Fig. 11 shows the frequency response of the filter and the filter along with the derivative. It can be seen how the noise would not be amplified, reducing the phase delay at frequencies where the resonance can be located consequently maintaining the sign of the real part of the virtual impedance unchanged. It should also be noted that the modified moving average filter is set to filter the even multiples of the

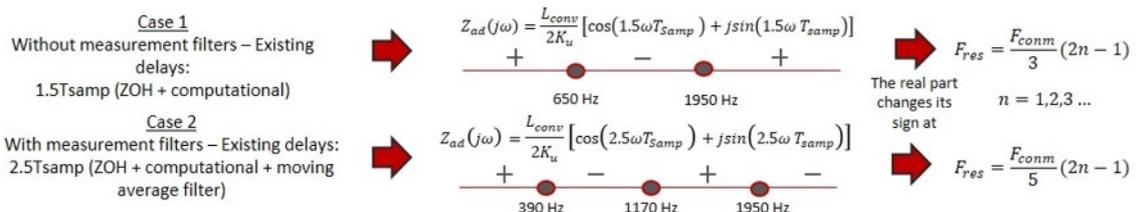


Fig. 10: Effect of the delay on the resistive component of the virtual impedance.

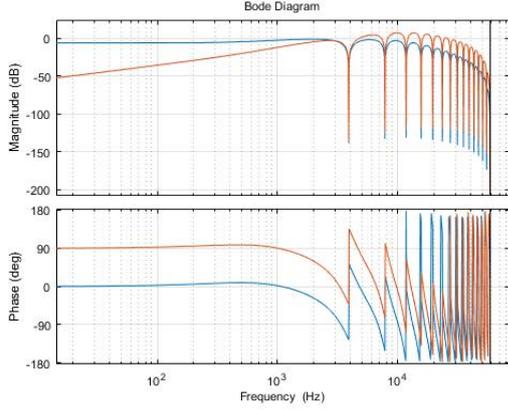


Fig. 11: Active damping filter (blue) and active damping filter and derivative action (red).

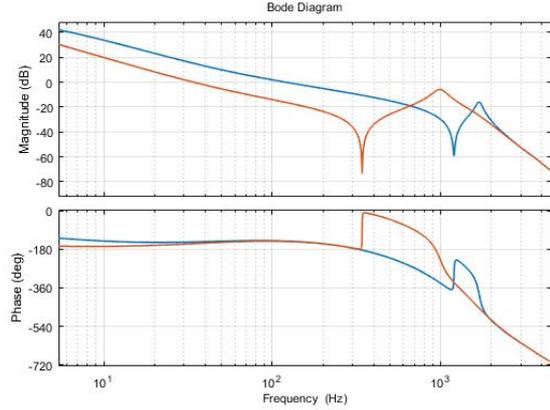


Fig. 12: Bode plot of the current control loop including the active damping feedback.

commutation harmonics, as the odd multiples are recirculated between both power converters as a result of the application of interleaving.

$$\Phi_{addelay} = \Phi_{ZOH} + \Phi_{computational} + \Phi_{adfilters} \quad (2)$$

The stability of the current loop is verified again for a grid inductance of $1 \mu H$ ($SCR = 380$) and $250 \mu H$ ($SCR = 1.5$). It can be confirmed, by analysing the Bode plot in Fig. 12, that the system is stable in both cases, as there are not unstable poles in the open loop Bode plot and no negative or positive crossings. The value of the virtual resistor implemented is set to 0.46Ω . The selection of the optimal value for the emulated resistor is performed through a study of the closed loop resonant poles. Fig. 13 and Fig. 14 show the closed loop resonant poles trajectory as the virtual resistor is increased, for a strong grid situation ($SCR = 380$) and a weak grid scenario ($SCR = 1.5$). In both cases the optimal damping of the poles is for a virtual resistor around 0.4Ω . This value provides a damping close to the optimal one for the whole operating range of grid inductances at the resonant poles. A value of 0.46 has been selected because it is a compromise between the optimal value and a reduced damping action, in terms of voltage, the greater is the emulated resistor the lower remains the required action.

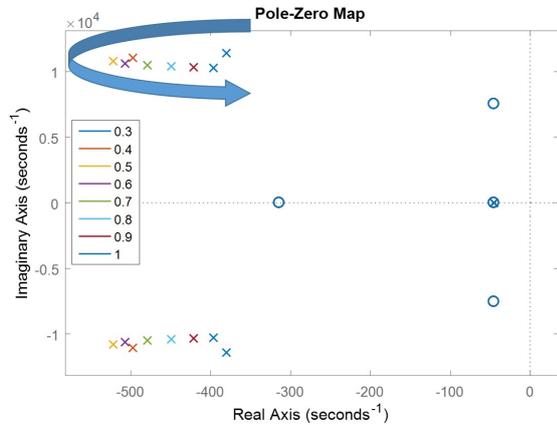


Fig. 13: Evolution of the closed loop resonant poles as the virtual resistance is increased for a $SCR = 380$.

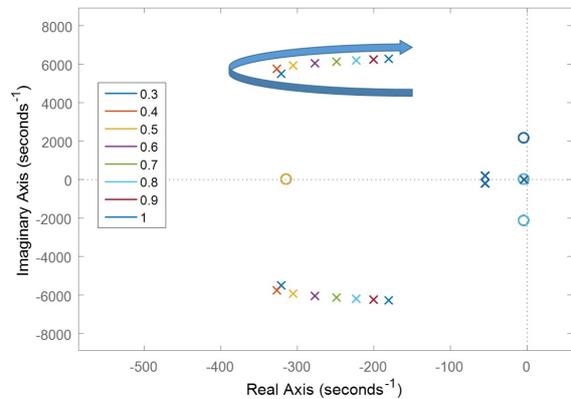


Fig. 14: Evolution of the closed loop resonant poles as the virtual resistance is increased for a $SCR = 1.5$.

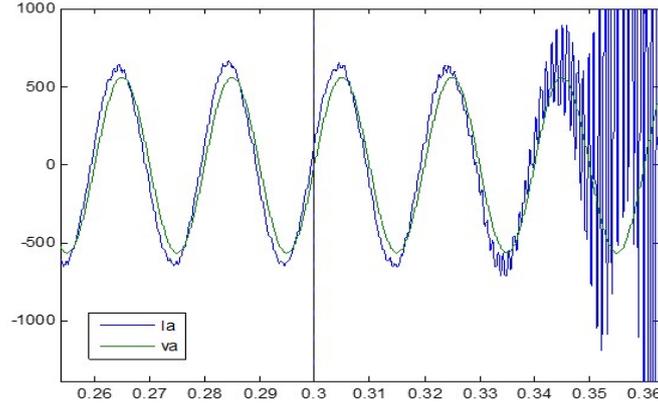


Fig. 15: Grid current for a weak grid (SCR=1.5) as the active damping is disconnected.

Even though the stability analysis has been performed for one equivalent power converter, the real system is formed by two phase shifted units. To properly implement the active damping strategy, the derivative action must be programmed in only one power converter, as the harmonics modulated by each converter are phase shifted.

Simulation results

To test the performance of the proposed active damping strategy, simulations using Matlab SimPower-Systems toolbox have been carried out. The simulated system is formed by two parallel 2 MW power converters with the specifications of Table I, to create a 4 MW power conversion structure. The modulation used is the space vector modulation SVPWM7. The CCU and the FPGA are programmed in separated S-Functions programmed in C. The output of the CCU are the gate signals, Fig. 1, with a dead time of $4 \mu s$. The parasitic series resistance of the transformer, converter inductance and filter capacitor are considered to be $0.15 m\Omega$, $0.1 m\Omega$ and $1 m\Omega$ respectively.

Fig. 15 proves the stability analysis performed in the previous section. For a weak grid, initially, as the AD strategy is enabled the converter operates in a stable mode, when it is disconnected, the converter current cannot be controlled. In contrast, for strong grids, the system is stable as it was previously analysed, independently of the activation or deactivation of the active damping. In Fig. 16 the grid current harmonic content is compared to the limits imposed by the BDEW when the derivative active

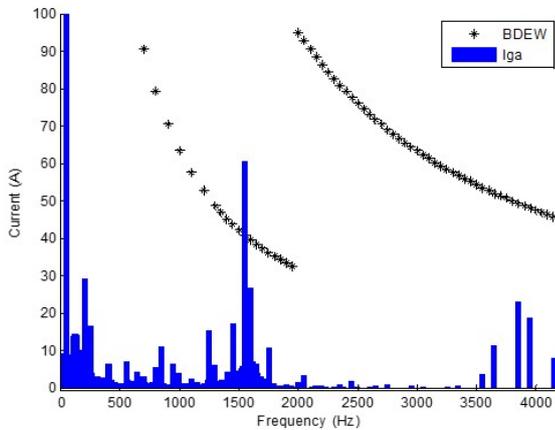


Fig. 16: Grid current harmonics compared to the BDEW limits (SCR 380), with the active damping disabled.

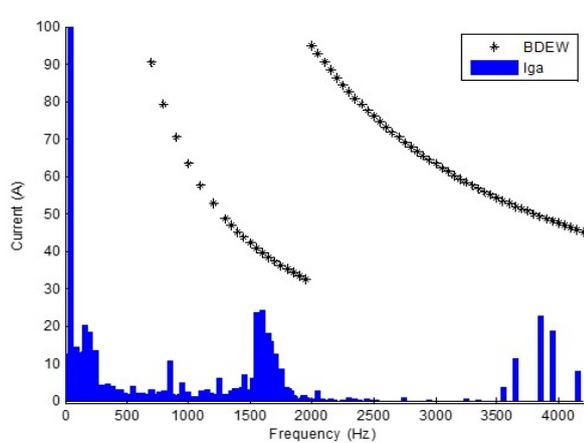


Fig. 17: Grid current harmonics compared to the BDEW limits (SCR 380), with the active damping enabled.

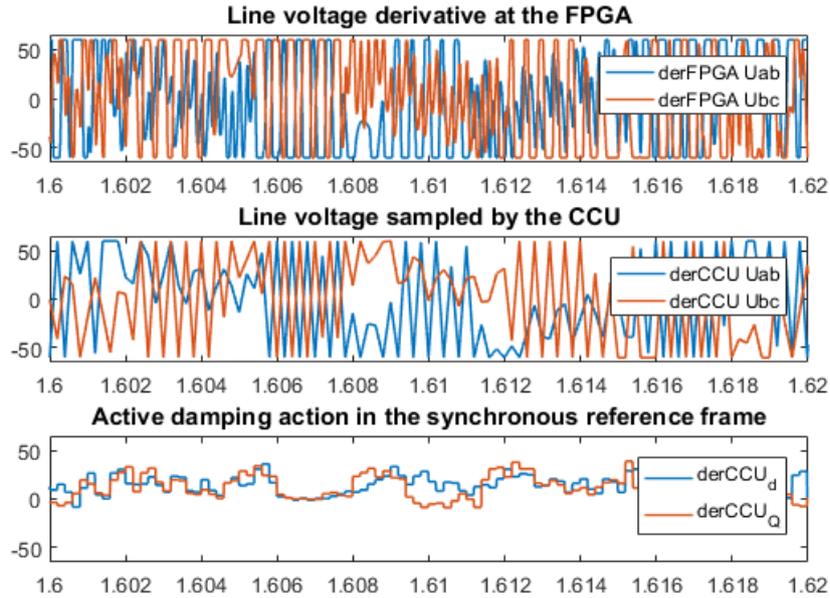


Fig. 18: Line voltage derivative at the output of the FPGA (upper graph), derivative sampled by the CCU (middle graph) and action applied in the synchronous reference frame (lower graph).

damping is disabled. It can be concluded that even though the system is stable, it is not able to meet the grid codes since a great magnitude peak exists in the magnitude Bode plot, due to the undamped resonance frequency. In Fig. 17 the same analysis is performed enabling the AD action, verifying that the harmonics at the resonance frequency are highly reduced, meeting the grid codes without additional hardware damping methods.

In Fig. 18 the derivative at the output of the FPGA is shown in the first graph. In the second graph the derivative is sampled by the CCU and at last the applied action, in the synchronous reference frame, is plotted in the third graph, after being filtered by the low pass filter synthesized in the previous section. The required action to damp the system is confined within a 1.7 % of the DC bus voltage in permanent operation.

Conclusions

In this work the stability of the converter current control of two parallel interleaved VSC has been analyzed taking into account the influence of the filter measurements, commonly not included in the active damping literature. The measurement filters are digitally implemented in a FPGA. It has been concluded that the additional delays introduced by the measurement filters can help to stabilize digitally controlled systems. Nevertheless, additional damping actions must be introduced to stabilize the system as the effective grid inductance varies, a common problem in grid connected renewable energy systems, and to fulfil the stringent grid codes. The capacitor voltage derivative is one of the preferred options to actively damp the LCL filter resonance in grid connected VSC as the voltage at the capacitor is usually measured for grid synchronization purposes, avoiding the use of additional sensors. The discretization of the derivative limits the applicability of the active damping strategy in high power converters, where the resonance frequency is close to the Nyquist frequency. Even with the application of advanced implementations for the derivative, it becomes a proportional gain at the resonance frequency of the LCL filter of parallel interleaved VSC.

In this work, the use of a FPGA is proposed to properly implement the derivative, adjusting a digital filter to avoid noise amplification at higher frequencies. The filter chosen is a modified version of a moving average filter, minimizing the delay introduced at the CCU Nyquist frequency, avoiding the stability

problems of increasing the delay introduced by the PWM converter and the digital computation in the CCU. The proposed implementation of the active damping strategy for LCL interleaved VSC is a cost effective solution, able to guarantee a robust damping action face to effective grid inductance variations. Moreover it allows the fulfillment of the stringent grid codes as it actuates directly on the harmonics modulated at the resonance frequency.

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