CMOS Low-Voltage Indirect Current Feedback Instrumentation Amplifiers With Improved Performance

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***Abstract*—Indirect current feedback (ICF) is a very common operation principle used in the design of CMOS instrumentation amplifiers (IA). The input and output transconductors required in an ICF IA usually consist on resistive-degenerated simple differential pairs. In this contribution conventional source-follower (SF) structures used in IA transconductors are replaced by flipped-voltage-follower (FVF) and super-source-follower (SSF) cells, respectively. As a result, the overall performance and efficiency of the IA is enhanced with a minimum cost. The principle of operation governing CMRR is also analyzed and its behavior is confirmed by means of extensive simulations. A single-stage IA with a fixed voltage gain equal to 10 V/V has been designed in 0.35-µm standard CMOS technology to operate with 1.8 V supply. Simulation results show improved metrics in terms of voltage gain accuracy, while the overall performance of the IA is comparable to other contributions in the literature.**

Keywords—instrumentation amplifiers; indirect current feedback; enhanced voltage follower; source degeneration; resistive sensor.

I. INTRODUCTION

Sensors are ubiquitous components that have outstanding importance in the context of fields such as industry, biomedical devices or internet of things (IoT), among others. The instrumentation amplifier (IA) is an analogue block essential in the conditioning of signals provided by sensors. The traditional approach to implement an IA is based on resistive feedback [1]. A difference amplifier processes only the differential-mode (DM) signal, while the input resistance of the overall IA is increased by isolating its input terminals with two balanced noninverting amplifiers. This structure leads to demanding area and power requirements [1, 2], as well as constraints to adapt the input and output common-mode (CM) voltages of the three amplifiers [2]. Besides, the CM rejection ratio (CMRR) of the overall structure relies on the matching of the feedback resistors, which must be trimmed when a high CMRR value is desired.

Current feedback (CF) [2]-[7] is an efficient approach for implementing IAs. Indeed, in CF instrumentation amplifiers isolation and balancing techniques are used to enhance CMRR [2]. Besides, a single feedback loop is established around the IA. Depending on how the CF solution is implemented, we can distinguish between direct current feedback (DCF) [3] or indirect current feedback (ICF) [2]. Alternatively, the local current feedback (LCF) technique, in which two independent feedback loops are established in the IA, has also been proposed [4].

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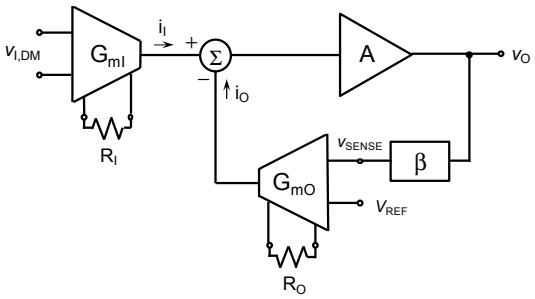

Fig. 1. Block diagram of a current feedback IA.

II. ICF IA TRANSCONDUCTORS

The block diagram of an ICF IA is illustrated in Fig. 1. Two transconductors are required, one of them devoted to process the input signal and the other one to feed back the output signal, whereas a summing stage provides additional voltage gain. The input transconductance cell, or voltage-to-current (V-to-I) converter, G_{mI}, generates a current i_I from the DM input voltage, $v_{I,DM} = v_I^+ - v_I^-$. Similarly, the transconductor G_{mO} provides a current i_O from the voltage difference $v_{SENSE} - V_{REF}$, where v_{SENSE} is the output voltage, v_O, scaled down by the feedback factor, β, and V_{REF} is a reference voltage used as the desired DC voltage level at the output of the IA. The feedback action established around G_{mO} forces i_I and i_O to be equal and, hence, it can be derived that the voltage gain, A_v, approximately coincides with:

$$A_v \equiv \frac{v_O}{v_{I,DM}} = \frac{G_{mI}}{G_{mO}} \cdot \frac{1}{\beta} \tag{1}$$

where transconductances G_{mI} and G_{mO} are a function of resistors R_I and R_O, which are a part of input and output V-to-I converters.

A well-known implementation of a transconductance cell is based on resistive source degeneration, by using two voltage

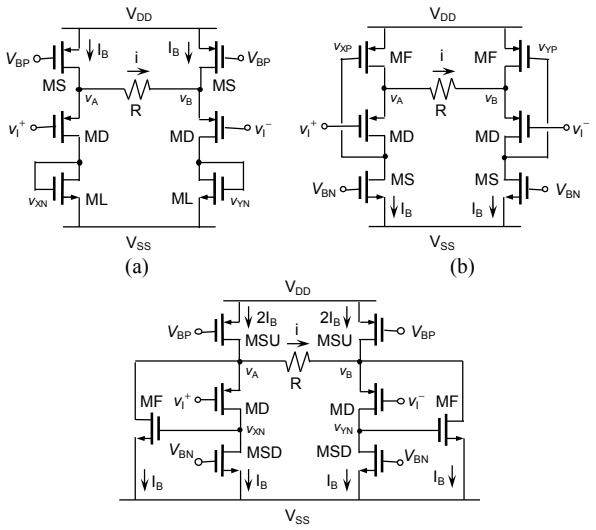

Fig. 2. Transconductors based on the (a) SF, (b) FVF and (c) SSF approach.

followers and a resistor, as illustrated in the different approaches in Fig. 2. The general principle of operation is based on isolating from the preceding stage the resistor in which *V*-to-*I* conversion takes place. The voltage followers generate shifted copies of voltages v_I^+ and v_I^-, named v_A and v_B, respectively, which are applied at both terminals of resistor *R*, thus creating current *i*. In Fig. 2(a), which corresponds to the traditional design approach, the voltage followers are implemented as conventional source followers (SF). A PMOS configuration has been selected in order to avoid the body effect in an *n*-well technology, while the purpose of transistors ML is to collect and reflect to subsequent stages the current signal generated in the *V*-to-*I* converter. However, the use of SF presents two main drawbacks. On the one hand, the output resistance of the SF is roughly given by

$$R_{OUT,SF} \approx \frac{1}{g_{mD}} \tag{2}$$

where g_{mD} is the transconductance of the driver transistors MD. The output resistance given by (2) is not sufficiently low as compared to usual resistance values implementable in integrated circuits fabrication technologies and, hence, the SF with resistive source degeneration suffers from severe load regulation limitations. On the other hand, it is worth to point out that the current flowing through the driver transistor MD of the SF is a function of the signal applied to the input of the voltage follower, which reduces the intrinsic linearity of the circuit in Fig. 2(a).

The overall performance of the transconductor may be improved by using a flipped-voltage-follower (FVF) [8] or a super-source-follower (SSF) [9] instead of the conventional SF, to drive resistor *R*, as illustrated in Figs. 2(b) and 2(c), respectively. In these cases, the output resistance of the corresponding voltage buffers may be expressed, respectively, as:

$$R_{OUT,FVF} \approx \frac{1}{g_{mD}} \cdot \frac{1}{\frac{g_{mF}}{g_{oD}+g_{oS}}} \tag{3}$$

$$R_{OUT,SSF} \approx \frac{1}{g_{mD}} \cdot \frac{1}{\frac{g_{mF}}{g_{oD}+g_{oSU}}} \tag{4}$$

where g_{mj} and g_{oj}, with j = D, F, S, and SU, represent the transconductance and output conductance of driver transistors, MD, feedback transistors, MF, and current source transistors, MS and MSU, also respectively. In each realization, the output resistance of the improved followers is reduced by an amount equal to the gain of the implicit feedback loop made up of transistors MF and MD. This significant decrease in the value of R_{OUT} highly reduces the load regulation of the corresponding voltage follower and brings the value of its voltage gain much closer to the ideal target of unity. Indeed, simulations show that while the voltage gain of the SF is far from unity, even for *R* above 10 kΩ, the gains of the FVF and SSF approaches remain very close to the ideal value even for *R* below 1 kΩ. The current flowing through the driver transistors in the FVF and SSF configurations is fixed and independent of the signal level, thus leading to increased linearity as compared to the SF solution. In addition, it is worth to note that performance improvement is obtained without significant cost in terms of silicon area and power consumption with respect to the SF approach.

III. DM *VS* CM TRANSCONDUCTANCE

The transconductance of a *V*-to-*I* cell, G_m, may be defined as the output current when a purely DM signal, $v_{I,DM}$, is applied at the input terminals. When the transconductor is implemented by using ideal voltage followers, the effective transconductance is equal to 1/*R*, that is, the inverse of the value of the resistor where *V*-to-*I* conversion takes place. In case SF are used as voltage followers, i.e., by following the approach shown in Fig. 2(a), the effective transconductance of the circuit is given by:

$$G_{m,SF} = \frac{1}{R} \cdot \frac{1}{1+\frac{2}{R}\cdot\frac{1}{g_{mD}}} \tag{5}$$

In effect, it may be inferred from (5) that $G_{m,SF}$ is inversely proportional to the value of resistor *R*. In addition, there is a factor also relying on *R*, which represents the loading effect of *R* on the non-ideal voltage followers.

When the voltage buffers used in the transconductor implementation are based on the FVF and the SSF approaches, illustrated in Figs. 2(b) and 2(c), respectively, the effective transconductance of the circuits becomes:

$$G_{m,FVF} = \frac{1}{R} \cdot \frac{1}{1+\left(1+\frac{2}{R}\cdot\frac{1}{g_{mD}}\right)\cdot\frac{g_{oD}+g_{oS}}{g_{mF}}} \tag{6}$$

$$G_{m,SSF} = \frac{1}{R} \cdot \frac{1}{1+\left(1+\frac{2}{R}\cdot\frac{1}{g_{mD}}\right)\cdot\frac{g_{oD}+g_{oSU}}{g_{mF}}} \tag{7}$$

The load regulation effect is now greatly reduced by the effect of the feedback action in the FVF and SSF cells. Indeed, this term is clearly identified in the denominator of the right-side term in (6) and (7).

The impact of resistor *R* on the effective transconductance of the *V*-to-*I* converters based on the SF, the FVF and the SSF solutions is depicted in Fig. 3. As observed, transconductance response of the FVF and the SSF *V*-to-*I* converters is very close to the ideal behavior, represented by the hyperbola 1/*R*. On the other hand, the response of the SF solution in Fig. 3 remains far from the intended operation, as already evidenced by (5).

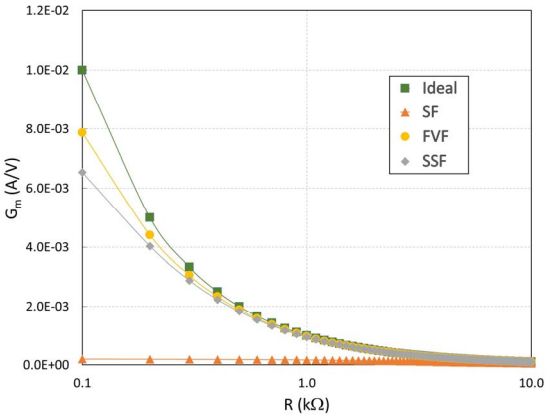

Fig. 3. Effect of resistor R on the effective transconductance G_m for the SF, FVF and SSF transconductors as compared to the ideal response.

The main contribution to the overall transconductance of the input and output transconductors of the ICF IA is due to the response to the input DM voltage, $v_{I,DM}$. Nevertheless, there is a second-order effect over the transconductance due to the joint contribution of input CM voltage, $v_{I,CM}$, and unavoidable mismatches. This aspect, whereas can be neglected for the output transconductor, G_{mO} in Fig. 1, results of critical importance for the input V-to-I converter, G_{mI}. In fact, this is the main limitation of CMRR in an IA. The residual transconductance associated to $v_{I,CM}$ is defined as:

$$\Delta G_m \equiv \frac{\Delta i_O}{\Delta v_{I,CM}} \tag{8}$$

Under perfect matching conditions, ΔG_m for the three approaches mentioned would be equal to zero. Nevertheless, random mismatches are unavoidable and, hence, the residual transconductance, ΔG_m, will be always different from zero. If the small-signal equivalent circuit of each transconductor in Fig. 2 is considered, circuit simulations allowed us to verify that the main contribution to ΔG_m is due to mismatches in the transconductance of the driver transistors, Δg_{mD}, resulting in:

$$\Delta G_{m,SF} = \frac{1}{R}\cdot\frac{\Delta g_{mD}}{g_{mD}}\cdot\frac{g_{oD}+g_{oS}}{g_{mD}}\cdot\frac{1}{1+\frac{2}{R}\cdot\frac{1}{g_{mD}}} \tag{9a}$$

$$\Delta G_{m,FVF} = \frac{1}{R}\cdot\frac{\Delta g_{mD}}{g_{mD}}\cdot\frac{g_{oD}}{g_{mD}}\cdot\frac{1}{1+\frac{2}{R}\cdot\frac{1}{g_{mD}}\cdot\frac{g_{oD}+g_{oS}}{g_{mF}}} \tag{9b}$$

$$\Delta G_{m,SSF} = \frac{1}{R}\cdot\frac{\Delta g_{mD}}{g_{mD}}\cdot\frac{g_{oD}}{g_{mD}}\cdot\frac{1}{1+\frac{2}{R}\cdot\frac{1}{g_{mD}}\cdot\frac{g_{oD}+g_{oSU}}{g_{mF}}} \tag{9c}$$

As observed, the feedback loop inherent in the FVF and SSF solutions reduces the contribution of the denominator of the last term in (9b) and (9c) as compared to (9a), thus increasing the corresponding value of ΔG_m for the solutions based on improved voltage followers. Nevertheless, as it will be shown next, the ratio $G_m/\Delta G_m$, which is indicative of CMRR, is greater for approaches based on FVF and SSF transconductors, due to the severe degradation of G_m as R is reduced in the case of the conventional SF structure.

The values of G_m and ΔG_m for the three transconductors in Fig. 2, i.e., SF, FVF and the SSF approach, have been determined by means of Montecarlo simulations, taking into account mismatches and process variations over 500 runs. The differential-to-common transconductance ratio, $G_m/\Delta G_m$, for the SF, FVF and SSF-based transconductors were determined to be 88.6 dB, 122.7 dB and 136.5 dB, respectively. The DM-to-CM transconductance ratio provides an idea of the CMRR. Indeed, it is shown in Section V that the values provided for the $G_m/\Delta G_m$ ratio are related to CMRR values obtained for each different of the IA, i.e., SF, FVF and SSF.

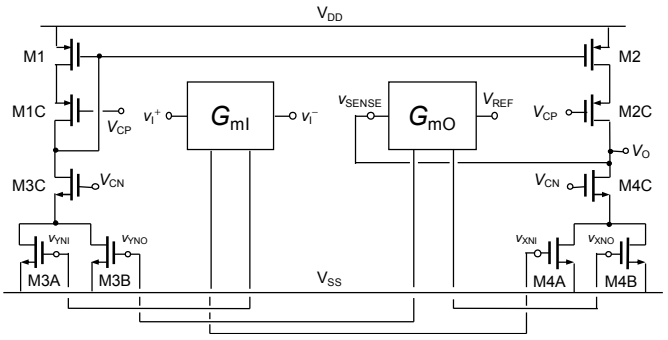

Fig. 4. Implementation of the proposed ICF IA.

IV. ICF IA Implementation

Figure 4 illustrates the circuit implementation of the proposed IA based on ICF. It consists of input and output transconductors, represented as black boxes, and a single gain stage. The input and output V-to-I converters have been implemented by following the SF, FVF and SSF configurations in Fig. 2. The current-mirroring approach is followed for current signals summation, as it results more convenient taking into account the FVF and SSF structures. In Figs. 2(a) and 2(c) it may be seen that in the SF and SSF cells the current signals of input and output transconductors are copied to the output terminal by means of NMOS current mirrors, signals v_{XN} and v_{YN}. Therefore, the circuit in Fig. 4 corresponds particularly to the exact implementation of these two solutions. On the contrary, the FVF configuration, Fig. 2(b), uses PMOS current mirrors for signal processing, signals v_{XP} and v_{YP}, and, hence, the complementary structure of the single-stage IA was implemented. Only one circuit schematic is drawn here for the sake of conciseness.

The nominal voltage gain of the IA, which is given by (1), has a fixed value of 10 V/V. It may be rewritten as R_O/R_I for the FVF and SSF cases, as, according to (6) and (7), the effective transconductance of these cells is essentially the inverse of the value of the resistor in the V-to-I converter.

V. Simulated Performance Comparison

The IA illustrated in Fig. 4 has been designed in standard 0.35-μm CMOS technology following the three previously mentioned approaches to operate with a 1.8 V supply voltage ($V_{DD} = -V_{SS} = 0.9$ V). The nominal threshold voltages for NMOS and PMOS transistors were equal to 0.50 V and –0.65 V, respectively, while the degeneration resistors were implemented with the available polysilicon layer. Bias current of each voltage follower branch, i.e., I_B in Figs. 2(a) and 2(b) and $2I_B$ in Fig. 2(c),

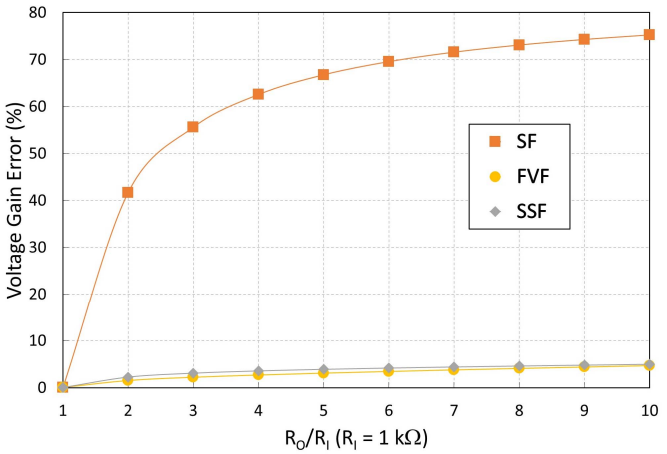

Fig. 5. Voltage gain error of the ICF IA for different R_O/R_I ratios (R_I = 1 kΩ).

was set to 20 μA. Thus, the quiescent current flowing through the driver transistors in the SF and FVF transconductors was twice than in the case of the SSF structure, according to the circuit schematics in Fig. 2. Current sources were implemented as single-transistor structures and $v_{I,CM}$ was set equal to 0.9 V.

As indicated previously, the voltage gain of the IA relies on the ratio of the input and output transconductances, G_{mI}/G_{mO}, which is a function of the degeneration resistors ratio, R_O/R_I. In the case of the SF V-to-I converter, this relationship is difficult to be predicted after fabrication, while for the FVF and SSF transconductors the ratio G_{mI}/G_{mO} is almost constant and equal to R_O/R_I. Nevertheless, as G_{mI} and G_{mO}, and consequently R_I and R_O, are made different to adjust the voltage gain, a systematic error is produced. Figure 5 shows the voltage gain error in each approach as a function of the nominal voltage gain. As observed, the value of the voltage gain of the SF solution substantially differs from the expected value. In contrast, the IAs based on FVF and SSF transconductors provide voltage gains close to the ratio R_O/R_I. As previously mentioned, the error induced in both approaches is due to systematic mismatch between input and output transconductance cells, which appears when R_I and R_O take a different value and is predicted by the terms on the right side in (6) and (7).

The rest of the three IA performance is summarized in Table I. Parameters on which mismatches and process variations have a key impact, such as CMRR and offset voltage (V_{off}), have been derived from Montecarlo analyses. Even though performance comparison should consider that biasing conditions of each kind of transconductor are not exactly the same, the overall response of the FVF and SSF amplifiers seems to be superior to the conventional SF counterpart. In particular, the improved followers provided much higher voltage gain accuracy and CMRR, even though the CMRR of the FVF approach is lower at DC as compared to the other two approaches. Besides, the CMRR responses are in general in agreement with the $G_m/\Delta G_m$ results provided in Section III. Finally, it is worth to mention that the performance in Table I is comparable to other IAs that can be found in the literature, [2]-[7].

TABLE I. SIMULATED PERFORMANCE SUMMARY OF THE ICF IA (TECHNOLOGY: 0.35-µm CMOS, V_{DD} = 1.8 V, $A_{V,NOMINAL}$ = 10 V/V)

Parameter	SF	FVF	SSF
Current consumption (µA)	159.7	172.3	119.5
DC voltage gain error (%)	75.23	4.70	4.97
BW (MHz)	11.55	9.48	7.26
CMRR±σ(CMRR) @ DC (dB)	71.7±14.2	67.8±15.5	87.0±12.2
CMRR±σ(CMRR) @ BW (dB)	38.6±3.1	59.9±10.5	52.2±5.0
V_{off}±σ(V_{off}) (mV)	1.1±9.6	1.0±11.7	0.7±12.6
THD @ v_I = 5 mV_{pp} / f_I = 1 kHz (dB)	-69.46	-44.0	-61.1
SR^+ / SR^- (V/μs)	2.4 / 2.4	9.7 / 6.1	7.1 / 7.0
Integrated input-referred voltage noise 1 Hz to BW (μV_{rms})	41.5	21.9	23.1

VI. CONCLUSIONS

The analysis and extensive simulation of transconductance cells based on three different approaches of resistive source degeneration, has shown that the use of improved voltage followers, i.e., the FVF and the SSF, leads to an improved behavior in terms of ratio $G_m/\Delta G_m$ with respect to the conventional approach, that is, the SF. A single-stage ICF IA, incorporating SF, FVF and SSF in the input and output V-to-I converters, has been designed in standard 0.35-µm CMOS technology to operate in a 1.8 V supply voltage. Simulated results, including Montecarlo analyses, have confirmed higher voltage gain accuracy as well as better CMRR, SR and noise metrics, among others, for the improved FVF and SSF solutions as compared to the conventional SF configuration.

REFERENCES

[1] J.H. Huijsing, Operational amplifiers: theory and design, 2nd ed., Springer, 2011.

[2] B.J. van den Dool and J.H. Huijsing, "Indirect current feedback instrumentation amplifier with a common-mode input range that includes the negative rail," *IEEE J. Solid-State Circtuits*, vol. 28, pp. 743-749, July 1993.

[3] M.S.J. Steyaert, W.M. Sansen, and C. Zhongyuan, "A micropower low-noise monolithic instrumentation amplifier for medical purposes," *IEEE J. Solid-State Circtuits*, vol. SC-22, pp. 1163-1168, December 1987.

[4] A. Worapishet, A. Demosthenous, and X. Liu, "A CMOS instrumentation amplifier with 90-dB CMRR at 2-MHz using capacitive neutralization: analysis, design considerations, and implementation," *IEEE Trans. Circuits and Sistems I*, vol. 58, pp. 699-710, April 2011.

[5] R. Wu, K.A.A. Makinwa, and J.H. Huijsing, "A chopper current-feedback instrumentation amplifier with a 1 mHz 1/f noise corner and an AC-coupled ripple reduction loop," *IEEE J. Solid-State Circtuits*, vol. 44, pp. 3232-3243, December 2009.

[6] G.T. Ong and P.K. Chan, "A power-aware chopper-stabilized instrumentation amplifier for resistive wheatstone bridge sensors," *IEEE Trans. Instrumentation and Mesurement*, vol. 63, pp. 2253-2263, September 2014.

[7] C.-H. Chang, S.A. Zahrai, K. Wang, L. Xu, I. Farah, and M. Onabajo, "An analog front-end chip with self-calibrated input impedance for monitoring of biosignals via dry electrode-skin interfaces," *IEEE Trans. Circuits and Sistems I*, vol. 64, pp. 2666-2678, October 2017.

[8] R.G. Carvajal, J. Ramírez-Angulo, A.J. López-Martín, A. Torralba, J.A. Gómez Galán, A. Carlosena, and F. Muñoz-Chavero, "The flipped voltage follower: a useful cell for low-voltage low-power circuit design," *IEEE Trans. Circuits and Sistems I*, vol. 52, pp. 1276-1291, July 2005.

[9] P.R. Gray, P.J. Hurst, H. Lewis, and R.G. Mayer, Analysis and design of analog integrated cicuits, 4th ed., John Wiley and Sons, New York, 2001.