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Título del proyecto:

Design and implementation of an operational amplifier with mosfet technology

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Pamplona, Fecha de defensa

Sinopsis

En este proyecto se ha realizado el diseño de un amplificador mediante el uso de transistores MOSFET. Este amplificador debe cumplir unos requisitos que previamente se han fijado. En primer lugar se decidió el diseño del amplificador y se optó por un OTA Miller. Tras elegir el tipo de amplificador se procede al cálculo manual de las características del amplificador. Después se simula el diseño en el simulador LTSpice para comprobar distintas características del amplificador en este orden:

- Impedancia de salida
- Rango de voltaje de entrada en modo común
- Rango de voltaje de salida en modo común
- Distorsión armónica total
- Voltaje de salida máximo con carga
- Slew rate positivo y negativo
- Comparación con nivel de simulación 49.

Contrastamos los cálculos manuales con los realizados en el simulador y tras comprobar que todo es correcto se realiza el layout. Por último se redactan las conclusiones del proyecto.

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1. Project summary

I propose in this project an optimization procedure for the design of a classical Miller OTA CMOS integrated circuit.

The schematic of a classical Miller OTA integrated circuit implemented with CMOS transistors is illustrated in Fig.1. Its consists of two amplification stages. The first stage is a basic differential pair implemented with PMOs transistors (M1 and M2), which has a single-ended current source as active load implemented with NMOS transistors (M3 and M4). This stage is biased with the current mirror formed with PMOS transistors M7 and M8, whose reference current source is I_{REF}. The second stage is a basic common source amplifier with a NMOS transistor (M6) acting as amplifier and a PMOS transistor (M5) acting as a current source load. This Miller OTA is designed to drive a load capacitor, C_L, of 2.5pF. The second stage has a feedback compensation capacitor, C_c. This Miller OTA is biased with voltage sources $V_{DD} = -V_{SS} = 2.5V$ We use level 2 and level 49 for the SPICE.

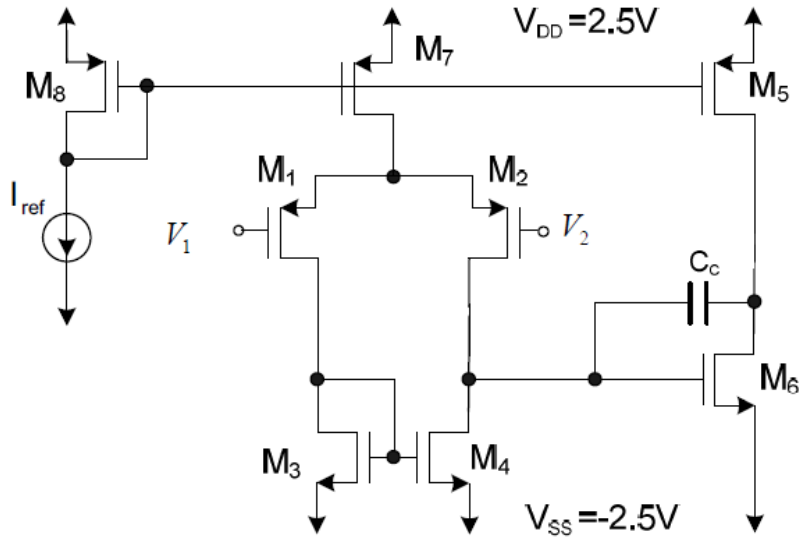

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Figure 1.Schematic of OTA Miller

We use 0.5µm Technology., the device characteristics are shown in the following tables: [1]

Operating Voltage	5,12 V
Substrate Material	P-Type, Bulk or EPI
Drawn Transistor Length	0.6µm
Gate Oxide Thickness	13.5nm
Contact/Via Size	0.5µm
Contacted Gate Pitch	3.9µm
Top Metal Thickness	675nm
Contacted Metal Pitch	
Metal 1	1.5µm
Metal 2,3	1.6µm
Metal Composition	TiN/AlCu/Tin

Table 1.Process Characteristics

N-Channel	**Typical Value**	**Unit**
V_t	0.7	V
I_{dsat}	450	µA/µm
P-Channel	**Typical Value**	**Unit**
V_t	-0.9	V
I_{dsat}	-260	µA/µm

Table 2.Standard Transistors characteristics

2. Design specification

Having selected the technology process, the design of our classical CMOS OTA-Miller integrated circuit starts by defining the design specifications in terms of the performance parameters of interest, such that the open loop voltage gain, *Av*, the phase margin, *PM*, the common-mode rejection ratio, *CMRR*, the slew rate, *SR*, the input common voltage range, *ICMR* and the output impedance, R_{out}. The design specifications required for our circuit are shown in Table I.

SPECIFICATION	REQUIRED
A_V(dB)	>80
PM(°)	>65
SR^+(V/ms)	1.5
SR^-(V/ms)	1.5
ICMR(V)	>3
R_{out}(Ω)	100K
Iref(μA)	10

Table 3.Amplifier specification

3. Steps for the correct design of the Amplifier

For the amplifier design carried out in this thesis these steps have been followed:

- Determine the specifications of the circuit
- Determine circuit features depending on the required specifications. We will calculate transistors dimensions (W/L), currents through them, Miller capacitor capacitance, output impedance... with the available equations.
- Represent LT Spice model of the circuit and check that the calculations made in the previous point are correct. Simulate as much as necessary to calculate gain, GBW, output impedance, input and output ranges, dissipated power, slew-rate...
- Elaborate the circuit layout using Microwind program.
- Post layout analysis.

4. The MOSFET transistor

i. Introduction

The knowledge of MOSFET transistor operation is fundamental for the design of integrated circuits. [2]

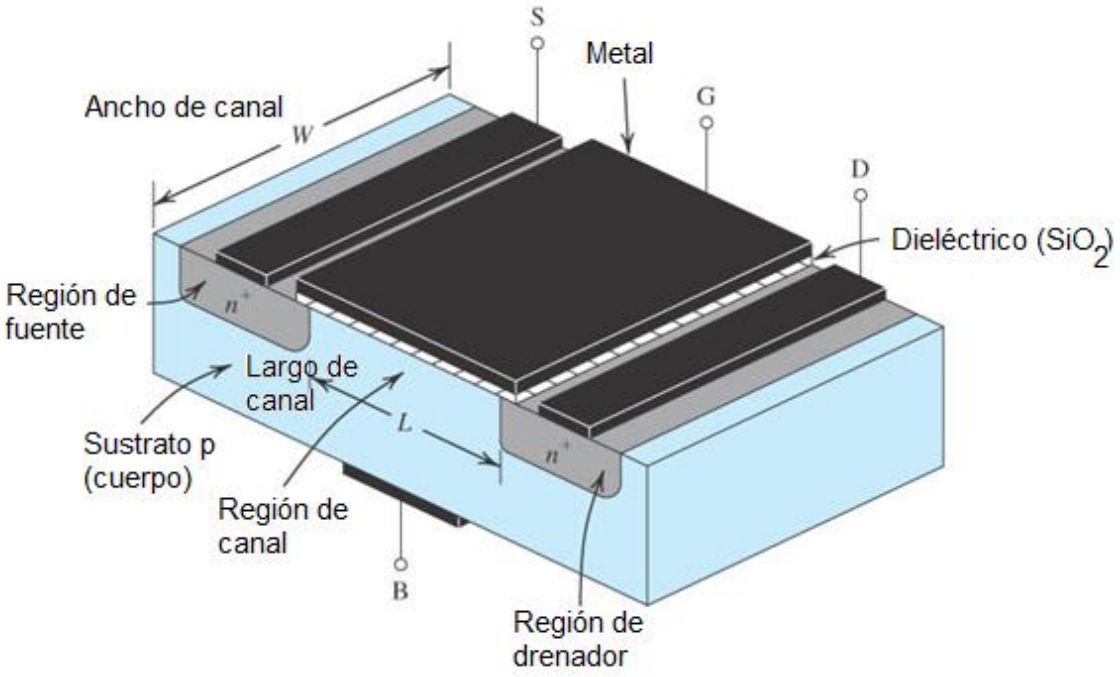


Figure 2. The MOSFET transistor

The MOSFET transistor is a four-terminal device called source (S), gate (G), drain (D), and body (B) terminals [3], the body (or substrate) of the MOSFET is often connected to the source terminal, making it a three-terminal device like other field-effect transistors. Because of these two terminals are normally connected to each other (short-circuited) internally, only three terminals appear in electrical diagrams. The MOSFET transistor is by far the most common transistor in both digital and analog circuits, though the bipolar junction (BJT) transistor was once much more common.

In *enhancement mode* MOSFETs, a voltage drops across the oxide inducing a conduction channel. The channel can contain electrons (called a nMOSFET or nMOS), or holes (called a pMOSFET or pMOS), opposite in type to the substrate, so nMOS is made with a p-type substrate, and pMOS with an n-type substrate.

The electrical features of the MOS transistor depend directly on physical dimensions: the length of the channel (L) is defined as the distance that separates both islands n + (p +), and the width of channel (W) as the dimension perpendicular to this one of the thin oxide.

Applying a tension (positive in case of the transistor MOS type N, or negative in case of the transistor MOS type P) over a certain threshold value between gate and substrate ,

produces a current flowing between drain and source and its value will be dependent on the differential tension V_D-V_S (linear zone of the transistor operation curve) [4].If the Gate-Substrate voltage becomes very big and overcomes a certain saturation value, the current that flows between drain and source takes a value approximately constant, independently of the $V_D - V_S$ tension applied.

ii. Modes of operation

The operation of a MOSFET can be separated into three different modes, depending on the voltages at the terminals [5]. In the following discussion, a simplified algebraic model is used. This model is used in most books about electronics [6] [5]. Modern MOSFET characteristics are much more complex than the algebraic model presented here. [7]. For an enhancement-mode, n-channel MOSFET, the three operational modes are:

Cutoff or weak inversion mode ($V_{GS} < V_{TH}$):

According to the basic threshold model, the transistor is turned off, and there is no conduction between drain and source. A more accurate model considers the effect of thermal energy on the Boltzmann distribution of electron energies which allow some of the more energetic electrons at the source to enter the channel and flow to the drain. This results in a subthreshold current that is an exponential function of gate–source voltage. While the current between drain and source should ideally be zero when the transistor is being used as a turned-off switch, there is a weak-inversion current, sometimes called subthreshold leakage.

In weak inversion the current varies exponentially with V_{GS} given approximately by:

$$I_D \approx I_{D0} e^{\frac{V_{GS}-V_{th}}{nV_T}}$$

Where I_{D0} current at $V_{GS} - V_{th}$, the thermal voltage $V_T = kT/q$ and the slope factor n is given by $n = 1 + C_D/C_{OX}$ with C_D= capacitance of the depletion layer and C_{OX}= capacitance of the oxide layer.

Triode mode ($V_{GS} > V_{TH}$ and $V_{DS} < (V_{GS} - V_{TH})$) [8]:

The transistor is turned on, and a channel has been created which allows current to flow between the drain and the source. The MOSFET operates like a resistor, controlled by the gate voltage relative to both source and drain voltages. The current from drain to source is modeled as:

$$I_D = \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

Where μ_n is the charge-carrier effective mobility, W is the gate width, L is the gate length and C_{OX} is the gate oxide capacitance per unit area. The transition from the exponential subthreshold region to the triode region is not as sharp as the equations suggest.

Saturation mode ($V_{GS} > V_{TH}$ and $V_{DS} \geq (V_{GS} - V_{TH})$) [6]**:**

The switch is turned on, and a channel has been created, which allows current to flow between the drain and source. Since the drain voltage is higher than the gate voltage, the electrons spread out, and conduction is not through a narrow channel but through a broader, two- or three-dimensional current distribution extending away from the interface and deeper in the substrate. The onset of this region is also known as **pinch-off** to indicate the lack of channel region near the drain. The drain current is now weakly dependent upon drain voltage and controlled primarily by the gate–source voltage, and modeled approximately as:

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{th})^2 \left(1 + \lambda (V_{DS} - V_{DSsat})\right).$$

The additional factor involving λ , the channel-length modulation parameter comes out.

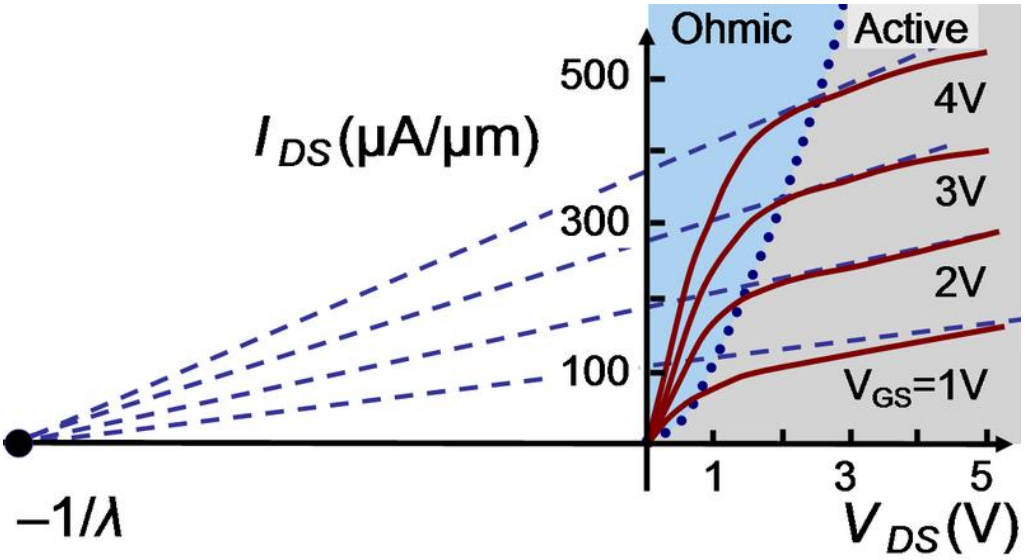


Figure 3. Channel length modulation effect

Channel length modulation (CLM) is an inverted channel region length shortening with increase in drain bias for large drain biases. The result of CLM is an increase in current with drain bias and a reduction of output impedance.
According to this equation, a key design parameter, the MOSFET transconductance is:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{2I_D}{V_{GS} - V_{th}} = \frac{2I_D}{V_{ov}},$$

where the combination $V_{ov} = V_{GS} - V_{th}$ is called the overdrive voltage and accounts for a small discontinuity in I_D which would otherwise appear at the transition between the triode and saturation regions.
Another key design parameter is the MOSFET output resistance r_{out} given by:

$$r_{out} = {}^{1}/_{(\lambda I_D)}$$

r_{out} is the inverse of g_{DS} where $g_{DS} = \frac{\partial I_{DS}}{\partial V_{DS}}$. I_D is the expression in saturation region.

If λ is taken as zero, an infinite output resistance of the device results that leads to unrealistic circuit predictions, particularly in analog circuits.
As the channel length becomes very short, these equations become quite inaccurate. [9]

5. Circuit design

i. Design parameters

The principal parameters that determine the characteristics of the amplifier are:

- Miller capacitor capacity (Cc) which is directly related to GBW.
- Transistors ratio (W/L) directly related to the current through them.
- Transistors parasite capacity which determine if we can use a sigle dominant pole approaching for the amplifier design, or not.
- Current mirror sizes used to bias the amplifier which will establish the current within it.
- Transistors resistances that determine the amplifier output impedance.

With all these parameters we must find a balanced solution that fulfill all the design requirements. This process is explained in section iii) OTA design.

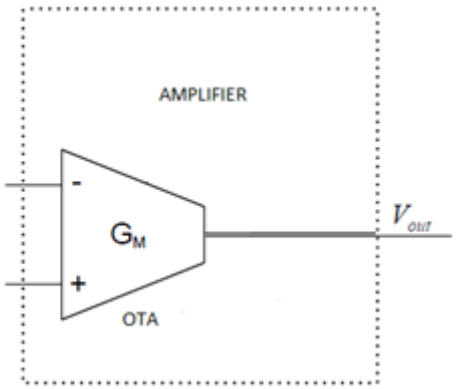


Figure 4. Amplifier symbol

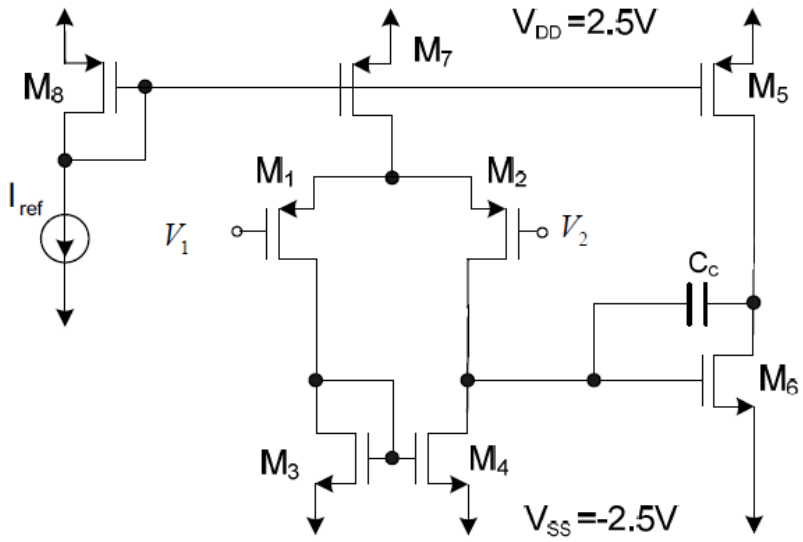


Figure 4. OTA circuit

- First we do the handmade calculations.
- Then we design the amplifier in SPICE with the information obtained in the previous phase. Level 2 and level 49 models will be used to compare the behavior differences in the circuit.
- Finally, design will be made using Layout.
- Analysis post Layout.

ii. OTA block

The operational transconductance amplifier, according to its architecture, has following analogical basic blocks:

- **Bias circuit:** In this block, the current mirrors are used. Its working principle is based on the transistor working in the saturation region with a high output resistance, in such a way that for two same size transistors the Gate-Source current would be the same as well. A property of the current mirrors is their low input resistance. To assure a proper functioning of the current mirror, that is to say, a correct current copy, it is necessary to take into account that the output resistance must be much bigger than the load resistance, so as to ensure that transistors work in the saturation region.

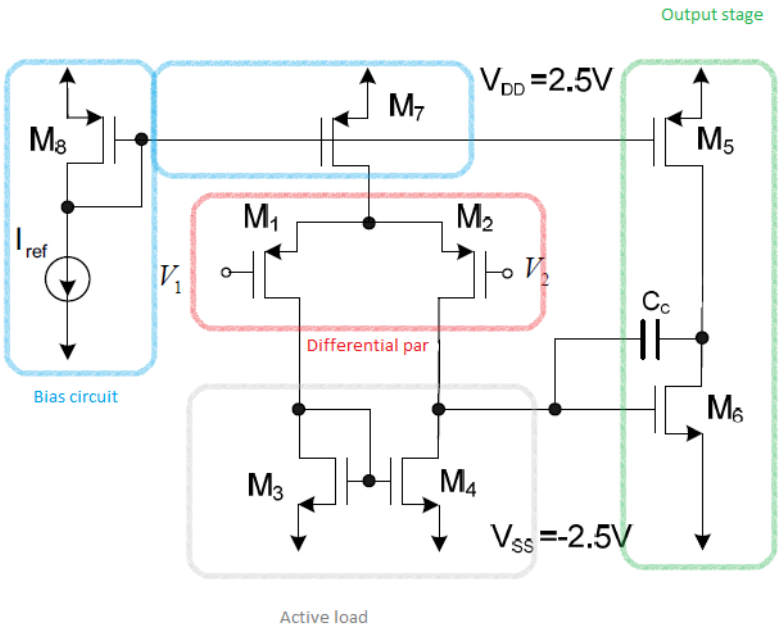


Figure 5.Blocks of the OTA

- **Differential par**: analogical basic block to which has a differential input instead of a single input signal. For its design it is necessary that both transistors of the differential couple stay in the saturation region.

- **Active Load:** analogical block entrusted to assure the saturation of the differential par and to determine the maximum possible variation of the analogical block output.
- **Output stage:** block that serves to amplify the differential input signal. The transistors must be used in saturation mode.

iii. OTA design

The CMOS OTA is shown in figure 7. [10] [11] It is composed of two stages, the first of them is a differential stage with active load whose input transistor are PMOS type, M1 and M2, being the load a simple current mirror built up by M3 and M4 transistors. The second stage is a CMOS inverter where M6 transistor is providing gain and M5 transistor used for M6 bias, and at the same time, as load. This stage output is connected to its input, differential pair output, within a compensation capacitor, Cc. This capacitor behaves as a Miller capacity; therefore it is called Miller OTA. The gain of the first stage is well known and it is given by:

$$|A_{v1}| = \frac{g_{m1}}{g_{o24}} \quad (1)$$

Where $g_{o24} = g_{o2} + g_{o4} = 1/r_{o2} + 1/r_{o4} = {}^{1}/_{(\lambda * I_{D2})} + {}^{1}/_{(\lambda * I_{D4})}$

The gain of the second stage is:

$$|A_{v2}| = \frac{g_{m6}}{G_L} \quad (2)$$

Where $G_L = g_L + g_{o5} + g_{o6} = 1/R_L + 1/r_{o5} + 1/r_{o6}$ is de conductance of last stage.

The total gain of stage at low frequency is the product of the gains of the previous stages, expressions (1) and (2), whose result is:

$$|A_{vo}| = A_{v1}.A_{v2} = \left(\frac{g_{m1}}{g_{o24}}\right)\left(\frac{g_{m6}}{G_L}\right) \quad (3)$$

Small signal equivalent OTA circuit:

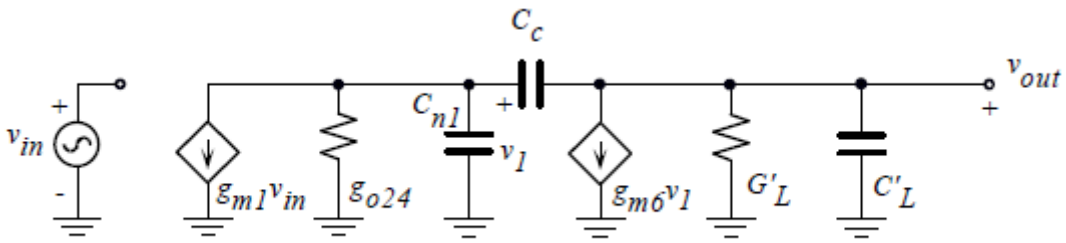


Figure 6.Miller-OTA small signal equivalent

From this circuit we can calculate the equations that characterize the OTA

The position of the dominant pole comes given by [11]:

$$f_d = \frac{g_{o24}}{2\pi A_{v2} C_c} \quad (4)$$

The position of the not dominant pole comes given by:

$$f_{nd} = \frac{gm_6}{2\pi C_L} \frac{1}{1+\frac{C_{n1}}{C_L}+\frac{C_{n1}}{C_c}} \quad (5)$$

The Gain Bandwidth product is:

$$GBW = \frac{gm_1}{2\pi(Cn_5+Cc)} \quad (6)$$

The phase margin is:

$$PM = 90 - arctg\frac{GBW}{f_{nd}} \quad (7)$$

iv. Calculation of I_{D6} and C_c

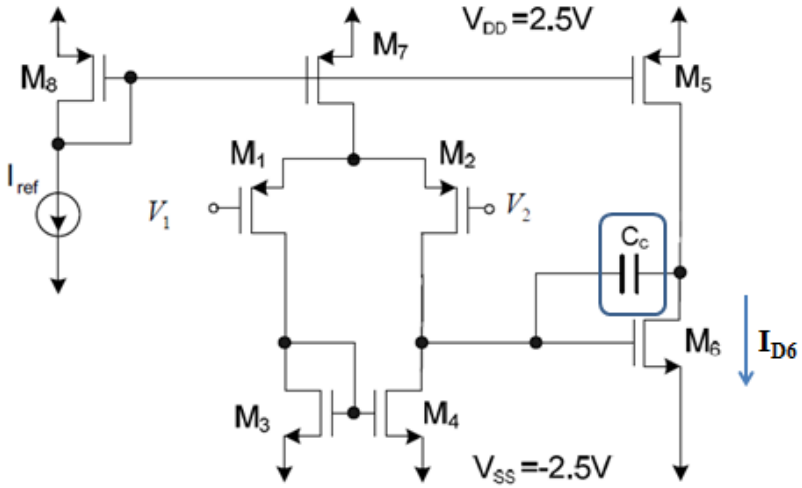


Figure 7.Cc location inside the circuit

The first thing that we must do is to establish the value of I_{D6} and Cc, for it we design a circuit in spice using the following equations [6]:

$$f_{nd} = \frac{gm_6}{2\pi C_L} \frac{1}{1+\frac{C_{n1}}{C_L}+\frac{C_{n1}}{C_c}} \quad (5)$$

$$C_{gs} = \frac{2}{3} C_{0X} + CGS0 * W \quad (8)$$

$$C_{OX} = C_{ox} * W * L_{eff} \quad (9)$$

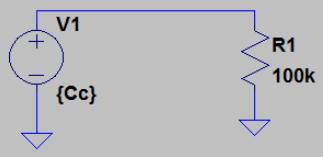
$$C_{ox} = (\varepsilon_0 * \frac{\varepsilon_{ox}}{TOX}) \quad (10)$$

$$L_{eff} = L - 2LD \quad (11)$$

$$gm_n = \frac{2*Id_n}{Vgs_n - Vt} \quad (12)$$

$$\left(\frac{W}{L}\right)_n = \frac{gm_n}{K_n*(Vgs_n - Vt)} \quad (13)$$

To assure the stability of the system, the frequency of the not dominant pole (f_{nd}) must have a value at least three times the GBW value. [12]




```
.op      .step param id6 1u 100u 0.5u
.PARAM GBW=10MEG cl=2.5p L=3u delta6=0.2 CGSO=300p TOX=14n LD=0.1p kn=112.2u
.PARAM cc={cn1/(gm6/(3*GBW*2*3.14*cl)-1-cn1/cl)}
.PARAM gm6={2*Id6/delta6}
.PARAM W6={gm6/(kn*delta6)*L}
.PARAM cn1={2/3*COX+CGSO*W6}
.PARAM COX={W6*Leff*COX1}
.PARAM Leff={L-2*LD}
.PARAM COX1={812u*42.5n/TOX}
```

Circuit for calculating I_{D6} and C_c

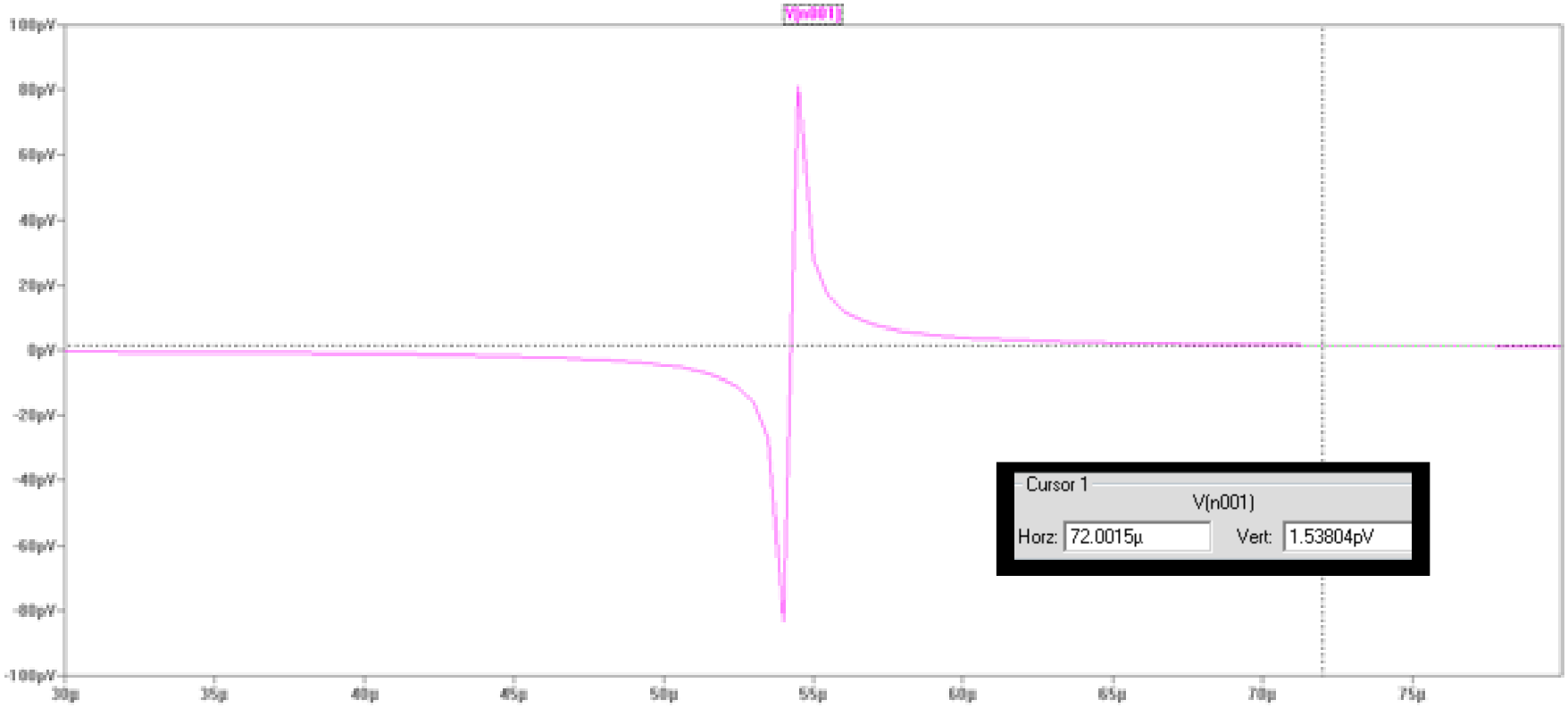


Figure 8. Calculation I_{D6} and C_c

It is observed when the Cc begins to become stable and take a value for Cc and Id6. In this case it is taken Cc=1.53pF , I_{D6}=72µA

v. Transistors dimensions calculation

In this paragraph the OTA designing process is described, Its schematic graph is shown in the next figure, and the methodology used for the calculation of OTA transistor dimensions is explained.

The first step is drawing the circuit small signal analysis to design the symmetrical OTA.

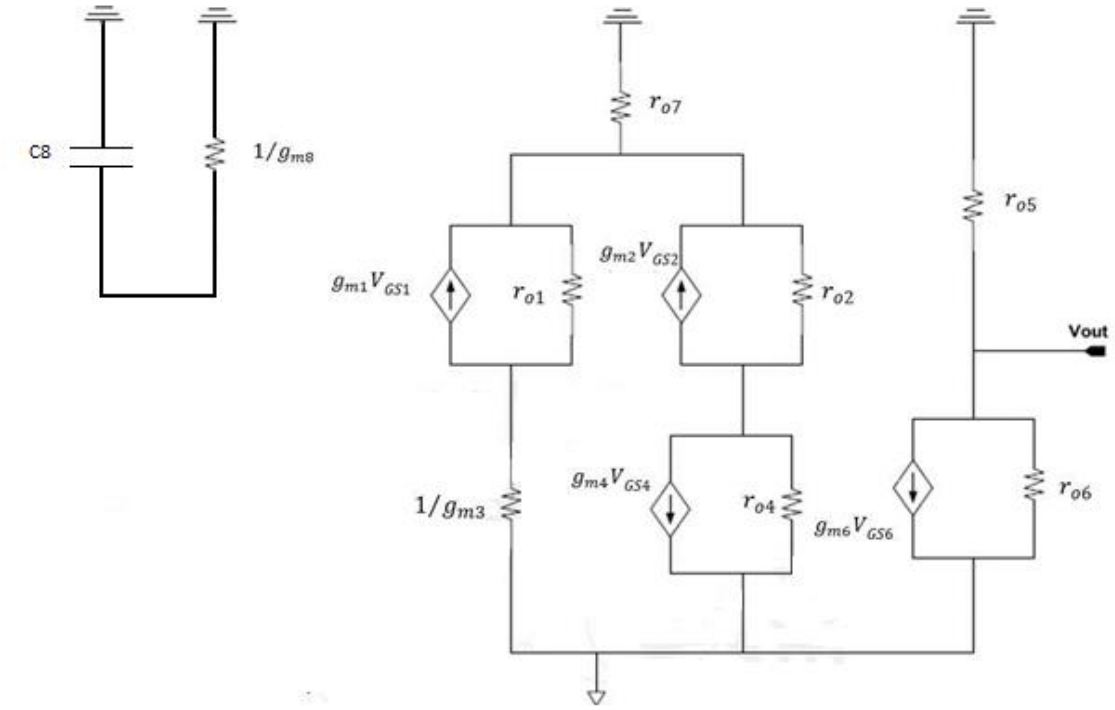


Figure 9.Small-signal circuit equivalent

Once calculated the value of the current I_{D6} and of Miller's capacitor ,Cc, already we can proceed to calculate all the rest design parameters of the amplifier. For it we are going to use the following equations:

$$gm_n = \frac{2 * Id_n}{Vgs_n - Vt}$$

$$\left(\frac{W}{L}\right)_n = \frac{gm_n}{K_n * (Vgs_n - Vt)}$$

$$\frac{Id_n}{Id_m} = \frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_m}$$

We take L=0.5 µm,(the minimum length possible in this technology). Therefore the amplifier size will be minimize as much as possible

We take (Vgs-Vt) =0.5V for the transistors that form a part of mirrors of current and 0.2V for the others. [6]

We take $K_n = 112 * 10^{-6}$ and $K_p = 49 * 10^{-6}$, these values are provided by the models of spice. The units of the conductance (gm_n) are Siemens[S]=[Ω^{-1}].

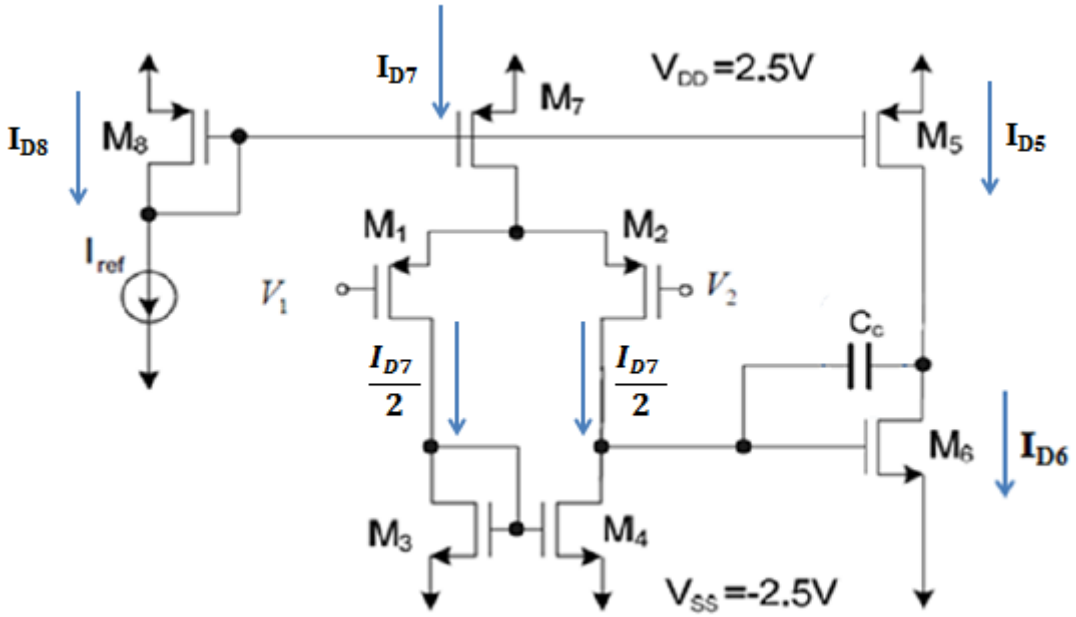


Figure 10.Details of the currents that flow the circuit and their values

We proceed to calculate several transistors in the circuit's dimensions , gm and currents.

- **M_5:**

$$gm_5 = \frac{2 * Id_5}{Vgs_5 - Vt} \Rightarrow gm_5 = \frac{2 * 72 * 10^{-6}}{0.5} = 288 * 10^{-6}[S]$$

$$\left(\frac{W}{L}\right)_5 = \frac{gm_5}{K_p * (Vgs_5 - Vt)} = \frac{2 * Id_5}{K_p * (Vgs_5 - Vt)^2} = \frac{2 * 72 * 10^{-6}}{49 * 10^{-6} * 0.5^2} \Rightarrow \left(\frac{W}{L}\right)_5 = 11.75$$

- **M_6:**

$$gm_6 = \frac{2 * Id_6}{Vgs_6 - Vt} \Rightarrow gm_6 = \frac{2 * 72 * 10^{-6}}{0.2} = 720 * 10^{-6}[S]$$

$$\left(\frac{W}{L}\right)_6 = \frac{gm_6}{K_n * (Vgs_6 - Vt)} = \frac{2 * Id_6}{K_n * (Vgs_6 - Vt)^2} = \frac{2 * 72 * 10^{-6}}{112 * 10^{-6} * 0.2^2} \Rightarrow \left(\frac{W}{L}\right)_6 = 32.14$$

- **M_1 and M_2:**

$$GBW = \frac{gm_1}{2\pi(Cn_5 + Cc)} \Rightarrow gm_1 = GBW * 2\pi(Cn_5 + Cc)$$

$$gm_1 = 10 * 10^6 * 2\pi * 1.53 * 10^{-12} = 9.61 * 10^{-5}[S]$$

$$gm_1 = \frac{2 * Id_1}{Vgs_1 - Vt} \Rightarrow Id_1 = \frac{gm_1 * (Vgs_1 - Vt)}{2}$$

$$Id_1 = \frac{9.61 * 10^{-5} * 0.2}{2} = 9.61 * 10^{-6}[A]$$

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \frac{gm_1}{K_p * (Vgs_1 - Vt)} = \frac{9.61 * 10^{-5}}{49 * 10^{-6} * 0.2} = 9.8$$

The size of M_1 and M_2 is the same due to the fact that the intensity that pass within them is the same and $(Vgs_1 - Vt)$ is equal that $(Vgs_2 - Vt)$.

- **M_7:**

We know $Id_7 = 2 * Id_1 = 19.22 * 10^{-6}[A]$

$$\frac{Id_7}{Id_5} = \frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_5} \Rightarrow \left(\frac{W}{L}\right)_7 = \frac{Id_7}{Id_5} * \left(\frac{W}{L}\right)_5 = 3.137$$

$$gm_7 = \frac{2 * Id_7}{Vgs_7 - Vt} = \frac{2 * 19.22 * 10^{-6}}{0.5} = 7.688 * 10^{-5}[S]$$

- **M_3 and M_4:**

$$\left(\frac{W}{L}\right)_3 = \frac{gm_3}{K_n * (Vgs_3 - Vt)} = \frac{2 * Id_3}{K_n * (Vgs_3 - Vt)^2}$$
$$= \frac{2 * 9.61 * 10^{-6}}{112 * 10^{-6} * 0.2^2} \Rightarrow \left(\frac{W}{L}\right)_6 = 4.29$$

$$gm_3 = \frac{2 * Id_3}{Vgs_3 - Vt} = \frac{2 * 9.61 * 10^{-6}}{0.2} = 9.61 * 10^{-5}[S]$$

The size of M_3 and M_4 is the same due to the fact that the intensity that crosses them is the same and $(Vgs_3 - Vt)$ is equal that $(Vgs_4 - Vt)$.

- **M_8:**

$$\frac{Id_5}{Id_8} = \frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_8} \Rightarrow \left(\frac{W}{L}\right)_8 = \frac{Id_8}{Id_5} * \left(\frac{W}{L}\right)_5 = \frac{10 * 10^{-6}}{72 * 10^{-6}} * 11.75 = 1.632$$

$$gm_8 = \frac{2 * Id_8}{Vgs_8 - Vt} = \frac{2 * 10 * 10^{-6}}{0.5} = 4 * 10^{-5}[S]$$

The characteristics of the transistors remain reflected in the following table:

Nº trt	I[µA]	gm[S]	K[A/V^2]	(Vgs-Vt)[V]	W[µm]	L[µm]
1	9.61	96.1	49	0.2	4.90	0.5
2	9.61	96.1	49	0.2	4.90	0.5
3	9.61	96.1	112.2	0.2	2.145	0.5
4	9.61	96.1	112.2	0.2	2.145	0.5
5	72	288	49	0.5	5.877	0.5
6	72	720	112.2	0.2	16.07	0.5
7	19.22	76.88	49	0.5	1.568	0.5
8	10	40	49	0.5	0.8167	0.5

Table 4.Feautres of transistors

Proposing such a small channel length undesired effects can appear. These effects are consequence of channel length modulation and they are: drain-induced barrier lowering (which lowers the threshold voltage, increasing the current and decreasing the output resistance), velocity saturation (which tends to limit the increase in channel current with drain voltage, thereby increasing the output resistance) and ballistic transport (which modifies the collection of current by the drain, and modifies drain-induced barrier lowering so as to increase supply of carriers to the pinch-off region, increasing the current and decreasing the output resistance)

Due to this transistors length are increased in order to avoid CLM effects. Length is increased to 3um. Final transistors characteristics appear in the following table:

Nº trt	I[µA]	gm[S]	K[A/V^2]	(Vgs-Vt)[V]	W[µm]	L[µm]
1	9.61	96.1	49	0.2	29.4	3
2	9.61	96.1	49	0.2	29.4	3
3	9.61	96.1	112.2	0.2	12.87	3
4	9.61	96.1	112.2	0.2	12.87	3
5	72	288	49	0.5	35.262	3
6	72	720	112.2	0.2	96.42	3
7	19.22	76.88	49	0.5	9.408	3
8	10	40	49	0.5	4.9002	3

Table5.Features of transistor with L optimized

6. Implementation with the program LTspice

Once we have designed transistors to implement the complete circuit in LTSpice. In the next figure we can see the models of transistor for level 3 in LTspice

```
.model n_05 nmos (LEVEL=3 KP=112.2e-6 VT0=0.67
+CGBO=1.0e-10 CGDO=3.0e-10 CGSO=3.0e-10 CJ=5.6e-4
+CJSW=3.147e-10 DELTA=5.054 ETA=3.7e-6 GAMMA=0.6 KAPPA=0.3
+LD=1e-13 MJ=0.56 MJSW=0.1977 NFS=1e12 NSUB=1e17 PB=1
+PHI=0.7 RSH=7.5e-3 THETA=0.101 TOX=1.4e-8 TPG=1 U0=550 XJ=0.2e-6
+VMAX=1.44e5 )

.model p_05 pmos ( LEVEL=3 KP=49e-6 VT0=-0.97
+CGBO=1e-10 CGDO=2.4e-10 CGSO=2.4e-10 CJ=7.2e-4
+CJSW=2.9e-10 DELTA=0.11 ETA=0 GAMMA=0.62 KAPPA=30.1
+LD=5e-13 MJ=0.47 MJSW=0.31 NFS=1e12 NSUB=1e17 PB=1
+PHI=0.7 RSH=33.96 THETA=0.16 TOX=1.4e-8 TPG=-1 U0=135 XJ=0.2e-6
+VMAX=1e6)
```

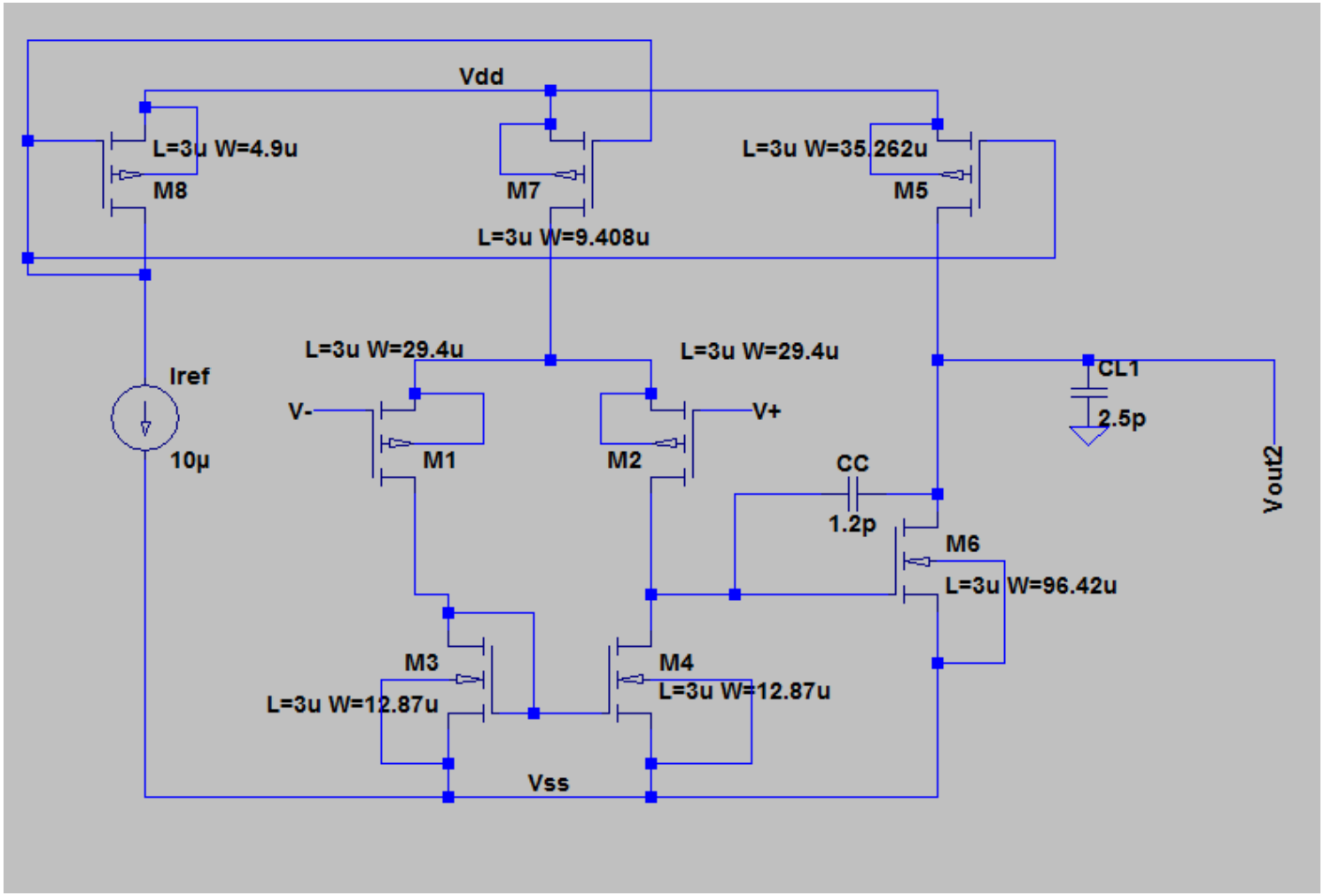


Figure 11.Circuit in LTSpice

Detail of the power circuit:

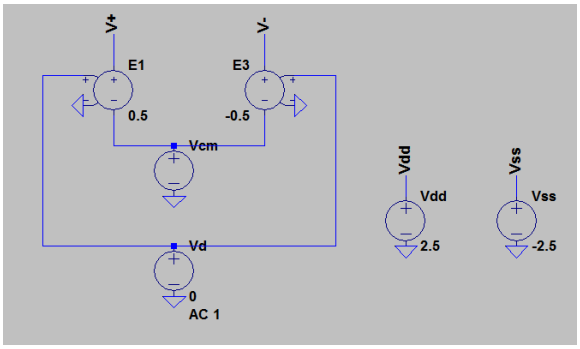


Figure 12.Detail of bias circuit

We carry out a frequency sweep to see if we fulfill the conditions of GBW and of phase margin of the design:

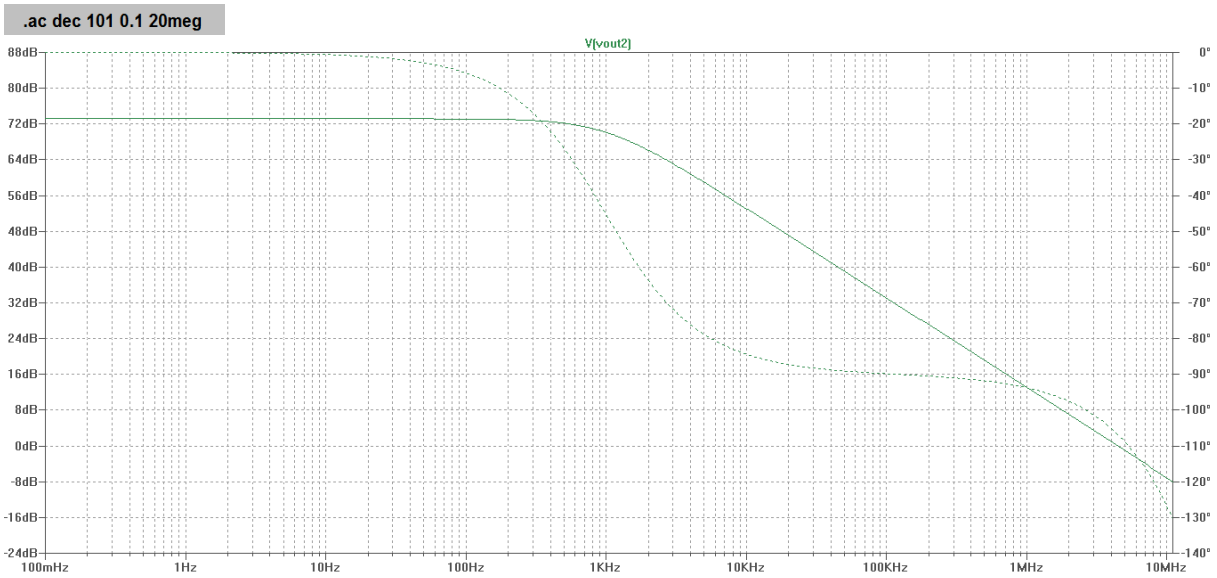


Figure 13. GBW calculation

The conditions are not fulfilled since the phase margin is lower than 65º for what the system is not stable, the GBW is also lower than 10MHz and the gain is not too high.

The first step should be making zero the possible offset voltage. For this purpose, we do a sweep of the source [V_{offset}] and see when the output is zero for a void input signal.

The device mismatches inevitably present in the input stage produce an input offset voltage. Because of the fact that these mismatches are random, the resulting offset voltage is referred to as random offset. This is to distinguish it from another type of input offset voltage that can be present even if all the appropriate devices are perfectly matched. This predictable or systematic offset can be minimized by a careful design. Although it occurs also in BJT op amps, it is usually much more pronounced in CMOS op amps because their gain per stage is rather low.

To see how systematic offset can occur in the circuit of Figure 11, let the two input terminals be grounded. If the input stage is perfectly balanced, then the voltage appearing at drain of M_4 will be equal to that at the drain of M_3, wich is $(-V_{SS} + V_{GS4})$. Now this is also the voltage that is fed to the gate of M_6. In other words, a voltage equal to V_{GS4} appears between gate an source of M_6. Therefore drain current of M_6, I_6, will be related to the drain current of M_4, which is equal to $I/2$, by the relationship

$$I_6 = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_4}(I/2)$$

In order to avoid offset voltage to appear at the output, this current must be exactly equal to the current supplied by M_5. The latter current is related to the current I of the parallel transistor M_7 by

$$I_5 = \frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_7} I$$

Now, the condition for making $I_6 = I_5$ can be found from previous equations as

$$\frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_4} = 2\frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_7}$$

If this condition is not met, a systematic offset will result. From the specification of the device geometries, we can verify if this condition is satisfied, and, therefore, the op amp analyzed in this project should not exhibit a systematic input offset voltage.

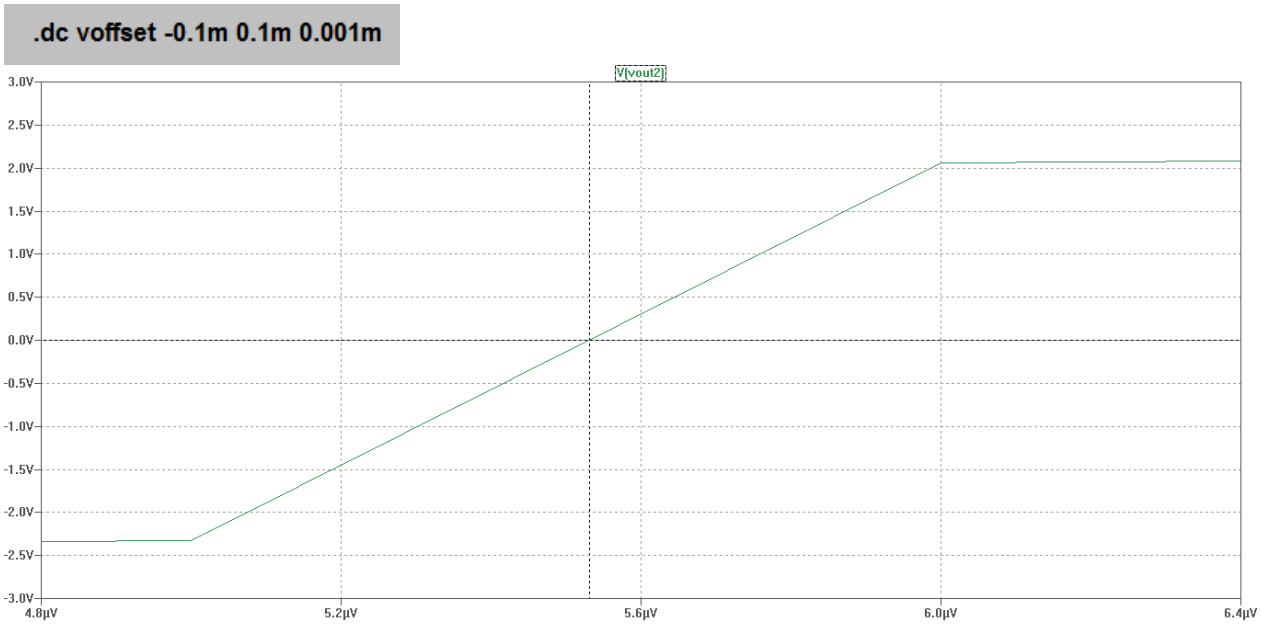
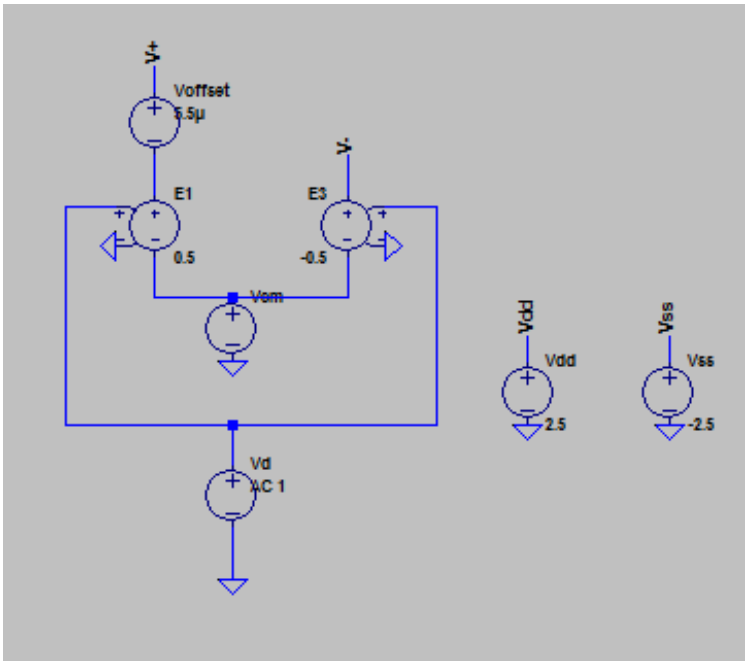


Figure 14.Offset voltage calculation

We should put an offset voltage about 5.5µV. Now the power circuit is:



After doing it we see as the graph improves considerably, but yet we don't obtain a GBW of 10MHz.

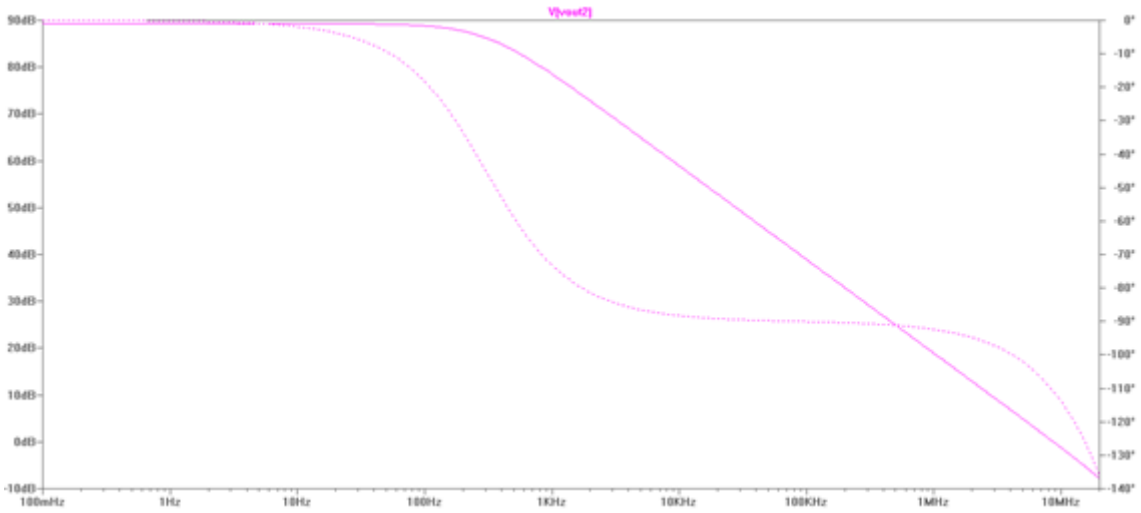


Figure 15.New GBW with offset voltage

Now we must change some another parameters of the circuit to fulfill with the requirements of the GBW. [13]

$$GBW = \frac{gm_1}{2\pi(Cn_5 + Cc)}$$

$$gm_1 = \frac{2 * Id_1}{Vgs_1 - Vt}$$

$$\left(\frac{W}{L}\right)_1 = \frac{gm_1}{K_1 * (Vgs_1 - Vt)}$$

After these equations we observe that to change the GBW we can change gm1 or the values of the capacitors. We can change the size of the transistors 1 and 2 to increase the GBW or change the capacity of the capacitor Cc.

- **Change of Cc size**

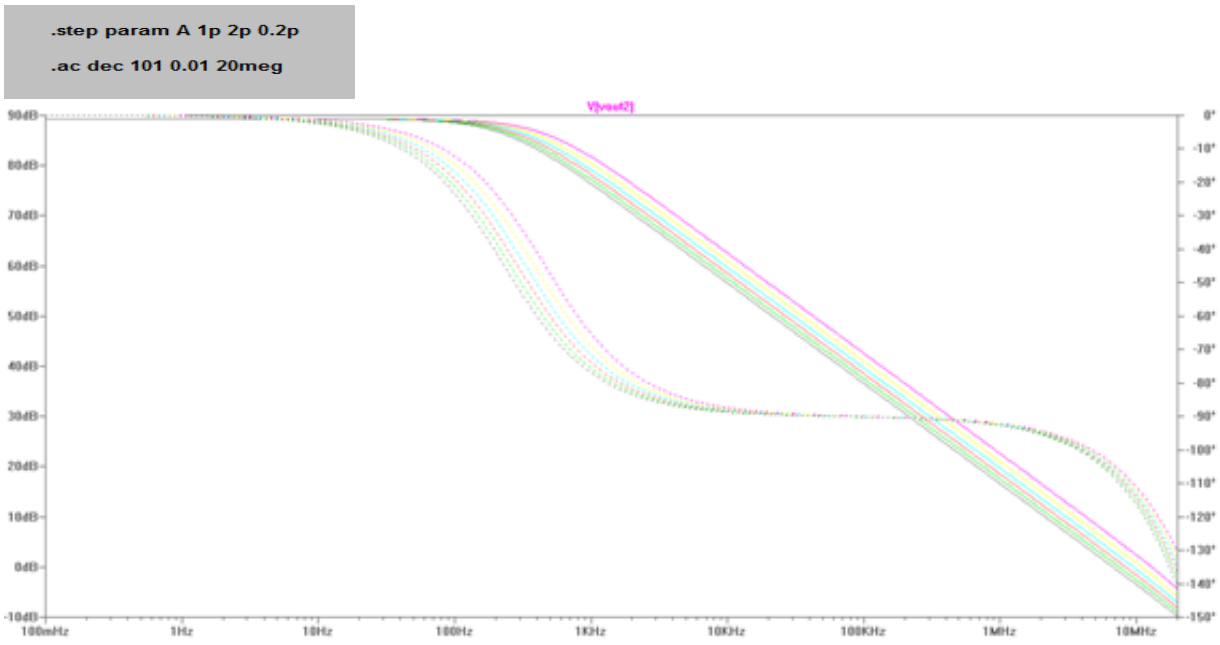


Figure 16.GBW with different Cc sizes

Choosing Cc's value of 1.2pF we obtain a GBW higher than 10MHz and one stable phase margin, therefore this one is the ideal configuration of the amplifier.

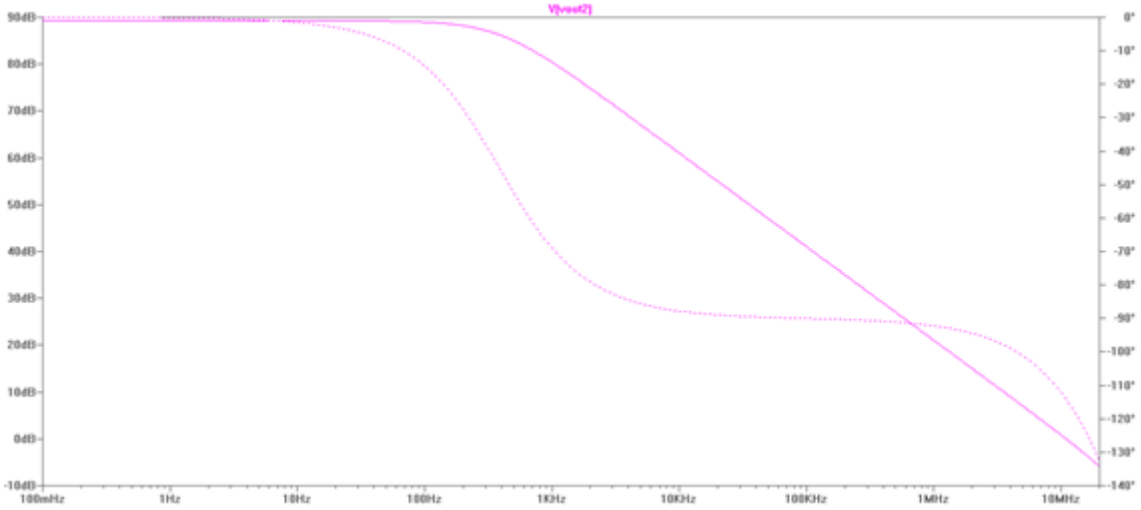


Figure 17.GBW with new Cc size

- **Change of transistor 1 and 2 size**

  We must increase the size of the transistors 1 and 2 to increase the GBW, for it, we do a frequency sweep with different transistor sizes.

  The initial size of the transistors is 29.4 µm, seeing the graphs we conclude that the ideal size of the trasistors is 30µm since we obtain a major gain that 90 dB.

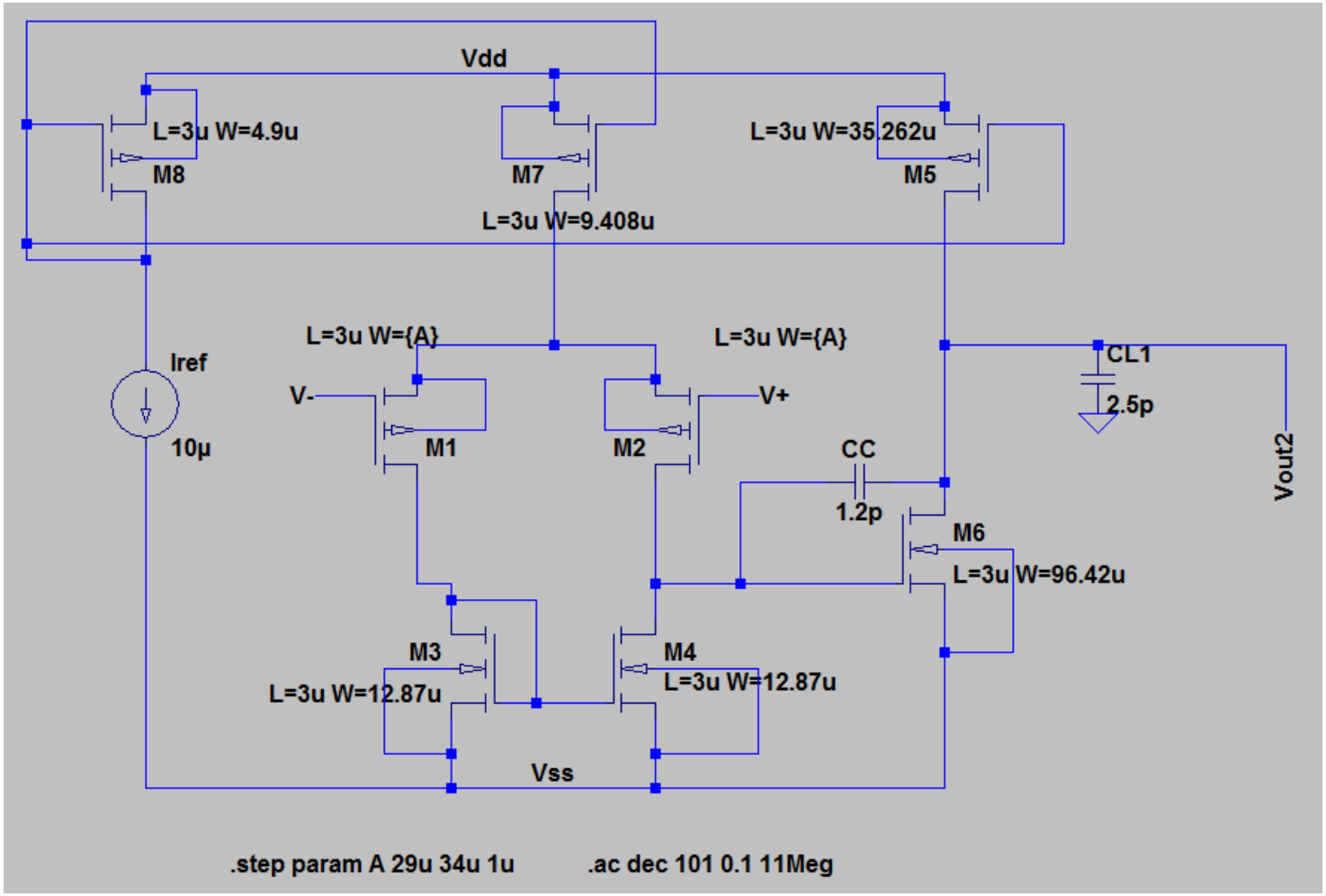


Figure 18. Parameterization of the transistors 1 and 2

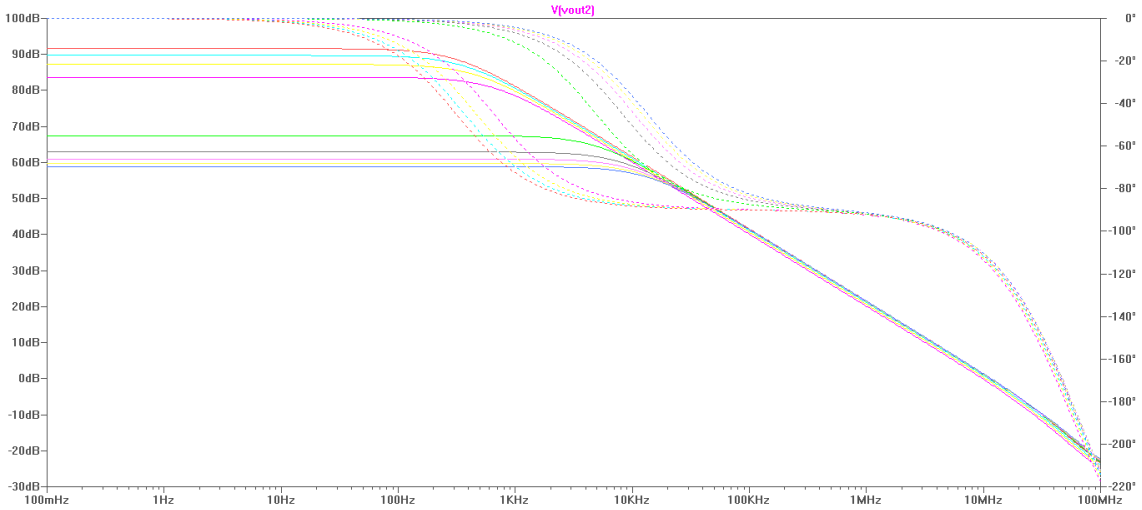


Figure 19.GBW with different trt 1 and 2 sizes

i. Output impedance

Doing the necessary calculations we obtain that :

$$R_o = r_{o5} \,//\, r_{o6}$$

We know that $r_{oi} = {}^{1}/_{\lambda_i I_{Di}}$ so

$$R_o = \left({}^{1}/_{\lambda_p I_{D5}}\right) // \left({}^{1}/_{\lambda_n I_{D6}}\right) = {}^{1}/_{(\lambda_p + \lambda_n) I_{D5}}$$

$$R_o = {}^{1}/_{(73.5\mu A * 0.09)} = 307214\Omega = 0.3M\Omega$$

This is the theoretical result, the values of $\lambda_p \; and \; \lambda_n$ are normalized in

$$\lambda_p = 0.04 \; and \; \lambda_n = 0.05$$

In LTspice we can calculate the Ro in two different forms. The first option is to do a DC transfer and we obtain directly the Ro like it appears in the following figure

.tf V(vout2) vd

```
        --- Transfer Function ---

Transfer_function:              29098.7         transfer
vd#Input_impedance:             1e+020          impedance
output impedance at V(vout2):                   312322          impedance
```

Figure 20.Detail of Rout and Gain

In the figure we can see that the output impedance has a value of $0.312M\Omega$ and also that the linear gain has a value of 29098.7 that in $dB = 20 \log_{10}(29098.7) = 89.9dB$, approximately like in the Bode diagram represented previously.

Other option is doing a .op and see the values of g_{dsi}. We know that:

$$r_{oi} = {}^{1}/_{g_{dsi}}$$

$$R_o = {}^{1}/_{g_{ds5}} // {}^{1}/_{g_{ds6}} = {}^{1}/_{(g_{ds5} + g_{ds6})} = 0.312M\Omega$$

--- MOSFET Transistors ---

Name:	m:m8:2	m:m7:2	m:m5:2	m:m2:2	m:m1:2
Model:	p_05	p_05	p_05	p_05	p_05
Id:	-1.00e-05	-1.94e-05	-7.35e-05	-9.66e-06	-9.72e-06
Vgs:	-1.45e+00	-1.45e+00	-1.45e+00	-1.10e+00	-1.10e+00
Vds:	-1.45e+00	-1.40e+00	-2.71e+00	-2.78e+00	-2.67e+00
Vbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Vth:	-9.40e-01	-9.37e-01	-9.35e-01	-9.35e-01	-9.35e-01
Vdsat:	-4.83e-01	-4.87e-01	-4.91e-01	-1.90e-01	-1.90e-01
Gm:	3.37e-05	6.50e-05	2.45e-04	8.62e-05	8.64e-05
Gds:	2.93e-09	5.72e-09	2.18e-08	1.24e-09	1.25e-09
Gmb:	8.40e-06	1.59e-05	5.91e-05	2.19e-05	2.20e-05
Cbd:	2.84e-15	4.27e-15	1.03e-14	8.70e-15	8.81e-15
Cbs:	3.99e-15	6.04e-15	1.78e-14	1.52e-14	1.52e-14
Cgsov:	1.97e-16	3.76e-16	1.41e-15	1.18e-15	1.18e-15
Cgdov:	1.97e-16	3.76e-16	1.41e-15	1.18e-15	1.18e-15
Cgbov:	5.00e-17	5.00e-17	5.00e-17	5.00e-17	5.00e-17
Cgs:	6.74e-16	1.29e-15	4.83e-15	4.03e-15	4.03e-15
Cgd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgb:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00

Name:	m:m6:1	m:m3:1	m:m4:1
Model:	n_05	n_05	n_05
Id:	7.35e-05	9.72e-06	9.66e-06
Vgs:	8.22e-01	9.36e-01	9.36e-01
Vds:	2.29e+00	9.36e-01	8.22e-01
Vbs:	0.00e+00	0.00e+00	0.00e+00
Vth:	6.51e-01	7.47e-01	7.47e-01
Vdsat:	1.76e-01	1.72e-01	1.72e-01
Gm:	6.29e-04	7.59e-05	7.53e-05
Gds:	3.18e-06	5.59e-07	5.77e-07
Gmb:	1.67e-04	3.05e-05	3.03e-05
Cbd:	2.33e-14	5.33e-15	5.45e-15
Cbs:	3.90e-14	6.84e-15	6.84e-15
Cgsov:	4.82e-15	6.44e-16	6.44e-16
Cgdov:	4.82e-15	6.44e-16	6.44e-16
Cgbov:	5.00e-17	5.00e-17	5.00e-17
Cgs:	1.32e-14	1.76e-15	1.76e-15
Cgd:	0.00e+00	0.00e+00	0.00e+00
Cgb:	0.00e+00	0.00e+00	0.00e+00

Figure 21.Detail of LTSpice file

We can verify that the three values of R_o, the theoretical one and both practical ones have similar values.

ii. Input common voltage range

In this section for easier notation we will call $\Delta_n = V_{GSn} - V_t$.

Highest input common voltage range value must assure that the transistor 7 should remain in saturation; that is to say, the voltage through the transistor 7, V_{SD7}, must not fall down below $|\Delta_7|$. In an equivalent way, the voltage in transistor 7 drain should not be higher than $V_{DD} - |\Delta_7|$

Lowest input common voltage range value has to be big enough to support transistors 1 and 2 in saturation mode, therefore this value must not be less than drain voltage in transistor 1.

Upper limit:

In order to kept transistor 7 in saturation mode it is necessary to verify $V_{DS7} \leq \Delta_7$.

$$V_{cm} = V_{G1} \; and \; (V_{GS1} = cte) so \; if \; V_{cm} \uparrow\uparrow \rightarrow V_{G1} \uparrow\uparrow \; and \; V_{S1} \uparrow\uparrow$$

$$V_{DS7} \leq \Delta_7 \rightarrow V_{D7} \leq \Delta_7 + V_{S7} \qquad \text{(a)}$$

We know $V_{D7} = V_{cm} - V_{GS1}$ and $V_{S7} = V_{DD}$

So we can write (a) as: $V_{cm} - V_{GS1} \leq \Delta_7 + V_{DD} \rightarrow V_{cm} \leq \Delta_7 + V_{DD} + V_{GS1}$

$$Vcmi|_{max} = V_{DD} - |\Delta_7| - |\Delta_1| - Vt_1 = 2.5 - 0.5 - 0.2 - 0.97 = 0.83V$$

Lower limit:

$$(V_{GS3} = cte) and \; V_{S3} = V_{SS} = cte = -2.5V \rightarrow V_{G3} = cte = V_{D3} = V_{D1}$$

$$V_{DS1} \leq V_{GS1} - V_{tp} \rightarrow V_{G1} \geq V_{SS} + V_{GS1} + V_{tp}$$

$$Vcmi|_{min} = Vss + |\Delta_3| + Vt_n - |Vt_p| = -2.5 + 0.2 + 0.67 - 0.97 = -2.6V$$

We verify the results in LTspice and see that they are correct:

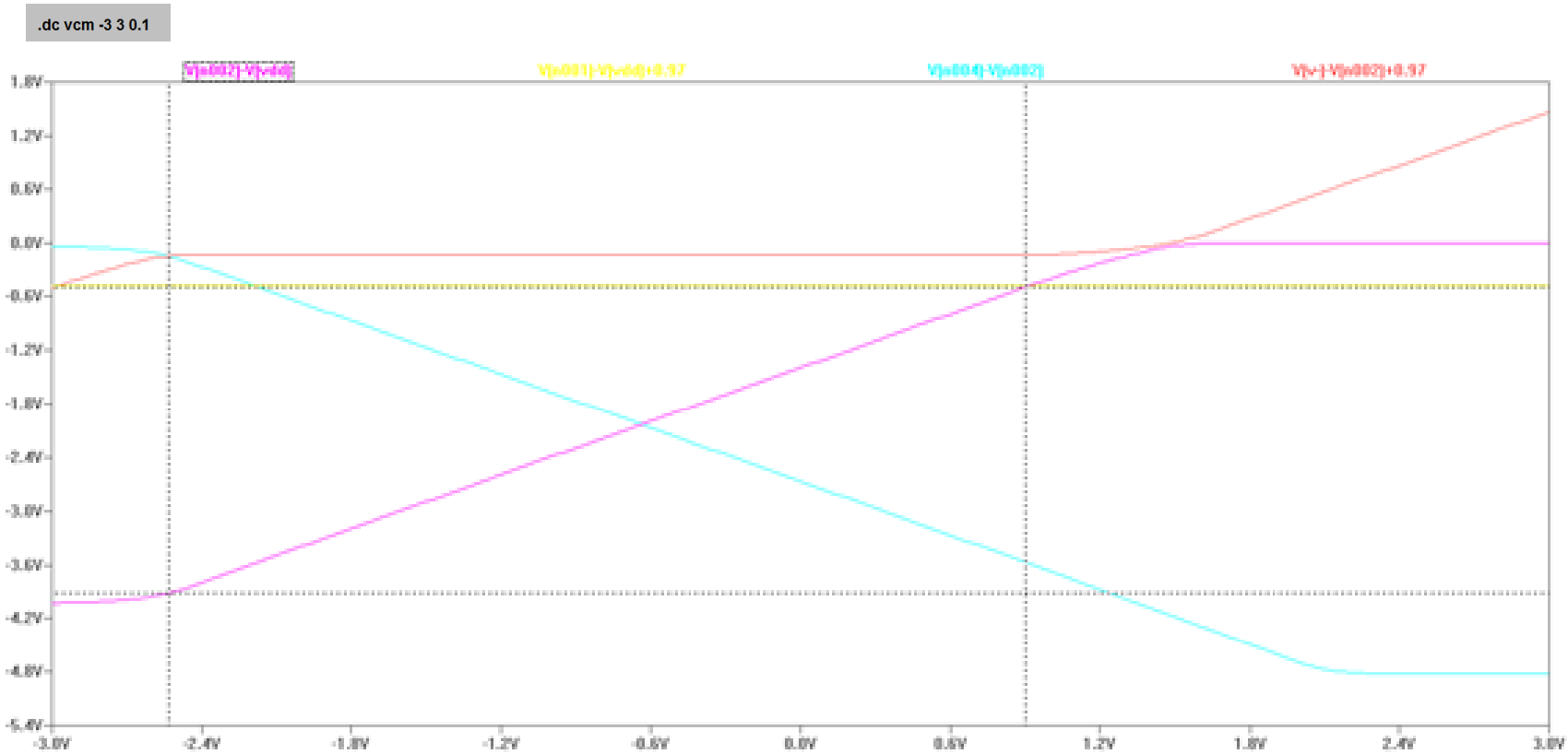


Figure 22.input common voltage range

The values obtained with LTspice are very near to the theoretical ones.

$$-2.5 < V_{cm} < 0.766$$

iii. Output common voltage range

Upper limit: This limit is fixed by trt 5

$V_o = V_{D5} = V_{D6}$

$V_{DS5} \leq V_{GS5} - V_{tp} \rightarrow V_{D5} \leq \Delta_5 + V_{S5}$

$V_o \leq \Delta_5 + V_{DD}$

$$Vcm|_{max} = V_{DD} - |\Delta_5| = 2.5 - 0.5 = 2V$$

Lower limit:

$V_{DS6} \geq V_{GS6} - V_{tn} \rightarrow V_{D6} \geq \Delta_6 + V_{S6}$

$V_o \geq \Delta_6 + V_{SS}$

$$Vcmo|_{min} = V_{SS} + |\Delta_6| = -2.5 + 0.2 = -2.3V$$

iv. Total harmonic distortion (THD)

The total harmonic distortion, or THD, of a signal is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency. THD is used to characterize the linearity of audio systems and the power quality of electric power systems. [14]

In audio systems, lower THD means that components in a loudspeaker, amplifier or microphone or other equipment produce a more accurate reproduction by reducing harmonics added by electronics and audio media.

In power systems, lower THD means reduction in peak currents, heating, emissions, and core loss in motors

To understand a system with an input and an output, such as an audio amplifier, we start with an ideal system where the transfer function is linear and time-invariant. When a signal passes through a non-ideal, non-linear device, additional content is

added at the harmonics of the original frequencies. THD is a measurement of the extent of that distortion.

When the input is a pure sine wave, the measurement is most commonly the ratio of the sum of the powers of all higher harmonic frequencies to the power at the first harmonic, or fundamental, frequency: [15]

$$THD = \frac{P_1 + P_2 + P_3 + \cdots + P_\infty}{P_1} = \frac{\sum_{i=2}^{\infty} P_i}{P_1}$$

which can equivalently be written as

$$THD = \frac{P_{TOTAL} - P_1}{P_1}$$

if there is no source of power other than the signal and its harmonics.

Measurements based on amplitudes (e.g. voltage or current) must be converted to powers to make addition of harmonics distortion meaningful. For a voltage signal, for example, the ratio of the squares of the RMS voltages is equivalent to the power ratio:

$$THD = \frac{V_2^2 + V_3^2 + V_4^2 + \cdots + V_\infty^2}{V_1^2}$$

where V_i is the RMS voltage of *i*th harmonic and i = 1 is the fundamental frequency.

THD is also commonly defined as an amplitude ratio rather than a power ratio, resulting in a definition of THD which is the square root of that given above:

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \cdots + V_\infty^2}}{V_1^2}$$

This latter definition is commonly used in audio distortion (percentage THD) specifications. It is unfortunate that these two conflicting definitions of THD (one as a power ratio and the other as an amplitude ratio) are both in common usage.

As a result, THD is a non-standardized specification and the results between manufacturers are not easily comparable. Since individual harmonic amplitudes are measured, it is required that the manufacturer disclose the test signal frequency range, level and gain conditions, and number of measurements taken. It is possible to measure the full 20–20kHz range using a sweep. For all signal processing equipment, except microphone preamplifiers, the preferred gain setting is unity. For microphone preamplifiers, standard practice is to use maximum gain.

Measurements for calculating the THD are made at the output of a device under specified conditions. The THD is usually expressed in percent as distortion factor or in dB relative to the fundamental as distortion attenuation.

We performed the calculation of the THD in LTSpice by order *.four* as seen in the following figure:

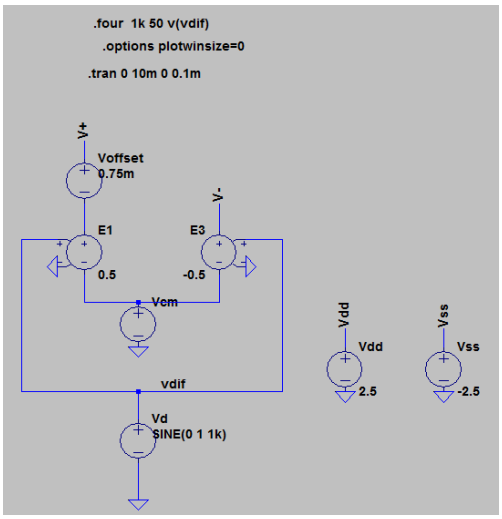


Figure 23.Sinusoidal input signal

Introduce as input signal a pure tone with fundamental frequency 1µV and amplitude of 1kHz . We can see the result in the next figure:

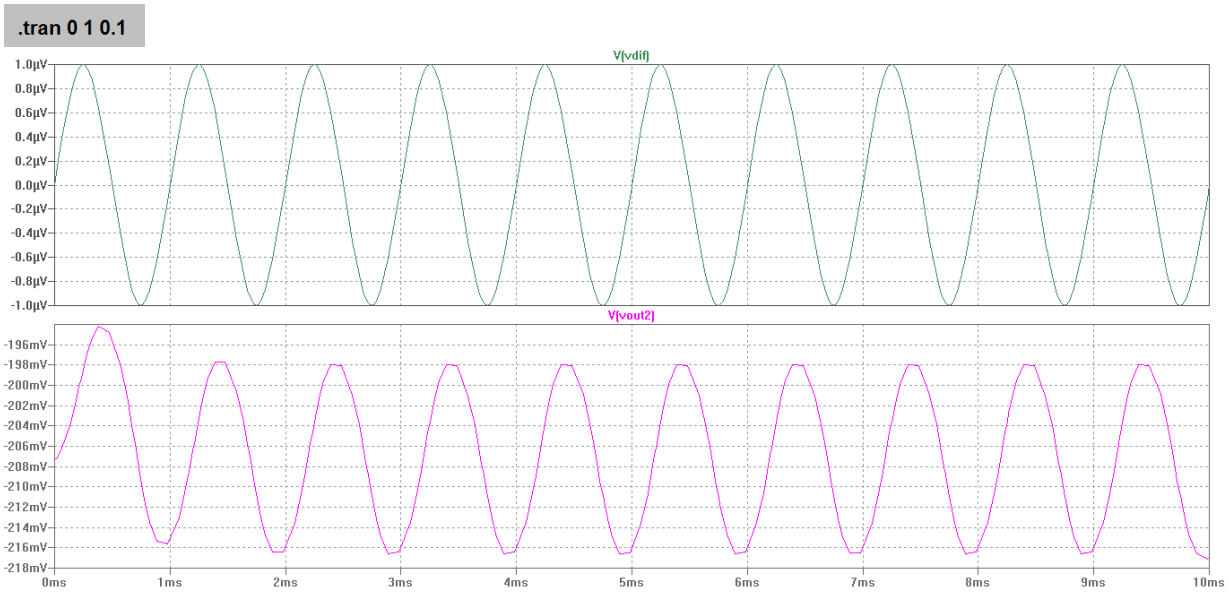


Figure 24.Input and output signal

Doing the FFT we get:

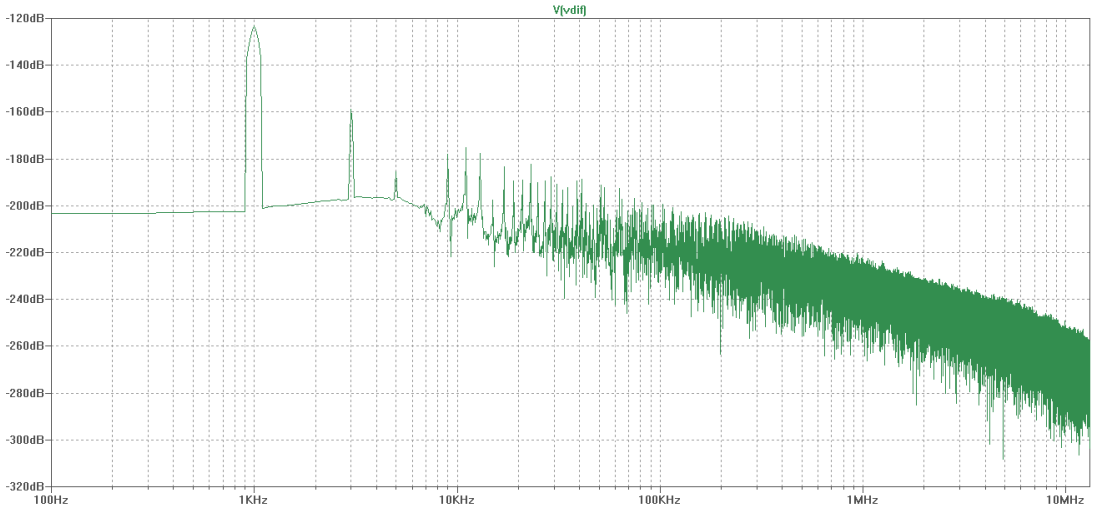


Figure 25.Input FFT(logarithmic scale)

In figure 25 logarithmic scale of the input signal FFT is observed. We can see a pure tone at a 1 KHz fundamental frequency although the signal also has energy in some harmonics. Signal power is around -120dB which is absolutely normal due to the fact that the signal has a 1 µV amplitude and thereby a low power.

Figure 26 shows output signal FFT. This signal, obviously, has higher power and energy since it has passed within the amplifier and it has been amplified. Because of having passed thought the circuit it suffers from nonlinearities and its power is divided among the rest of harmonics. This makes THD rise.

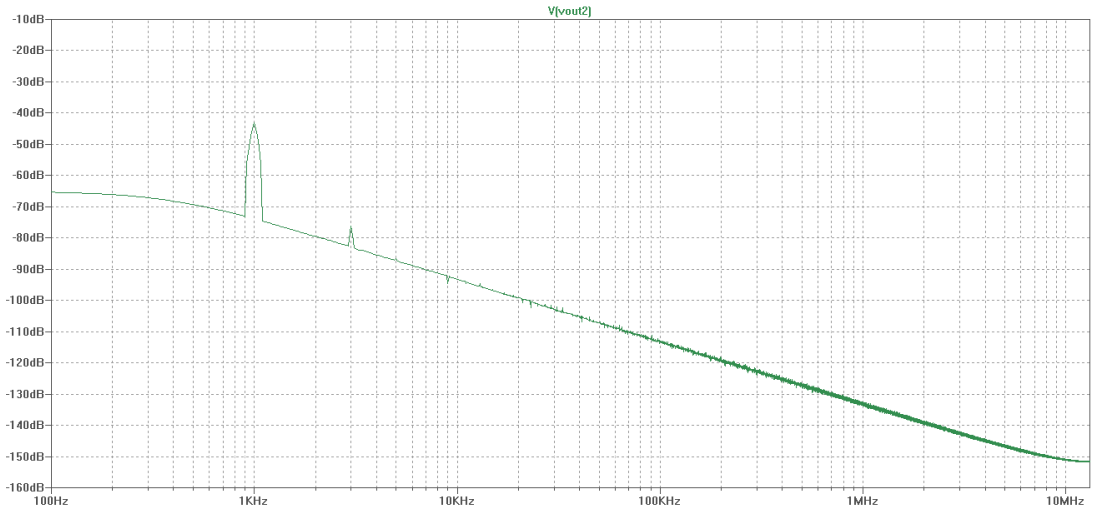


Figure 26.Output FFT(logarithmic scale)

On the one hand we see that the THD of the input signal a little bit over 1%. This is because our signal is a pure tone and does not suffer nonlinearities, focusing practically all the energy in the tone frequency

Fourier components of V(vdif)
DC component:-0.000131423

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]	Normalized Phase [deg]
1	1.000e+03	9.784e-01	1.000e+00	0.51°	0.00°
2	2.000e+03	2.740e-04	2.800e-04	-135.10°	-135.60°
3	3.000e+03	1.504e-02	1.537e-02	-162.30°	-162.81°
4	4.000e+03	2.437e-04	2.491e-04	143.30°	142.79°
5	5.000e+03	5.405e-03	5.524e-03	-22.77°	-23.27°
6	6.000e+03	1.608e-04	1.643e-04	110.14°	109.63°
7	7.000e+03	3.244e-03	3.316e-03	-37.31°	-37.81°
8	8.000e+03	3.151e-04	3.220e-04	57.52°	57.01°
9	9.000e+03	1.722e-03	1.760e-03	-60.99°	-61.50°
10	1.000e+04	2.930e-04	2.995e-04	29.74°	29.24°
11	1.100e+04	1.751e-03	1.790e-03	10.41°	9.90°
12	1.200e+04	1.778e-04	1.817e-04	-175.15°	-175.66°
13	1.300e+04	1.048e-03	1.071e-03	50.23°	49.73°
14	1.400e+04	5.411e-04	5.530e-04	-153.68°	-154.18°
15	1.500e+04	8.478e-04	8.665e-04	169.68°	169.18°
16	1.600e+04	7.575e-05	7.742e-05	138.74°	138.23°
17	1.700e+04	6.168e-04	6.304e-04	-127.56°	-128.07°
18	1.800e+04	3.409e-04	3.484e-04	41.08°	40.58°
19	1.900e+04	1.191e-03	1.217e-03	48.26°	47.75°
20	2.000e+04	2.525e-04	2.581e-04	-91.45°	-91.96°
21	2.100e+04	4.385e-04	4.481e-04	109.39°	108.88°
22	2.200e+04	4.462e-04	4.560e-04	-111.54°	-112.05°
23	2.300e+04	6.916e-04	7.068e-04	-104.11°	-104.62°
24	2.400e+04	1.089e-04	1.113e-04	108.96°	108.46°
25	2.500e+04	1.334e-04	1.364e-04	141.20°	140.69°

Total Harmonic Distortion: 1.702169%

Figure 27.THD input signal

On the other hand we see that the THD of the output signal exceeds the 3%, that is because our signal nonlinearities suffered through the circuit to output. Energy is scattered in different harmonics of the signal.

Fourier components of V(vout2)
DC component:-0.20731

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]	Normalized Phase [deg]
1	1.000e+03	9.667e-03	1.000e+00	-68.35°	0.00°
2	2.000e+03	8.905e-05	9.212e-03	-63.43°	4.92°
3	3.000e+03	2.245e-04	2.322e-02	113.25°	181.60°
4	4.000e+03	7.737e-05	8.003e-03	-39.74°	28.61°
5	5.000e+03	8.946e-05	9.255e-03	-19.63°	48.72°
6	6.000e+03	5.887e-05	6.090e-03	-21.19°	47.16°
7	7.000e+03	8.057e-05	8.335e-03	-22.98°	45.37°
8	8.000e+03	3.826e-05	3.957e-03	-12.43°	55.93°
9	9.000e+03	7.902e-05	8.175e-03	-28.29°	40.07°
10	1.000e+04	2.460e-05	2.545e-03	-18.86°	49.49°
11	1.100e+04	8.033e-05	8.310e-03	-21.63°	46.73°
12	1.200e+04	2.134e-05	2.208e-03	-26.42°	41.94°
13	1.300e+04	5.142e-05	5.319e-03	-7.92°	60.43°
14	1.400e+04	2.151e-05	2.225e-03	-17.54°	50.81°
15	1.500e+04	1.064e-05	1.100e-03	27.16°	95.51°
16	1.600e+04	2.048e-05	2.118e-03	-7.30°	61.05°
17	1.700e+04	9.475e-06	9.801e-04	-19.26°	49.10°
18	1.800e+04	1.830e-05	1.893e-03	-9.86°	58.49°
19	1.900e+04	3.470e-05	3.589e-03	7.18°	75.54°
20	2.000e+04	1.647e-05	1.703e-03	-18.35°	50.00°
21	2.100e+04	2.843e-05	2.941e-03	17.88°	86.23°
22	2.200e+04	1.492e-05	1.543e-03	-18.83°	49.53°
23	2.300e+04	1.305e-05	1.350e-03	-7.98°	60.37°
24	2.400e+04	1.377e-05	1.424e-03	-12.21°	56.14°
25	2.500e+04	1.173e-05	1.214e-03	6.03°	74.38°

Total Harmonic Distortion: 3.345099%

Figure 28.THD output signal

v. Maximum output voltage with load

In this point we use a load that is modeled as a 1KΩ resistor. With LTSpice we obtain:

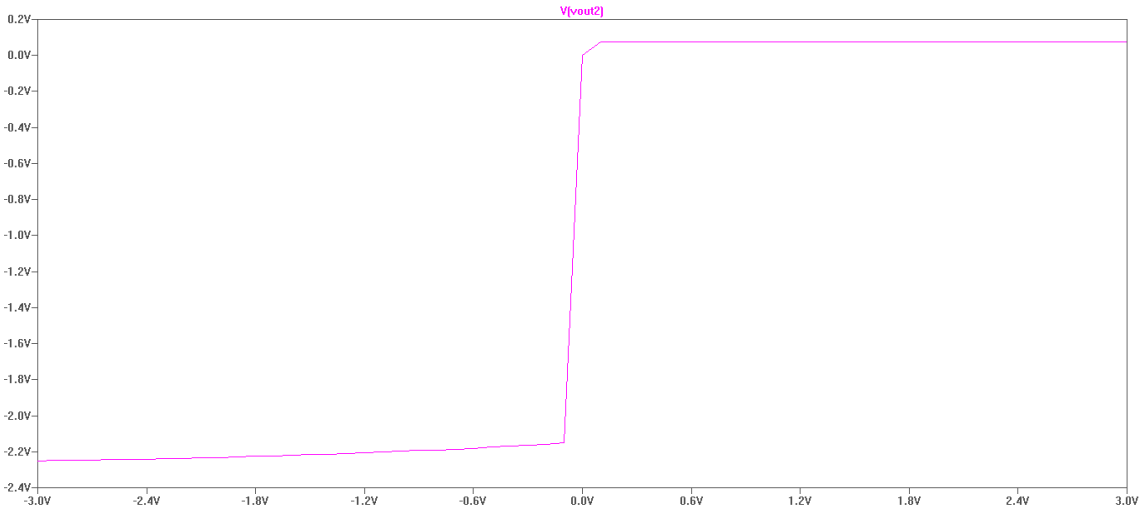


Figure29.Output voltage with load (level3)

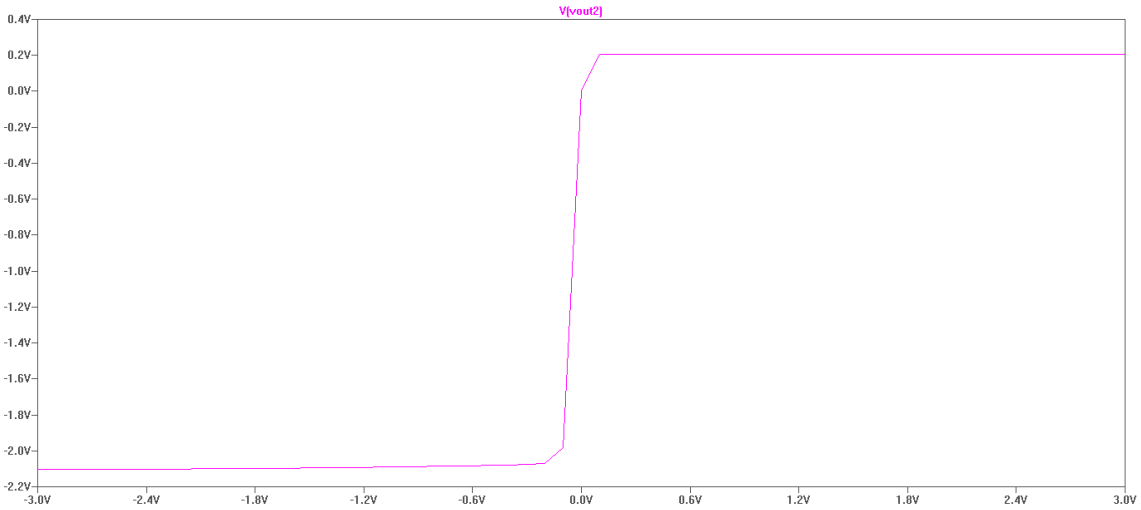


Figure30.Output voltage with load (level49)

The maximum output is practically the same in both cases.

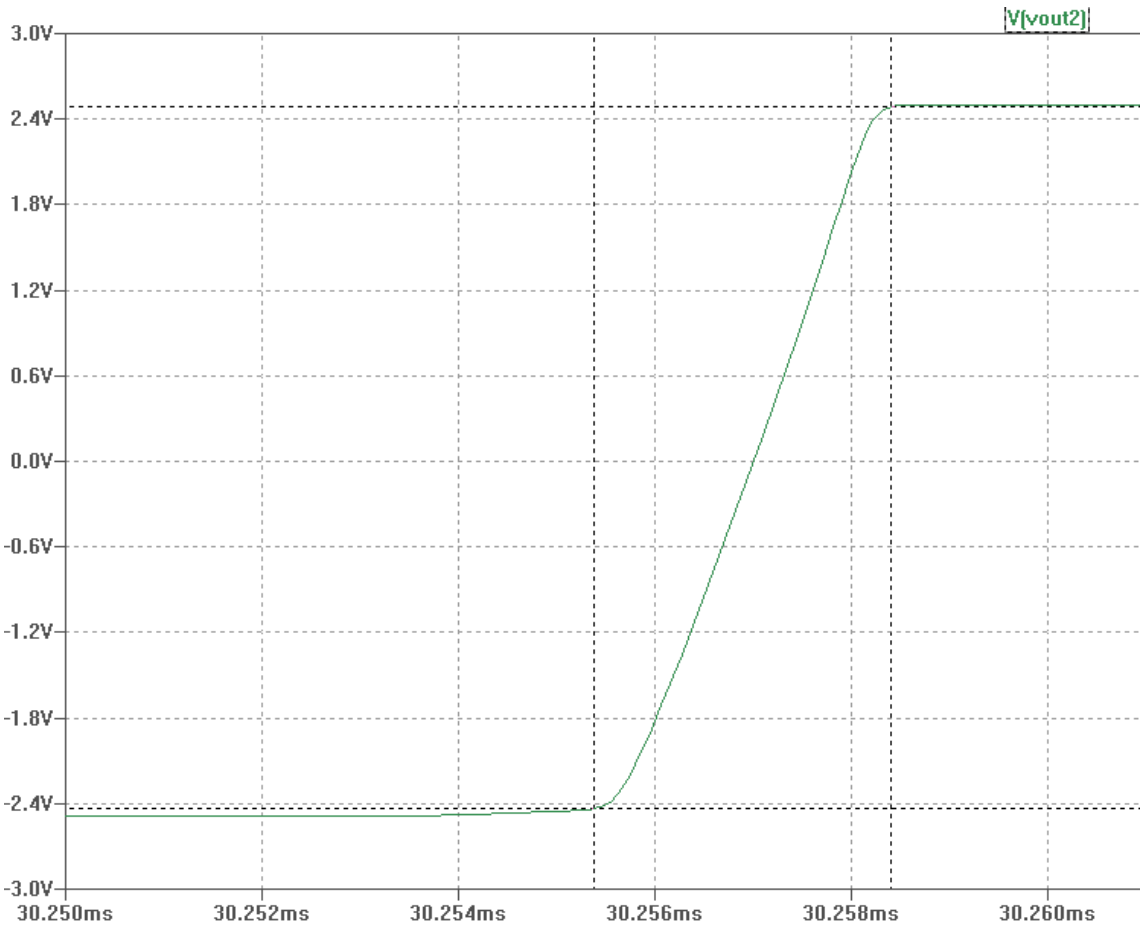
vi. Slew Rate

Signal cannot have infinite slop since the non-electronic components has not instantaneous reply. This line slope corresponds to the speed the transistor reacts to abrupt voltage changes.

We have to analyze slew rates, the negative and the positive one, that are not equal but very similar.

It can be checked in figure 31 that the amplifier positive slew rate is 1.63 V/µs.

Negative slew rate is shown in figure 32, it is somehow smaller, around 1.15 V/ µs.



Cursor 1			
	V(vout2)		
Horz:	30.2554ms	Vert:	-2.43925V
Cursor 2			
	V(vout2)		
Horz:	30.2584ms	Vert:	2.48912V
Diff (Cursor2 - Cursor1)			
Horz:	3.02326µs	Vert:	4.92837V
Freq:	330.769KHz	Slope:	1.63015e+006

Figure 31.Positive slew rate

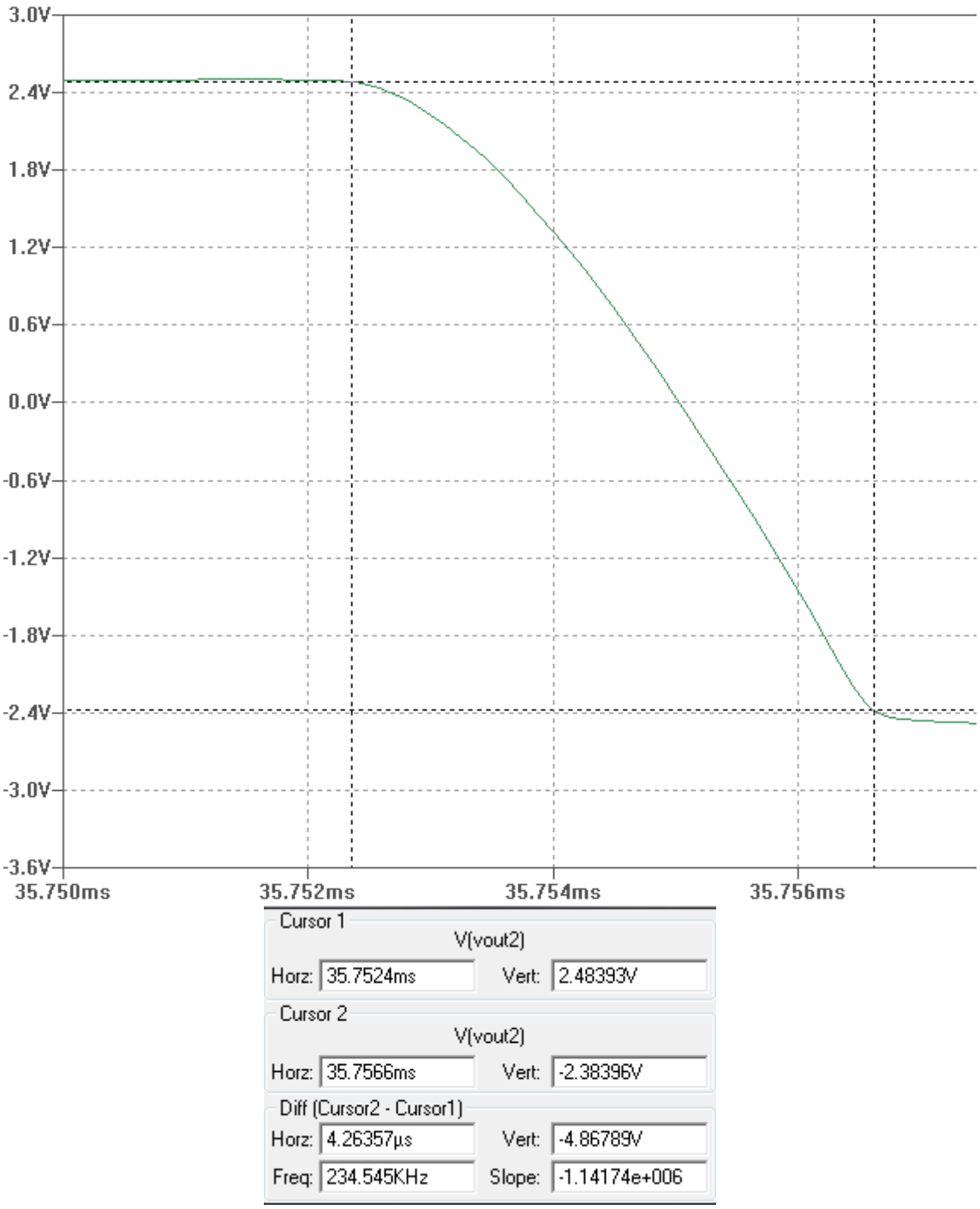


Figure 32.Negative slew rate

vii. Results of simulation level 49

Now use a higher level of complexity in modeling transistors. We use a level 49. These are the features of the model 49:

```
.MODEL n_05 NMOS (                              LEVEL   = 49
+VERSION = 3.1          TNOM    = 27            TOX     = 1.43E-8
+XJ      = 1.5E-7       NCH     = 1.7E17        VTH0    = 0.6174975
+K1      = 0.8876598    K2      = -0.0951675    K3      = 20.9151529
+K3B     = -9.6382243   W0      = 1.020585E-8   NLX     = 1.08112E-9
+DVT0W   = 0            DVT1W   = 0             DVT2W   = 0
+DVT0    = 0.8186693    DVT1    = 0.3372827     DVT2    = -0.4471971
+U0      = 449.7033083  UA      = 1E-13         UB      = 1.481183E-18
+UC      = -4.35408E-13 VSAT    = 1.750272E5    A0      = 0.6637676
+AGS     = 0.1269501    B0      = 2.281394E-6   B1      = 5E-6
+KETA    = -2.932031E-3 A1      = 7.951274E-7   A2      = 0.319673
+RDSW    = 1.044541E3   PRWG    = 0.1113887     PRWB    = 0.0124254
+WR      = 1            WINT    = 2.035444E-7   LINT    = 9.118243E-8
+XL      = 1E-7         XW      = 0             DWG     = -6.76768E-10
+DWB     = 2.626198E-8  VOFF    = -8.709001E-4  NFACTOR = 0.3274632
+CIT     = 0            CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0            ETA0    = 2.542626E-3   ETAB    = -9.003453E-4
+DSUB    = 0.1345826    PCLM    = 2.7474125     PDIBLC1 = 0.673548
+PDIBLC2 = 3.953974E-3  PDIBLCB = 0.0676693     DROUT   = 0.8884749
+PSCBE1  = 7.0944E8     PSCBE2  = 5.636482E-4   PVAG    = 0
+DELTA   = 0.01         RSH     = 81.6          MOBMOD  = 1
+PRT     = 0            UTE     = -1.5          KT1     = -0.11
+KT1L    = 0            KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0            WLN     = 1             WW      = 0
+WWN     = 1            WWL     = 0             LL      = 0
+LLN     = 1            LW      = 0             LWN     = 1
+LWL     = 0            CAPMOD  = 2             XPART   = 0.5
+CGDO    = 2.22E-10     CGSO    = 2.22E-10      CGBO    = 1E-9
+CJ      = 4.258295E-4  PB      = 0.9372076     MJ      = 0.4456534
+CJSW    = 3.076063E-10 PBSW    = 0.8           MJSW    = 0.181535
+CJSWG   = 1.64E-10     PBSWG   = 0.8           MJSWG   = 0.181535
+CF      = 0            PVTH0   = 0.0162776     PRDSW   = 278.4786758
+PK2     = -0.0814166   WKETA   = -7.283165E-3  LKETA   = -4.020995E-3  )
*
```

```
.MODEL p_05 PMOS (                              LEVEL   = 49
+VERSION = 3.1          TNOM    = 27            TOX     = 1.43E-8
+XJ      = 1.5E-7       NCH     = 1.7E17        VTH0    = -0.9152268
+K1      = 0.553472     K2      = 7.871921E-3   K3      = 53.4949014
+K3B     = -3.7856731   W0      = 6.738971E-6   NLX     = 2.795695E-7
+DVT0W   = 0            DVT1W   = 0             DVT2W   = 0
+DVT0    = 1.3395264    DVT1    = 0.267458      DVT2    = -0.0568881
+U0      = 201.3603195  UA      = 2.408572E-9   UB      = 1E-21
+UC      = -1E-10       VSAT    = 1.272242E5    A0      = 0.7748807
+AGS     = 0.0598168    B0      = 6.64175E-7    B1      = 5E-6
+KETA    = -4.865785E-3 A1      = 1.799339E-4   A2      = 0.4844663
+RDSW    = 3E3          PRWG    = -0.0304277    PRWB    = -0.0443398
+WR      = 1            WINT    = 2.824041E-7   LINT    = 1.186971E-7
+XL      = 1E-7         XW      = 0             DWG     = -1.16725E-9
+DWB     = -1.237634E-8 VOFF    = -0.0735326    NFACTOR = 0.6345367
+CIT     = 0            CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0            ETA0    = 9.767795E-4   ETAB    = -0.2
+DSUB    = 1            PCLM    = 2.2583753     PDIBLC1 = 0.0394748
+PDIBLC2 = 3.705722E-3  PDIBLCB = -0.0320804    DROUT   = 0.212888
+PSCBE1  = 2.49175E10   PSCBE2  = 2.457905E-9   PVAG    = 0
+DELTA   = 0.01         RSH     = 109           MOBMOD  = 1
+PRT     = 0            UTE     = -1.5          KT1     = -0.11
+KT1L    = 0            KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0            WLN     = 1             WW      = 0
+WWN     = 1            WWL     = 0             LL      = 0
+LLN     = 1            LW      = 0             LWN     = 1
+LWL     = 0            CAPMOD  = 2             XPART   = 0.5
+CGDO    = 2.89E-10     CGSO    = 2.89E-10      CGBO    = 1E-9
+CJ      = 7.243769E-4  PB      = 0.9580741     MJ      = 0.4957715
+CJSW    = 2.398685E-10 PBSW    = 0.99          MJSW    = 0.3331245
+CJSWG   = 6.4E-11      PBSWG   = 0.99          MJSWG   = 0.3331245
+CF      = 0            PVTH0   = 5.98016E-3    PRDSW   = 14.8598424
+PK2     = 3.73981E-3   WKETA   = 6.989253E-3   LKETA   = -7.31204E-3
*
```

Figure33.level 49 characteristics

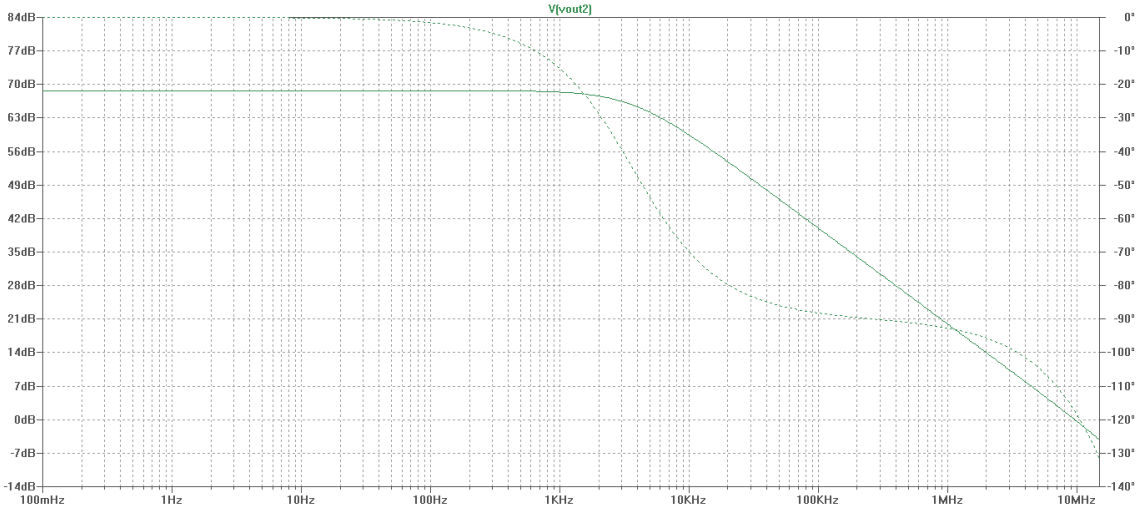


Figure 34.GBW level 49

Comparing both answers we observe that the only difference between a level and the other one is the gain, this difference is due to the offset voltage, since this voltage was calculated according to the 2 level model. If we change the BSIM offset level we see gain raises even the 80 dB.

The BSIM amplifier shows a slightly minor GBW that the one in level 2, this is logical since this model is a more realistic one.

7. Layout design

i. Layout elaboration

The last stage of the design process of an integrated circuit is the layout development, which is the set of geometric patterns representing the architecture of integrated circuit level layers of polysilicon, metal 1, metal 2, metal 3 metal4, diffusion N +, P + diffusion, well N, for further manufacture. This section briefly describes the processes involved in the fabrication of an integrated circuit, then comments on CMOS technology to end rules in developing design and layout techniques used in this work.

ii. Manufacturing Process

Integrated circuits are fabricated on thin wafers made of silicon slightly doped acceptors (n-type substrates) or donor (type substrates p), about 18 cm in diameter and approximately 0.5 mm thick. Over these wafers the regions where polysilicon and/or metal tracks will be deposited are being successively defined. These tracks will make up gates, connections and drain or sources islands.

A basic technological processed used during the manufacture of a circuit is composed as follows [16]:

- **Oxidation:** The isolation between the different tracks which conform the integrated circuit is got making a silicon oxide (SiO2).layer growing right there. These layers thickness widely determines the electrical features of all the devices composing the integrated circuit.

- **Deposition or metallization:** It consists of putting a thin layer of a certain substance (polysilicon/aluminum) over the wafer, which having been trimmed using photolithographic techniques will set up conductive or isolating tracks.

- **Diffusion:** This process lets atomic movements inside a solid using high temperature, and it is used to dope certain zones in the wafer.

- **Ion Implantation:** This process has the same goal than the broadcasting process, which is creating doped regions inside the wafer, when it is necessary to control very accurately the thickness and the concentration of those zones to be doped. The ionic implantation process consists of putting dopers inside the silicon by ionic bombing at a high energy level.

iii. CMOS Technology

CMOS integration consists of forming semiconductive N and regions and the gate oxide zone with polysilicon over it; and interconnecting the several transistors between them and with the bias source. Every single connection is made by metallic lines (aluminum). [16] The mentioned regions are not only in the same plane but also in

successive "floors": the broadcasting penetrates in the semiconductive wafer, gate oxide and polysilicon rise and the metal flows over the whole. Several oxide layers separate the transistors between each others and the metal they have under themselves, excluding those points where connections must be established.

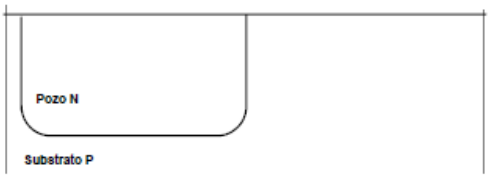
But, furthermore, N broadcastings require a P substrate which is the own doping of the wafer, whilst P broadcastings need a N substrate that must be previously achieved over the wafer: this N substrate zones are known as wells. P substrate must be biased at the most negative voltage an N-wells at the most positive one, in both cases with the purpose that joints broadcasting-substrate are isolated, in inverse bias.

Due to that, in the wafer surface, separated by the oxide called field, we will have transistors and substrate bias contacts. We will call active zones to the whole of them.

Basic stages of the integration CMOS [16]

- **Initial wafer of doped Silicon type P**
  Diameter: 100 - 125 nm thickness: 0.5nm = 500µm

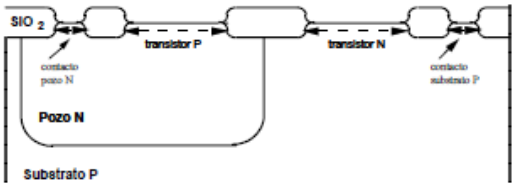
- **Formation N- Wells**
  NMOS transistors are formed over the wafer for this purpose it is necessary to create zones of N substrate, this zones are named wells.



MÁQSCARA 1: pozos

profundidad de los pozos ~ 5 µm

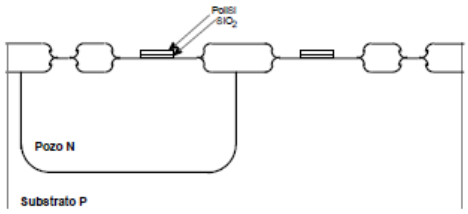
- **Demarcation of the active zones**
  A few intermediate barriers of silicon oxide separate the transistors between each other's and these from the bias contacts. Transistors and bias contacts are considered active zones.



MÁSCARA 2: zonas activas

espesor del óxido de campo ~ 1 µm

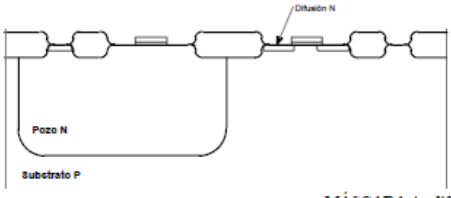
- **Oxidize of gate and Polysilicon**



MÁSCARA 3: polisilicio

espesor del óxido de puerta ~ 0,05 µm
espesor del polisilicio ~ 0,2 µm

- **Diffusion**

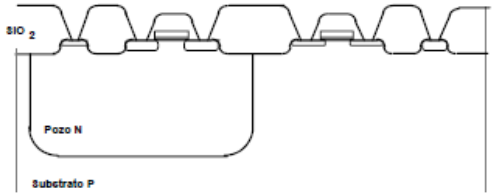


MÁSCARA 4: difusión N

profundidad de la difusión N ~ 0,2 µm

- **Contacts**

A layer of silicon oxide, oxide of isolation, serves to separate the metal (that connects the different transistors between them and with bias voltage) regarding to the polysilicon and the diffusion that are found under themselves.
The above mentioned oxide layer must have "holes" for the contacts of the metal lines with the several zones that must be connected (the contacts are like the weld points in the plates of printed circuits).

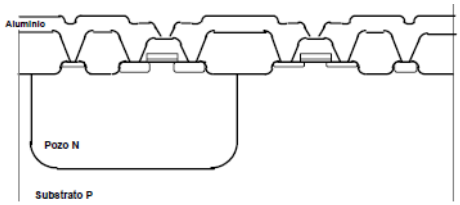


MÁSCARA 6: contactos

espesor del óxido de aislamiento ~ 0,7 µm
dimensiones de los contactos ~ 2 x 2 µm

- **Connections in metal**

Nowadays several superposed metals join and each of them needs a silicon oxide layer to separate it from the previous metal. Each metal needs two masks: one for the routes and other one to delimit the lines of the own metal.

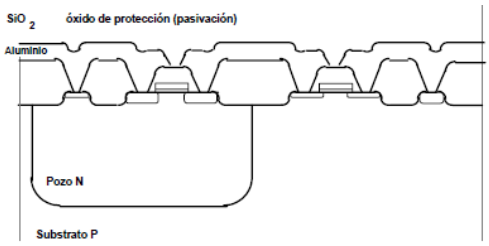


MÁSCARA 7: metal

espesor del aluminio ~ 0,5 µm

- **Passivation**

  A thick top layer of silicon oxide serves to protect the whole integrated circuit; in it opened "holes" (PADs) have to be left from the zones where threads will be welded joining the circuit with the terminals (pins) of the plastic or ceramic case which contains them



MÁSCARA 8: pasivación

espesor de la capa exterior de oxido ~ 2 µm

The passivation mask delimits the metal spaces (PADs) where the mentioned threads connect the case terminals.

iv. Design rules

For the layout, it is very important follow some basic rules (Rules are defined on the basis of the parameter λ whose value depends on the technology to use, for this work the technology is in use, CMOS 0.5). [17]

- Minimal Sizes of the tracks.
- Minimal Distance between tracks.
- Minimal Overflow of a track with regard to other one.
- Minimal Distance between polysilicon and contacts.
- Minimal overlapping, between others.

The most common rules in the elaboration of layout appear in the following figure

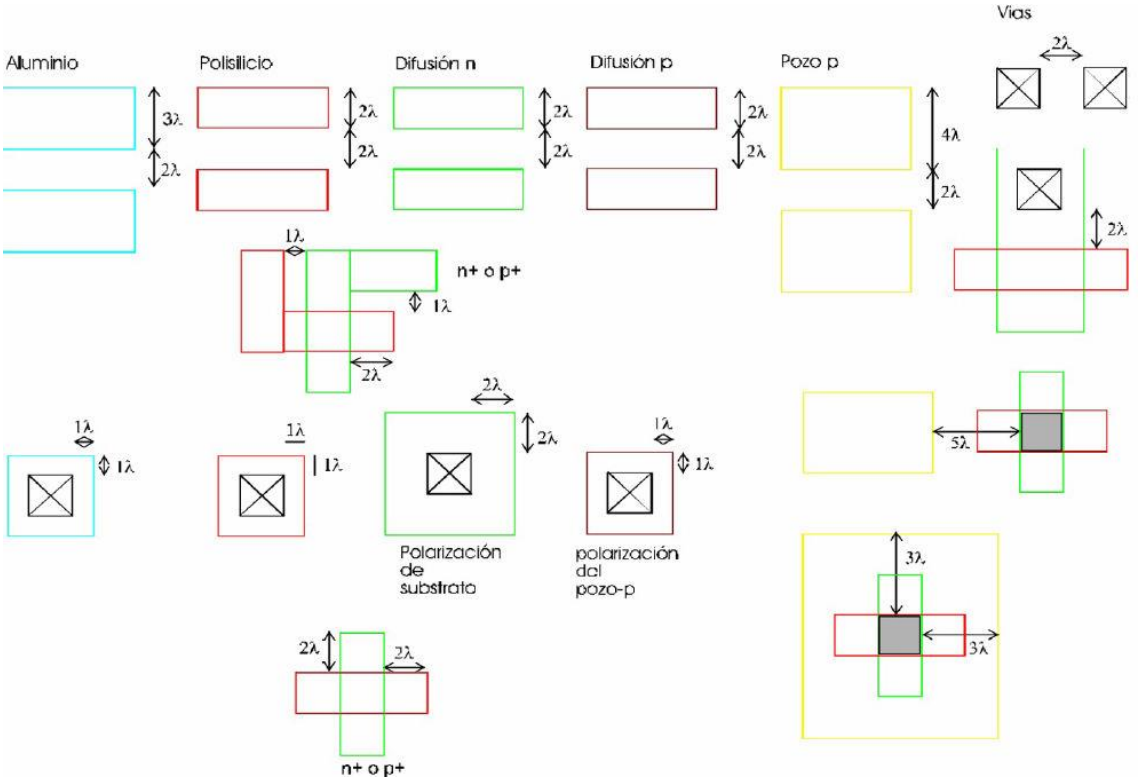


Figure35.Principal layout design rules

These rules have to of be followed to avoid problems in the integrated circuit manufacturing process.

For the production of the layout corresponding to the symmetrical OTA, some technologies and considerations of design have to be taken into account:

- **Interdigitizing :** This technique consists of reducing the area of separation between the union drain-source. For example, if we have a transistor with a width of channel (W) very big it is necessary to divide the transistor in smaller transistors , every small transistor shares a diffusion region with its neighbors, optimizing area.

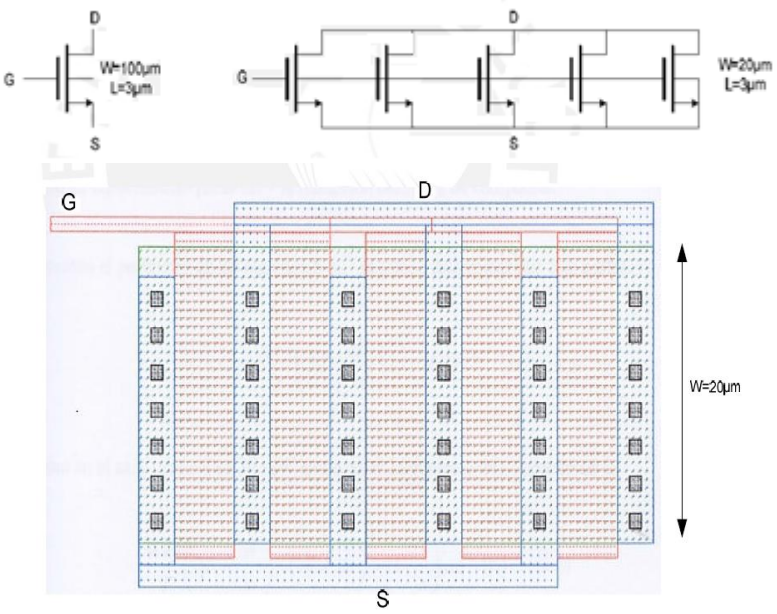


Figure 36.Example of interdigitized

- **Symmetry:** This consideration is very important to make the differential par layout. A symmetry lack can provoke referred to the signal offset appearance. At the same way, keeping symmetry in the differential par contributes to reduce common mode noise and par nonlinearities. An alternative to keep this symmetry in the differential par is use "useless transistors", which has no electrical use, but their presence is decisive to help each transistor surrounding being the same.

- In the interdigitizing that case where the length of the channel (L) is too big regarding to the channel width (W) has been analyzed. In this case , a snake shape has to be used to make a step by step diffusion as it is shown in figure 33

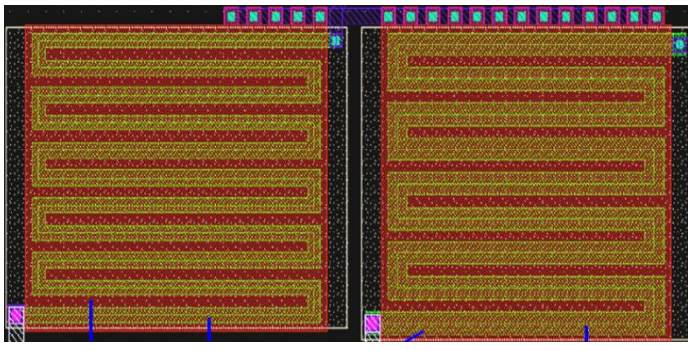


Figure 37. "snake" method

v. Final design

To do our amplifier layout we will proceed to construct the amplifier using the program Dsch2. Later, we will use the file created in Dsch2 to create the layout in Microwind. This program creates the layout from our file of Dsch2

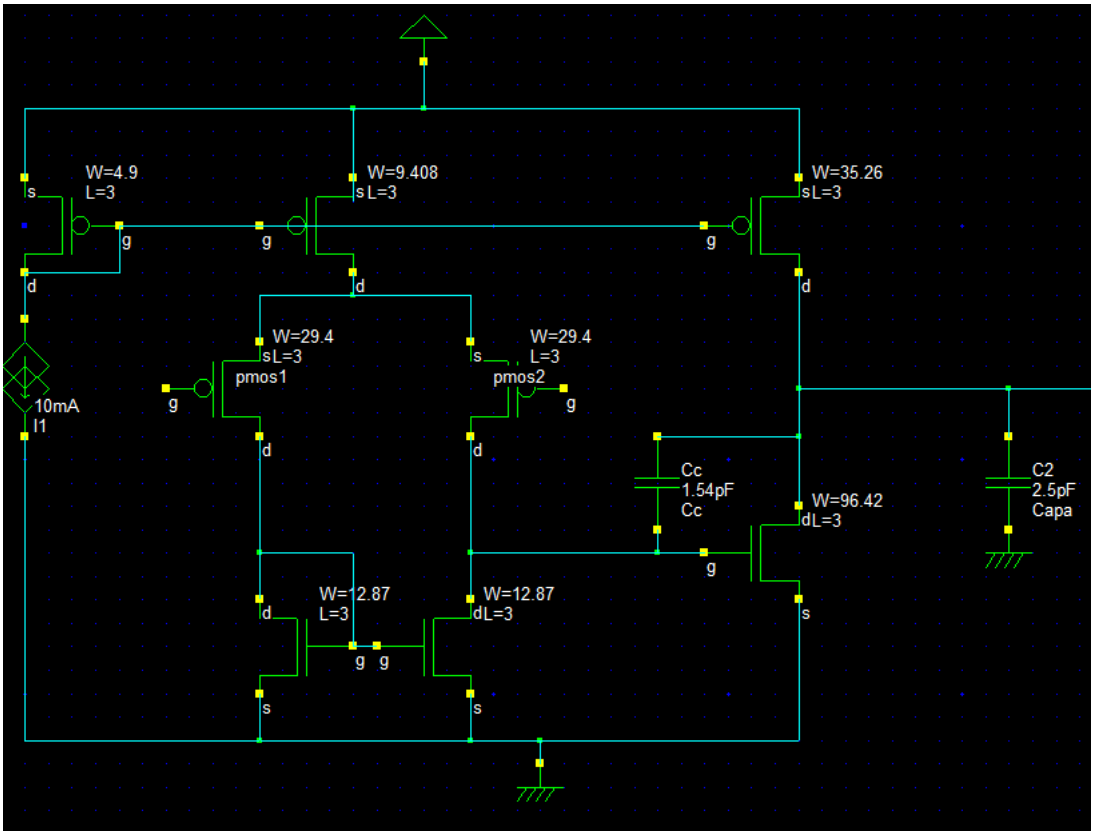


Figure 38. Dsch2 design

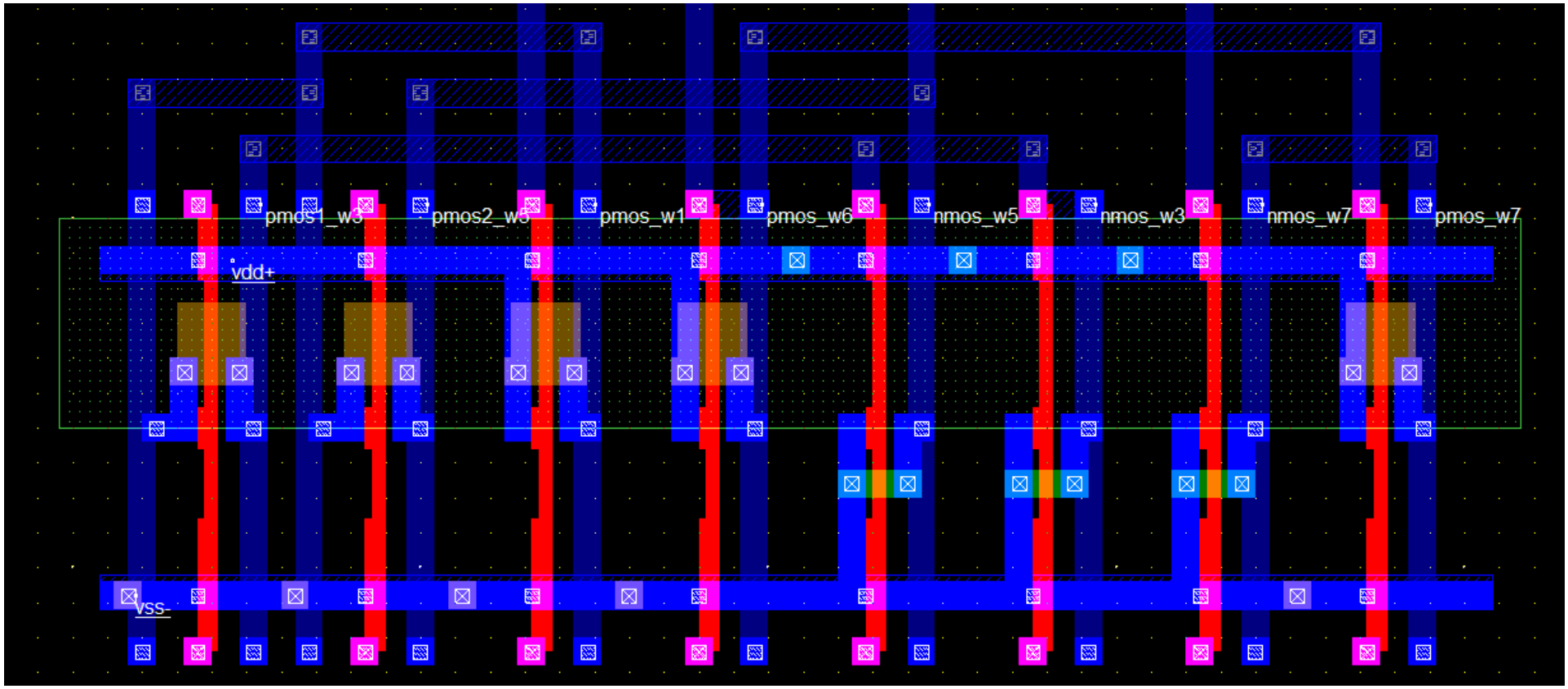


Figure 39.Layout design

In the figure 35 above, it is shown simulation as of Layout. We can distinguish the slew rate which was comment in prior sections and how results match up. In this case input signal is square.

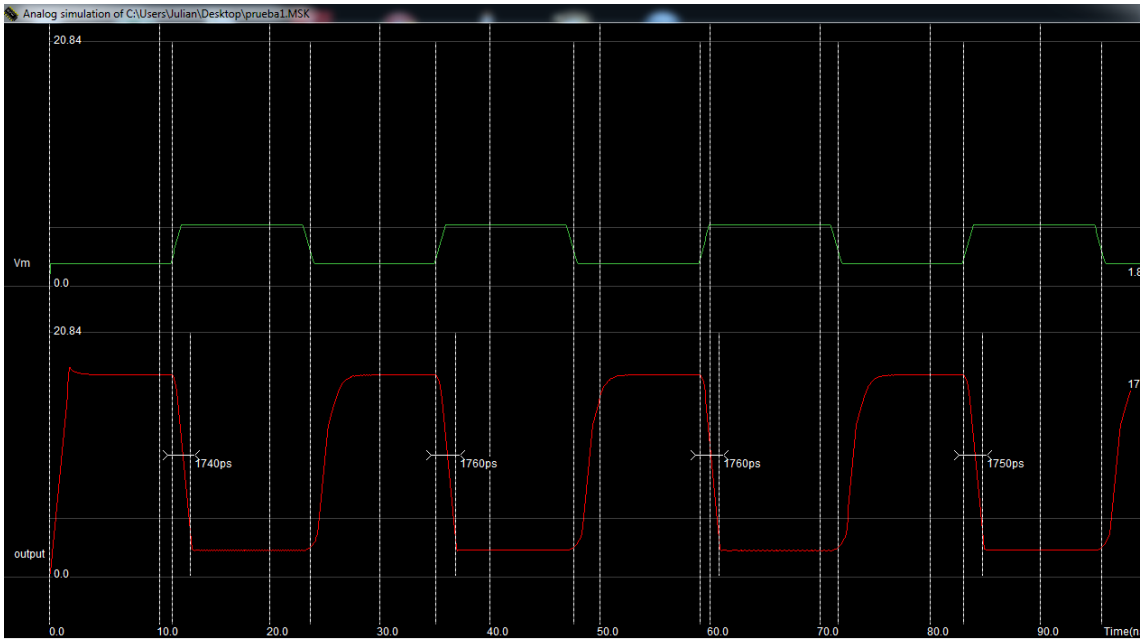


Figure 40.Layout simulation

8. Conclusions

The design of operational transconductance amplifier using 0.5 µm technology is presented in this project. In table 2 it is shown how project starting point specifications have been accomplished. With the load capacitor of 2.5 pF, the design demonstrates a DC gain of 91.1 dB with a unity gain frequency of 10.7 MHz and phase margin of 77°. The amplifier has an input dynamic range going from -2.6V to 0.38V. Reaching all requirements above mentioned, we achieve an outstanding design of the amplifier.

SPECIFICATION	REQUIRED	ACHIEVED
A_V(dB)	>80	91
PM(°)	>65	77
SR^+(V/ms)	1.5	1.63
SR^-(V/ms)	1.5	1.15
ICMR(V)	>3	0.83/-2.6
R_{out}(Ω)	100K	0.3M
Iref(µA)	10	10

Table 6.Amplifier specifications

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Design and implementation of an operational amplifier with mosfet technology

Julián Martínez Irizar
Luis Serrano Arriezu
Daniele Caviglia
Pamplona, 7 de Octubre 2013

Index

1. Project summary
2. Design specification
3. Circuit design
4. Implementation with LTSpice
5. Layout design
6. Conclusions

Project summary

- We propose in this project an optimization procedure for the design of a classical Miller OTA CMOS integrated circuit
- Its consists of two amplification stages

Project summary

- The first stage is a basic differential pair implemented with PMOs transistors (M1 and M2) and a active load implemented with NMOS transistors (M3 and M4).

- The second stage is a basic common source amplifier with a NMOS transistor (M6) acting as amplifier and a PMOS transistor (M5) acting as a current source load.

Project summary

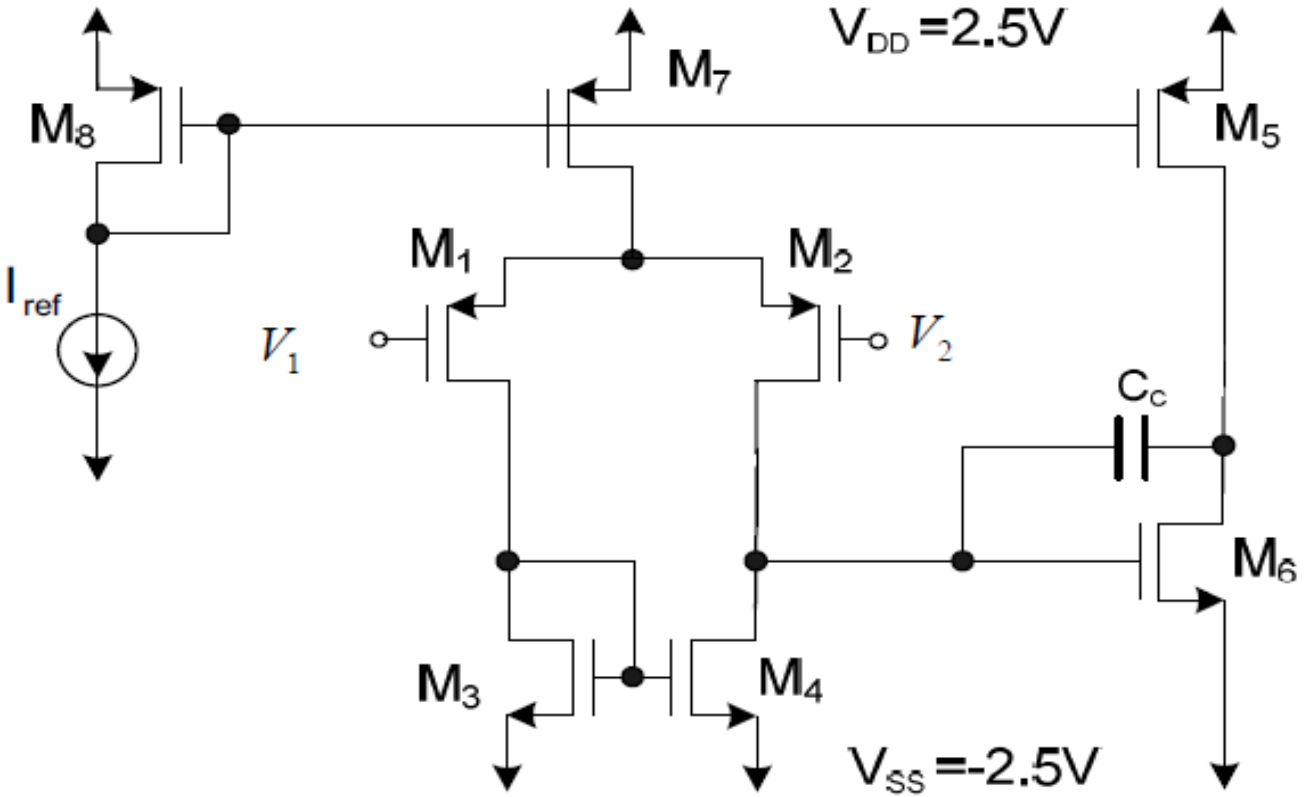


Figure 4. OTA circuit

Project summary

- The first stage is a basic differential pair implemented with PMOs transistors (M1 and M2), which has a single-ended current source as active load implemented with NMOS transistors (M3 and M4)

- The second stage is a basic common source amplifier with a NMOS transistor (M6) acting as amplifier and a PMOS transistor (M5) acting as a current source load. This stage has a feedback compensation capacitor, *Cc*

Project summary

- We use 0.5µm Technology, the device characteristics are shown in the following tables:

Operating Voltage	5,12 V
Substrate Material	P-Type, Bulk or EPI
Drawn Transistor Length	0.6µm
Gate Oxide Thickness	13.5nm
Contact/Via Size	0.5µm
Contacted Gate Pitch	3.9µm
Top Metal Thickness	675nm
Contacted Metal Pitch	
Metal 1	1.5µm
Metal 2,3	1.6µm
Metal Composition	TiN/AlCu/Tin

Table 1.Process Characteristics

N-Channel	Typical Value	Unit
V_t	0.7	V
I_{dsat}	450	µA/µm
P-Channel	**Typical Value**	**Unit**
V_t	-0.9	V
I_{dsat}	-260	µA/µm

Table 2.Standard Transistors characteristics

Design specification

- The design of our classical CMOS OTA-Miller integrated circuit starts by defining the design specifications in terms of the performance parameters of interest

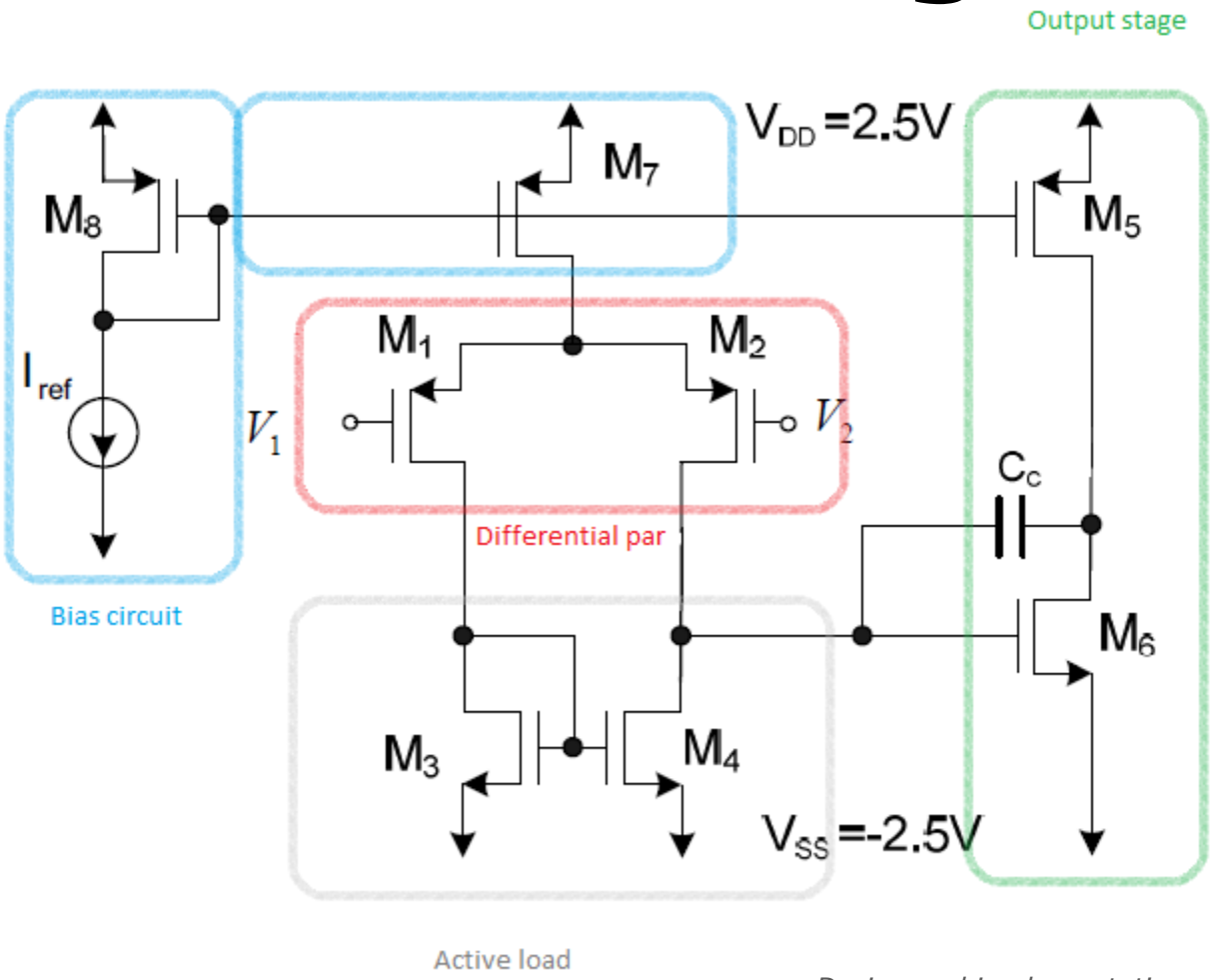
SPECIFICATION	REQUIRED
A_V(dB)	>80
PM(°)	>65
SR^+(V/ms)	1.5
SR^-(V/ms)	1.5
ICMR(V)	>3
R_{out}(Ω)	100K
Iref(µA)	10

Table 3.Amplifier specification

Circuit Design

- First we do the handmade calculations.
- Then we design the amplifier in SPICE with the information obtained in the previous phase. Level 2 and level 49 models will be used to compare the behavior differences in the circuit.
- Finally, design will be made using Layout.
- Analysis post Layout.

Circuit Design



Circuit Design

- **Active Load:** analogical block entrusted to assure the saturation of the differential par and to determine the maximum possible variation of the analogical block output.

- **Output stage:** block that serves to amplify the differential input signal. The transistors must be used in saturation mode.

Circuit Design

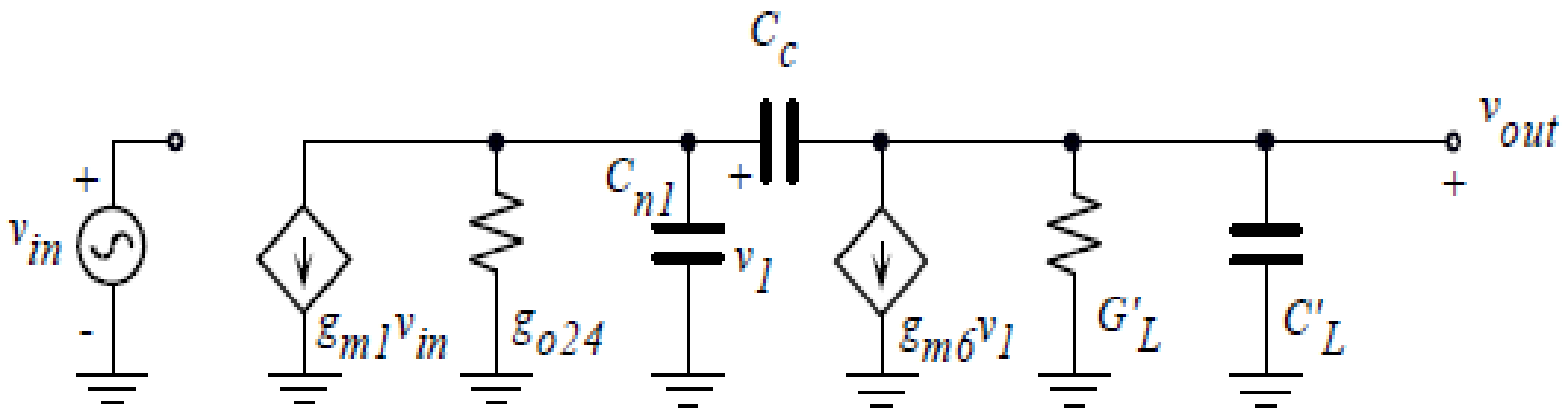
- **Bias circuit** : To assure a correct current copy, it is necessary to take into account that the output resistance must be much bigger than the load.

- **Differential par**: analogical basic block to which has a differential input instead of a single input signal. For its design it is necessary that both transistors of the differential couple stay in the saturation region.

Circuit Design

- The total gain of stage at low frequency is the product of the gains of the previous stages whose result is:

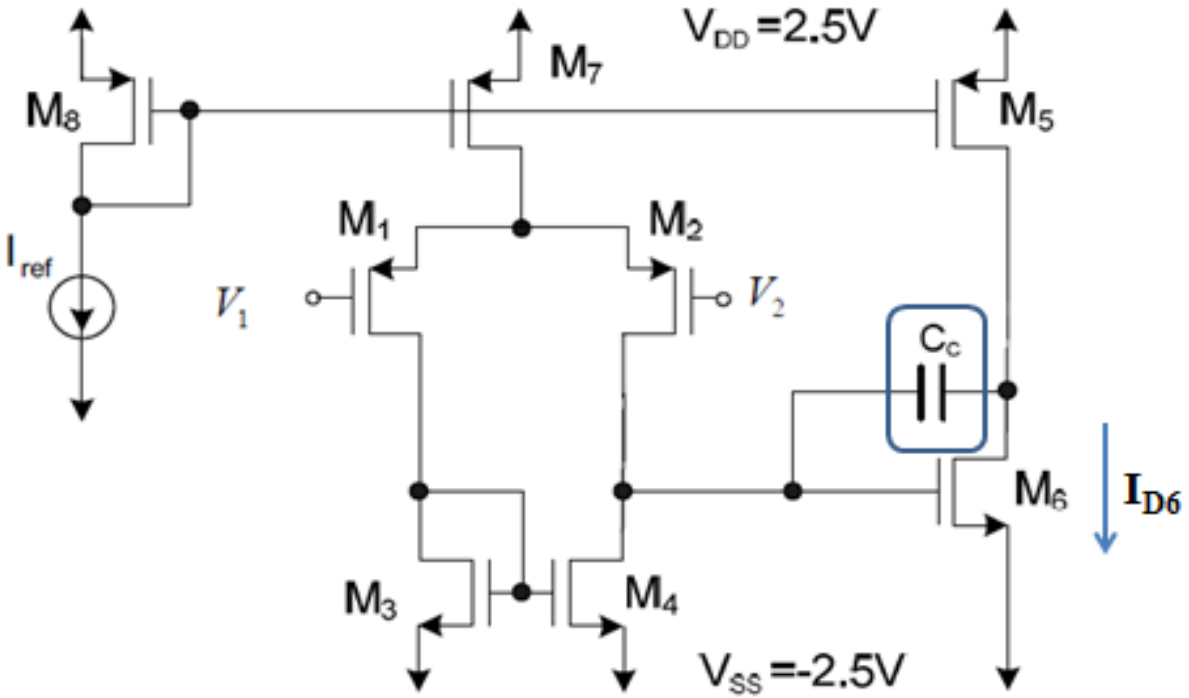
$$|A_{vo}| = A_{v1}.A_{v2} = \left(\frac{g_{m1}}{g_{o24}}\right)\left(\frac{g_{m6}}{G_L}\right)$$



Miller-OTA small signal equivalent

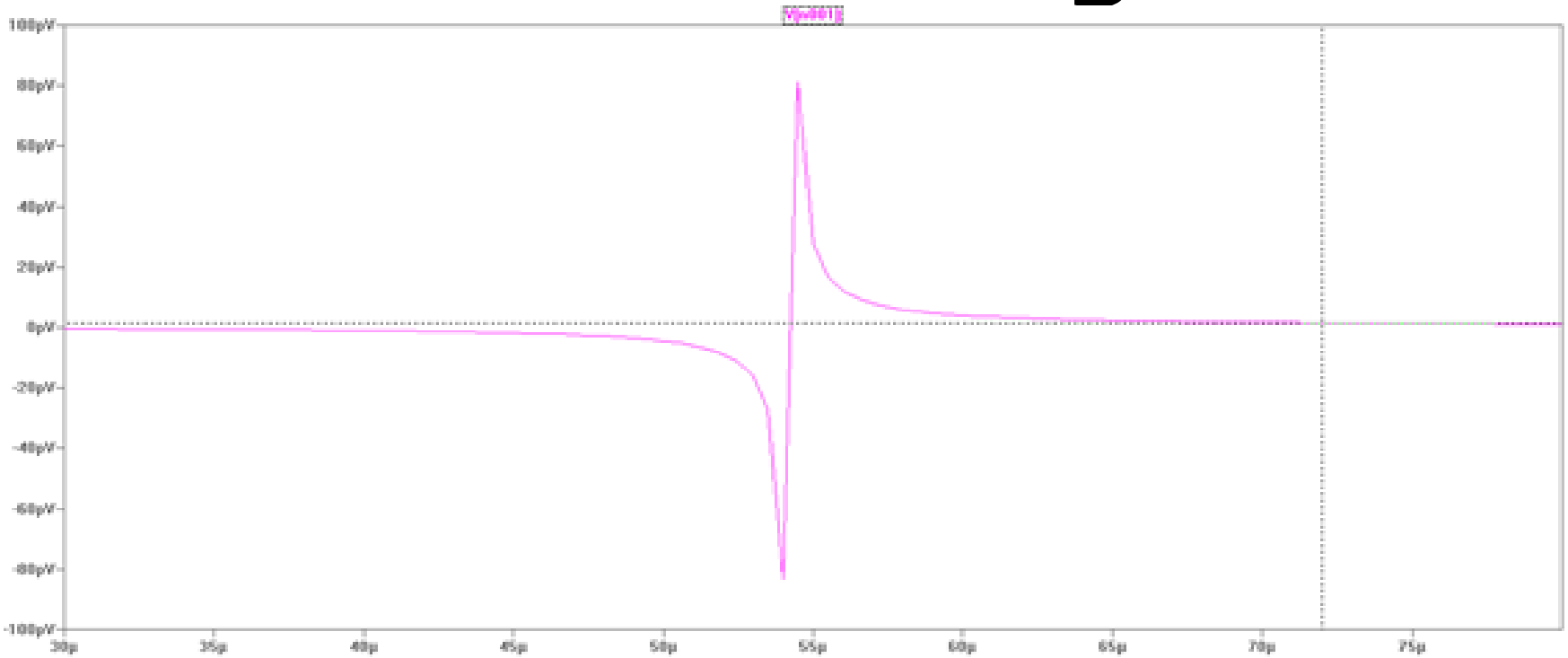
Circuit Design

- **Calculation of I_{D6} and C_c**



Cc location inside the circuit

Circuit Design



It is observed when the Cc begins to become stable and take a value for Cc and Id6. In this case it is taken Cc=1.53pF, I_{D6}=72µA

Circuit Design

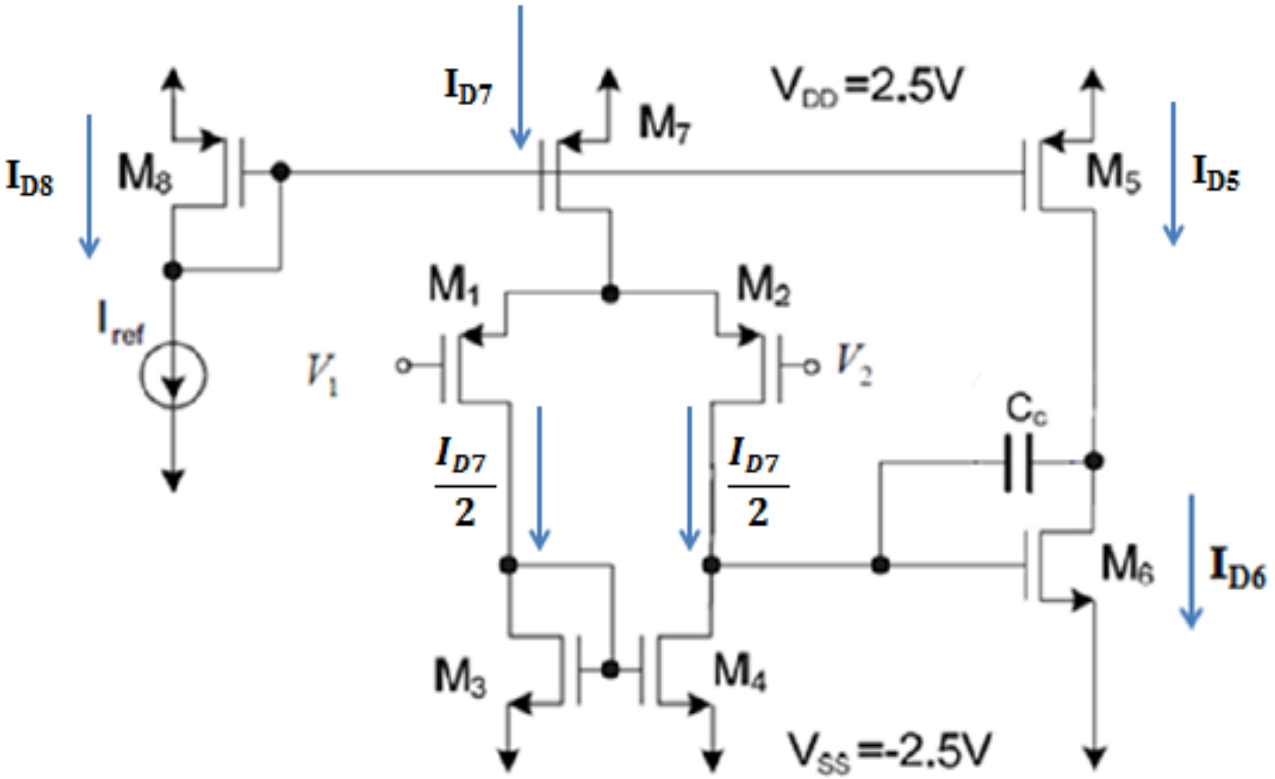
- Once calculated the value of the current ID6 and of Miller's capacitor ,Cc, already we can proceed to calculate all the rest design parameters of the amplifier. For it we are going to use the following equations:

$$gm_n = \frac{2 * Id_n}{Vgs_n - Vt} \qquad \left(\frac{W}{L}\right)_n = \frac{gm_n}{K_n * (Vgs_n - Vt)} \qquad \frac{Id_n}{Id_m} = \frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_m}$$

Circuit Design

- We take (Vgs-Vt) =0.5V for the transistors that form a part of mirrors of current and 0.2V for the others.
- We take $K_n = 112 * 10^{-6}$ and $K_p = 49 * 10^{-6}$, these values are provided by the models of spice. The units of the conductance (gm_n) are Siemens[S]=[Ω^{-1}].
- We proceed to calculate several transistors in the circuit's dimensions , gm and currents.

Circuit Design



Details of the currents that flow the circuit and their values

Circuit Design

Nº trt	I[µA]	gm[S]	K[A/V²]	(Vgs-Vt)[V]	W[µm]	L[µm]
1	9.61	96.1	49	0.2	29.4	3
2	9.61	96.1	49	0.2	29.4	3
3	9.61	96.1	112.2	0.2	12.87	3
4	9.61	96.1	112.2	0.2	12.87	3
5	72	288	49	0.5	35.262	3
6	72	720	112.2	0.2	96.42	3
7	19.22	76.88	49	0.5	9.408	3
8	10	40	49	0.5	4.9002	3

Features of transistor with L optimized

Implementation with spice simulator

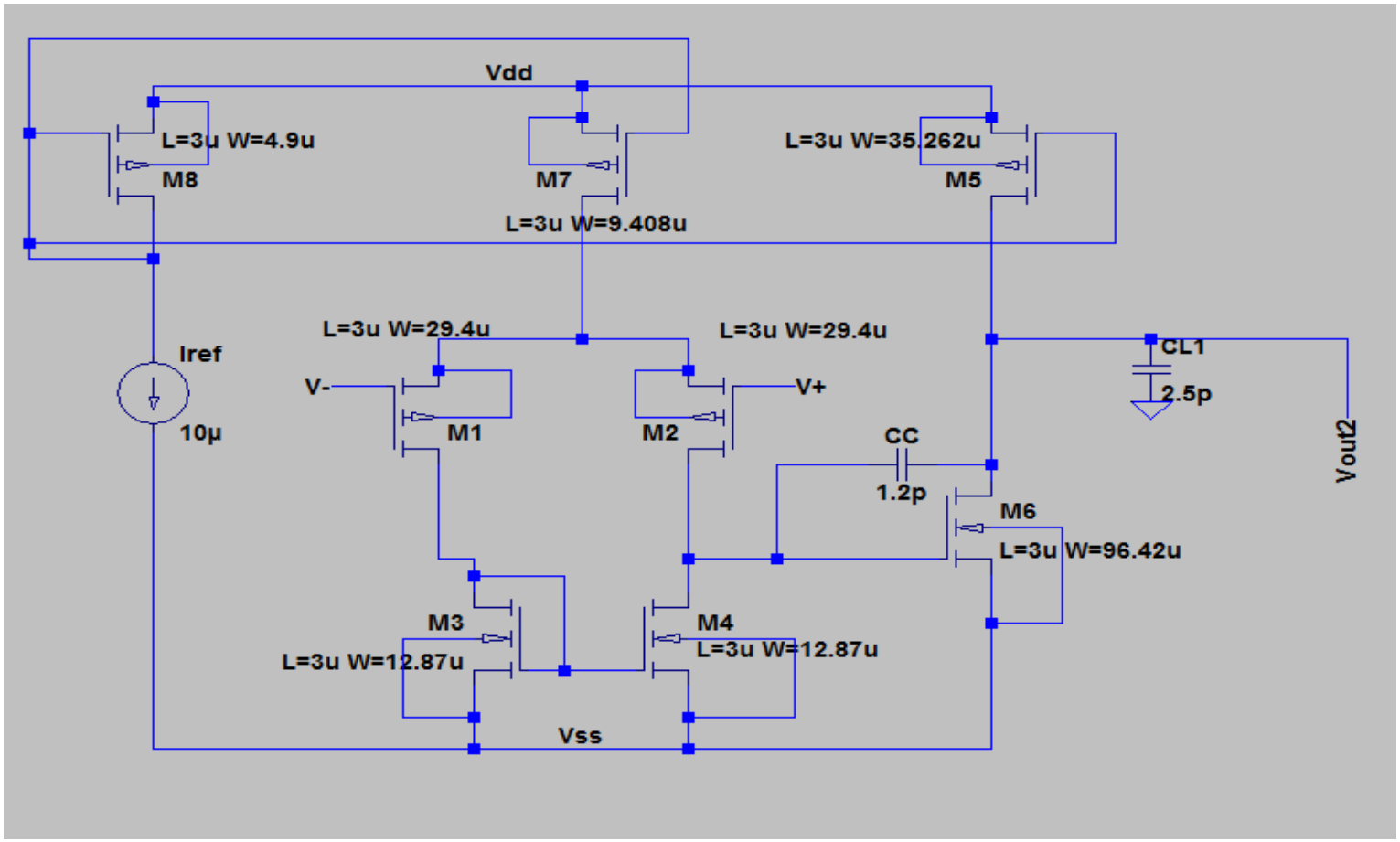
- Once we have designed transistors to implement the complete circuit in LTSpice

```
.model n_05 nmos (LEVEL=3 KP=112.2e-6 VT0=0.67
+CGBO=1.0e-10 CGDO=3.0e-10 CGSO=3.0e-10 CJ=5.6e-4
+CJSW=3.147e-10 DELTA=5.054 ETA=3.7e-6 GAMMA=0.6 KAPPA=0.3
+LD=1e-13 MJ=0.56 MJSW=0.1977 NFS=1e12 NSUB=1e17 PB=1
+PHI=0.7 RSH=7.5e-3 THETA=0.101 TOX=1.4e-8 TPG=1 U0=550 XJ=0.2e-6
+VMAX=1.44e5 )

.model p_05 pmos ( LEVEL=3 KP=49e-6 VT0=-0.97
+CGBO=1e-10 CGDO=2.4e-10 CGSO=2.4e-10 CJ=7.2e-4
+CJSW=2.9e-10 DELTA=0.11 ETA=0 GAMMA=0.62 KAPPA=30.1
+LD=5e-13 MJ=0.47 MJSW=0.31 NFS=1e12 NSUB=1e17 PB=1
+PHI=0.7 RSH=33.96 THETA=0.16 TOX=1.4e-8 TPG=-1 U0=135 XJ=0.2e-6
+VMAX=1e6)
```

Models of transistor for level 3 in LTSpice

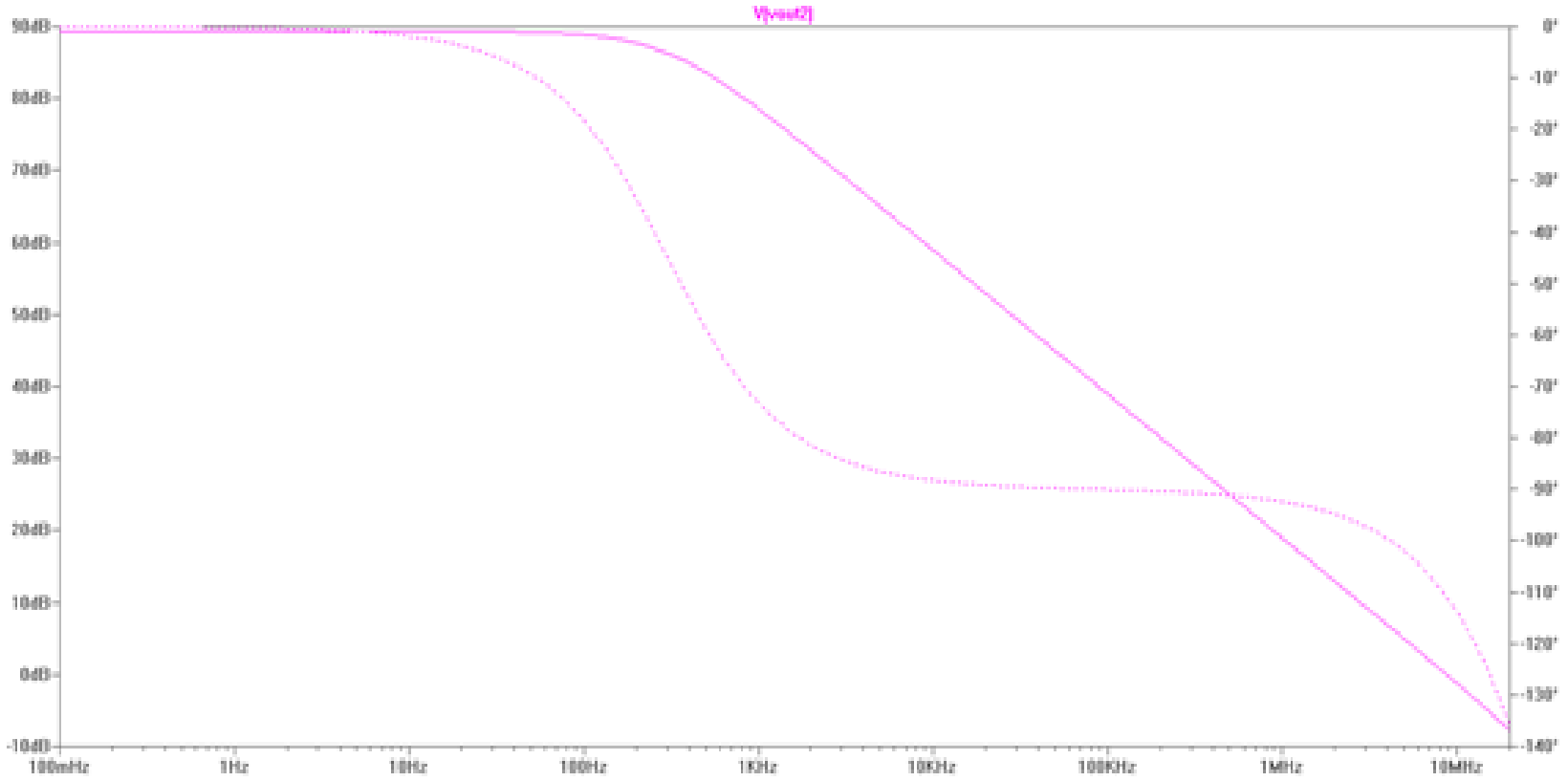
Implementation with spice simulator



Circuit in LTSpice

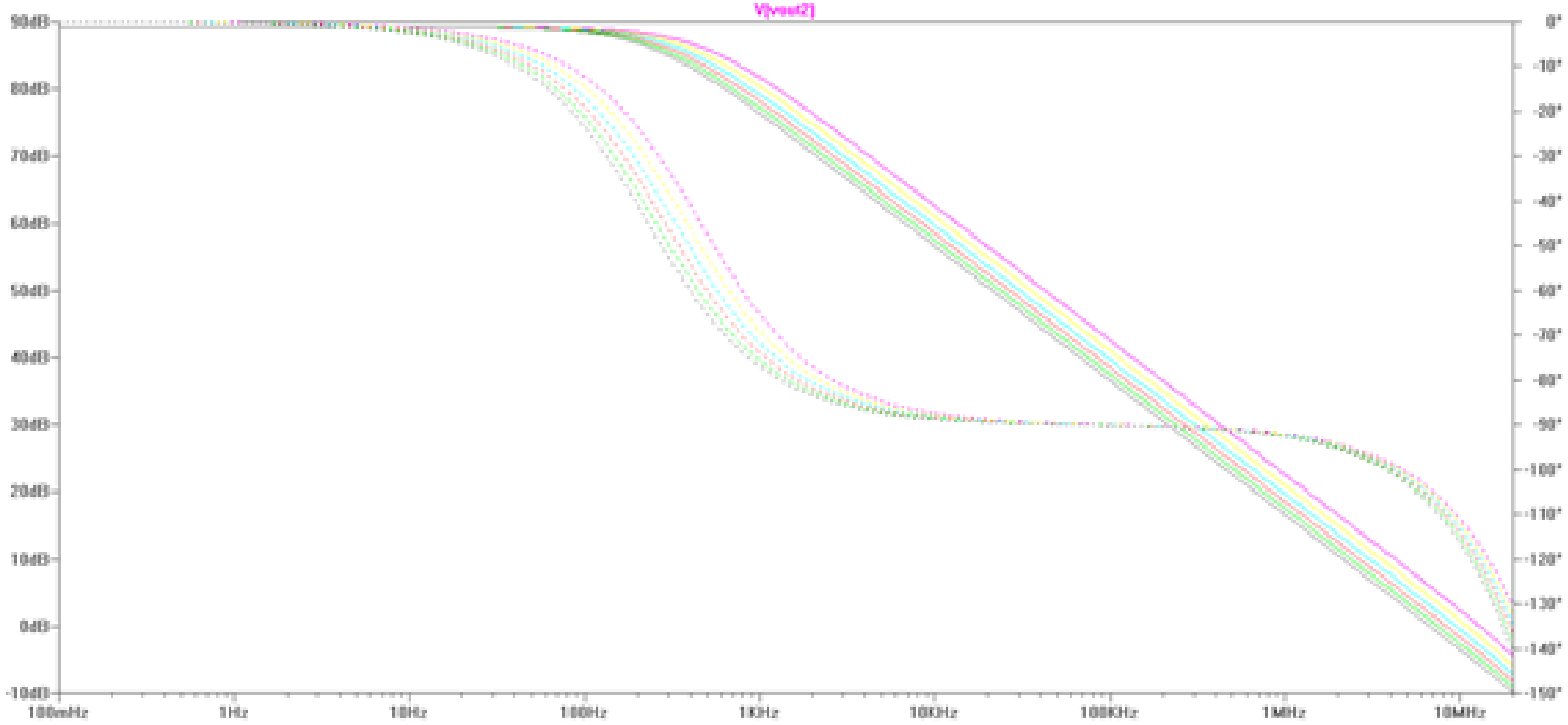
Implementation with spice simulator

- We carry out a frequency sweep to see if we fulfill the conditions of GBW and of phase margin of the design:



Implementation with spice simulator

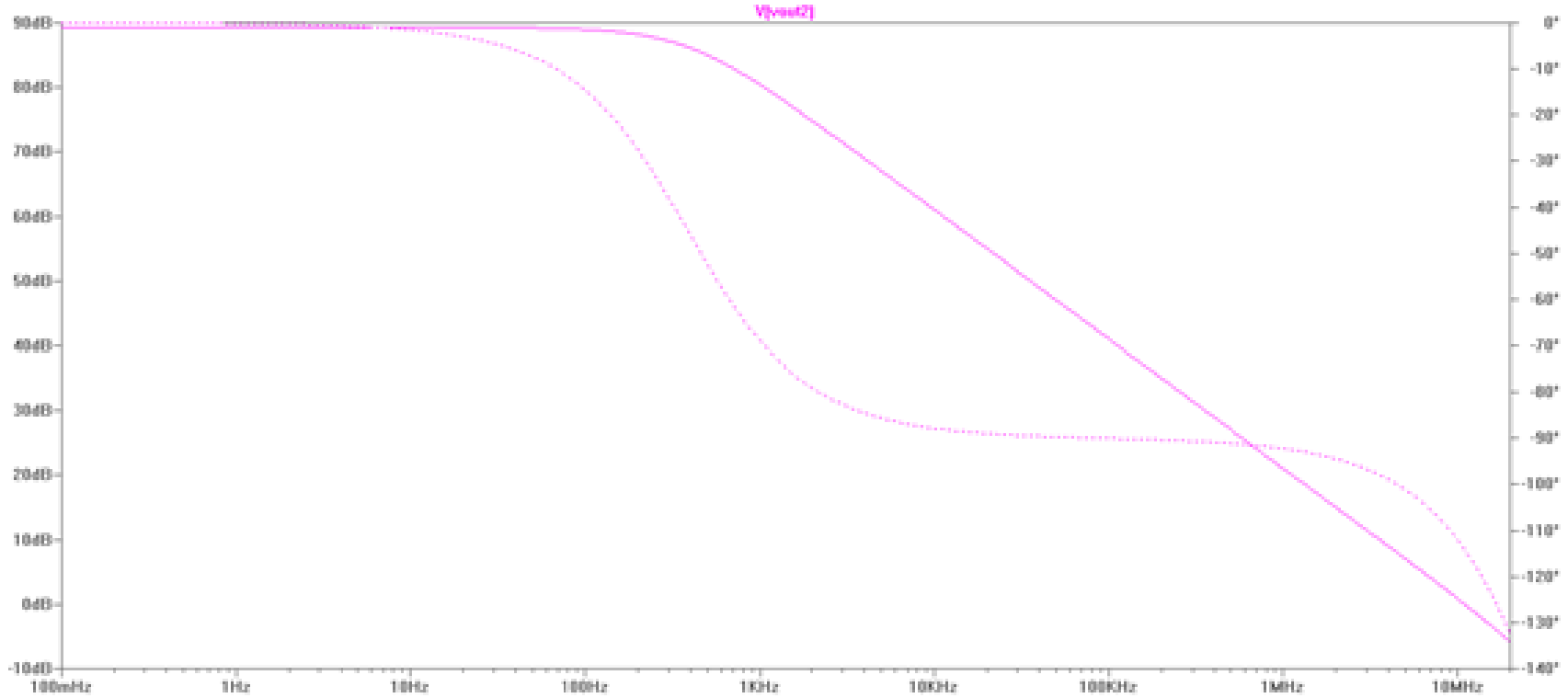
- We don’t obtain the goal, a GBW of 10MHz.
- We change the capacity of Cc.



GBW with different Cc sizes

Implementation with spice simulator

- Choosing Cc's value of 1.2pF we obtain a GBW higher than 10MHz and one stable phase margin.



GBW with new Cc size

Implementation with spice simulator

Output impedance

- Theoretical value $R_o = r_{o5} // r_{o6} = 0.3M\Omega$

- Simulation value

.tf V(vout2) vd

```
--- Transfer Function ---

'ransfer_function:                29098.7        transfer
'd#Input_impedance:               1e+020         impedance
)utput impedance at V(vout2):                    312322         impedance
```

- We can verify that theoretical and the practical have similar values.

- The linear gain has a value of 29098.7 that in $dB = 20\log_{10}(29098.7) = 89.9dB$, approximately like in the Bode diagram represented previously.

Implementation with spice simulator

Input common voltage range

- In this section for easier notation we will call $\Delta_n = V_{GSn} - V_t$.
- **Upper limit:** In order to kept transistor 7 in saturation mode it is necessary to verify $V_{DS7} \leq \Delta_7$.

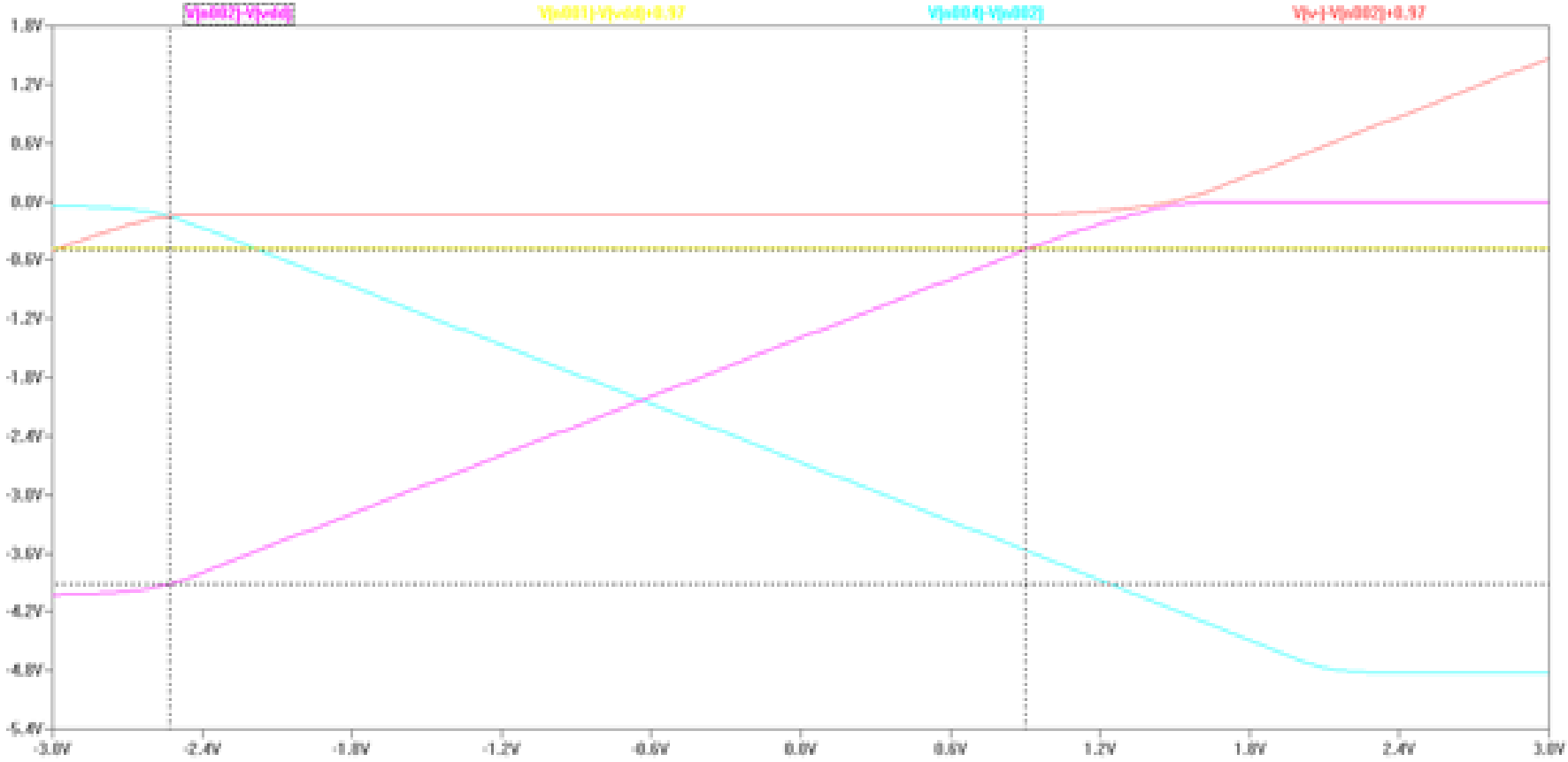
$$Vcmi|_{max} = V_{DD} - |\Delta_7| - |\Delta_1| - Vt_1 = 2.5 - 0.5 - 0.2 - 0.97 = 0.83V$$

- **Lower limit:**

$$Vcmi|_{min} = Vss + |\Delta_3| + Vt_n - |Vt_p| = -2.5 + 0.2 + 0.67 - 0.97 = -2.6V$$

Implementation with spice simulator

Input common voltage range



Simulation input common voltage range

Implementation with spice simulator

Output common voltage range

- In this section for easier notation we will call $\Delta_n = V_{GSn} - V_t$.

- **Upper limit:** This limit is fixed by trt 5

$$Vcm|_{max} = V_{DD} - |\Delta_5| = 2.5 - 0.5 = 2V$$

- **Lower limit:**

$$Vcmo|_{min} = V_{SS} + |\Delta_6| = -2.5 + 0.2 = -2.3V$$

Implementation with spice simulator

Total harmonic distortion (THD)

- THD is defined as an amplitude ratio rather than a power ratio, resulting in a definition of THD which is the square root of that given above:

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \cdots + V_\infty^2}}{V_1^2}$$

- We performed the calculation of the THD in LTSpice by order *.four*

Implementation with spice simulator

Total harmonic distortion (THD)

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- We performed the calculation of the THD in LTSpice by order *.four*

Implementation with spice simulator

Total harmonic distortion (THD)

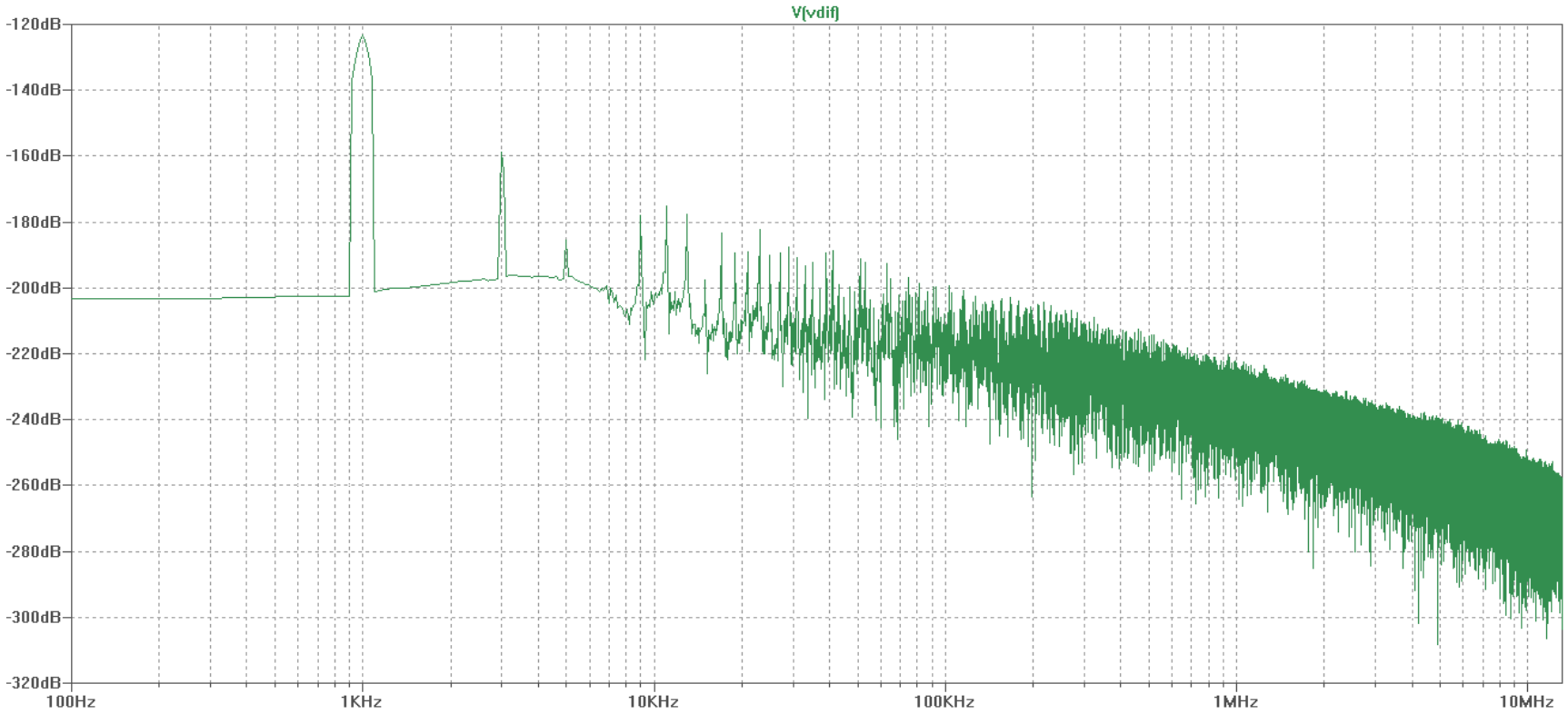


Figure a) Input FFT(logarithmic scale)

Implementation with spice simulator

Total harmonic distortion (THD)

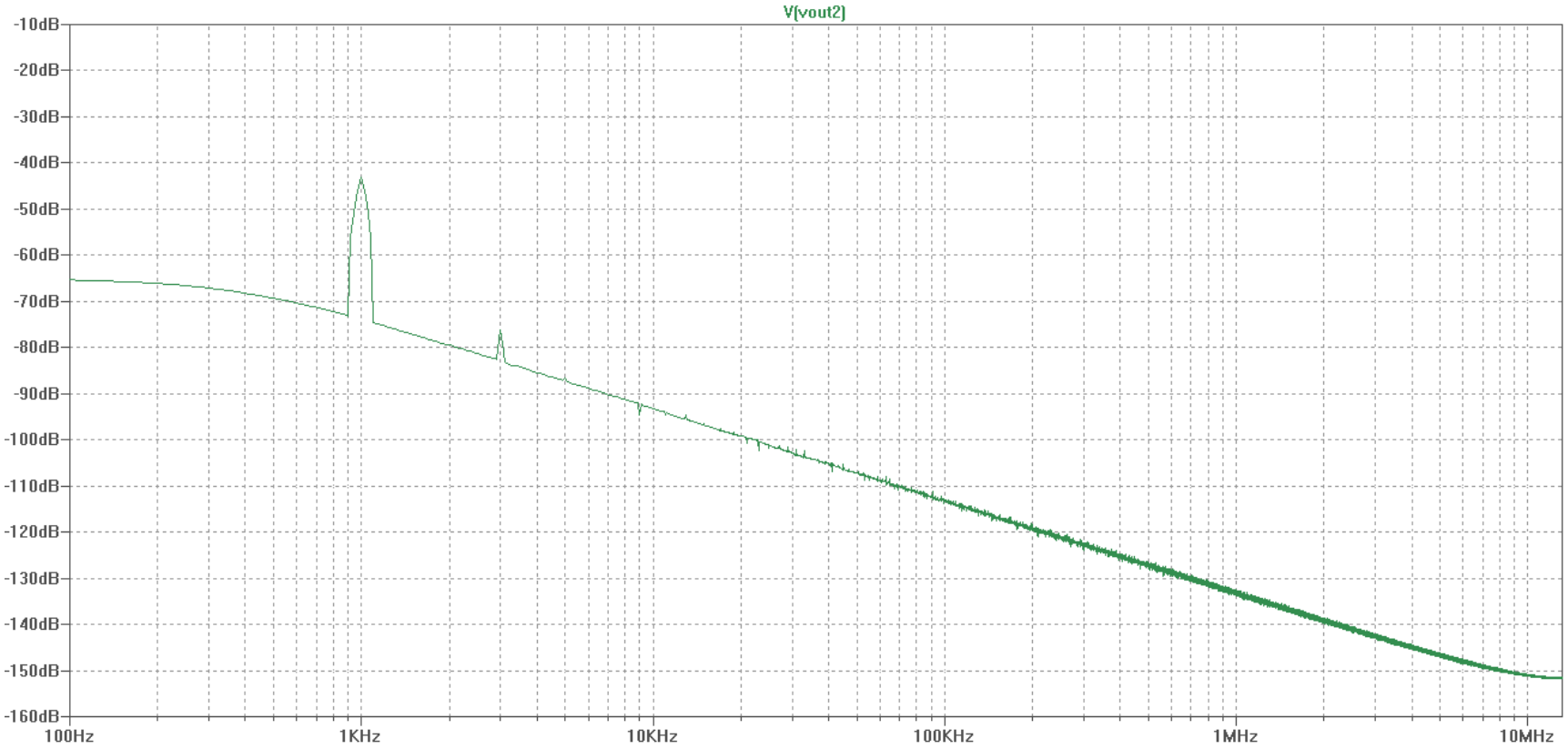


Figure b) Output FFT(logarithmic scale)

Implementation with spice simulator

Total harmonic distortion (THD)

- In figure a) We can see a pure tone at a 1 KHz fundamental frequency although the signal also has energy in some harmonics. Signal power is around -120dB which is absolutely normal due to the fact that the signal has a 1 μV amplitude and thereby a low power.

- Figure b) shows output signal FFT. This signal, obviously, has higher power and energy since it has passed within the amplifier and it has been amplified. Because of having passed thought the circuit it suffers from nonlinearities and its power is divided among the rest of harmonics. This makes THD rise.

Implementation with spice simulator

Total harmonic distortion (THD)

Fourier components of V(vdif)
DC component:-0.000131423

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]	Normalized Phase [deg]
1	1.000e+03	9.784e-01	1.000e+00	0.51°	0.00°
2	2.000e+03	2.740e-04	2.800e-04	-135.10°	-135.60°
3	3.000e+03	1.504e-02	1.537e-02	-162.30°	-162.81°
4	4.000e+03	2.437e-04	2.491e-04	143.30°	142.79°
5	5.000e+03	5.405e-03	5.524e-03	-22.77°	-23.27°
6	6.000e+03	1.608e-04	1.643e-04	110.14°	109.63°
7	7.000e+03	3.244e-03	3.316e-03	-37.31°	-37.81°
8	8.000e+03	3.151e-04	3.220e-04	57.52°	57.01°
9	9.000e+03	1.722e-03	1.760e-03	-60.99°	-61.50°
10	1.000e+04	2.930e-04	2.995e-04	29.74°	29.24°
11	1.100e+04	1.751e-03	1.790e-03	10.41°	9.90°
12			1.817e-04	-175.15°	-175.66°
13			1.071e-03	50.23°	49.73°
14			5.530e-04	-153.68°	-154.18°
15			8.665e-04	169.68°	169.18°
16	1.600e+04	7.575e-05	7.742e-05	138.74°	138.23°
17	1.700e+04	6.168e-04	6.304e-04	-127.56°	-128.07°
18	1.800e+04	3.409e-04	3.484e-04	41.08°	40.58°
19	1.900e+04	1.191e-03	1.217e-03	48.26°	47.75°
20	2.000e+04	2.525e-04	2.581e-04	-91.45°	-91.96°
21	2.100e+04	4.385e-04	4.481e-04	109.39°	108.88°
22	2.200e+04	4.462e-04	4.560e-04	-111.54°	-112.05°
23	2.300e+04	6.916e-04	7.068e-04	-104.11°	-104.62°
24	2.400e+04	1.089e-04	1.113e-04	108.96°	108.46°
25	2.500e+04	1.334e-04	1.364e-04	141.20°	140.69°

Total Harmonic Distortion: 1.702169%

THD INPUT SIGNAL

Implementation with spice simulator

Total harmonic distortion (THD)

Fourier components of V(vout2)
DC component:-0.20731

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]	Normalized Phase [deg]
1	1.000e+03	9.667e-03	1.000e+00	-68.35°	0.00°
2	2.000e+03	8.905e-05	9.212e-03	-63.43°	4.92°
3	3.000e+03	2.245e-04	2.322e-02	113.25°	181.60°
4	4.000e+03	7.737e-05	8.003e-03	-39.74°	28.61°
5	5.000e+03	8.946e-05	9.255e-03	-19.63°	48.72°
6	6.000e+03	5.887e-05	6.090e-03	-21.19°	47.16°
7	7.000e+03	8.057e-05	8.335e-03	-22.98°	45.37°
8	8.000e+03	3.826e-05	3.957e-03	-12.43°	55.93°
9	9.000e+03	7.902e-05	8.175e-03	-28.29°	40.07°
10	1.000e+04	2.460e-05	2.545e-03	-18.86°	49.49°
11	1.100e+04	8.033e-05	8.310e-03	-21.63°	46.73°
12			208e-03	-26.42°	41.94°
13			319e-03	-7.92°	60.43°
14			225e-03	-17.54°	50.81°
15	1.500e+04	1.064e-05	1.100e-03	27.16°	95.51°
16	1.600e+04	2.048e-05	2.118e-03	-7.30°	61.05°
17	1.700e+04	9.475e-06	9.801e-04	-19.26°	49.10°
18	1.800e+04	1.830e-05	1.893e-03	-9.86°	58.49°
19	1.900e+04	3.470e-05	3.589e-03	7.18°	75.54°
20	2.000e+04	1.647e-05	1.703e-03	-18.35°	50.00°
21	2.100e+04	2.843e-05	2.941e-03	17.88°	86.23°
22	2.200e+04	1.492e-05	1.543e-03	-18.83°	49.53°
23	2.300e+04	1.305e-05	1.350e-03	-7.98°	60.37°
24	2.400e+04	1.377e-05	1.424e-03	-12.21°	56.14°
25	2.500e+04	1.173e-05	1.214e-03	6.03°	74.38°

Total Harmonic Distortion: 3.345099%

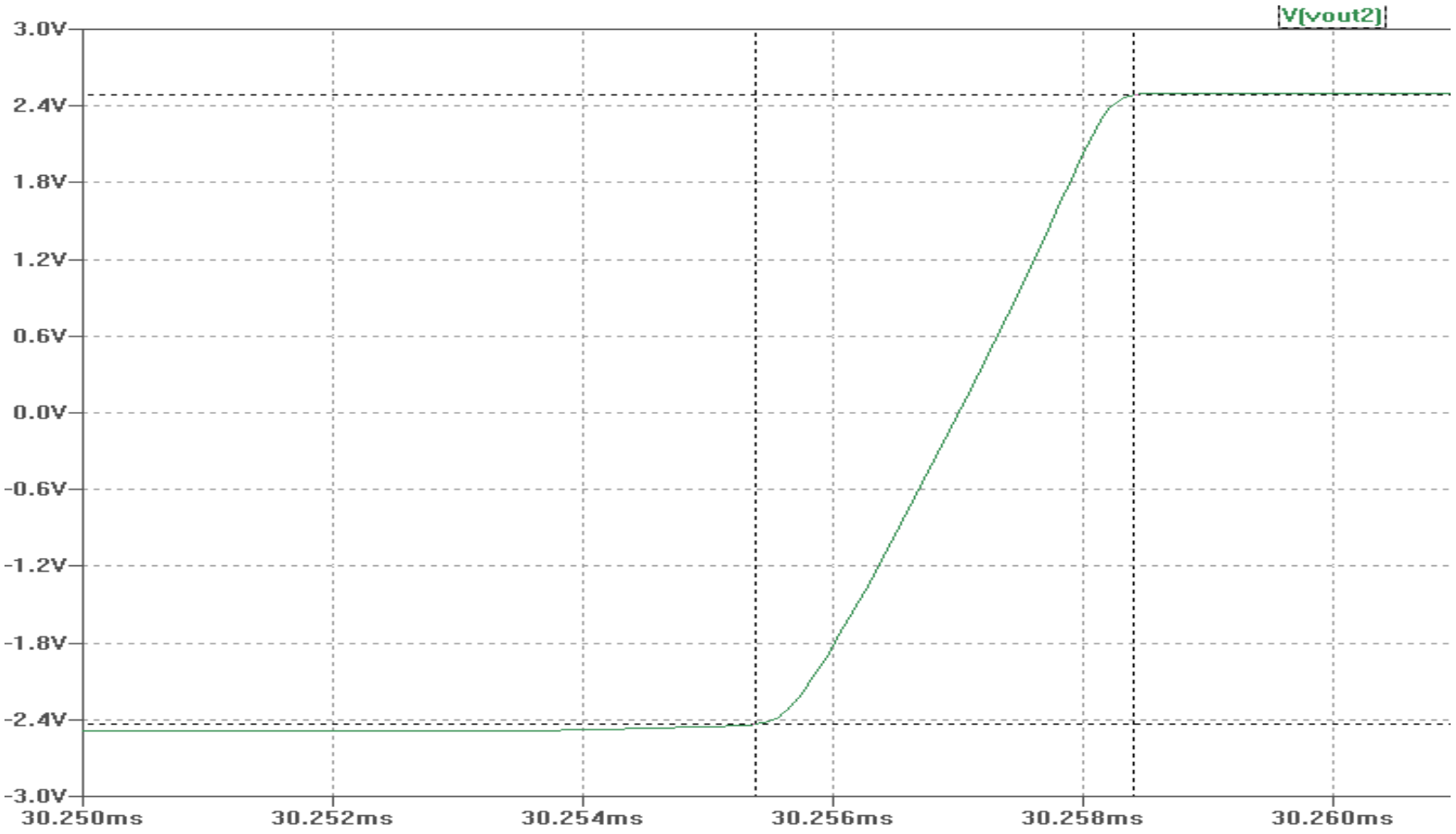
THD OUTPUT SIGNAL

Implementation with spice simulator

Slew Rate

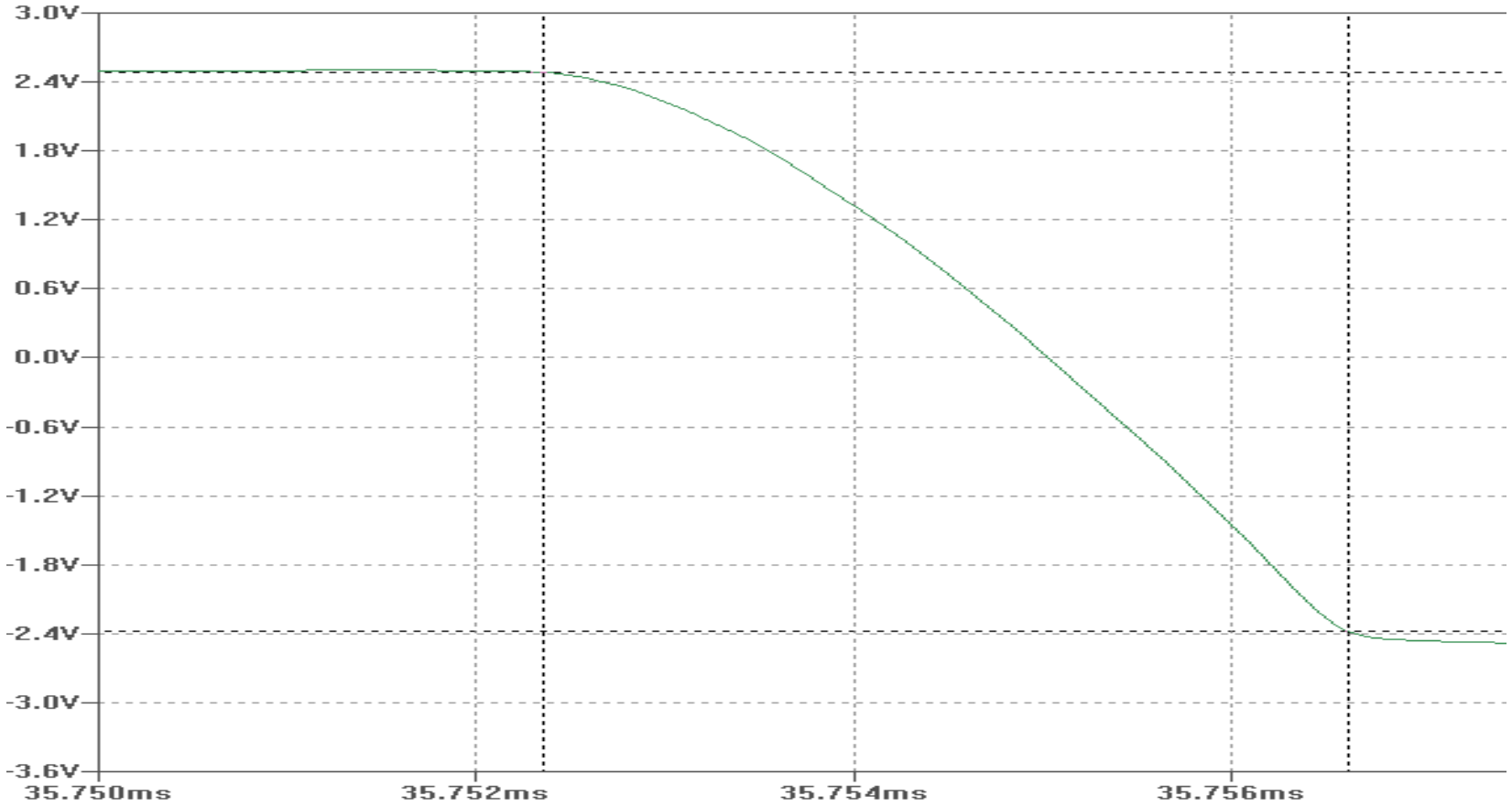
- Signal can not have infinite slop since the non-electronic components has not instantaneous reply. This line slope corresponds to the speed the transistor reacts to abrupt voltage changes.
- We have to analyze slew rates, the negative and the positive one, that are not equal but very similar.
- Positive slew rate is 1.63 V/μs.
- Negative slew rate is 1.15 V/μs.

Implementation with spice simulator



Positive slew rate

Implementation with spice simulator

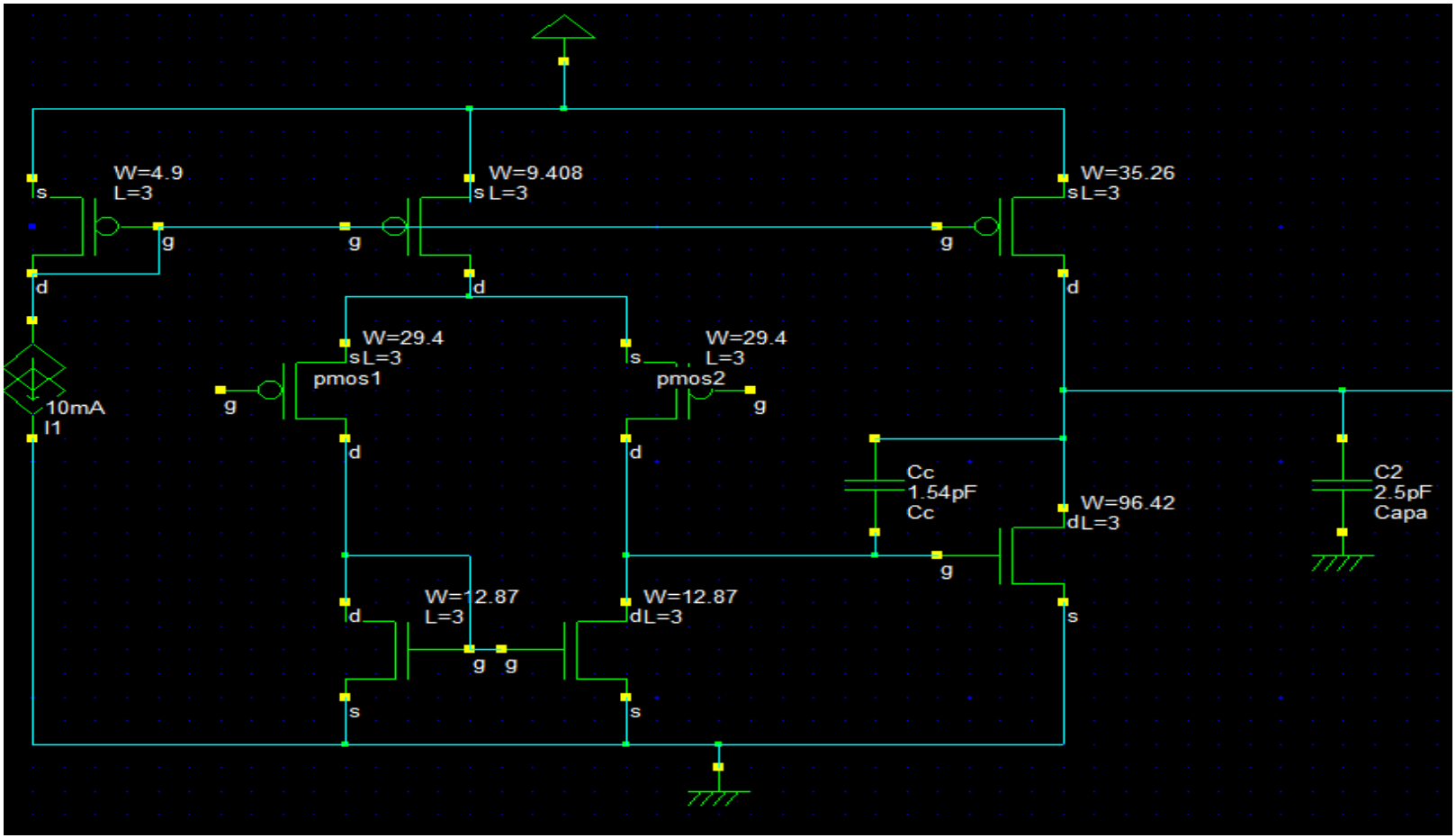


Negative slew rate

Layout design

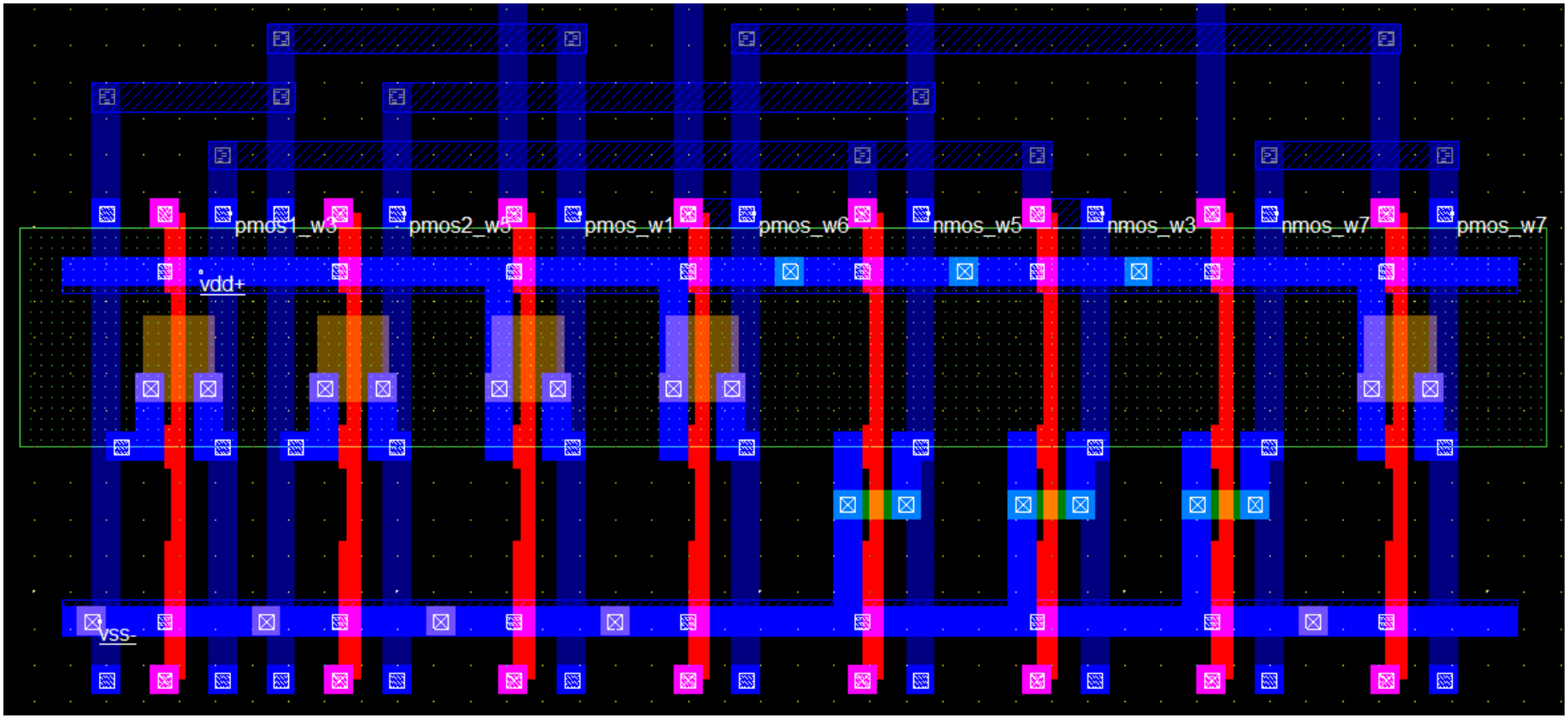
- To do our amplifier layout we will proceed to draw the schematic using the program Dsch2.
- Later, we will use the file created in Dsch2 to create the layout in Microwind. This program creates the layout from our file of Dsch2

Layout design



Dsch2 design

Layout design



Layout design

Conclusions

- The design of operational transconductance amplifier using 0.5 µm technology is presented in this project. In table it is shown how project starting point specifications have been accomplished. With the load capacitor of 2.5 pF, the design demonstrates a DC gain of 91.1 dB with a unity gain frequency of 10.7 MHz and phase margin of 77°.

- The amplifier has an input dynamic range going from -2.6V to 0.38V. Reaching all requirements above mentioned, we achieve an outstanding design of the amplifier.

Conclusions

SPECIFICATION	REQUIRED	ACHIEVED
A_V(dB)	>80	91
PM(°)	>65	77
SR^+(V/ms)	1.5	1.63
SR^-(V/ms)	1.5	1.15
ICMR(V)	>3	0.83/-2.6
R_{out}(Ω)	100K	0.3M
Iref(µA)	10	10

Amplifier specifications