






A family of AC amplifiers for ultra-low frequency operation

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Funding information

AEI/FEDER, Grant/Award Number: PID2019-107258RB-C32; Ministry of Universities, Grant/Award Number: BES-2017-080418; Public University of Navarra

Abstract

A family of capacitively coupled alternating current (AC) amplifiers featuring ultra-low (below 1 Hz) corner frequency is presented. This is achieved by using high-gain devices which actively boost feedback resistance and thus reduce corner frequency. This procedure is often termed, though with a different purpose, as “bootstrapping.” The proposed architectures are very general and admit several possible practical implementations. To demonstrate their usefulness, the circuits are implemented with two operational amplifiers (OA), but other active devices such as operational transconductance amplifiers (OTAs) can be alternatively used. All circuits have been theoretically analyzed, extensively simulated and measured, exhibiting high-pass cutoff frequencies as low as 30 mHz.

KEYWORDS

AC amplifiers, biosignal amplifiers, bootstrapping, DC-blocking, high-pass amplifiers, network transformation, nullors

1 | INTRODUCTION

Alternating current (AC) amplifiers are used in many instrumentation applications when a low-level signal needs to be amplified, blocking at the same time a DC or very low frequency signal component. Typical applications are, among others, seismology and remarkably biosignals.^{1–3} These circuits are basically high-gain and high-pass filters with a very low corner frequency. Even though it is believed that the design of such very low frequency circuits, that is, in the range of a few Hertz, is easier than in the range of KHz or MHz, this is not true particularly for integrated implementations, as was already pointed out in some early references.⁴ There are a number of particular limitations which make such designs difficult and tricky and require very specific design techniques to overcome or circumvent them. Among the limitations we can mention are the influence of flicker noise, the effect of DC current or voltage offsets, and remarkably, the need to implement very large time constants, which means large resistors and/or capacitors. This also means large silicon area and added thermal noise.

Another problem to achieve very low and particularly ultra-low frequency circuits (in the range of less than 1 Hz) is the inherent difficulty in testing and measuring very large time constants and thus long measurement times. Moreover,

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general purpose instrumentation is not very friendly in such ranges, which are the domain of instrumentation applications as diverse as seismology, modal testing of large structures and biomedical signals.

Coming back to the problem of implementing very large time constants in all kinds of circuits, be it amplifiers, filters, or DC blockers, and regardless of the application or implementation technology, it is possible to distill two basic principles which allow the design of such large time constants from passive, and in some cases active, resistive and capacitive impedances with lower and affordable values. These common principles are sometimes hidden in very specialized and specific designs, which abound for instance in the case of biosignal applications.⁵⁻⁷ To make things even more confusing, different names are used to describe what actually is a common principle when one leaves apart the concrete implementations, which contributes to entangle the analysis and comparison of the plethora of published circuits.

To cut it short, the first principle is based on scaling up, or down, the current flowing through a resistor or capacitor while keeping the voltage at its driving node, modifying in this way its equivalent impedance seen from such node.^{8,9} The other way around, less frequent, is to keep currents unchanged while scaling the voltages. This can be accomplished in multiple ways: resistive dividers, current mirrors with large current ratios, or active resistors with scaled W/L ratios. The principle can be easily illustrated with the example of the basic AC amplifier (i.e., high-pass filter) shown in Figure 1, for its simplest version (Figure 1A) and its modification with a resistive T network in lieu of the single resistor (Figure 1B), whose equivalent feedback resistance is

$$R_{feq} = R_f \left(1 + \frac{R_1}{R_f} + \frac{R_1}{R_2} \right). \quad (1)$$

The circuit can be interpreted as if resistances R_1 and R_2 , provided that $R_2 \ll R_1$, drive a portion $R_2/(R_1 + R_2)$ of the current across R_f to the inverting operational amplifier (OA) input. Since R_2 is necessarily small in comparison with both R_f and R_1 , intermediate node plays a role of an approximate virtual ground leaving the voltage of R_f almost unchanged with respect to the basic topology in Figure 1A. As a consequence, the resistance “seen” from the inverting node is higher than R_f .

It is illustrative to realize that the circuit in Figure 1C, completely equivalent to circuit in Figure 1B, can be interpreted as if R_1 and R_2 are acting now as a voltage divider of the circuit output, dropping the voltage at the intermediate node. In this way, current across R_f reduces proportionally to the voltage dividing ratio, that is, $R_2/(R_1 + R_2)$.

The circuit in Figure 1B, or generally speaking the resistive T networks, have been often revamped in recent publications such as Wong et al.⁸ and Li et al.^{10,11} by simply implementing the resistors with transistors. The principle invoked is the so called “current steering,” which is nothing essentially new from our viewpoint. Something similar happens with some designs of very low G_m operational transconductance amplifiers (OTAs) to emulate high resistances, which are essentially based on current scaling.¹²

Anyway, call it current scaling, current steering, or even voltage scaling, the common property is that the scaling factor for the impedance depends on resistor ratios or, equivalently, W/L ratios. This limits the possible multiplication values to not more than three orders of magnitude, which is enough in some applications but not in others. However, the solution brings along a number of drawbacks due to mismatches mainly in the form of DC offsets.

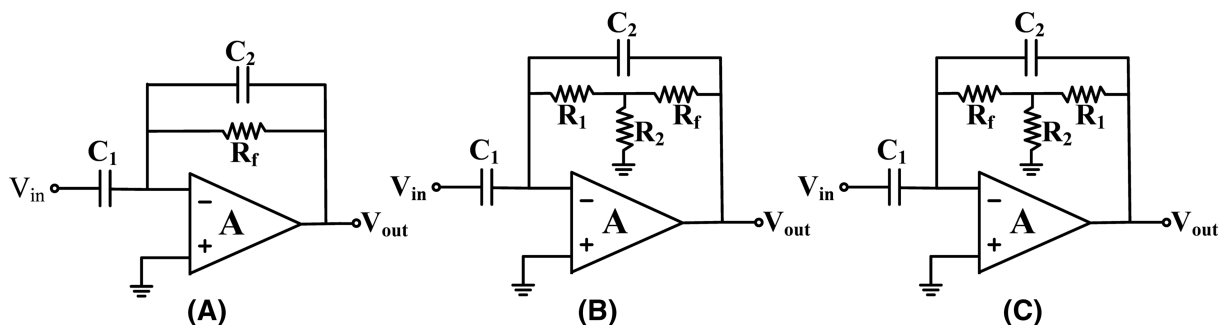


FIGURE 1 Conventional AC amplifier topologies using (A) a feedback resistor, (B) resistive T network, and (C) alternative T network

The second principle, which will be exploited in this paper, is based on the use of high gain stages, mainly OAs and OTAs, used in local feedback configurations to force very close voltages at two nodes (corresponding to the input of the amplifier). The net effect is the modification of the equivalent impedance at a given node, increasing the R or C value, as the case may be. This procedure is often termed as “bootstrapping” and is also used with a different goal: increasing the gain of an amplifier without cascading additional stages.^{13,14} Sometimes, it is also denoted as partial positive feedback, making reference to the fact that in most cases some kind of positive local feedback is applied, though the circuit is globally stable. However, the circuits tend to exhibit additional peaking in the frequency response if feedback is not properly adjusted.

The use of high gain devices is in many cases equivalent to the use of close-to-unity gain devices. This is so because, as we said before, the effect of the high gain amplifier is to force two equal, or in practice very close, voltages at two nodes. The well-known Miller effect, for a gain close to 1, can be seen as a particular case. This principle allows for higher multiplication factors of the impedance (those of the amplifier gain), but at the cost of more complexity (is inherently an active technique) and a more careful design in terms of stability.

In this paper, we will make use of this last principle to propose several novel topologies for the design of high-pass or AC coupled amplifiers with ultra-low corner frequency. The topologies are implemented and demonstrated here in discrete form with OAs, but their architectures can also be implemented with other devices (e.g. OTAs) in both discrete and integrated forms.

The boosting factor for the time constants can be, theoretically, up to the order of A^2 , A being the gain of the OA. In practice, the boosting factor is not so high due mainly to parasitic (output) impedances and frequency roll-off of the OA response.

The paper is organized as follows. In Section 2, and based on the idea of impedance boosting, three novel topologies of AC-coupled amplifiers (high-pass filters) are proposed. Their implementation makes use of (two) OAs but can be realized with other active devices. In Section 3, a network transformation is applied to the above topologies to obtain a set of three new ones, which retain the basic properties of the original ones but offer a distinct performance. In Section 4, the topologies are analyzed in terms of frequency response, and DC offsets, and compared accordingly. Section 5 is devoted to the experimental analysis of the topologies, which demonstrate their ability to achieve ultra-low cutoff frequencies, and is followed by Section 6 drawing the most important conclusions.

2 | BASIC TOPOLOGIES FOR AC AMPLIFIERS

Let us begin with the basic circuit in Figure 1A, which is often termed as AC-coupled capacitive feedback amplifier. It has, essentially, a first-order high-pass response. Assuming infinite gain for the OA, the corner frequency and band-pass gain are given by

$$\omega_c = \frac{1}{R_f C_2}, \quad (2)$$

$$\text{Gain} = -\frac{C_1}{C_2}. \quad (3)$$

R_f plays the role of providing a discharge path for the feedback capacitor, setting in this way the high-pass corner frequency.

However, if the gain of the OA, A , is high but finite, and assuming its correct DC operation, the resistor can be alternatively grounded as shown in Figure 2A. The main difference now being that voltage across R_g is very low, resulting in a resistance seen from the inverting input terminal equivalent to R_g multiplied by A . In Table 1, we show the amplifier gain and corner frequencies of amplifiers in Figures 1A and 2. Both offer the same high-frequency gain, which slightly departs from the ideal $-C_1/C_2$, but differences in cut-off frequencies are evident.

It is obvious however that circuit in Figure 2A cannot properly work if a DC feedback path is not provided. Alternatively, it can work for lower A values or if an auto-zero mechanism is included.¹⁵ Therefore, a straightforward modification is shown in Figure 2B including a buffer and an additional resistor R , where R_g accounts for an externally connected resistance, or the buffer input impedance. Resistor R does not affect either corner frequency or gain, ideally.

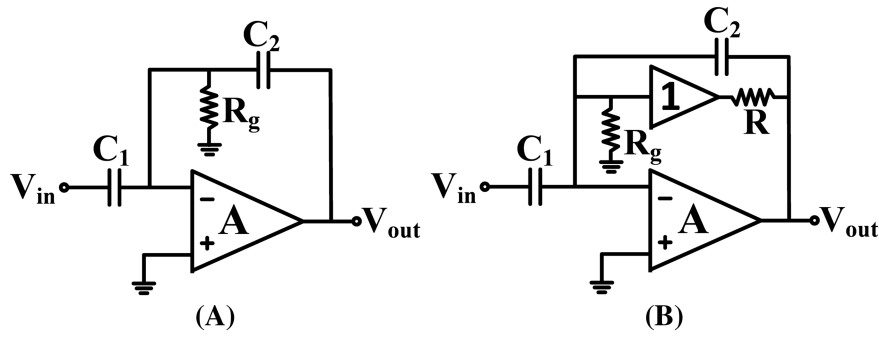


FIGURE 2 Modified AC amplifier topologies

TABLE 1 Gain and cutoff frequency of the amplifiers in Figures 1 and 2

Circuit	Gain	Cutoff frequency, ω_c
Figure 1A	$-\frac{C_1/C_2}{1+\frac{1}{A_1}\left(1+\frac{C_1}{C_2}\right)}$	$\frac{1}{R_f C_2} \cdot \frac{1}{1+\frac{C_1}{(1+A_1)C_2}}$
Figure 2A,B	$-\frac{C_1/C_2}{1+\frac{1}{A_1}\left(1+\frac{C_1}{C_2}\right)}$	$\frac{1}{R_g C_2 A} \cdot \frac{1}{1+\frac{1}{A_1}\left(1+\frac{C_1}{C_2}\right)}$

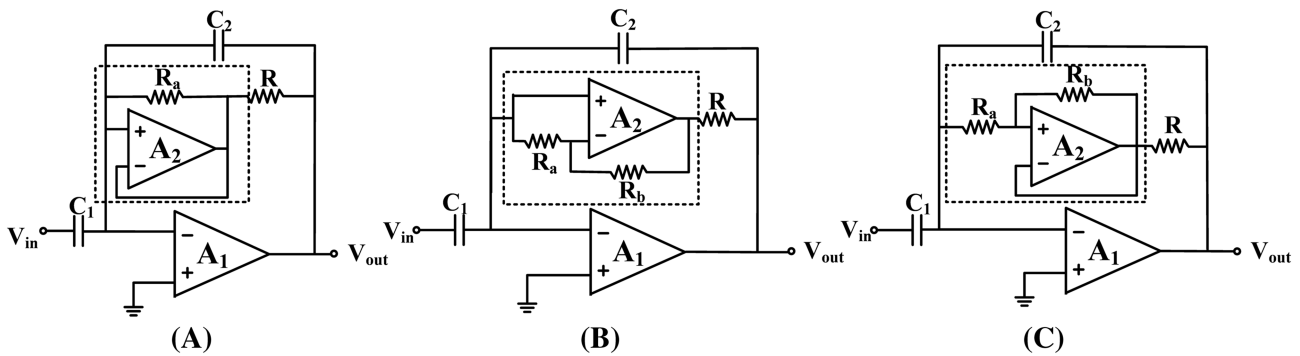


FIGURE 3 Schematic of the first (odd) three proposed ultra-low corner frequency AC amplifier topologies: (A) Topology 1, (B) Topology 3 and (C) Topology 5

TABLE 2 Buffer impedance and cutoff frequency of the amplifiers in Figure 3

Circuit	Buffer impedance	Cutoff frequency, ω_c
Figure 3A	$R_a(1+A_2)$	$\frac{1}{R_a C_2 A_1 (1+A_2)} \cdot \frac{1}{1+\frac{(1+C_1/C_2)}{A_1}}$
Figure 3B,C	$R_a(1+A_2)+R_b$	$\frac{1}{R_a C_2 A_1 A_2} \cdot \frac{1}{\left(1+\frac{(1+R_a/R_b)}{A_2}\right) \cdot \left(1+\frac{(1+C_1/C_2)}{A_1}\right)}$

Keeping OAs as building active elements, the scheme in Figure 2B can be implemented in at least three basic forms, as shown in Figure 3, where the buffers are highlighted in dotted lines. It is important to note that the three buffers allow for a correct DC feedback for OA 1, with the help of the output OA impedance.

Another interesting, and relevant in this context, property of the buffers is that their input impedance is, essentially, R_a multiplied by the OA gain, as shown in Table 2. This property reflects directly in the cutoff frequency of the amplifier, which is scaled down by a factor that is essentially the product of the two amplifier gains, as shown in Table 2. The frequency response of the circuit remains of first order, since the amplifiers' gain has been assumed finite but frequency independent.

The merit of the three topologies is that the two OAs work together to boost resistance R_a and thus reduce considerably the cutoff frequency achievable with the passive elements: OA 2 bootstraps resistor R_a to increase the (grounded) input impedance of the buffer, which is further increased by the bootstrap effect of OA 1. Another way to explain the circuit's behavior is to realize that voltage across R_a is very low due to OA 2 input, forcing a very low current in the feedback path, meaning a very high resistive impedance seen from the inverting input terminal of OA 1. Since such equivalent impedance is grounded, the small voltage at OA 1 increases further the impedance value.

We have shown in a recent publication some basic results for the circuit in Figure 3A,¹⁶ but to the best of our knowledge, the circuit set has not been published before. In the same way, the topologies to be presented in the next section are novel.

3 | A NEW SET OF AC AMPLIFIERS BY A NETWORK TRANSFORMATION

Topologies in Figure 3 contain two OAs and thus are susceptible to be transformed by swapping their output nodes. The transformation can be easily formulated resorting to the nullor concept^{17,18} (an OA is basically the combination of a nullator plus a grounded norator) and making all possible pairings between nullators and norators. The transformation preserves the transfer function assuming ideal OAs. However, assuming OAs with gains A_1 and A_2 , it is expected that, if not the exact transfer function, the high-pass character is at least preserved.

We will avoid deepening into the details of the transformation, which can be found elsewhere, and just limit ourselves to give the resulting circuits, which are shown in Figure 4. A first coarse analysis of the topologies shows that no buffer can be identified and isolated, as a result of the transformation. However, the fundamental property of OA 2 forcing a reduced voltage across R_a remains unchanged, whereas OA 1 is no longer the circuit output and as such does not contribute to boost the overall resistance.

This intuitive analysis has a direct reflection in the transfer function of the three circuits, as shown in Table 3. It is apparent how the cutoff frequency is in all cases reduced "only" by a factor A_2 , confirming the analysis in the previous paragraph. Gain can still be approximated by $-C_1/C_2$, although there is now a dependence on the ratio R_b/R_a , ideally.

4 | COMPARATIVE ANALYSIS OF THE SIX TOPOLOGIES

Expressions given in Tables 2 and 3 constitute a first approach to circuits' behavior but do not suffice to completely explain it in a satisfactory manner. For a more sensible analysis, we should incorporate the effects of amplifiers gain

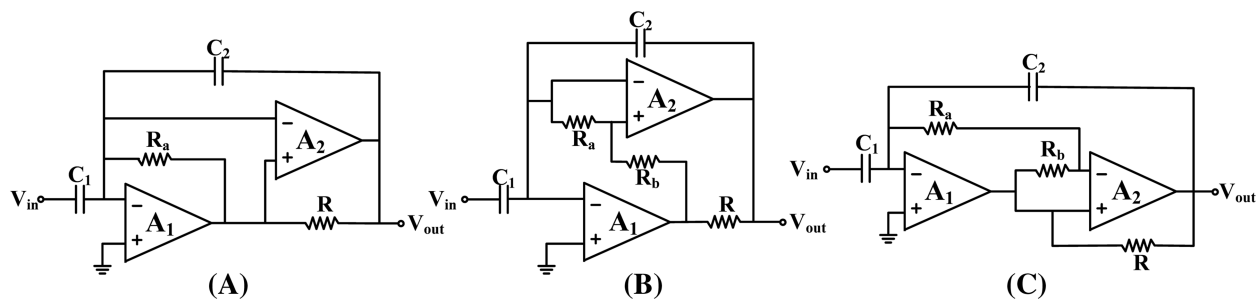


FIGURE 4 Schematic of the second (even) three proposed ultra-low corner frequency AC amplifier topologies: (A) Topology 2, (B) Topology 4, and (C) Topology 6

TABLE 3 Gain and cutoff frequency of the amplifiers in Figure 4

Circuit	Gain	Cutoff frequency, ω_c
Figure 4A	$-\frac{C_1/C_2}{1 + \frac{C_1/C_2}{A_2(1+A_1)}}$	$\frac{1}{R_a C_2 A_2} \cdot \frac{1}{1 + \frac{C_1/C_2}{A_2(1+A_1)}}$
Figure 4B,C	$-\frac{C_1/C_2}{1 + \frac{C_1/C_2}{A_2(1+A_1)} \frac{(1+R_b/R_a)(1+C_1/C_2)}{A_2(1+A_1)}}$	$\frac{1}{R_a C_2 A_2} \cdot \frac{1}{1 + \frac{(1+R_b/R_a)(1+C_1/C_2)}{A_2(1+A_1)}}$

roll-off and output impedance. However, the resulting expressions are too cumbersome and difficult to simplify and interpret.

Alternatively, we have resorted to extensive numerical (PSpice[®]) and symbolic simulations (Sapwin^{®19}), together with intuitive analysis, to gain some insight into the circuits' behavior and make comparisons between the six topologies. We have used, as a reference, the popular TL081 OA, for both numerical simulations and then experimental measurements.

First, we focused on checking to which extent the reduction in the cut-off frequency, as promised by equations in Tables 2 and 3, is achieved. To this end, we have carried out Spice simulations with characteristic frequencies ($1/R_a C_2$), well below the gain bandwidth product of the OA. A safety margin of 10% GBW has been considered. Gains tested, that is, ratios C_1/C_2 , are in the range from 20 to 40 dBs.

In all cases, the desired high-pass response is obtained, with a gain very close to the predicted one and a corner frequency in the range of millihertz. However, the reduction factor in the frequency with respect to $1/R_a C_2$ is far from the one predicted by the formulas, particularly in the case of the topologies in Figure 3 (which we will name as "odd" topologies in the remainder of the paper). According to such simulations, the ratio between the characteristic frequency and the simulated corner frequency is in the order of 4×10^5 , only a factor 3 with respect to a single amplifier gain, when the theoretical prediction is $A_1 \cdot A_2$. In the case of the circuits in Figure 4, named as "even" topologies, the factor is lower, 1.5×10^5 , but much closer to A_2 , the value predicted theoretically.

Resorting to symbolic simulations, we have confirmed that the introduction of the frequency-dependent effects of both output impedance and frequency roll-off (single dominant pole) of the OA gives results very close to the numerical simulations with Spice and thus confirms the disparities between the theoretical predictions and the simulations in terms of gain and cutoff frequency. Figure 5 shows the model employed for the OA at hand. It is not easy to know, and of course measure, the output impedance of the OA since data sheets offer contradictory curves depending on the version. Anyway, it seems that output impedance at very low frequencies can be even higher than those included in the spice model.²⁰

In the same way, high-frequency behavior and stability margins are difficult to predict analytically. Therefore, resorting again to simulations, we have seen that, under the conditions explained above, all circuits are stable. In the case of even topologies, they exhibit some peaking at high frequencies for R values higher than a few kilohertz. In general, even topologies show higher bandwidths than those of odd ones, though this is not an advantage since it increases noise. However, both peaking and high-frequency rolloff can be easily shaped with a capacitor in parallel with R_a . Figure 6 shows a representative comparative simulation between circuits of Figures 3B and 4B (they correspond to a transformed pair), making use of the same component values. It is clear that the high-pass corner frequency for Figure 3B is only slightly better (lower), while Figure 4B exhibits a higher bandwidth, but without peaking.

Regarding the influence of amplifiers voltage offsets, a routine analysis²¹ shows a distinct behavior of even and odd topologies. This is not strange due to the different role that the two amplifiers play in the multiplicative effect of resistance R_a , which has a reflection in the way offsets transmit to the output. Odd topologies can be modeled, to this purpose, as shown in Figure 7A, where r_{o2} is the resistive output impedance of the amplifier 2, and V_{o1} and V_{o2} are the input voltage offsets of the two amplifiers. Output resistance r_{o1} has not been included in the model, and thus in the analysis, since it does not have influence in the offset analysis. The voltage output can be approximated as

$$V_{out} = \frac{1 + A_1}{A_1} V_{o1} - \frac{A_1 \cdot A_2}{(1 + A_1)} \frac{R}{r_{o2}} V_{o2}. \quad (4)$$

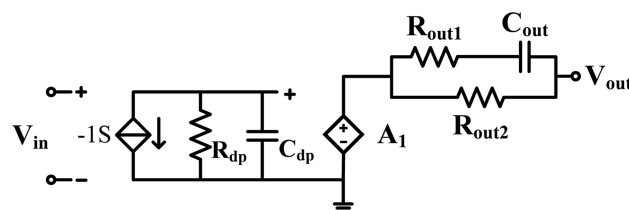


FIGURE 5 Operational amplifier model used in Sapwin

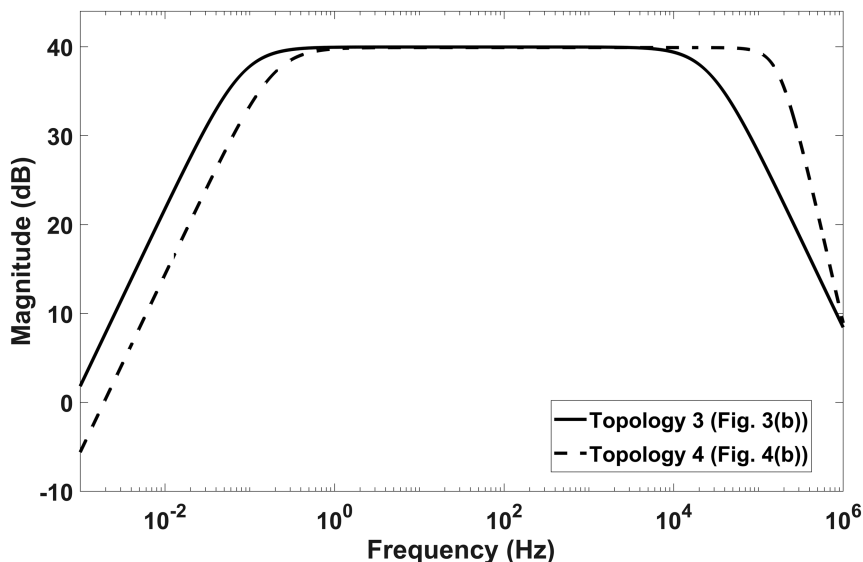


FIGURE 6 Simulated frequency response for circuits in Figures 3B (Topology 3) and Figure 4B (Topology 4)

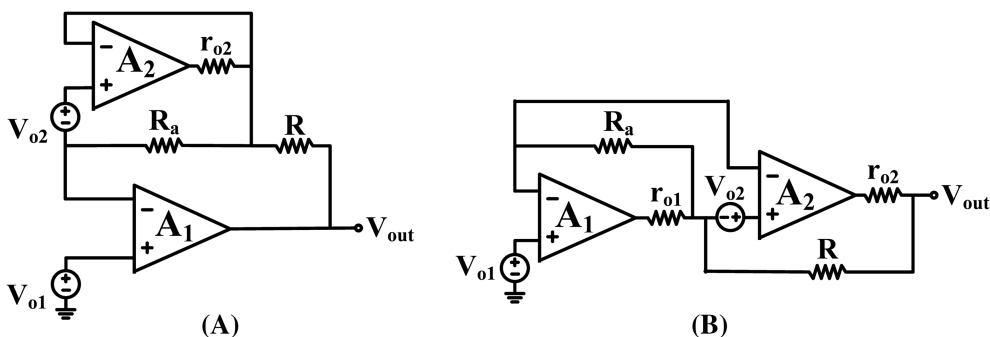


FIGURE 7 Schematics for the offset analysis of amplifiers in (A) Figure 3A and (B) Figure 4A

Whereas amplifier 1 offset has no relevant influence, V_{o2} is amplified by A_2 at the output and R can also contribute if it is not chosen low enough. Regarding the even topologies, they can be modeled as shown in Figure 7B (we have chosen Figure 4A for simplicity but the others are equivalent). The calculation of the output voltage gives the following result:

$$V_{out} = \frac{1}{1 + \frac{r_{o2}}{R}} V_{o1} + \frac{A_2}{1 + \frac{r_{o2}}{R}} V_{o2}. \tag{5}$$

In this case, apart from a less relevant influence of R , V_{o2} is amplified by the effect of amplifier 2. According to the expression, the circuit would saturate for moderate offset values and/or high gains.

Both simulations and experimental measurements show that DC values at the output can be kept within saturation limits by a proper selection of R and of course making use of low offset voltage devices. In our case, the compensation mechanism included in the TL081, common to other amplifiers, has demonstrated its effectiveness to adjust the DC level at the output. Anyway, we have found that this standard DC model for amplifier offsets overestimates the actual DC level at the output, due likely to a gain-offset interaction,²² not to mention the simplicity of the model itself.

5 | EXPERIMENTAL RESULTS

The six circuits in Figures 3 and 4 have been thoroughly measured in similar conditions as those used for the simulations. These conditions allow for actual high-pass corner frequencies in the range from few millihertz to few hertz and gains from 20 to 40 dB. Both time- and frequency-domain measurements have been taken. The measured frequency responses have been obtained with a dynamic signal analyzer, HP 89440A, using an external signal source Agilent 33522A to generate sine chirps. The analyzer is working at its very low frequency limit (2 mHz), and therefore the calculation of the corner frequency is complemented with time-constant measurements under transient step excitations. In such frequency ranges, every measurement takes several minutes, and both scopes and network analyzers are difficult to tune.

As a first general conclusion, the three odd circuits have a very similar behavior, in the same way even circuits perform very closely too. Circuit I, in Figure 3A (Topology 1) was described in Martincorena-Arraiza et al,¹⁶ and thus we will give here details on its counterpart in Figure 4A (Topology 2). In the left part of Table 4, we include the approximate values for the passive components used, with the calculation of the *reference* frequency $1/R_a C_2$. Then, the right side part of the table comprises the measured high-pass corner frequencies resulting from both time- and frequency-domain procedures. Two values, denoted as “+” and “-,” are shown, corresponding to positive and negative step excitations. Figure 8 shows a representative response to positive and negative steps. We attribute the difference to a nonlinear behavior under such fast steps.

Anyway, the differences between time- and frequency-domain measurements can be considered reasonable, taking into account the measurement limitations of the dynamic analyzer and the oscilloscope. Either way, a value as low as a few tenths of millihertz is achieved. Lower values can be surely obtained but are cumbersome to measure. In Figure 9,

TABLE 4 Configuration and measurement values of the proposed ultra-low cutoff frequency AC amplifier in Figure 4A (Topology 2)

	C_2 (nF)	C_1 (nF)	R_a (K Ω)	R (Ω)	$1/(2\pi R_a C_2)$	Cutoff frequency estimation by transient measurements	Cutoff frequency estimation by freq. sweep measurements	A_v
T2.1	0.96	96.3	5.57	465	29.16 KHz	2.16 Hz (+); 1.87 Hz (-)	2.3 Hz	39.3 dB
T2.2	0.96	96.3	38.4	465	4.23 KHz	340 mHz (+); 294.7 mHz (-)	295 mHz	39.3 dB
T2.3	9.55	97.2	5.57	465	2.99 KHz	215 mHz (+); 194.1 mHz (-)	215 mHz	19.7 dB
T2.4	9.6	96.3	38.4	465	434 Hz	34 mHz (+); 29.36 mHz (-)	45 mHz	19.7 dB

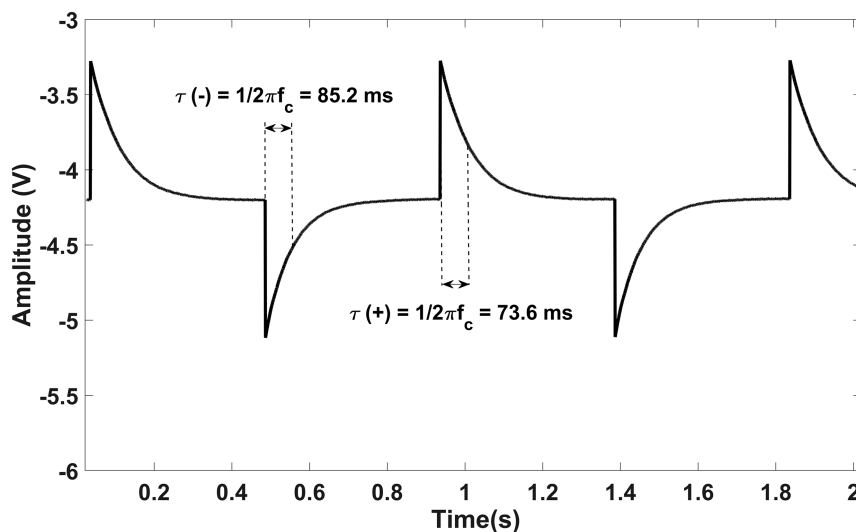


FIGURE 8 Measured time response

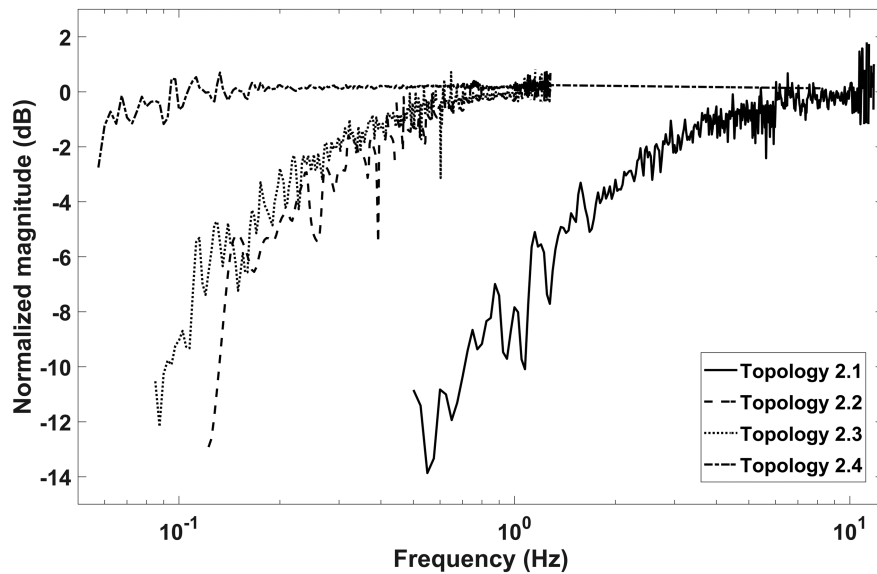


FIGURE 9 Normalized frequency response of Topology 2 with the four configurations in Table 4

TABLE 5 Configuration and measurement values of the proposed ultra-low cutoff frequency AC amplifiers in Figures 3 and 4 ($C_1 = 96.3$ nF, $C_2 = 0.96$ nF, $R_a = 38.4$ K Ω , $R_b = 5.57$ K Ω , $R = 465$ Ω ; with $1/(2\pi R_a C_2) = 4.23$ KHz)

	Cutoff frequency estimation by transient measurements	Cutoff frequency estimation by freq. Sweep measurements	A_v
T1.2	294.7 (+); 204 (-) mHz	240 mHz	39.8 dB
T2.2	340 (+); 294.7 (-) mHz	295 mHz	39.3 dB
T3.2	284.5 (+); 248.7 (-) mHz	280 mHz	39.6 dB
T4.2	335.8 (+); 307.2 (-) mHz	335 mHz	39.3 dB
T5.2	294.7 (+); 274.4 (-) mHz	262 mHz	39.7 dB
T6.2	333 (+); 281.2 (-) mHz	315 mHz	39.2 dB

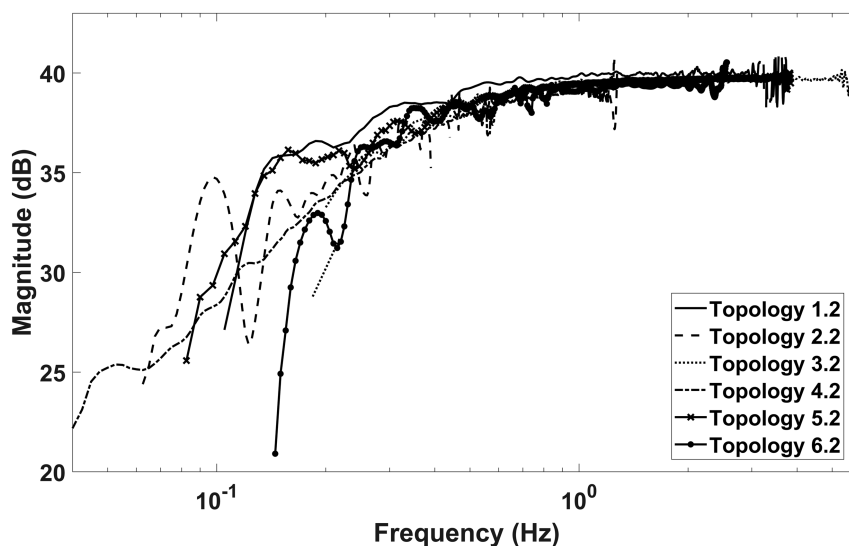


FIGURE 10 Frequency response of the six topologies with configuration 2 in Table 5 ($C_1 = 96.3$ nF, $C_2 = 0.96$ nF, $R_a = 38.4$ K Ω , $R_b = 5.57$ K Ω , $R = 465$ Ω)

we show frequency response plots for the circuit, under the same conditions given in Table 4. Gains are normalized to 0 dB for a clearer presentation. As anticipated, frequency resolution is poor around corner frequency due to instrumentation limitations.

To get a global picture of all topologies, we show in both Table 5 and Figure 10 a comparison of the measured corner frequencies obtained with the six circuits in Figures 3 and 4, under the same experimental conditions, that is, the same passive component values. They all show a very similar behavior.

As predicted by simulations, odd topologies do not achieve the reduction in corner frequency anticipated by formulas in Table 2, and the values given by experimental measurements are even a bit worse than those obtained in simulations, with values around 1.5×10^4 . This is anyway a very large number, but one order of magnitude below DC OA gain. In the case of even topologies, the results are, as shown by simulations, closer to theoretical predictions but experimental values depart also from simulations in an order of magnitude, the reduction factor being around 1.3×10^4 . We think that differences between simulations and experimental results are mainly due to the OA output impedance at ultra-low frequencies, which is underestimated by the model.

6 | CONCLUSIONS

We have described in this paper six novel AC amplifier topologies with the potential to achieve ultra-low (under 1 Hz) corner frequencies. They correspond to the classical capacitive coupled AC amplifiers, where feedback resistors are bootstrapped to increase their equivalent value by a factor theoretically determined by an amplifier gain. The ideas have been practically demonstrated with circuits making use of two OAs, but other implementations are possible based on the same principles.

Though the corner frequencies are not as low as theoretically predicted, mainly due to OA nonidealities (gain roll-off and output impedance), we think that the circuits are practical and useful. Moreover, the same architectures may be implemented with dedicated amplifiers, optimized for the application, with hopefully better behavior.

ACKNOWLEDGMENTS

This work was supported by AEI/FEDER (Grant PID2019-107258RB-C32), Ministry of Universities (grant BES-2017-080418), and Public University of Navarra.

DATA AVAILABILITY STATEMENT

The data that supports the findings of this study are available from the corresponding author upon reasonable request.

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REFERENCES

1. Casas O, Spinelli EM, Pallàs-Areny R. Fully differential AC-coupling networks: a comparative study. *IEEE Trans Instrum Meas.* 2009; 58(1):94-98. <https://doi.org/10.1109/TIM.2008.927200>
2. Hoseini Z, Nazari M, Lee K. Built-in differential electrode offset cancellation loop for ECG/EEG sensing frontend. *IEEE Trans Instrum Meas.* 2021;70:1-11.
3. Ihlenfeld WGK. A simple, reliable, and highly stable AC voltage amplifier for calibration purposes. *IEEE Trans Instrum Meas.* 2005; 54(5):1964-1967. <https://doi.org/10.1109/TIM.2005.853229>
4. Papananos Y, Georgantas T, Tsvividis Y. Design considerations and implementation of very low frequency continuous-time CMOS monolithic filters. *IEE Proc Circuits, Devices Syst.* 1997;144(2):68-74. <https://doi.org/10.1049/ip-cds:19970908>
5. Harrison RR. The design of integrated circuits to observe brain activity. *Proc IEEE.* 2008;96(7):1203-1216. <https://doi.org/10.1109/JPROC.2008.922581>
6. Jochum T, Denison T, Wolf P. Integrated circuit amplifiers for multi-electrode intracortical recording. *J Neural Eng.* 2009;6(1):012001. <https://doi.org/10.1088/1741-2560/6/1/012001>

7. Prasopsin P, Wattanapanitch W. Design of a low-power high open-loop gain operational amplifier for capacitively-coupled instrumentation amplifiers. *Int J Circuit Theory Appl*. 2017;45(11):1552-1575. <https://doi.org/10.1002/cta.2317>
8. Wong A, Pun KP, Zhang YT, Hung K. A near-infrared heart rate sensor IC with very low cutoff frequency using current steering technique. *Proc - IEEE Int Symp Circuits Syst*. 2005;52(12):2723-2726. <https://doi.org/10.1109/ISCAS.2005.1465189>
9. Li Y, Poon CCY, Zhang Y. Analog integrated circuits design for processing physiological signals. *IEEE Rev Biomed Eng*. 2010;3:93-105.
10. Li H, Zhang J, Wang L. A new technique to implement ultra-low frequency analog filters for electrophysiological signal acquisitions. In: *Proc - BSN 2012 9th Int Work Wearable Implant Body Sens Networks*. Vol.2012. IEEE:103-106 doi:10.1109/BSN.2012.20.
11. Li H, Zhang J, Wang L. 5 mHz highpass filter with -80 dB total harmonic distortions. *Electron Lett*. 2012;48(12):698-699. <https://doi.org/10.1049/el.2012.0132>
12. Pérez-Bailón J, Márquez A, Calvo B, Medrano N. A $0.18\mu\text{m}$ CMOS widely tunable low pass filter with sub-Hz cutoff frequencies. *Proc - IEEE Int Symp Circuits Syst*. 2018; 1-4, IEEE. <https://doi.org/10.1109/ISCAS.2018.8351166>
13. Seevinck E, Member S, Plessis M. Active-bootstrapped gain-enhancement technique for low-voltage circuits. *IEEE Trans Orn Circuits Syst II Analog Digit Signal Process*. 1998;45(9):1250-1254.
14. Martin KW. Gain enhancement technique for differential pairs. *Electron Lett*. 1987;23(4):154-156. <https://doi.org/10.1049/el:19870109>
15. Ramírez-Angulo J, López-Martín AJ, González Carvajal R, Muñoz Chavero F. Very low-voltage analog signal processing based on quasi-floating gate transistors. *IEEE J Solid-State Circuits*. 2004;39(3):434-442. <https://doi.org/10.1109/JSSC.2003.822782>
16. Martincorena-Arraiza M, Carlosena A, de la Cruz-Blas CA, Lopez-Martin AJ. AC amplifiers with ultra-low corner frequency by using bootstrapping. *Electron Lett*. 2021;57:203-205.
17. Carlosena A, Moschytz GS. Nullators and norators in voltage to current mode transformations. *Int J Circuit Theory Appl*. 1993;21(4): 421-424. <https://doi.org/10.1002/cta.4490210411>
18. Nałęcz M. A unified approach to autonomous and nonautonomous models of circuit elements. *Int J Circuit Theory Appl*. 2021;49(2): 401-414. <https://doi.org/10.1002/cta.2846>
19. Grasso F, Luchetta A, Manetti S, Piccirilli MC, Reatti A. SapWin 4.0—a new simulation program for electrical engineering education using symbolic analysis. *Comput Appl Eng Educ*. 2016;24(1):44-57. <https://doi.org/10.1002/cae.21671>
20. Wells C, Oljaca M. Modeling the output impedance of an op amp for stability analysis. *Analog Appl J*. 2016;3:1-6.
21. Massarotto M, Carlosena A, Lopez-Martin AJ. Two-stage differential charge and transresistance amplifiers. *IEEE Trans Instrum Meas*. 2008;57(2):309-320. <https://doi.org/10.1109/TIM.2007.909498>
22. Trump B. The Signal e-book: a compendium of blog posts on op amp design topics. *Texas Instruments*. Published online 2017:37.

How to cite this article: Martincorena-Arraiza M, Carlosena A, De La Cruz-Blas CA, Beloso-Legarra J, Lopez-Martin A. A family of AC amplifiers for ultra-low frequency operation. *Int J Circ Theor Appl*. 2021;49(10): 3317-3327. <https://doi.org/10.1002/cta.3122>