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±0.3V Bulk-Driven Fully Differential Buffer with High Figures of Merit

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Abstract: A high performance bulk-driven rail-to-rail fully differential buffer operating from ±0.3V supplies in 180 nm CMOS technology is reported. It has a differential–difference input stage and common mode feedback circuits implemented with no-tail, high CMRR bulk-driven pseudo-differential cells. It operates in subthreshold, has infinite input impedance, low output impedance (1.4 kΩ), 86.77 dB DC open-loop gain, 172.91 kHz bandwidth and 0.684 µW static power dissipation with a 50-pF load capacitance. The buffer has power efficient class AB operation, a small signal figure of merit FOM_{SS} = 12.69 MHzpFµW^{-1}, a large signal figure of merit FOM_{LS} = 34.89 (V/µs) pFµW^{-1}, CMRR = 102 dB, PSRR+ = 109 dB, PSRR− = 100 dB, 1.1 µV/$\sqrt{\text{Hz}}$ input noise spectral density, 0.3 mVrms input noise and 3.5 mV input DC offset voltage.

Keywords: low-voltage; analog buffer; bulk-driven op-amp; fully differential; micropower

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1. Introduction

Biomedical wearable and implantable systems are becoming widely used to sense and monitor biological signals such as EEG, ECG, respiratory signals, etc., in real time [1]. The electronic circuitry used in these systems requires very low power dissipation $P_Q < 1$ uW and very low supply voltages $V_{supply} < 1$ V [2]. In order to preserve battery life and/or to be able to operate with energy harvested sources in biological systems, these systems operate transistors in subthreshold and use bulk-driven circuits, where the input signals are injected through the bulk terminals rather than through the gate terminals [3]. To suppress large noise from digital and other analog sections of the chip and to increase dynamic range, analog signals on chips are usually processed using fully differential circuits.

An important building block of analog systems is the analog buffer that is required to have very low output impedance $R_{out} \ll R_L$, very high input impedance $R_{in} \gg R_{so}$ and close to unity gain $G = V_{out}/V_{in} = 1$ (R_{so} is the signal source impedance). The buffer is commonly used as an interface between subsystems on a chip or to bring signals out of a chip. The op-amp is commonly used to implement buffers. Figure 1a shows the conventional implementation of a single-ended voltage buffer based on the non-inverting op-amp configuration. A drawback of fully differential op-amp circuits is that they can only be used to implement inverting configurations with finite input impedance R_{in}. Figure 1b shows a possible implementation of a fully differential buffer using four equal valued resistors R. This requires the value of R to be in the order of tens of MΩs to avoid loading the signals sources that have typically impedances R_{so} in the order of MΩs for micropower circuits operating in subthreshold. These resistor values are impractical due to the large silicon area required for their implementation and to the large time constants associated with them that degrade the circuit's bandwidth. Another drawback is that the BW of a unity gain inverting buffer corresponds to one half of the gain bandwidth of the op-amp (BW = GB/2) as opposed to the voltage buffer based on the non-inverting configuration that has a factor two higher bandwidth BW = GB. Figure 1c shows the implementation of a true fully differential buffer using a fully differential op-amp with a differential–difference input stage [4–6] that has two pairs of input terminals.

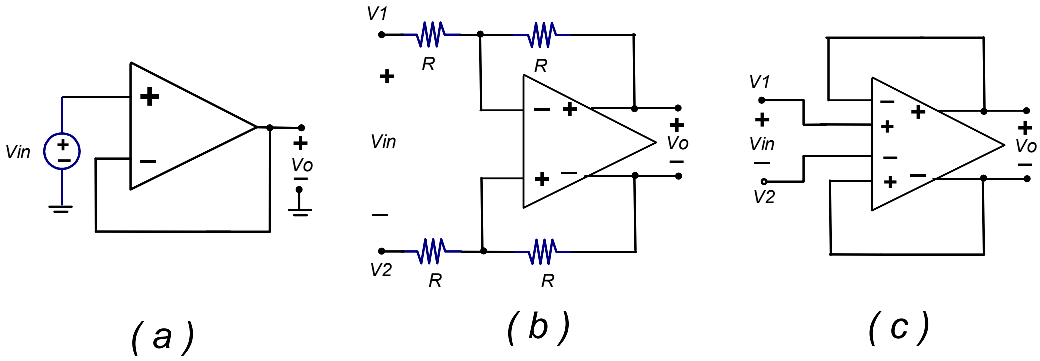


Figure 1. (**a**) Single-ended buffer based on non-inverting configuration; (**b**) fully differential unity gain amplifier with finite input impedance 2R based on conventional fully differential op-amp; (**c**) true fully differential analog buffer based on FD-DDA with infinite input impedance.

Figure 2 shows the architecture of a fully differential Miller op-amp using a differential–difference input stage (denoted here FD-DDA). The input stage has two differential pairs with two pairs of input terminals V_{i1+}, V_{i1-}, V_{i2+} and V_{i2-}, a common load for the input stage, two output stages and a common-mode feedback network. Upon application of negative feedback, the virtual short-circuit input rule of a conventional op-amp $(V_{i+} - V_{i-}) = 0$ is simply replaced by the composite virtual short circuit input rule: $(V_{i1+} - V_{i1-}) + (V_{i2+} - V_{i2-}) = 0$ in the differential–difference input stage [4]. In this paper the output stage operates in class AB based on the Free Class AB Technique reported in [7] as explained in detail in Section 3.

The buffer of Figure 1c is a true fully differential buffer with infinite input impedance. It does not require external resistors; therefore, signal sources V_{S+}, V_{S-} are not loaded by the buffer. Since it is based on a non-inverting configuration, the bandwidth of the buffer corresponds to the gain bandwidth of the op-amp, as opposed to the circuit of Figure 1b that has half the bandwidth. Negative feedback results in the input terminals having voltages $V1 = Vs+ = V_{i1+} = V_{i1-}$ ($V2 = Vs- = V_{i2+} = V_{i2-}$). These voltages follow the swing of the input signals V_{S+} (V_{S-}) similar to the case of the conventional single-ended buffer of Figure 1a. A drawback of gate-driven non-inverting op-amp circuits operating from low supply voltages ($V_{supply} < 1$ V) is that the peak-to-peak input signal swing $V_{PPswing}$ is severely limited by the differential pair headroom $HR_{DP} = |V_{GS}| + |V_{DSsat}|$. The input swing is given by $V_{PPswing} = V_{supply} - HR_{DP}$ (V_{GS} and V_{DSsat} are the gate-source and drain-source saturation voltage of the transistors in the input differential pairs). Bulk-driven differential amplifiers can operate with rail-to-rail input signals in low-voltage circuits [8–23]. The condition $V_{supply} < 1$ V is usually imposed in bulk-driven circuits to avoid forward biasing the bulk–substrate PN junctions of the bulk-driven differential pair input transistors. These circuits are usually operated in subthreshold.

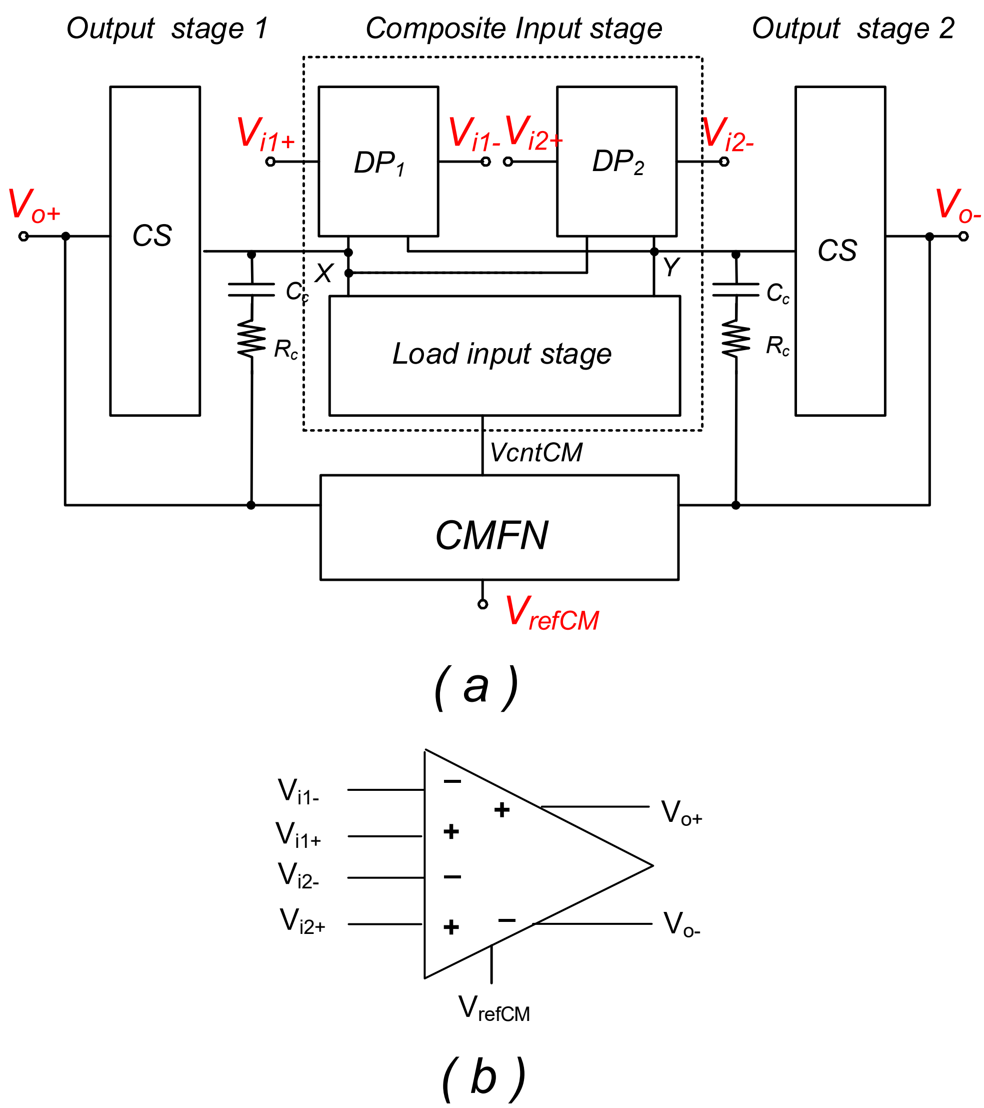


Figure 2. (**a**) Architecture of fully differential Miller op-amp with DDA input stage; (**b**) FD−DDA symbol.

In this paper, we show the implementation of a high performance fully differential buffer with rail-to-rail input and output swing based on a bulk-driven FD-DDA implemented using a high CMRR no-tail bulk-driven pseudo-differential cell.

2. High CMRR Bulk-Driven No-Tail Pseudo-Differential Pair

Figure 3 shows the schematic of a bulk-driven no-tail pseudo-differential pair cell. The input terminals Vi+, Vi− can have rail-to-rail swing. This cell is used to implement the two input pseudo-differential pairs of the differential–difference input stage and the common-mode feedback network of the proposed fully differential DDA with low supply voltage requirements, rail-to-rail input and output range, high CMRR and class AB operation. The cells include a high gain negative feedback loop through V_{Gcntl} that provides it with high common mode rejection as explained below. All transistors in the circuit of Figure 3 operate in subthreshold in high gain mode with $g_m r_o >> 1$.

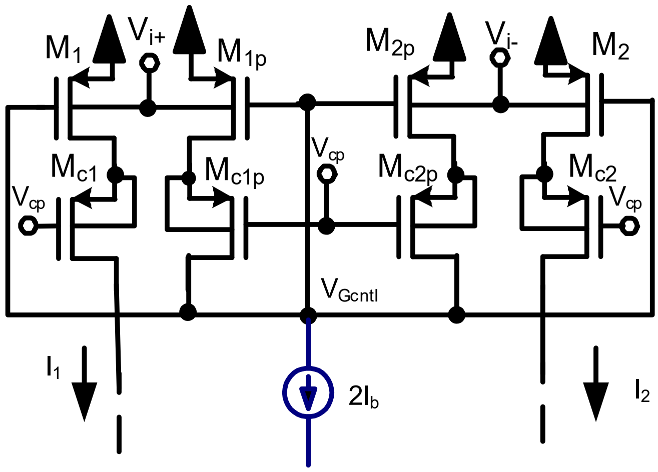


Figure 3. Low supply voltage bulk-driven class AB no-tail cascaded pseudo-differential pair with rail-to-rail input range and high common mode rejection ratio. The biasing current source $2I_b$ is also implemented as a cascoded current source.

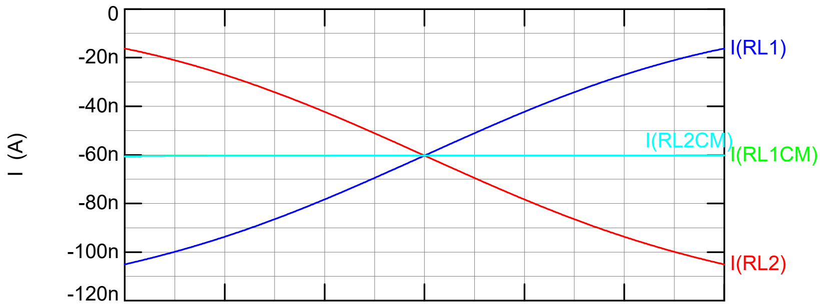
2.1. Differential Gain

Assume complementary input voltages V_{i+}, V_{i-}. In this case, for positive values of the input differential voltage $V_{d,}$ the voltage $V_{i+} = V_d/2$ increases and $V_{i-} = -V_d/2$ decreases by the same amount. Drain currents in M_1, M_{1p} decrease by–$\Delta I_D = -g_{mb}V_d/2$, and drain currents in M_2, M_{2P} increase by the same amount $\Delta I_D = g_{mb}V_d/2$. Since the sum of currents in M_{1p}, M_{2p} remains constant and equal to 2Ib the voltage V_{Gcntl} at the gate of M_1, M_{1p}, M_2, M_{2p} has only relatively small variations that compensate for channel-length modulation effects. The effective differential transconductance g_{md} has an approximate value $g_{md} = g_{mb} = (I_1 - I_2)/V_d$.

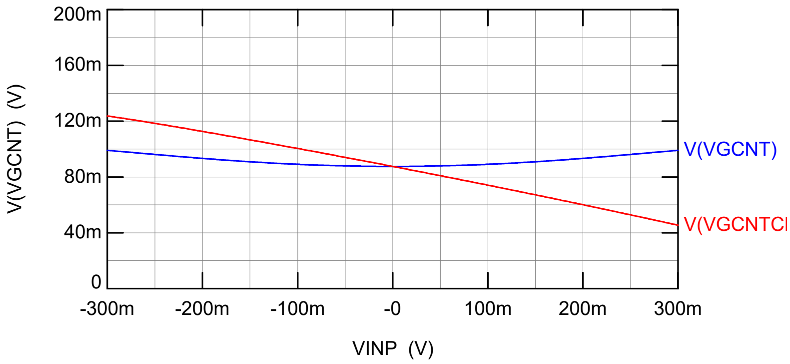
2.2. Common-Mode Gain

Assume now common-mode input voltages $V_{icm} = V_{i+} = V_{i-}$. Given that M_{1p}, M_{2p} satisfy the condition $2I_b = I_{1p} + I_{2p}$, negative feedback adjusts the voltage V_{Gcntl} so that the condition $I_b = I_{1p} = I_{2p} = I_1 = I_2$ is satisfied. Transistors M_1, M_{c1p} and M_2, M_{c2p} constitute high gain cascode amplifiers that provide a gain $A = (g_m r_o)^2$ to the local negative feedback loop (g_m and r_o are the small signal transconductance gain and output resistance of the MOS transistor assumed, for simplicity, equal for all transistors). In this case, all currents (I_{1p}, I_{2p}, I_1, I_2) remain constant, and the output differential current should be $I_{out} = I_1 - I_2 = 0$ which corresponds ideally to a zero common mode transconductance gain. In practice, however, the finite gain $A_{fb} = (g_m r_o)^2$ of the loop formed by M_{1p}, M_{c1p} and M_{2p}, M_{c2p} leads to a non-zero common mode transconductance gain g_{mCM} given by $g_{mCM} = g_{mb}/(g_m r_o)^{2,}$ The systematic common mode rejection ratio is given by $CMRR_{syst} = g_{md}/g_{mCM} = 1/(g_{m1} r_o)^2$. Other authors (i.e., [8–10]) have used non-cascoded no-tail bulk-driven pseudo-differential pairs which are characterized by much lower CMRR.

Figure 4a shows the currents in M_1 and M_2, denoted I_{RL1} and I_{RL2}, for complementary differential input voltages and denoted I_{RL1CM}, I_{RL2CM} for common mode input voltages. Figure 4b shows the value of V_{Gcntl} for differential input voltages and V_{gcntCM} for common mode input voltages. Notice that the bulk-driven pseudo-DP cell has high CMRR. It shows no noticeable changes in I_{RL1CM}, I_{RL2CM} for common mode input voltages, while V_{gcntCM} has relatively large changes that keep the current in M_1, M_2 approximately constant. On the other hand, currents I_{RL1} and I_{RL2} are subject to relatively large complementary changes, while V_{Gcntl} is subject to small changes that compensate for channel length modulation effects.



(**a**)



(**b**)

Figure 4. (**a**) Currents I_{RL1}, I_{RL2} in M_1, M_2 for complementary input signals Vi+ = $V_{INP}/2$, Vi− = $-V_{INP}/2$ and currents I_{RL1CM}, I_{RL2CM} in M_1, M_2 for common mode input signals Vi+ = Vi− = V_{INP}; (**b**) control voltage V_{Gcntl} for differential complementary input signals and $V_{GcntlCM}$ for common mode input signals.

3. Transistor Level Implementation of FD-DDA

Figure 5 shows the full transistor level schematic of the FD-DDA with the architecture of Figure 2a. It is a two-stage Miller op-amp with a differential–difference input stage that uses two of the bulk-driven no-tail pseudo-DPs described in Section 2. The common-mode feedback network also uses a bulk-driven no-tail pseudo-DP cell. In the CMFB cell, the bulk terminals of transistors M_{1p} and M_2 are connected to the output reference common-mode voltage $V_{refCM,}$ and the bulk terminals of M_1 and M_{2p} are connected to the FD-DDA output voltages V_{o+} and V_{o-}. In this case, the cascoded load transistor M_{LCM} is diode connected. The voltage V_{gntCM} shows changes proportional to the difference between the common-mode output voltage $V_{oCM} = (V_{o+} + V_{o-})/2$ and the output reference common-mode voltage V_{refCM}. It generates variations given by $\Delta V_{gcntCM} = -K(V_{Ocm} - V_{refCM})$ with K~1. The common mode feedback loop has approximately a gain $A_{CM} = (g_m r_o)^2$. It operates with rail-to-rail output voltage variations. This differs from the conventional gate-driven two-differential pair-based CMFN that has a very limited common-mode operating range limited by the headroom of the gate-driven differential pairs HD_{DP} used in its implementation. Conventional $R_c - C_c$ Miller compensation elements are used. The output stages use the free class AB technique reported in [7] to achieve current efficient push–pull operation with output quiescent current $I_{outQ} = I_b$ and dynamic peak output currents much larger than I_{outQ}. This is performed by transferring directly dynamic changes in nodes X and Y to the gates of the PMOS output transistors through capacitors C_{bat} that act as floating batteries. In practice, R_{large} and C_{bat} form a high-pass circuit with a very low 3 dB frequency (in the order of Hz). The large resistive elements R_{large} required in this technique are implemented using pseudo-resistors [7]. The input cascoded stage has a gain.

$$A_{inp} = g_{mb} g_m r_o{}^2 \tag{1}$$

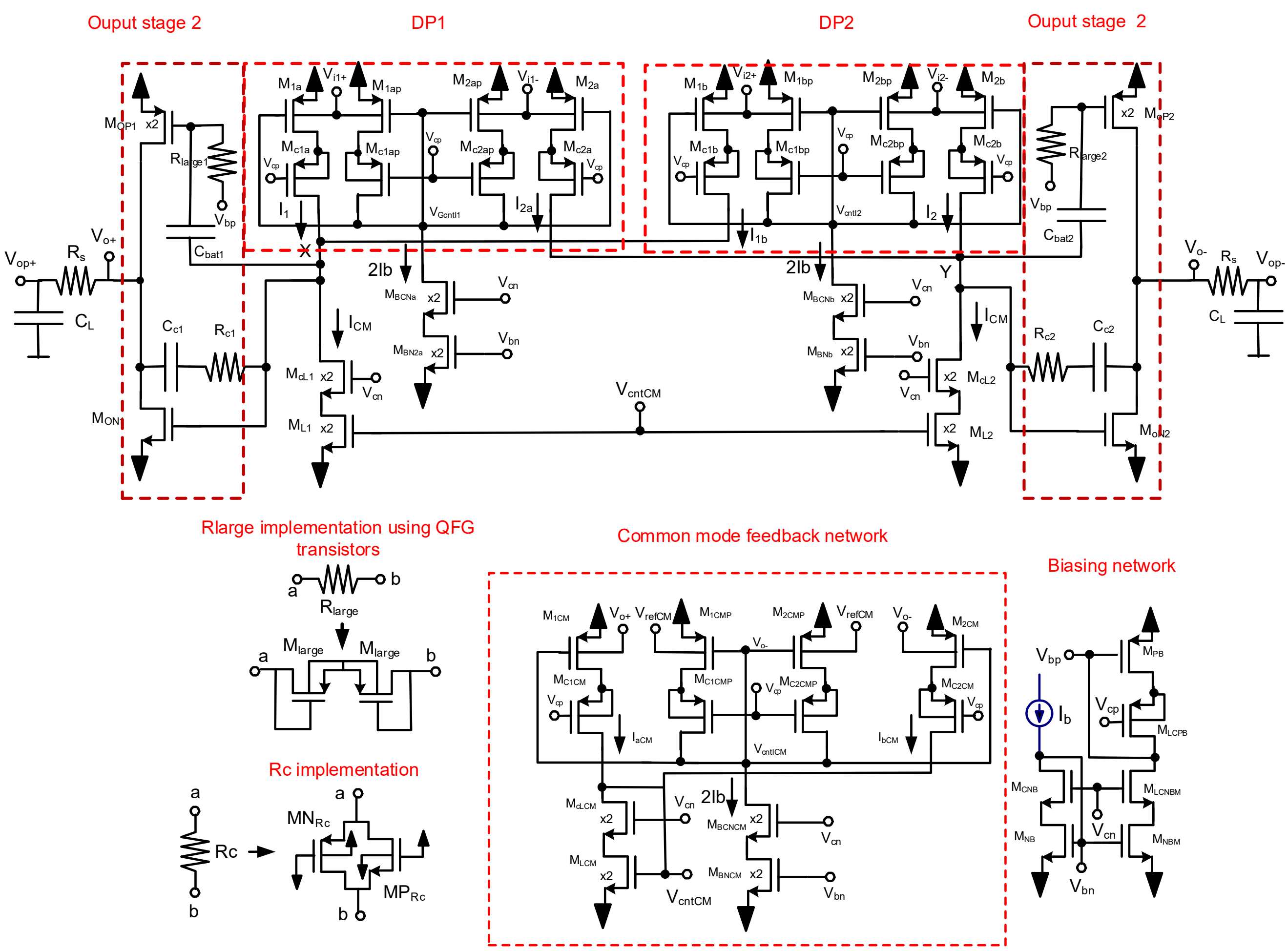


Figure 5. Transistor level schematic of FD−DDA.

The output stage has a gain.

$$A_{out} = (g_{moutP} + g_{moutN})\, r_{oP} \,||\, r_{oN} \tag{2}$$

The open-loop DC gain is given by $A_{ol} = A_{inp}A_{out}$, the gain bandwidth product by

$$GB = (1/2\pi)(g_{mb}/C_c) \tag{3}$$

The high frequency output pole is given by

$$f_{pout}HF = (1/2\pi)(g_{moutP} + g_{moutN})/C_L \tag{4}$$

The high frequency zero is given by

$$f_{zHF} = (1/2\pi)(1/((1/(g_{moutP} + g_{moutN}) - R_c)\, C_c)) \tag{5}$$

Resistor R_s is used for phase lead compensation to improve the phase margin of the FD-DDA. It generates a zero f_{zlead} in the transfer function with a value.

$$f_{zlead} = (1/2\pi)(1/R_sC_L) \tag{6}$$

4. Results

The buffer of Figure 1c using the FD-DDA circuit of Figure 5 was laid out and simulated in a commercial 180 nm CMOS technology using unit PMOS and NMOS transistor sizes W/L = 15 µm/0.4 µm. Ib = 60 nA. Some transistors are scaled by a factor two as shown by the "x2" in the schematic of Figure 5. Dual supply voltages VDD = 0.3 V, VSS = −0.3 V, C_L = 50 pF, R_s = 10 kΩ, C_c = 0.5 pF and R_c = 10 MΩ were used. Rlarge resistors were implemented with two PMOS transistors in series with dimensions 2 µm/0.2 µm. Compensation resistors R_c were implemented as shown in Figure 5 with the parallel combination of a PMOS and an NMOS transistor with dimensions W = 0.5 µm/1 µm.

Figure 6 shows the layout of the FD-DDA with dimensions 45.5 × 135.2 µm^2. Figure 7 shows the open-loop response of the FD-DDA It has a DC open-loop gain A_{olDC} = 86.77 dB, a unity gain frequency f_u = 88.1 kHz and a phase margin PM = 65.47°. Figure 8 shows the AC response of the buffer. It has a bandwidth BW = 172.91 kHz, with 0.556 dB peaking.

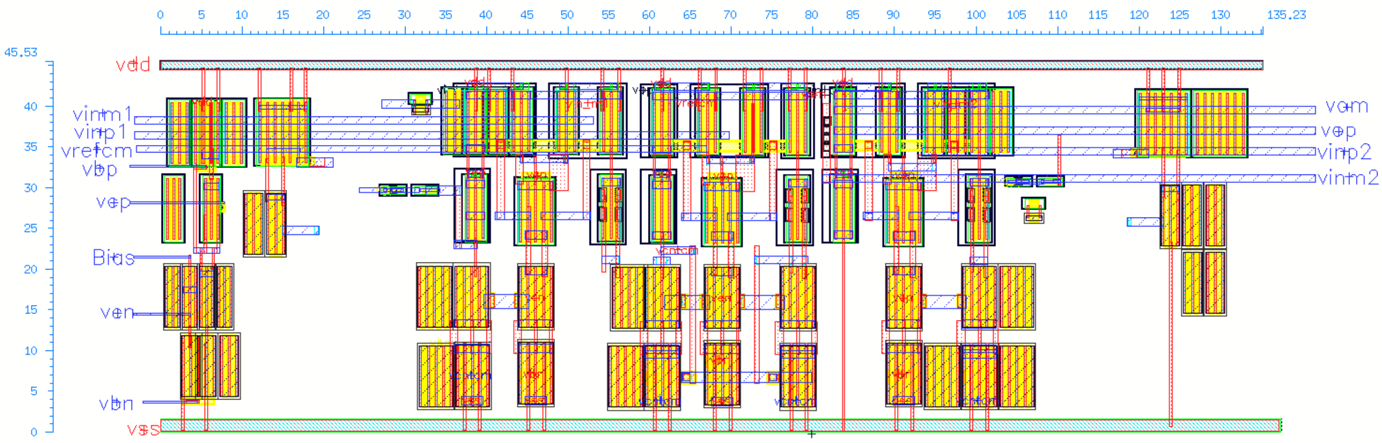


Figure 6. Layout of FD-DDA.

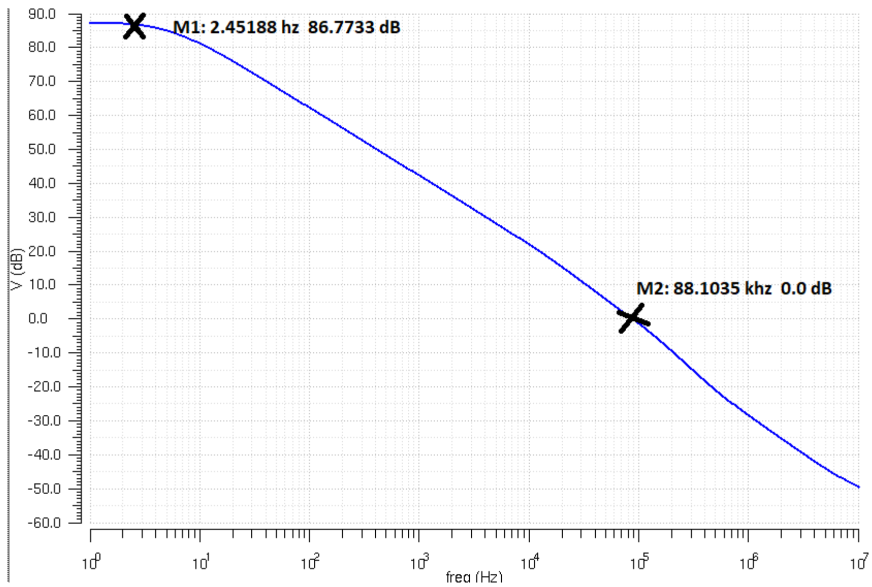


Figure 7. *Cont.*

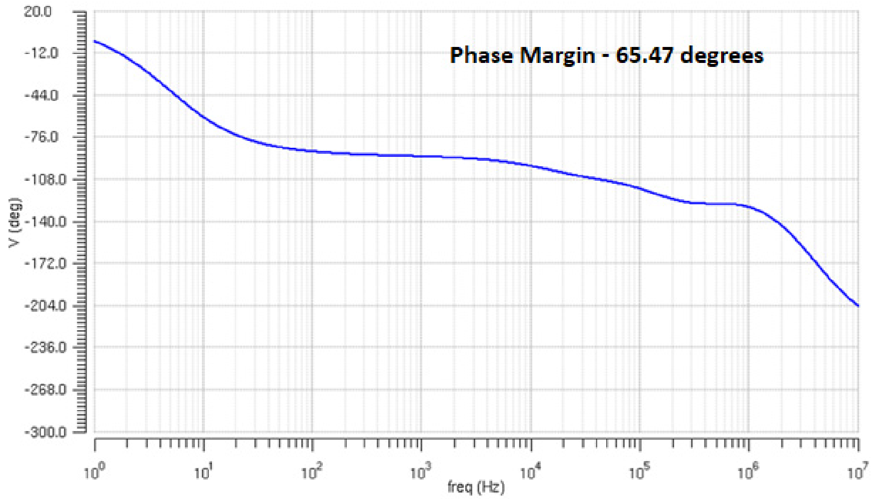


Figure 7. Open-loop response of proposed bulk-driven FD-DDA.

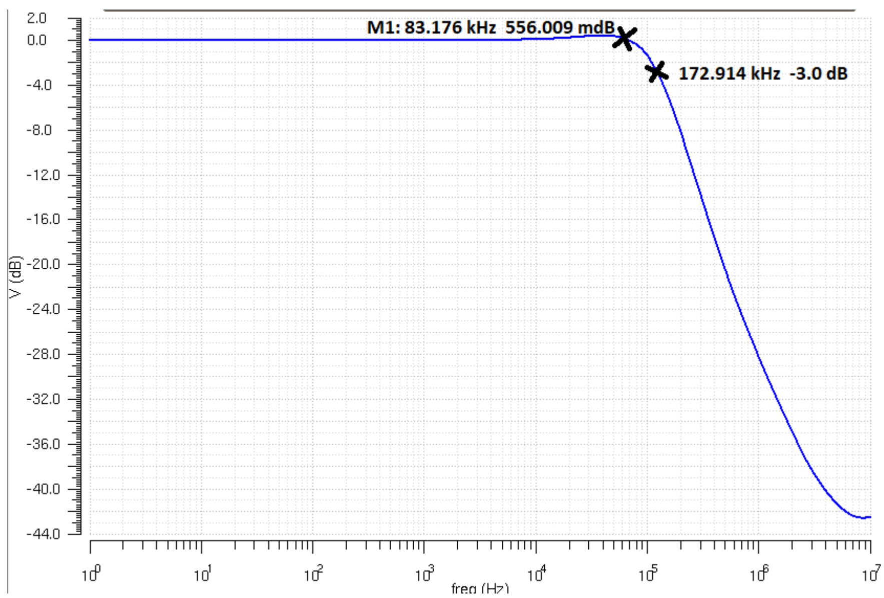


Figure 8. AC response of proposed buffer.

Figure 9 shows the transient response of the output waveforms V_{out}, V_{outp} and of the load capacitor currents I_{CL}, I_{CLP} to a 10 kHz, 0.4 V_{PP} input pulse. It can be seen that the peak positive and negative currents have values I_{pkpos} = 6 µA and I_{pkneg} = −4.6 µA, and the buffer has a symmetrical slew rate SR+ = SR− = 0.238 V/µs. These currents are essentially larger than the output quiescent current I_{outQ} = 60 nA and than the total FD-DDA quiescent current I_{totQ} = 1.12 µA. A conventional class A DDA would have a peak negative output current of I_{pk} = IoutQ = 60 nA and would be characterized by an essentially lower slew rate of only SR− = 0.0012 V/µs.

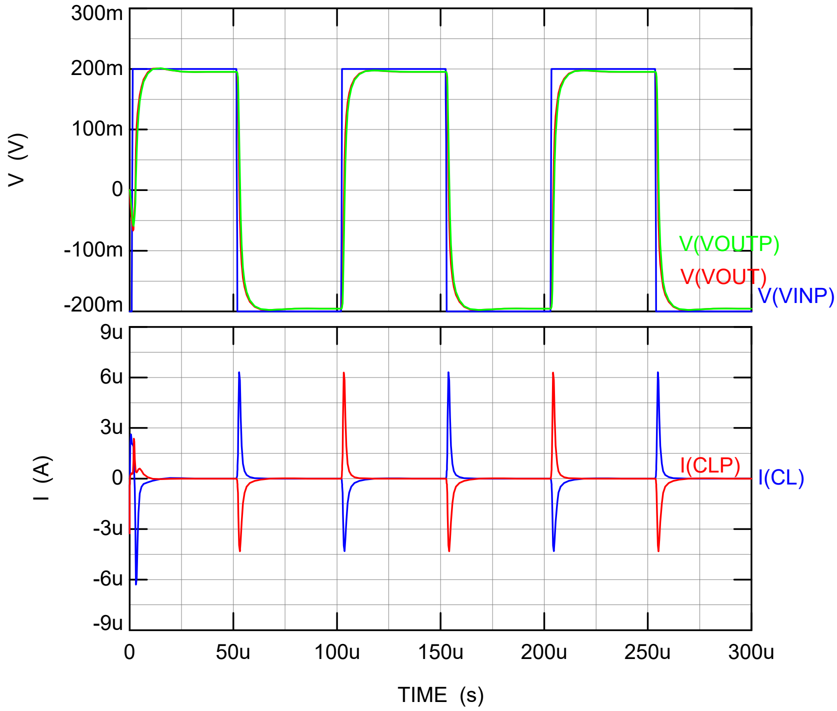


Figure 9. Top: transient voltage response of Vout, Voutp to 10 kHz, 0.4 V_{PP} input pulse Vinp; Bottom: transient load currents I_{CL}, I_{CLP} in load capacitors C_L, C_{LP}.

Other performance parameters obtained from simulations include: total quiescent power dissipation P_{totQ} = 0.666 µW, input noise spectral density at 1 kHz and RMS noise values 1.1 uV/$\sqrt{\text{Hz}}$ and 0.34 $mV_{RMS,}$ respectively. RMS noise was obtained by integrating noise spectral density over the noise bandwidth. CMRR = 102 dB, PSRR+ = 109 dB, PSRR− = 100 dB, input DC offset voltage V_{os} = 3.5 mV. V_{os} was obtained including typical 2% transistor W/L mismatches. The small signal and large signal figures of merit of the proposed FD-DDA are FOMss = GBC_{Ltot}/P_Q = 12.69 MHzpF/µW. FOM_{LS} = SRC_{Ltot}/P_Q = 34.79 (V/µs)pF/µW. The current efficiency is CE = $I_{outtotpk}/I_{totQ}$ = 8.9. Total harmonic distortion is THD = 0.09% for a 10 kHz 0.2 V_{PP} and 10 kHz sinusoidal input signal. Tables 1–3 show corner simulations of parameters at three temperatures spanning a 100 °C range.

Table 1. Corner simulations at T = 90 °C.

	tt	**ss**	**ff**	**fs**	**sf**
fu (kHz)	76.2	75.7	73.4	73.9	76.2
A_{OLDC} (dB)	72.8	77.5	56.2	59.3	75.8
PM	65.1°	64.7°	66.2°	65.2°	65.4°
CMRR (dB)	141	138	116	123	147
PSRR (dB)	81	101	70.4	71.4	76.6
Slew Rate (v/µs) positive	0.25	0.22	0.24	0.24	0.23
Slew Rate (v/µs) negative	0.248	0.22	0.24	0.24	0.23

Table 4 summarizes and compares the performance characteristics of the proposed op-amp and buffer to recently reported bulk-driven low-voltage circuits [11–19]. It can be seen that the proposed circuit has the highest small and large signal figures of merit.

Table 2. Corner simulations at T = 27 °C.

	tt	ss	ff	fs	sf
fu (kHz)	119.6	120.4	120.2	120.9	112.7
A_{OLDC} (dB)	85.3	81.6	84.1	84	83.6
PM	62.6°	63.5°	62.5°	62.9°	62.7°
CMRR (dB)	171.5	130	148	139.2	148
PSRR (dB)	97	75	112.4	84.6	75
Slew Rate (v/µs) positive	0.25	0.22	0.24	0.24	0.23
Slew Rate (v/µs) negative	0.248	0.22	0.24	0.24	0.23

Table 3. Corner simulations at T = −10 °C.

	tt	ss	ff	fs	sf
fu (kHz)	135.36	95.5	143.9	105	139.2
A_{OLDC} (dB)	71.3	52	88	62	79.6
PM	65°	75°	62.6°	73.4°	63.4°
CMRR (dB)	126	105	157	121.7	141
PSRR (dB)	70	40	91	52	96
Slew Rate (v/µs) positive	0.20	0.14	0.29	0.23	0.13
Slew Rate (v/µs) negative	0.20	0.14	0.29	0.23	0.13

Table 4. Comparison table of proposed circuit to recently published bulk-driven op-amps.

Parameter Year Sim/Exp	This Work Sim	[19] 2022 Sim	[18] 2021 Exp	[17] 2020 Exp	[16] 2020 Exp	[15] 2019 Exp	[14] 2016 Exp	[13] 2015 Exp	[12] 2013 Sim	[11] 2016 Exp
Vsupply (V)	0.6	0.5	0.5	0.25	0.3	0.3	0.5	0.4	1	0.7
Technology (µm)	0.18	0.18	0.18	0.065	0.18	0.18	0.18	0.05	0.35	0.18
Power Dissipation (µW)	0.684	0.312	0.0455	0.026	0.0126	0.022	0.07	31.84	197	22.4
C_L (pF) total	50 × 2	15	15	15	30	20	40	20 × 2	15	20
GB (MHz)	0.0868	0.0128	0.0075	0.0095	0.00296	0.00185	0.004	2.31	11.67	3
SR+/SR− (V/µs)	0.238	0.0158/ 0.0135	-	0.002/ 0.002	0.0019/ 0.0064	0.00165/ 0.00135	0.002/ 0.002	1.2	2.53/1.37	1.8/3.8
CMRR (dB)	102	60	85.7	62.5	110	82	55	92	40	19
PSRR+/PSRR− (dB)	109/ 100	66	68.1	38	56	57	52	64	40/46.8	52.1
Input noise spectral density ($\mu V/\sqrt{Hz}$)	1.1 @ 1 kHz	0.88	0.65 @ 1 kHz	-	1.6	2.58	-	0.164 @ 10 kHz	0.06 @ 1 MHz	0.1@ 1 MHz
FOM_{SS} (MHz.pF/µW)	12.69	0.614	2.5	5.48	7.047	1.68	2.28	2.88	0.88	2.67
FOM_{LS} ((V/µs).pF/µW)	34.79	0.647	2.76	1.15	4.52	1.22	1.14	1.5	0.10	1.60
Total Harmonic Distortion (%)	0.09 @ 1 kHz, 0.2 V_{PP}	0.28	1% @ 0.46 V_{PP}	-	-	-	-	-	-	0.2 @ 100 kHz 400 mV_{PP}
Input offset (mV)	3.2	6.14	2.3	-	3.2	4.73	4 (average)	-	8.4,10	11
Single-Ended/Fully differential	FD	SE	SE	SE	SE	SE	SE	FD	SE	SE

Remarks: (a) Given that the minimum of the rising and falling slew rates (SR+ and SR−) limits the large signal speed of an amplifier, calculation of FOM_{LS} was performed using the minimum of the two slew rates values min{SR^+, SR^-}. (b) For fully differential (FD) amplifiers, the total load capacitance CLtot = 2xCLwas used to calculate FOM_{SS} and FOM_{LS}.

5. Conclusions

A high performance true fully differential bulk-driven buffer operating from ±0.3V dual supply voltages is presented. A fully differential class AB Miller op-amp with differential–difference input stage is used to implement the buffer. A high CMRR no-tail bulk-driven cascoded pseudo-differential cell is used in the input stage and in the common mode feedback network of the op-amp. The circuit was verified with simulations in a commercial 180 nm CMOS technology.

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