Single-Stage Class-AB Non-Linear Current Mirror OTA

Javier Beloso-Legarra, Carlos A. De La Cruz-Blas, Antonio Jesús Lopez-Martin
Institute of Smart Cities - Public University of Navarra (UPNA)
Campus de Arrosadia - 31006 Pamplona, Spain
E-mail: {javier.beloso | carlos.aristoteles | antonio.lopez}@unavarra.es

***Abstract*—The analysis, design and experimental characterization of a single-stage class-AB operational transconductance amplifier (OTA) with enhanced large- and small-signal performance is presented. The OTA is biased in weak inversion to save power and employs a non-linear current mirror as active load, leading a boosting current directly at the output branch. As a result, the amplifier's performance is improved without additional circuit elements and/or power consumption. A chip prototype has been fabricated in a 180-nm CMOS process, consuming a quiescent power of 2.5 µW from a supply voltage of ±0.5 V and a silicon area of 0.0013 mm^2. For a load of 160 pF, it exhibits an average slew rate of 0.94 V/µs and a gain-bandwidth product of 22.1 kHz.**

***Index Terms*—Class-AB, single-stage amplifier, OTA, non-linear current mirror, power efficiency.**

I. Introduction

THE proliferation of energetically autonomous systems requires low-power devices that must satisfy the increasingly demanding standards. Such systems often employ the OTA as active element due to its versatility in a wide variety of scenarios. Consequently, the design of OTAs should consider such low-voltage low-power constraints while exhibiting high performance features.

Since power efficiency is a major priority, single-stage OTAs are the best option because the number of branches where current flows is minimized. In addition, their single-pole behavior avoids using frequency compensation that may increase power. By contrast, their low gain limits their use in high precision applications, requiring novel techniques to increase such values. Power efficiency is also achieved by class-AB operation. The main limitation of class-A amplifiers is the output current drivability. The advantage of class-AB is the improvement in large-signal performance without increasing quiescent current, leading outstanding results with the same class-A static power.

Along the years, different class-AB solutions have been proposed. Examples of such techniques are the use of flipped voltage followers as adaptive biasing floating batteries [1], [2]; the quasi-floating gate transistor [3] providing DC biasing and AC driving; the local common-mode feedback [4] as active load to increase both slew rate and bandwidth; or slew rate enhancers that inject an extra amount of driving current [5], [6]. However, these techniques require additional circuit elements that may affect power consumption, area or bandwidth, as well as increase complexity in the design.

An alternative class-AB strategy is to use non-linear current mirrors [7]-[10]. In DC conditions, the operation is similar to a linear current mirror; however, in dynamic operation the circuit enters in a non-linear region that boosts input pair's current beyond its quiescent bias. Moreover, if boosting occurs at output branch so that no internal current replication exists, a nearly optimal current efficiency factor, defined as the ratio between load and supply currents, $CE = I_{out}/I_{supply} \approx 1$ can be achieved.

Reference [7] is based on a current mirror as active load in which input transistor is biased near saturation and triode regions by a fixed bias voltage. Under transients, transistor enters in a non-linear deep triode region, thus boosting output current. To enter it in this deep triode state, a large input current is required, which in this case is supplied by an adaptive biasing input pair. Hence, this solution is only valid if an adaptive biasing input pair, or if very large bias currents are employed, limiting its usability. In [8], the proposed OTA employs dynamic current mirrors whose gain is dynamically changed by cross-coupled local partial-positive feedback. However, power consumption is in the order of mW, which cannot be considered a low-power solution. Reference [9] combines an adaptive biasing input pair with non-linear current mirrors. The non-linear current mirror employs two cross-coupled cascodes that dynamically bias output transistors between saturation and triode, achieving the desired boosting. However, the OTA has not been fabricated thus measurement results are not available. Finally, [10] employs an adaptive biasing input pair with non-linear active load that combines local-common mode feedback with partial-positive feedback. In spite of the outstanding large-signal results, the local-common mode resistors consume significant area.

This paper presents a simple and compact solution to design a power-efficient single-stage class-AB OTA based on non-linear current mirrors (NL-CM) as active load with enhancements of large- and small-signal performance. The NL-CM is based on two cross-coupled cascodes that dynamically bias the output transistors, generating a non-linear boosted output current while keeping a low DC static behavior. The cross-coupled approach leads to high output currents levels avoiding the use of additional circuit elements such as adaptive biasing input pairs. Consequently, the OTA consumes a low silicon area, making this amplifier suitable for those applications requiring a large

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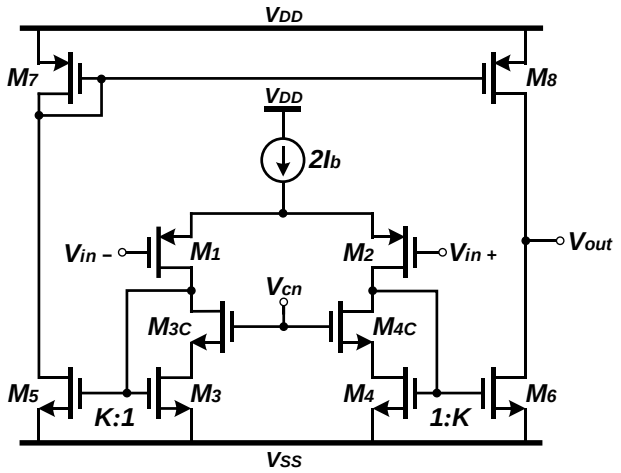

Fig. 1. Conventional single-stage class-A current mirror (CM) OTA.

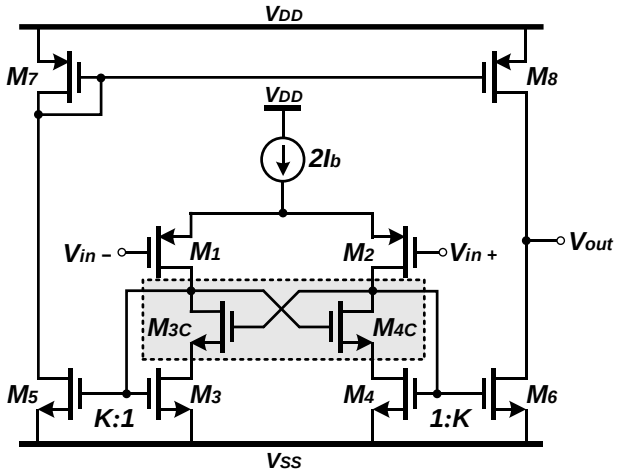

Fig. 2. Proposed class-AB non-linear current mirror (NL-CM) OTA.

quantity of devices as in multi-channel processing for large capacitive loads with high-performance slew rates, settling times and power efficiency. A similar approach was independently proposed in [9] without experimental results and published after the circuit design and chip fabrication was carried out by the authors of the present paper.

II. Proposed Non-Linear Current Mirror

The current mirror (CM) OTA is one of the most common single-stage amplifiers. Shown in Fig. 1, it offers an almost rail-to-rail output, and the current mirror ratio *K* provides flexibility. However, the class-A operation limits its use in those scenarios requiring high-performance slew rates and settling times with low-power constraints.

To circumvent these limitations, an improved class-AB version is proposed, as shown in Fig. 2. Coined as non-linear current mirror (NL-CM) OTA, the solution rearranges the active load to improve the amplifier's performance. This is achieved by cross coupling the drains of cascode transistors M_{3C}-M_{4C} with their opposite gates, allowing M_3-M_4 to operate between saturation and triode regions. As a result, output current is non-linearly related to M_1-M_2 input currents, generating an output current that is much larger than pair's bias under large dynamic variations. In addition to large-signal, the small-signal performance can be enhanced by setting an appropriate NL-CM bias point. This can be controlled by the drain-to-source voltage of

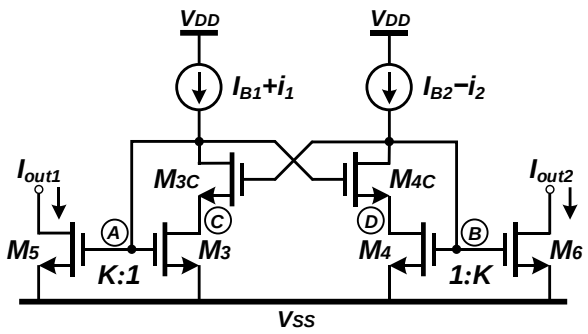

Fig. 3. Non-linear current mirror.

M_3-M_4, which in turn is set by the aspect ratio of M_{3C}-M_{4C}. To save power, the circuit is designed in weak inversion for quiescent operation. In order to simplify the explanations, in the following analysis only the left-half circuit is considered.

A. DC Static Behavior

The behavior of NL-CM can be explained with the circuit of Fig. 3, where I_{B1} and I_{B2} are DC static bias currents, and i_1 and i_2 are small-signal input currents that are supplied by differential pair. Hence, $I_{B1} = I_{B2} = I_b$, being I_b the OTA bias current.

Due to weak inversion operation, the following exponential current relationship is considered

$$I_d \approx I_o \frac{W}{L} e^{\frac{V_{GS}-V_{TH}}{nV_t}} \left(1 - e^{\frac{-V_{DS}}{V_t}}\right) \quad (1)$$

where I_o is the specific current, V_{GS} (V_{DS}) is the gate-to-source (drain-to-source) voltage, V_{TH} is the threshold voltage, $V_t \approx 26$ mV is the thermal voltage and $n \approx 1.5$ [11].

Depending on whether M_3 is in saturation or triode, NL-CM output current varies. For $V_{DS} \geq 100$ mV, the device operates in saturation. By contrast, under low values of $V_{DS} < V_t$ [11], it can be modelled as a linear resistor operating in triode. Assuming that M_3 can be in saturation or triode, and M_5 is always in saturation, the quiescent output current is defined as

$$I_{out}^{Q} = K I_{B1} \left(\frac{1}{1 - e^{-V_{DS3}/V_t}}\right) \quad (2)$$

where $K = (W/L)_5/(W/L)_3$ and $I_{B1} = I_b$. Note the non-linear dependence on V_{DS3}. When M_3 is in saturation, the exponential term can be neglected, leading a quiescent output current equal to $I_{out}^{Q} \approx K I_b$, as CM OTA. However, when it is in triode, output current is non-linearly increased. Interestingly, this property can be exploited to enhance small-signal behavior by setting M_3 at the edge of saturation and triode regions, increasing current gain with little power degradation.

B. Small-Signal Performance

When the differential input pair supplies two complementary small-signal currents i_1 and i_2, an AC current is generated at the output. Depending on whether M_3 is in saturation or triode, the operation changes. In order to model it, transistor intrinsic gain $g_m r_o$ deserves to be commented, which depends on V_{DS}. When it is in saturation, $g_m r_o \gg 1$ can be considered. When it is in triode, intrinsic gain is reduced and the latter assumption is no longer valid. In the lower limit, when $V_{DS} \approx 0$ V, $g_m r_o \approx 0$.

Then, the current gain is derived. To this end, all devices can be assumed in saturation except M_3 (which can be in saturation

or triode), thus term $g_m r_o \gg 1$ will be considered for expression where transistor M_3 is no involved. The small-signal output current as a function of i_1 is expressed by

$$i_{out1} = i_1 \frac{g_{m5}(1 + g_{m3C} r_{o3})}{g_{m3C}(g_{m3} r_{o3} - 1)}. \quad (3)$$

Defining the complementary input currents as $i_{in} = i_1 - i_2$, where i_{in} is the small-signal input current, and the differential output current as $i_{out} = i_{out1} - i_{out2}$, current gain is given by

$$A_I = \frac{i_{out}}{i_{in}} = K_{1eff} \frac{(1 + g_{m3C} r_{o3})}{g_{m3C} r_{o3} - g_{m3C}/g_{m3}} \quad (4)$$

where $K_{1eff} = g_{m5}/g_{m3} = K/(1 - e^{-V_{DS3}/V_t})$ is the effective aspect ratio. Note how V_{DS3} increases K_{1eff}. When all transistors are in saturation, $g_{m3} r_{o3} \gg 1$ and $A_i \approx K$ with $K_{1eff} \approx K$, as CM OTA. Conversely, when M_3 is in deep triode, $g_{m3} r_{o3} \approx 0$ and $A_i \approx -g_{m5}/g_{m3C}$. Last case is an extreme condition that should be avoid as the circuit behaves as a negative gain, leading to unstable topology. Hence, it is important to select an adequate V_{DS3} value to avoid potential instabilities.

C. Large-Signal Performance

To evaluate the non-linear behavior, the circuit is analyzed in large-signal conditions. Suppose that both inputs suffer a large differential step $I_{id} = I_{in1} - I_{in2}$. When $I_{in1} \gg I_{in2}$, transistors M_4, M_{4C} and M_6 are off. On the other hand, current in M_3 and M_{3C} is $I_{3,3C} \approx I_{in1} \approx 2I_b$. Because M_{3C} behaves like a voltage buffer, as I_{in2} reduces, V_{gs4} and consequently V_{gs3C} are reduced. Therefore, V_{ds3} is decreased, entering M_3 in deep-triode. In order to keep its drain current, $V_{gs3} = V_{gs5}$ is boosted, driving output transistor M_5 and achieving class-AB operation.

To model last operation, due to the large gate-to-source voltages of M_3 and M_5, $V_{gs} \gg V_{TH}$, so they enter in strong inversion. Moreover, M_3 is in triode and M_5 is in saturation. Defining the strong inversion currents in both triode and saturation as $I_d = \beta(V_{GS} - V_{TH})V_{DS}$ and $I_d = (\beta/2)(V_{GS} - V_{TH})^2$ respectively, in which $\beta = \mu_n C_{ox}(W/L)$, output current in M_5 is equal to

$$I_{out1} = \frac{K}{2\beta_3} \left(\frac{I_{in1}}{V_{ds3}} \right)^2 \quad (5)$$

where a squared boosting is produced with an output higher than bias current but at the same time an extra increment is due to the V_{DS3} reduction, increasing output current further.

D. Design Considerations

As seen, V_{DS3} is a key variable in NL-CM. The way to control it consists of setting an adequate aspect ratio of M_{3C} with respect to M_3. Assuming perfect matching, $V_{DS3} = V_{GS4} - V_{GS3C}$, in which case $V_{GS4} = V_{GS3}$ due to the circuit symmetry. M_3 can be in saturation or triode, and M_{3C} is assumed to be in saturation. Being M_{3C} x times larger than M_3, once substituted the corresponding V_{GSi} in V_{DS3}, that are defined as $V_{GS3} = V_{TH3} + nV_t \cdot \ln(I_b/[I_o(W/L)_3(1 - e^{-V_{DS3}/V_t})])$ and $V_{GS3C} = V_{TH3C} + nV_t \cdot \ln(I_b/[I_o(W/L)_{3C}])$, and assuming that $V_{TH3} = V_{TH3C}$ for simplicity, the aspect ratio x for a given V_{DS3} is

$$x(V_{DS3}) = \frac{(W/L)_{3C}}{(W/L)_{3C}} = e^{\frac{V_{DS3}}{nV_t}} \left(1 - e^{\frac{-V_{DS3}}{V_t}} \right) \quad (6)$$

where V_{DS3} is chosen by the circuit designer. For instance, to set M_3 in the limit of saturation and triode regions with a value of $V_{DS3} = 50$ mV, the aspect ratio should be set to $x \approx 3$.

III. Single-Stage Class-AB NL-CM OTA

The main performance parameters of the proposed OTA presented in Section II are analyzed below.

A. Transconductance and Stability Analysis

When a small-signal differential input voltage v_{id} is applied, the input differential pair provides two complementary currents $i_1 = (v_{id}/2)g_{m1}$ and $i_2 = -(v_{id}/2)g_{m2}$. Assuming that $g_{m1} = g_{m2}$, the OTA transconductance is

$$G_m = \frac{i_{out}}{v_{id}} = g_{m1} K_{1eff} \frac{(1 + g_{m3C} r_{o3})}{g_{m3C} r_{o3} - g_{m3C}/g_{m3}}. \quad (7)$$

Regarding stability, different poles appear in the system. The dominant one is located at the output, and depends on both load capacitance and output resistance $\omega_d = 1/r_{out} C_L$. According to Fig. 3, A, B, C and D represent the nodes of the non-dominant poles, which are defined as

$$\omega_{pA} = \omega_{pB} \approx \frac{g_{m3C}(g_{m3} r_{o3} - 1)}{(1 + g_{m3C} r_{o3}) C_A}$$
$$\omega_{pC} = \omega_{pD} \approx \frac{1 + g_{m3} r_{o3}}{r_{o3} C_C} \quad (8)$$

where C_i represents the parasitic capacitance associated to i-th node. By inspection, it can be seen how ω_{pA} and ω_{pC} depend strongly on the state of M_3. In saturation, $\omega_{pA} \approx g_{m3}/C_A$ and $\omega_{pC} \approx g_{m3}/C_C$. Both poles have similar expressions as in DC conditions, M_{3C} behaves like a cascade device. Consequently, in the small-signal model it can be roughly assumed that $v_C = v_A$ where v_i is the small-signal voltage associated to i-th node. However $C_A \gg C_C$, so $\omega_{pA} \gg \omega_{pC}$. In deep triode, $r_{o3} \to 0$ therefore $\omega_{pA} \approx -g_{m3C}/C_A$ and $\omega_{pC} \to \infty$. Intuitively, when r_{o3} is reduced, the C node time constant is reduced. The lower bound $r_{o3} = 0$ gives rise that nodes C and D are virtually connected to ground, shifting the node poles towards very high frequencies. In the case of ω_{pA}, it is shifted to right-half side plane as the circuit becomes a positive-feedback topology leading to instabilities. This situation should be avoided by controlling the factor $(g_{m3} r_{o3} - 1) > 0$ in (8). Therefore, the equations reveal how, as M_3 is in triode region, ω_{pA} is reduced whereas ω_{pC} is increased. Due to this, it can be assumed that pole at node A is the non-dominant one. However, some design aspects should be considered to prevent moving it to the right-half side plane or being at lower frequencies than dominant pole ω_d.

Using the phase margin expression $\varphi = 90° - tg^{-1}(\omega_{GBW}/\omega_{pA})$ where $\omega_{GBW} = G_m/C_L$,

$$\varphi \approx 90° - tg^{-1} \left(\frac{A_I g_{m1}[1 + g_{m3C} r_{o3}]}{g_{m3C}[g_{m3} r_{o3} - 1]} \cdot \frac{C_A}{C_L} \right). \quad (9)$$

Last equation models phase margin for those values of ω_{pA} that are higher or equal to ω_{GBW}, that is to say $\omega_{pA} \geq \omega_{GBW}$. This satisfies that OTA is still in normal operation mode, avoiding the aforementioned instabilities and positive-feedback.

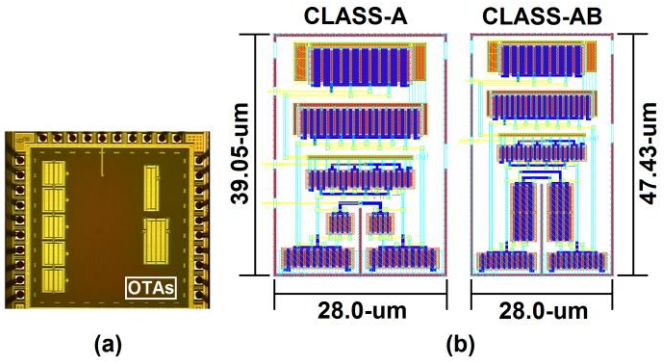

Fig. 4. (a) Test chip microphotograph and (b) OTA layouts.

TABLE I
TRANSISTOR ASPECT RATIOS

Transistor	Dimension (µm/µm)
M_1, M_2	8x(2.25/0.36)
M_3, M_4, M_5, M_6	4x(2.50/0.50)
M_{3C}, M_{4C}	12x(2.50/0.50)
M_7, M_8	8x(3.75/0.50)

Note how phase margin is degraded as current gain A_I is increased. As M_3 is entered in deep triode, r_{o3} is reduced. As expected, this increases current gain but also decreases the frequency of non-dominant pole ω_{pA} and increases the frequency of ω_{pC}. Very low V_{DS3} values shift pole at node A to the right-half plane, revealing how a trade-off between current gain and stability exists. During DC conditions, V_{DS3} should be set to a value that increases current gain while keeping pole at node A within a safe margin to avoid potential instabilities.

B. *Slew Rate Analysis*

Upon application of a large input step $V_{id} = V_{in+} - V_{in-}$, a differential current is delivered by input pair, which is defined in weak inversion as

$$I_{id} = I_1 - I_2 = 2I_b tanh\left(\frac{V_{id}}{2nV_t}\right). \quad (10)$$

When $V_{id} > 0$, the differential current can be approximated to $I_{id} \approx I_1 = 2I_b$ with $I_2 \approx 0$, turning off M_4, M_{4C} and M_6. Consequently, I_1 flows through M_3 and M_{3C}, reducing V_{gs4}, V_{gs3C} and V_{ds3}, and boosting V_{gs5} with an increment in output current I_5, where $I_6 \approx 0$. Thus, output current is $I_{out} = I_5 - I_6 \approx I_5$. In a similar manner, when $V_{id} < 0$, $I_{id} \approx I_2 = 2I_b$ with $I_1 \approx 0$, boosting V_{gs6} and output current I_6, where $I_5 \approx 0$ and $I_{out} = I_5 - I_6 \approx -I_6$. Consequently, once substituted equation (10) as input current in (5), the slew rate is

$$SR = \frac{I_{out}}{C_L} \approx \pm\frac{2{I_b}^2 K}{\beta_3 {V_{ds3}}^2 C_L} tanh^2\left(\frac{V_{id}}{2nV_t}\right) \quad (11)$$

where $I_{out} > 0$ when $V_{id} > 0$ and $I_{out} < 0$ when $V_{id} < 0$. Since boosting is produced directly at the output branch, current efficiency is near its optimal value, which is expressed as $CE = |I_{out}|/(|I_{out}| + 2I_b)$ [2]. Noting that $|I_{out}| \gg 2I_b$ under dynamic conditions, CE approaches the ideal value of 1.

IV. MEASUREMENT RESULTS

A prototype was fabricated in 0.18-µm CMOS technology. The chip contains the proposed class-AB NL-CM OTA and the class-A CM OTA version to validate the proposal and compare both designs. Both devices were loaded off-chip with 160 pF, which includes the pad, breadboard, and test probe capacitance. The chip microphotograph and layouts are shown in Fig. 4.

The class-AB amplifier was fabricated in both open-loop and unity-gain closed-loop to fully characterize it whereas the class-

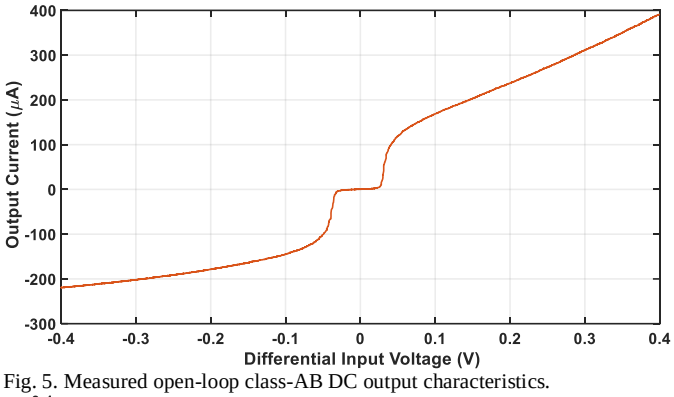

Fig. 5. Measured open-loop class-AB DC output characteristics.

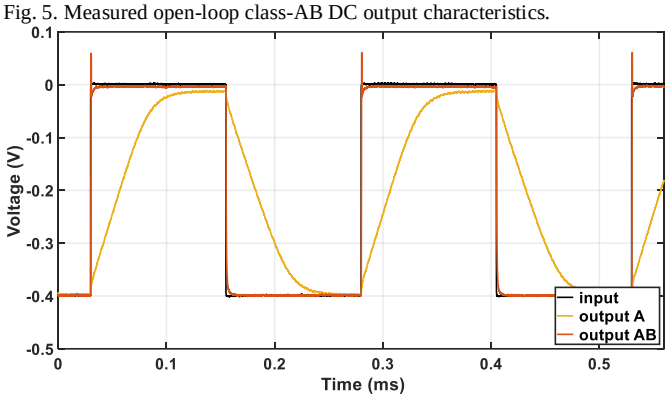

Fig. 6. Measured unity-gain class-A vs class-AB large-signal responses.

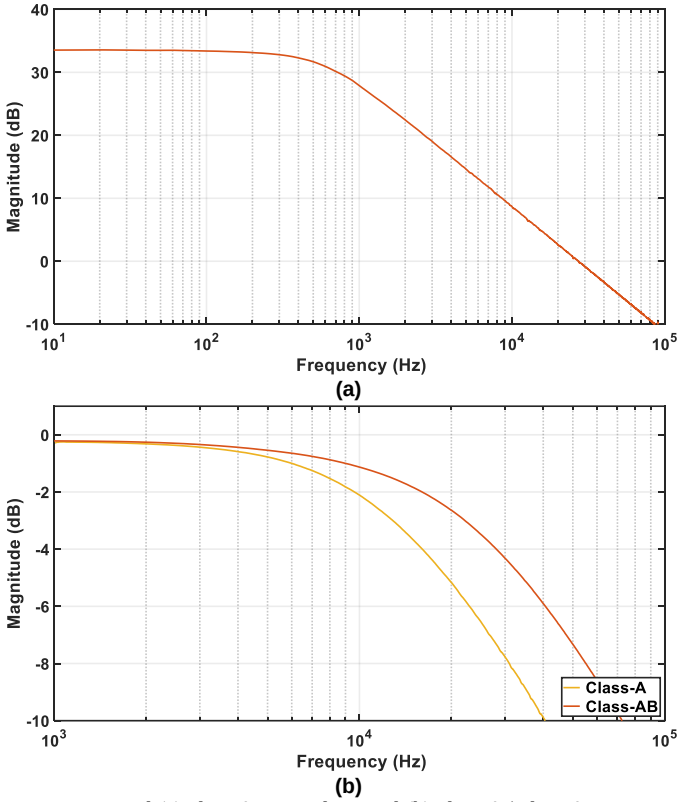

Fig. 7. Measured (a) class-AB open-loop and (b) class-A | class-AB unity-gain closed-loop frequency responses.

TABLE II
CLASS-A CM AND CLASS-AB NL-CM PERFORMANCE PARAMETERS AND COMPARISON

Parameter	[7]	[8]	[10]	[12]	[13]	[14]	[15]	This work	
CMOS process [µm]	0.5	0.18	0.18	0.18	0.5	0.5	0.18	0.18	0.18
Supply voltage [V]	± 1	1.8	± 0.75	1.1	± 1	± 1	0.8	± 0.5	± 0.5
Capacitive load [pF]	80	200	100	100	70	70	130	160	160
Stage Type	Single	Single	Single	Pseudo-Single	Single	Single	Single	Single	Single
Class Type	Super-AB	AB	Super-AB	AB	AB	Super-AB	Super-AB	A	AB
Pos. Slew Rate [V/µs]	20	74.1	4	8.7	9.8	13.2	1.24	0.063	1.28
Neg. Slew Rate [V/µs]	-54	--	-4.5	--	-7.6	-25.3	-0.826	-0.059	0.60
Pos. settling (1%) [µs]	--	--	9.5	1.2	0.096	0.12	0.55	91.9	5.3
Neg. settling (1%) [µs]	--	--	1.6	--	0.074	0.10	0.56	91.2	5.7
GBW [MHz]*	3.46	86.5	0.038	1.7	4.75	3.4	1.12	0.013	0.0221
Phase Margin [°]	58	50	90	69	60	75.1	67.9	90	90
THD [dB]	-41 @100 kHz 0.9 V_{pp}	--	-56 @1 kHz 0.75 V_{pp}	--	-41 @100 kHz 1 V_{pp}	-55.5 @25 kHz 0.5 V_{pp}	-56.3 @10 kHz 0.1 V_{pp}	-61.4 @1 kHz 0.2 V_{pp}	-61.2 @1 kHz 0.2 V_{pp}
Eq. Input Noise [nV/√Hz]	44.7 @100 kHz	0.8 @100 kHz	71.4 @38 kHz	--	35 @1 MHz	35 @1 MHz	68.8 @100 kHz	119.1 @10 kHz	107.2 @20 kHz
DC gain [dB]*	39	72	46	100	81.7	76.8	102.7	30.5	33.1
CMRR (DC) [dB]	70	--	106	--	78	112	137.7	--	67.6
PSRR+ (DC) [dB]	37	--	47	--	72	92	114.8	--	44.6
PSRR− (DC) [dB]	70	--	69	--	74	113	136.9	--	53.6
Input offset [mV]†	--	--	-0.3	--	6	--	1.24	-1.0	-1.5
Power [µW]	140	11900	1.8	7.4	120	100	36	2.2	2.5
Area [mm²]	0.054	0.070	0.012	0.0021	0.024	0.030	0.021	0.0011	0.0013
FOM_L [(V/µs)(pF/µW)]	21.14	1.25	236.1	117.57	5.08	13.48	3.73	4.44	60.16
FOM_S [(MHz)(pF/µW)]	1.98	1.45	2.1	22.97	2.77	2.38	4.04	0.95	1.41

* Extrapolated values with unity-gain closed-loop measurements.
† Averaged with 10 chips.

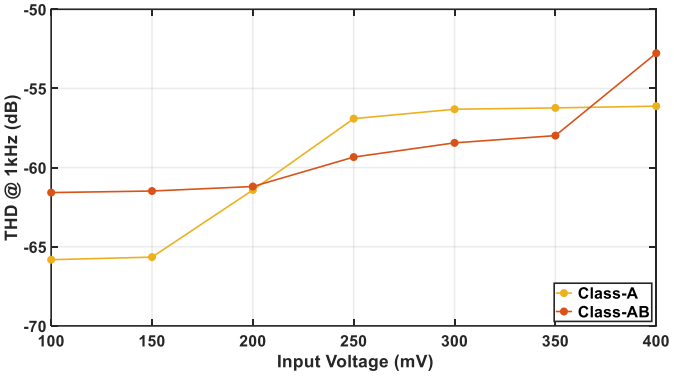

Fig. 8. Measured class-A | class-AB THD vs V_{in}.

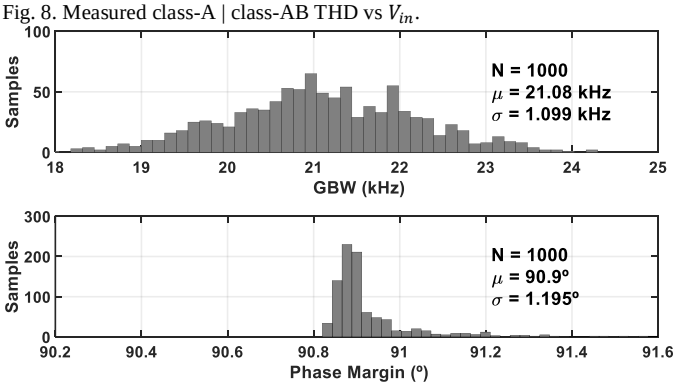

Fig. 9. GBW and phase margin Monte-Carlo analysis for $V_{DS3} = 50$ mV.

A OTA was fabricated in unity gain closed-loop. The transistor aspect ratios are set as summarized in Table I. The supply voltage was ±0.5 V, and the bias current I_b was 500 nA. In this way, all transistors were biased in weak inversion. Finally, V_{DS3} was set to 50 mV in the limit of saturation and triode regions to exploit the non-linear behavior. This was achieved by selecting $x = 3$ according to equation (6).

Fig. 5 shows the measured class-AB DC open-loop output current versus differential input voltage, driven by an Agilent 33522A arbitrary waveform generator. In order to measure it, a transimpedance amplifier was connected for current-to-voltage conversion. The response was measured in a Tektronix MSO44 oscilloscope. Note the class-AB effect, with an output not limited by the bias current. In this way, the current boosting factor (CB), i.e. the ratio between the maximum output current and the bias tail, is $CB = I_{out}^{MAX}/2I_b \approx 390$, which is computed with $I_{out}^{MAX} \approx 390$ µA and $2I_b = 1$ µA.

In order to characterize the slew rate, the unity-gain configurations were used with a 400 mV - 4 kHz square input signal. Fig. 6 shows both class-A and class-AB measured responses. It can be seen the slew rate and settling time improvement in the class-AB amplifier.

Measured open-loop and unity-gain closed-loop frequency responses are shown in Fig. 7. For the class-AB case, the open-loop gain was $A_{OL} \approx 33.5$ dB. The measured closed-loop unity gain was $A_{CL} \approx -190$ mdB. Defining $A_{CL} = A_{OL}/(1 + A_{OL})$, the extrapolated open-loop gain is 33.1 dB, both values being consistent with each other. The open-loop GBW was 27.2 kHz and the closed-loop -3 dB bandwidth was 22.1 kHz with a phase of −45º. Hence, the extrapolated phase margin is 90º that is a good approximation due to the strong dominant output pole. Regarding class-A amplifier, $A_{CL} \approx$ -255 mdB therefore the extrapolated open-loop gain is 30.5 dB. The closed-loop -3 dB bandwidth was 13.0 kHz with a phase of −45º. The increment

of GBW in class-AB amplifier is produced by the non-linear behavior that enhances current gain with very low power degradation. This also increases DC gain, with the corresponding improvement in closed-loop accuracy.

Fig. 8 shows the measured total harmonic distortion (THD) of both class-A and class-AB OTAs for an input sinusoid of 1 kHz and peak-to-peak input amplitudes ranging from 100 mV to 400 mV. It can be seen how linearity is degraded for higher input values, especially in the class-AB case, mainly produced by the strong non-linear behaviour.

A Monte-Carlo analysis in Fig. 9 reveals the effects of process as well as mismatch variations in terms of GBW and phase margin, obtained for a run of 1000 simulations. As seen, both GBW and phase margin values exhibit low variations since V_{DS} has been selected within a safe DC operation area that guarantees the amplifier's stability. Also, note how measurements are in concordance with the Monte-Carlo mean values. In order to increase the robustness against PVT and mismatch variations, various alternatives can be considered. For instance, larger transistor lengths may increase the robustness at the cost of degrading silicon area and bandwidth. A more sophisticate approach may contemplate the use of on-chip automatic correction mechanisms that could compensate electronically any V_{DS} variation, at the cost of increasing the amplifier's complexity, power consumption, noise and area.

Table II summarizes the main measured parameters and compares them with other existing amplifiers. To compare quantitatively the OTA performance with other reported designs, the following well-known two couples of figure-of-merit are used

$$FOM_L = SR\frac{C_L}{P} \tag{12}$$

$$FOM_S = GBW\frac{C_L}{P} \tag{13}$$

The equations reflect the performance in terms of large- and small-signal for a given capacitive load and power consumption, respectively. Comparing the proposed class-AB amplifier with the standard class-A, it can be seen the performance improvement, leading an outstanding result in large-signal with an excellent figure-of-merit. Regarding the other reported designs, references [7], [8] and [10] have been selected as they use the class-AB non-linear current mirror approach for driving large capacitive loads. Note how the proposed amplifier has an excellent FOM_L, only surpassed by [10]. However, [10] has used the local common-feedback technique with embedded passive resistors, increasing silicon area by approximately 10 times, and hence limiting its use those applications requiring a large quantity of devices. In spite of employing a non-linear current mirror approach, [9] has not been included in the comparison since the device has not been fabricated and only simulation results are provided. References [12]-[15] are amplifiers that also employ class-AB solutions for high driving capability. It can be seen how [12] has better FOM_L and FOM_S values in comparison with the proposed solution. However, this reported OTA includes an additional gain-booster circuit as well as several bias branches. For those applications requiring a large number of amplifiers, this would result in a significant increment in DC static power consumption as well as a reduction in current-efficiency.

V. Conclusions

A power-efficient class-AB technique and its application to single-stage OTAs has been presented. It is based on a NL-CM as an active load of a differential pair biased in weak inversion that boosts the input pair's current beyond its quiescent value directly at output branch, achieving a nearly ideal current efficiency. In addition to large-signal, a proper DC bias point can be set to enhance the small-signal properties. Due to low DC quiescent currents, high driving capability and low silicon area, the amplifier is highly suitable for those applications requiring a large quantity of devices for large capacitive loads with high-performance slew rates, settling times and power efficiency.

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