# Zero-Loss Switching in $LLC$ Resonant Converters under Discontinuous Conduction Mode: Analysis and Design Methodology

David Elizondo, *Graduate Student Member, IEEE,* Ernesto L. Barrios, *Member, IEEE,* Iñaki Larequi, Alfredo Ursúa, *Senior Member IEEE,* Pablo Sanchis, *Senior Member IEEE*

***Abstract*—Many thriving applications where isolation is required, such as LED drivers, traction and EV fast charging, implement $LLC$ resonant converters, particularly when voltage regulation is not required or an additional conversion stage is in charge of it. The $LLC$ converter can be operated under discontinuous conduction mode (DCM), due to its advantages such as unregulated and sensorless operation, fixed switching frequency and voltage gain, and zero-current switching (ZCS). However, ZCS results in EMI and switching losses in the primary converter, particularly for ≥1200-V devices. Alternatively, zero-loss switching (ZLS) can be accomplished by means of a proper design of the $LLC$ converter, overcoming the drawbacks of ZCS. The focus of this paper is to perform an exhaustive research on the $LLC$ converter under DCM-ZLS: discontinuous conduction mode with lossless switching in the primary and secondary sides. As a result of this analysis, a set of design boundaries are deduced for parameters such as the magnetizing inductance, the leakage inductance, and the gate resistance. A comprehensive, step-by-step design methodology is proposed and applied to a 18-kW, 200-kHz test bench. The designed parameters are implemented in the converter and several experiments are conducted, including a test at rated input voltage and rated power (600 V, 18 kW). The conduction states studied theoretically in the analysis of the $LLC$ converter are identified in the experimental results, and the operation of the test bench under DCM-ZLS is verified.**

***Index Terms*—$LLC$ converter, zero-loss switching, discontinuous conduction mode, high-frequency power transformer, resonant power conversion, soft-switching.**

## I. Introduction

POWER applications where isolation is required, such as LED drivers [1]–[3], electric vehicles [4]–[14], and solid-state transformer (SST) for traction [15]–[17] and smart grids [18]–[21], tend to avoid the implementation of transformers operating in line frequency (50-60 Hz). The main reason is that low-frequency power transformers are bulky and heavy [22]. The preferred alternative is to use high-frequency (HF) power transformers within dc-dc power conversion structures. Operating at high switching frequencies, the size and weight of the transformer can be significantly reduced [23]. However, the boost in the switching frequency is restricted by the capability of the semiconductor system of dissipating the consequent extra switching power losses. Aiming to overcome this limitation, soft-switching mechanisms such as zero-voltage switching (ZVS) and zero-current switching (ZCS) have been widely studied in the literature [22], [24], [25].

This work is part of the project PID2019-110956RB-I00, funded by MCIN/AEI/10.13039/501100011033/, and has also been supported by the Public University of Navarra (UPNA) under a PhD scholarship.

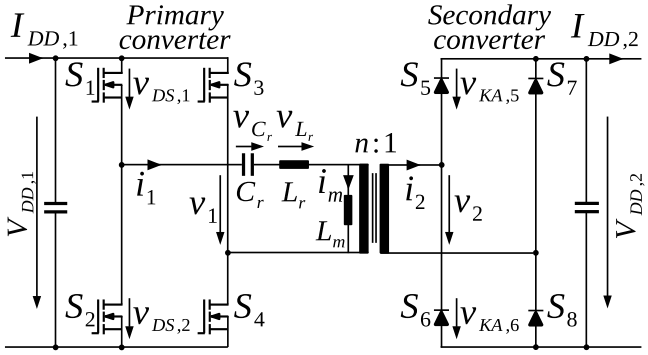



Fig. 1. Circuit diagram of unidirectional, full-bridge $LLC$ resonant converter.

One of the most used dc-dc topologies is the $LLC$ resonant converter [5], [10], [13], [26]–[31], such as the one depicted in Fig. 1 for a unidirectional, full-bridge $LLC$ converter. It is derived from the series resonant tank, which comprises of a capacitor $C_r$ and an inductance $L_r$ in series. Since there is a high-frequency transformer to provide the required galvanic isolation, a parallel inductance, which is the magnetizing inductance $L_m$, is also present in the resonant tank, thus becoming $LLC$. There are plenty of isolated dc-dc applications where voltage regulation is not required [32], [33] or regulation is provided by another conversion stage [26], [27], [31], [34], [35]. Hence, the $LLC$ converter can be operated under discontinuous conduction mode (DCM) at a fixed switching frequency $f_{sw}$, which enables a constant voltage gain. In this conduction mode, the resonant converter is operated below the resonance ($f_{sw} < f_r$), and with a fixed duty cycle of 0.5 in an unregulated, sensorless manner.

DCM is an interesting option, for it enables the optimization of the magnetic components in the resonant tank for a single frequency [30], instead of the lowest of a wide range of switching frequencies, as in converters under continuous conduction mode (CCM) [36]–[38]. Furthermore, ZCS is accomplished for both primary and secondary converters [22], [32], [39]. Nevertheless, as discussed in several papers [22], [40], ZCS in primary switches is not free of switching losses. ZCS also results in EMI, due to the abrupt voltage transient in the parasitic capacitances of the semiconductors. Typically, the alternative is the turn-on ZVS, achieved by means of the magnetizing current. However, the research on this matter is focused on the primary converter, neglecting the influence

on the switching process of the stray capacitance of the HF transformer, the parasitic capacitances of the secondary converter, or the initial blocking voltage of the secondary devices [11], [33], [41].

With the converter accomplishing turn-on ZVS, turn-off losses may still take place in the primary, but the current during the switching process is only the magnetizing current nonetheless, independently of the delivered power. This makes it possible to achieve lossless turn-off too by means of a proper design of the gate resistance, resulting in a zero-loss switching (ZLS). Hence, DCM-ZLS ensures lossless turn-on and turn-off in both primary and secondary converters, regardless of the load condition, and a fixed voltage gain. It is worth mentioning that the $LLC$ converter under DCM-ZLS works so the magnetizing inductance is used as a current source to achieve soft-switching, not as a resonant element as in CCM with $f_{sw} < f_r$ [4], [36].

To the best of the authors knowledge, despite $LLC$ converters under DCM are frequently used in industrial applications, and notions such as DCM, ZCS and ZVS are common in the literature, there is a lack of a comprehensive, all-in-one review of these concepts applied to $LLC$ resonant converters under DCM. This paper aims to provide an in-depth analysis of discontinuous conduction mode (DCM) in Section II. This conduction mode is the basis to achieve the aforementioned ZLS.

In Section III, a detailed review on conventional ZCS is performed. The drawbacks of this switching mechanism are summarized and the switching power losses due to ZCS are obtained. Then, the concept of ZLS is explained in Section IV. It is the result of combining a conventional turn-on ZVS using the magnetizing current with a fast, lossless turn-off process, which is achieved by putting out the channel of the conducting primary switches before they start blocking voltage. Supported by figures and equations, the switching process is analyzed and two requirements are deduced: for the magnetizing current in order to achieve lossless turn-on, and for the gate resistances in the primary converter to accomplish lossless turn-off.

Aiming to provide a straightforward and useful application of the obtained requirements to real converters, a step-by-step design methodology is proposed in Section V. The procedure can be easily followed, even if the designer skips the sections where the principles of the $LLC$ converters under DCM-ZLS are studied. The proposed methodology includes design limits for the series resonant inductance, the magnetizing inductance and the gate resistance in order to operate under DCM-ZLS. A simple expression, independent of the input voltage and the load condition, to estimate the required dead time for the soft-switching event is also obtained. Additionally, each step in the design is applied to a 18-kW, 200-kHz test bench. Finally, experiments are conducted on the test bench with the designed characteristics. Two tests are performed: at partial load and with a dc input voltage of 400 V, and at rated power and rated dc input voltage of 600 V. The experimental results are presented in Section VI. The conduction states of the $LLC$ converter analyzed theoretically in Section IV are identified. The accomplishment of DCM-ZLS, and the accuracy of the required dead time estimation are also discussed.

## II. Discontinuous Conduction Mode

Discontinuous conduction mode (DCM) in resonant converters has been deeply analyzed in various publications, e.g. [24], [42]. DCM has gathered attention due to the accomplishment of zero-current switching (ZCS) in both primary and secondary converters, regardless of the load condition. In this section, the specifications to operate the resonant converter under DCM are deduced.

The primary side of the $LLC$ resonant converter switches with a duty cycle of 0.5 and the secondary side works as a synchronous rectifier. In this analysis, the positive half-switching period is considered, that is when $v_1 > 0$. In order to operate under DCM, the resonant converter must fulfill the next two conditions:

*1) The resonant current must reach zero before the end of each half-switching period:* This means that the switching-to-resonant frequency ratio must fulfill:

$$k < 1, \tag{1}$$

where:

$$k = f_{sw}/f_r = f_{sw} 2\pi \sqrt{L_r C_r}, \tag{2}$$

being $f_{sw}$ the switching frequency, $f_r$ the series resonant frequency, $L_r$ the series resonant inductance, and $C_r$ the series resonant capacitance. The rms value of the resonant current in the primary depends on $k$, the primary dc-link bus voltage $V_{DD,1}$, and the delivered active power $P$ as follows:

$$I_1 = \frac{P\pi}{2\sqrt{2k} V_{DD,1}}. \tag{3}$$

*2) The resonant current must remain at zero during the switching process of the converter:* At t = 0, the primary converter applies a voltage $v_1 = V_{DD,1}$ which excites the series resonant tank, comprised of $L_r$ and $C_r$. As a result, a resonant current circulates through the HF tank. After one half-cycle of the resonance, the current in the secondary $i_2$ reaches zero at $t = T_r/2$. It must remain at zero until $t = T_{sw}/2$ in order to work under DCM. This means that the initial condition of the resonant current is zero too. Therefore, the resonant current intensity in the secondary under DCM can be expressed as:

$$\begin{aligned} i_2 = \frac{P\pi n}{2k V_{DD,1}} sin(t 2\pi f_{sw}/k), \qquad & t \in (0, T_r/2), \\ i_2 = 0, \qquad & t \in (T_r/2, T_{sw}/2), \end{aligned} \tag{4}$$

where $n$ is the transformer turns ratio, $T_r/2$ is half of the period of the series resonance, and $T_{sw}/2$ is half of the switching period.

As can be seen in Fig. 2 (a), during the first time interval $v_{L_r} = -v_{C_r}$ due to the series resonance. The equivalent circuit of the converter is shown in Fig. 2 (b). Then, during the second time interval $t_{DCM}$, the discontinuity in $i_2$ takes place, which is only possible if all the four diodes of the secondary converter become reverse biased simultaneously at $t = T_r/2$. At this instant, the current in the primary side $i_1$ equals the magnetizing current $i_m$. The voltage across the resonant capacitor becomes approximately constant and at its

peak value ($v_{C_r} = V_{C_r}$), while $v_{L_r} \approx 0$, since it is only due to $i_m$.

The ac secondary voltage referred to the primary side, which is defined by $v_2' = v_1 - v_{C_r} - v_{L_r}$, can be particularized as $v_2' = V_{DD,1} - V_{C_r}$ at the instant when the discontinuity time begins. Then, the voltages in the diodes of the secondary converter can be deduced considering also that $v_2' = V_{DD,2}' - v_{KA,5}' - v_{KA,8}'$. Assuming identical diodes, the share of the voltage in the diodes are:

$$\begin{aligned} v_{KA,5}'(T_r/2) = v_{KA,8}'(T_r/2) = (V_{DD,2}' - V_{DD,1} + V_{C_r})/2, \\ v_{KA,6}'(T_r/2) = v_{KA,7}'(T_r/2) = (V_{DD,2}' + V_{DD,1} - V_{C_r})/2. \end{aligned} \tag{5}$$

The equivalent circuit of the converter during $t_{DCM}$ is depicted in Fig. 2 (c). All the diodes in the secondary side become reverse biased if all the voltages in (5) are positive, so:

$$\begin{aligned} V_{DD,2}' - V_{DD,1} + V_{C_r} > 0, \\ V_{DD,2}' + V_{DD,1} - V_{C_r} > 0, \end{aligned} \tag{6}$$

which can be simplified by introducing the ratio between the primary and secondary dc voltages.

The voltage gain of the $LLC$ resonant converter under DCM can be deduced from the following expressions for the dc input and output currents, respectively, regarding that the converter works with no reverse energy flow:

$$\begin{aligned} I_{DD,1} = \frac{1}{T_{sw}/2} \int_0^{T_{sw}/2} i_1 \, dt, \\ I_{DD,2} = \frac{1}{T_{sw}/2} \int_0^{T_{sw}/2} |i_2| \, dt = \frac{1}{T_{sw}/2} \int_0^{T_{sw}/2} i_2 \, dt. \end{aligned} \tag{7}$$

In the $LLC$ converter, $i_1 = i_m + i_2/n$, but the effect of the magnetizing current on the voltage gain is negligible nonetheless, since typically $L_m >> L_r$. Thus, $i_1 \approx i_2/n$ can be assumed. Introducing this identity into (7), it is obtained that:

$$I_{DD,1} \approx \frac{1}{T_{sw}/2} \int_0^{T_{sw}/2} i_2/n \, dt = I_{DD,2}/n. \tag{8}$$

Applying the power balance $V_{DD,1} I_{DD,1} = V_{DD,2} I_{DD,2}$, the voltage gain is as follows:

$$\frac{V_{DD,2}}{V_{DD,1}} = \frac{1}{n} \Rightarrow V_{DD,2}' = V_{DD,1}. \tag{9}$$

As a consequence of operating under DCM, the voltage gain of the $LLC$ converter is constant and only dependent on the transformer turns ratio [24], [42].

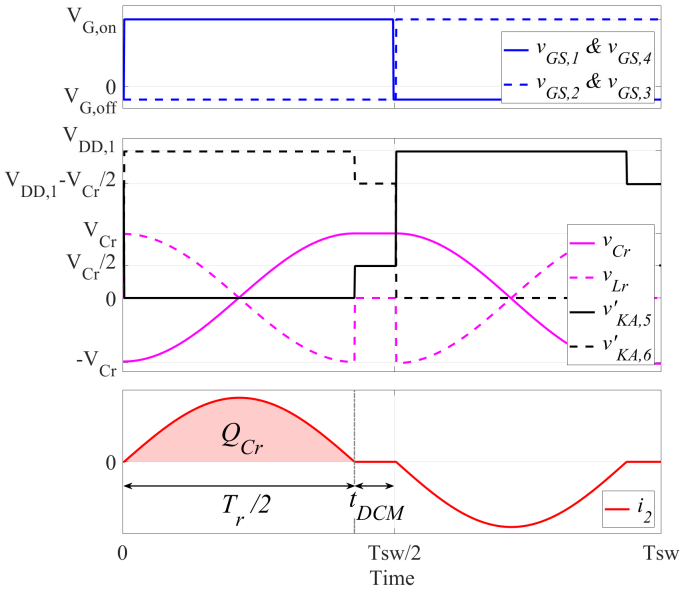
Updating the expressions in (5) and (6), respectively, the voltages across the diodes of the secondary at the beginning of $t_{DCM}$ become:

$$\begin{aligned} v_{KA,5}'(T_r/2) = v_{KA,8}'(T_r/2) = V_{C_r}/2, \\ v_{KA,6}'(T_r/2) = v_{KA,7}'(T_r/2) = V_{DD,1} - V_{C_r}/2, \end{aligned} \tag{10}$$

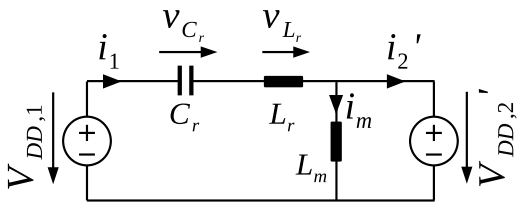
and the following boundaries for the resonant capacitor voltage in order to ensure DCM are obtained:

$$0 < V_{C_r} < 2V_{DD,1}, \tag{11}$$

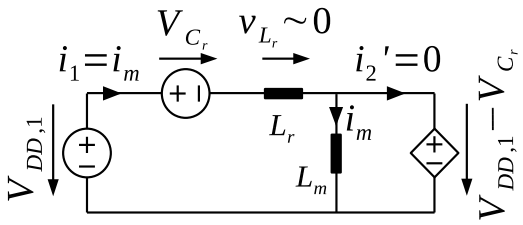
where the lower limit is trivial. Despite the simplicity of the upper boundary, it may not be a straightforward expression to be used during design. Thus, it is convenient to transform it into a more useful expression, linking it to the load condition. First, $V_{C_r}$ is related to its charge $Q_{C_r}$. During the resonant half cycle, the voltage in the series resonant capacitor changes from its negative peak value at $t = 0$ to its positive peak




(a)




(b)




(c)

Fig. 2. $LLC$ resonant converter under DCM: (a) Main waveforms, referred to the primary side. (b) Equivalent circuit referred to the primary during the series resonance, $t \in (0, T_r/2)$. (c) Equivalent circuit referred to the primary during the discontinuity time $t_{DCM}$, $t \in (T_r/2, T_{sw}/2)$

value at $t = T_r/2$, as depicted in Fig. 2 (a). Hence, the charge introduced in the capacitor during the resonant half cycle is:

$$Q_{C_r} = \int_{-V_{C_r}}^{V_{C_r}} C_r \, dv_{C_r} = 2C_r V_{C_r}. \tag{12}$$

The introduced charge is also linked to the primary current. While the positive half-switching period is taking place, the resonant current is positive, so it charges $C_r$. The capacitor charge and the current are related through:

$$Q_{C_r} = \int_0^{T_r/2} i_1 \, dt. \tag{13}$$

The input dc current intensity can be obtained as:

$$I_{DD,1} = \frac{1}{T_{sw}/2} \int_0^{T_{sw}/2} |i_1| \, dt \approx \frac{1}{T_{sw}/2} \int_0^{T_r/2} i_1 \, dt, \tag{14}$$

where the contribution of $i_m$ can be neglected. Then, (13) and (14) can be combined, resulting in:

$$Q_{C_r} = \frac{T_{sw}}{2} I_{DD,1} = \frac{I_{DD,1}}{2f_{sw}}. \tag{15}$$

The resonant capacitor peak voltage can be related to $I_{DD,1}$ by introducing (15) into (12), resulting in:

$$V_{C_r} = \frac{I_{DD,1}}{4C_r f_{sw}}. \tag{16}$$

The following identity can be introduced for the delivered active power: $P = V_{DD,1} I_{DD,1}$. The relationship between $L_r$ and $C_r$, that can be deduced from (2) as:

$$C_r = \frac{k^2}{(2\pi f_{sw})^2 L_r}, \tag{17}$$

can also be introduced in the expression for $V_{C_r}$, which becomes:

$$V_{C_r} = \frac{P\pi^2 L_r f_{sw}}{k^2 V_{DD,1}}. \tag{18}$$

Finally, substituting (18) into (11), and rearranging the expression, the active power limit to operate under DCM is:

$$P < P_{lim} = \frac{2k^2 V_{DD,1}^2}{\pi^2 L_r f_{sw}}. \tag{19}$$

To sum up, from the performed analysis, it can be observed that:

- The closer $k$ to unity ($f_{sw} \to f_r$), the lower the current intensity rms value for a given active power, according to (3), which results in lower conduction losses.
- The closer $k$ to unity, the shorter the discontinuity time $t_{DCM}$, which influences the switching process, as it is discussed later in this paper.
- The voltage gain of the converter under DCM is fixed, with a value of $1/n$, as obtained in (9).
- DCM is ensured as long as $k$ and $P$ fulfill (1) and (19), respectively.
- The smaller $L_r$, the greater the power capability achievable under DCM.
- This analysis and the resulting requirement for the active power are also valid for bidirectional, CLLLC resonant converters. In that case, $C_r$ and $L_r$ are the equivalent series capacitance and inductance, respectively, referred to the primary side.

## III. Review on Zero-Current Switching (ZCS) and Incomplete Zero-Voltage Switching (iZVS)

Under DCM, the resonant current becomes zero before the half-switching period ends. Therefore, ZCS is accomplished for the secondary switching devices [24], [42], [43]. It must be noted that ZCS in the primary converter, i.e. switching process with null $i_1$, only takes place in the series resonant converters. Since in the $LLC$ converter there is the magnetizing inductance of the transformer, the current in the primary side is not zero. Certain charge is switched in the primary devices during the dead time due to the magnetizing current.

The converter must be properly designed to meet the requirements for turn-on ZVS in the primary, which are discussed in the following Section IV. In this current section, the switching process when the converter fails to achieve turn-on ZVS is reviewed: the incomplete ZVS (iZVS) and, particularly, the zero-current switching (ZCS). In these scenarios, the transistors in the primary side turn on when they still block voltage. Both ZCS and iZVS cause switching power losses [15], [25], [40] and EMI in the primary converter, although the former is logically more severe, since the energy associated with the full bus voltage is dissipated.

The ZCS/iZVS process can be explained starting from the equivalent circuit of a single switching cell of the primary converter, as shown in Fig. 3, where the output parasitic capacitances $C_{oss}$ and the channel resistance $R_{ds,on}$ have been included. When $S_i$ is conducting, $v_{DS,i} \approx 0$. Thus, the complementary switch of the cell $S_j$ is blocking with $v_{DS,j} \approx V_{DD,1}$, where $V_{DD,1}$ is the dc-link bus voltage.

At the end of the resonant half cycle [see Fig. 3 (a)], the resonant current becomes zero. As a consequence, $i_1 \to i_m$ and $S_i$ turns off with quasi-zero current in the $LLC$ converter. During the dead time, the available current charges $C_{oss,i}$ and discharges $C_{oss,j}$ [see Fig. 3 (b)]. Assuming a general case, at the end of the dead time the switch $S_i$ has a voltage $v_{DS,i} = \Delta v$, and $S_j$ has thus a voltage $v_{DS,j} = V_{DD,1} - \Delta v$ [see Fig. 3 (c)]. When the following half-switching period starts and $S_j$ is turned on, $C_{oss,i}$ and $C_{oss,j}$ are spontaneously charged/discharged through the channel resistance of $S_j$ [Fig. 3 (d)]. Hence, ZCS/iZVS are not lossless. Take into account that ZCS is a particular case of iZVS, where $L_m \to \infty$, so $i_1 = 0$ and no charge/discharge of $C_{oss}$ takes place during the dead time.

The switching power losses resulting from ZCS/iZVS can be calculated by means of an energy balance, following the approach in [25]. The initial state is just at the end of the dead time, and the final state is just after the turn-on of $S_j$. During the dead time, $C_{oss,i}$ has been charged from 0 to $\Delta v$ and $C_{oss,j}$ has been discharged from $V_{DD,1}$ to $V_{DD,1} - \Delta v$. Hence, the initial energy in the primary converter is:

$$E_i = 2E_{oss}(\Delta v) + 2E_{oss}(V_{DD,1} - \Delta v), \tag{20}$$

regarding that the converter is a full bridge working with a duty cycle of 0.5, so there are two switching cells. $E_{oss}(v)$ is the energy stored in the output capacitance $C_{oss}$ when $v_{DS,i} = v$. $E_{oss}(v)$ can be calculated by means of:

$$E_{oss}(v) = \int_0^v v_{DS} C_{oss}(v_{DS}) \, dv_{DS}, \tag{21}$$

where it can be observed that $C_{oss}$ varies with the voltage. Actually, the dependence of the output capacitance on the voltage is nonlinear, which must be regarded in the calculations.
Once $S_j$ has turned on, $v_{DS,i} = V_{DD,1}$ and $v_{DS,j} = 0$. Therefore, the final energy in the primary converter, considering again both switching cells, is:

$$E_f = 2E_{oss}(V_{DD,1}). \tag{22}$$

As can be seen in Fig. 3 (d), represented with a green arrow, the source of the primary converter provides the necessary charge to $S_i$ to switch $v_{DS,i}$ from $\Delta v$ to $V_{DD,1}$. As a result, the delivered energy from the source to the switches is:

$$E_s = 2[Q_{oss}(V_{DD,1}) - Q_{oss}(\Delta v)]V_{DD,1}. \tag{23}$$

Applying the energy balance $E_i + E_s = E_f + E_d$, the dissipated energy in the semiconductors of the primary converter can be obtained as follows:

$$\begin{aligned} E_d = E_i - E_f + E_s = \\ 2E_{oss}(\Delta v) + 2E_{oss}(V_{DD,1} - \Delta v) - 2E_{oss}(V_{DD,1}) + \\ 2[Q_{oss}(V_{DD,1}) - Q_{oss}(\Delta v)]V_{DD,1}. \end{aligned} \tag{24}$$

It can be deduced that, under ZCS, no charge is switched during the dead time, so $\Delta v = 0$ and $E_i = E_f = 2E_{oss}(V_{DD,1})$. The dissipated energy is hence $E_d = 2Q_{oss}(V_{DD,1})V_{DD,1}$. Regarding that this energy loss takes place each time the primary converter switches voltage, which is twice a switching period, the switching power losses in the primary converter under ZCS can be obtained as:

$$\begin{aligned} P_{sw} &= 4Q_{oss}(V_{DD,1})V_{DD,1}f_{sw} = \\ &= 4C_{ossQeq}(V_{DD,1})V_{DD,1}^2 f_{sw}, \end{aligned} \tag{25}$$

where $C_{ossQeq}$ is the charge-equivalent output capacitance, which is calculated by integration of $C_{oss}$ with respect to $v_{DS}$ from 0 to $V_{DD,1}$, keeping in mind that the output capacitance has a nonlinear behavior. As can be seen, the charging/discharging of the output parasitic capacitances under ZCS/iZVS leads to power losses in the channel of the device which is turned on, regardless of the channel resistance $R_{ds,on}$ [44]. It becomes clear from (25) that the larger $C_{oss}$ and the higher $V_{DD,1}$, the greater the switching power loss. Hence, the switching losses under ZCS/iZVS are not negligible, particularly in power converters that require $\geq$1200-V devices.

Additionally to the switching losses, iZVS/ZCS also lead to EMI, for part/all of the dc-link bus voltage is abruptly switched from one transistor to the complementary. As a result, the output capacitances resonate with the stray inductance of the semiconductors, as depicted in Fig. 4 (a) for ZCS and in Fig. 4 (b) for iZVS.

## IV. Zero-Loss Switching (ZLS)

If the $LLC$ resonant converter is conveniently designed, DCM-ZLS can be achieved, which is the combination of ZCS in the secondary devices, and turn-on ZVS and no-channel (lossless) turn-off in the primary devices, while operating the converter under DCM. The conditions for DCM have already been deduced in Section II. Nevertheless, additional requirements apply to achieve lossless switching in the primary.

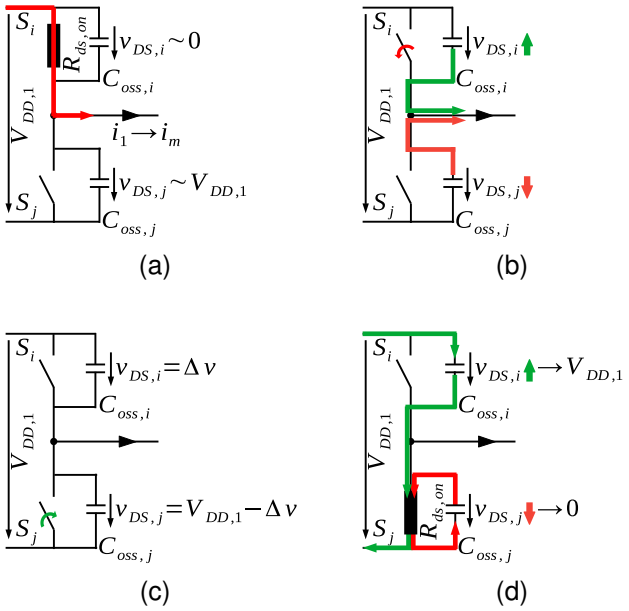



Fig. 3. Step-by-step iZVS process in a switching cell: (a) $S_i$ is on, $S_j$ is off, $i_1$ becomes $i_m$. (b) $S_i$ turns off and there is a partial charge/discharge of $C_{oss}$ during the dead time. (c) $S_j$ turns on when it is still blocking voltage. (d) Charging of $C_{oss,i}$, and discharging of $C_{oss,j}$ through the channel resistance of $S_j$.

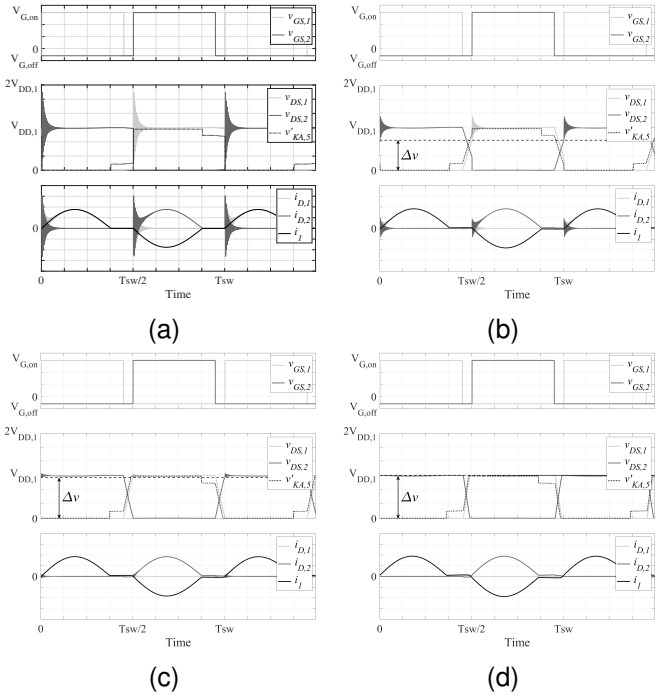



Fig. 4. Switching of the resonant converter under DCM: (a) With ZCS. (b) With iZVS, breach of the first requirement for $i_m$. (c) With iZVS, breach of the second requirement for $i_m$. (d) With ZVS.

### A. Conduction states

The $LLC$ resonant converter under DCM-ZLS shows up to four conduction states. For the sake of clarity, the main waveforms are depicted in Fig. 5 (a), together with the circuits of the converter in each conduction state, where the key components are highlighted. The conduction states can be

summarized as:

*1) State 1:* See Fig. 5 (b). It comprises of the resonant half-cycle between $L_r$ and $C_r$. Regarding the positive half-switching period, $S_1$ and $S_4$ in the primary, and $S_5$ and $S_8$ in the secondary, are on. Hence, $v_1 = V_{DD,1}$ and $v_2 = V_{DD,2}$. During this state, power is delivered. The magnetizing inductance $L_m$ is clamped to $V_{DD,1}$ by the primary converter.

*2) State 2:* Represented in Fig. 5 (c). It begins when $i_2 = 0$. The secondary devices are reverse biased, while the dead time in the primary converter has not started yet. Thus, $v_1 = V_{DD,1}$ and $v_{C_r} = V_{C_r}$, so $L_m$ becomes clamped to $V_{DD,1} - V_{C_r}$. The blocking voltage of $S_5$ and $S_8$ has a mean value of $V_{C_r}/2$ referred to the primary, as obtained in Section II. Additionally, since the diodes are not conducting, there is a parasitic resonance between $L_r$ and $C_{sec}/n^2$. The resonant capacitor $C_r$ is large enough to be considered as a constant voltage source until the next half-switching period.

*3) State 3:* Refer to Fig. 5 (d). It takes place once all the switches are turned off. During the dead time, the voltages of the primary and the secondary sides switch simultaneously. The role of the magnetizing current $i_m$ is to charge/discharge the parasitic capacitances of the primary switches $C_{pri}$, the HF transformer $C_{str}$ and the secondary devices $C_{sec}$. The share of the current in this process is proportional to the relative value of the parasitic capacitance, so the slope of the voltage is the same in the primary and the secondary. Additionally, there is a parasitic resonance between $L_r$ and $(C_{pri} + C_{str})C_{sec}/n^2/(C_{pri} + C_{str} + C_{sec}/n^2)$, since during this state no semiconductor is on.

*4) State 4:* Depicted in Fig. 5 (e). If the conventional ZVS requirement for $i_m$ is met, the secondary converter switches its voltage within the dead time, and $S_6$ and $S_7$ start to conduct. There is a disadvantaged initial condition of the primary with respect to the secondary devices, i.e. $v_{DS,1} = 0$ while $v'_{KA,5} = V_{C_r}/2$ at the beginning of state 3. As a result, when $v'_{KA,5}$ reaches $V'_{DD,2}$, $v_{DS,1} < V_{DD,1}$. Then, $L_m$ becomes clamped to $-V'_{DD,2}$ by the secondary converter, so all the magnetizing current flows through the secondary side, leaving the primary with no net current. Therefore, the conventional requirement on $i_m$ may not be enough to ensure that the primary actually turns on under ZVS. An additional condition of $i_m$, which is obtained later in this section, is required so $v_{DS,1}$ reaches $V_{DD,1}$ before the dead time ends. In this state, $L_r$ resonates with $C_{pri} + C_{str}$.

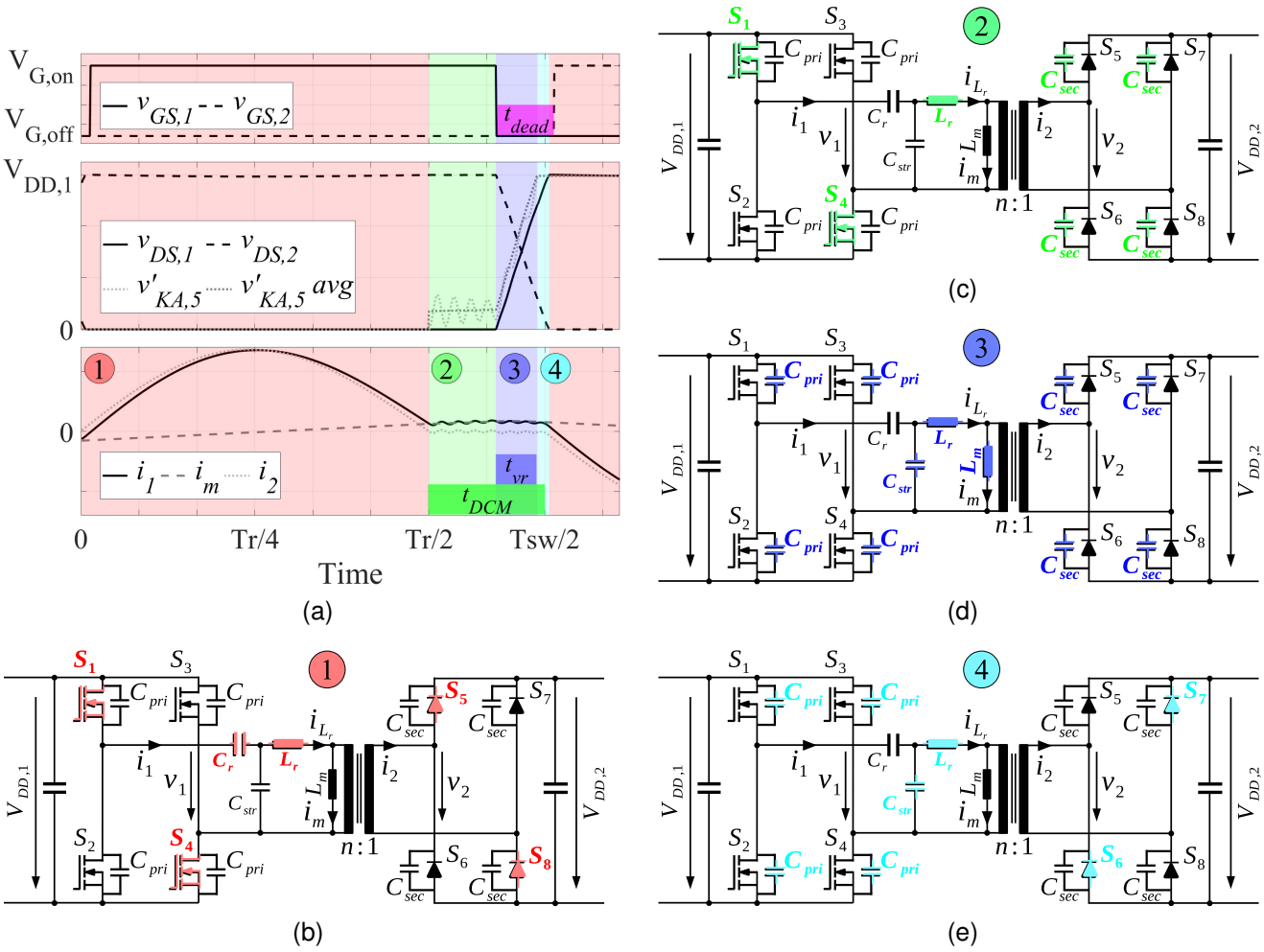



Fig. 5. Conduction states of the $LLC$ resonant converter under DCM-ZLS: (a) Main waveforms: top, gate voltages in a switching cell of the primary converter; middle, voltages across selected transistors and diode; bottom, selected currents. (b) State 1, positive resonant half cycle. (c) State 2. (d) State 3. (e) State 4.

### B. Turn-on zero-voltage switching

To achieve turn-on ZVS in the primary devices, it is necessary that enough current remains in the primary of the resonant tank, so the parasitic capacitances can be completely charged/discharged during the dead time (state 3 + state 4). This way, the body diode of $S_j$ is forward biased before its MOSFET is turned on. Then, the MOSFET of $S_j$ is turned on with zero losses.

*1) Magnetizing current in the switching process:* During state 1, $L_m$ is clamped to $V_{DD,1}$. As a result, the magnetizing current has a constant slope from $t = 0$ to $t = T_r/2$ and responds to:

$$\frac{di_m}{dt} = \frac{V_{DD,1}}{L_m}. \tag{26}$$

Then, during state 2, the applied voltage to $L_m$ is no longer $V_{DD,1}$, but $V_{DD,1} - V_{C_r}$ (assuming that the voltage drop in $L_r$ due to $i_m$ is negligible). Thus, the slope of $i_m$ is:

$$\frac{di_m}{dt} = \frac{V_{DD,1} - V_{C_r}}{L_m}. \tag{27}$$

As a result, the current available for state 3, that is the switching event, can be obtained as:

$$i_m = i_m(0) + \frac{V_{DD,1}}{L_m}\frac{T_r}{2} + \frac{V_{DD,1} - V_{C_r}}{L_m}(t - \frac{T_r}{2}), \tag{28}$$

where $i_m(0)$ is the magnetizing current intensity at $t = 0$. As can be seen, $i_m$ increases if $V_{DD,1} - V_{C_r} > 0$, or decreases if $V_{DD,1} - V_{C_r} < 0$. Logically, the first scenario is the desired one, since it leads to larger available current during the switching process [45]. Therefore, $V_{C_r} < V_{DD,1}$ should be achieved [see Section V-C].

The available current to achieve ZVS, $i_m(ZVS)$, depends on the instant when the switching process begins, i.e. depends on the dead time $t_{dead}$ of the switches in the primary converter. For the design process, the conservative scenario in which $i_m$ remains constant for $t \in (T_r/2, T_{sw}/2)$ can be considered. In that case, the magnetizing current during the switching event is assumed to be:

$$i_m(ZVS) = \frac{V_{DD,1}k}{4L_m f_{sw}}. \tag{29}$$

*2) First requirement for the magnetizing current:* Under DCM, the discontinuity time $t_{DCM}$ takes place between $t = T_r/2$ and $t = T_{sw}/2$, regardless of the load. During $t_{DCM}$, the resonant current is zero, as explained in Section III, but turn-on ZVS can be achieved if the magnetizing current of the transformer $i_m$ is large enough to switch the charge in the parasitic capacitances of the converter during this time. Thus, $i_m$ needs to be large enough to ensure:

$$t_{vr} \leq t_{DCM} = \frac{T_{sw} - T_r}{2} = \frac{1-k}{2f_{sw}}, \tag{30}$$

where $t_{vr}$ is the time required by the full switching event in the primary/secondary devices, which corresponds to conduction state 3 [see Fig. 5 (a) for the waveforms and (d) for the circuit during $t_{vr}$].

It must be noted that three different parasitic capacitances are to be charged/discharged in the switching event: $C_{pri}$, $C_{sec}$ ($C_{sec}/n^2$ referred to the primary side), and $C_{str}$. Fig. 6 shows the schematic of the resonant converter, including the relevant parasitics, during state 3. In the primary side, $C_{pri}$ of $S_1$ and $S_4$ switch their voltage from 0 to $V_{DD,1}$ and $C_{pri}$ of $S_2$ and $S_3$ from $V_{DD,1}$ to 0. It is worth mentioning that due to the no-channel turn-off switching, there is no current through the channel of the devices that are turned off in the primary, as it is explained in detail in Section IV-C. As a consequence, during state 3 all the current in the primary is only used to charge/discharge the output parasitic capacitances of the primary switches.

The two cells of the full bridge in the primary switch their voltages simultaneously, and they are complementary ($S_1$ with $S_4$, and $S_2$ with $S_3$). Hence, there is a recirculation of the primary current $i_1$, which is associated to the charge introduced/extracted in one switching cell, that is $2Q_{pri}(V_{DD,1})$. Equivalently, in the secondary side $i_2$ is associated to $2Q_{sec}(V_{DD,2})$. As can be seen, $i_2$ is negative durint $t_{vr}$ according to the sign convention in Fig. 6. The voltage of $C_{str}$ switches from $V_{DD,1} - V_{C_r}$ to $-V_{DD,1} - V_{C_r}$, so $C_{str}$ has to be discharged in this process, extracting a charge of $Q_{str}(2V_{DD,1}) \approx 2Q_{str}(V_{DD,1})$. To sum up, $i_m = i_1 - i_{C_{str}} - i_2/n$. Regarding the sign convention, it becomes $i_m = |i_1| + |i_{C_{str}}| + |i_2|/n$, and thus:

$$i_m = \frac{2Q_{pri}(V_{DD,1}) + 2Q_{str}(V_{DD,1}) + 2Q_{sec}(V_{DD,2})/n}{t_{vr}}, \tag{31}$$

where it can be seen that the larger $i_m$, the shorter $t_{vr}$. Considering the charge-equivalent values of the parasitic capacitances and that $V_{DD,2} = V_{DD,1}/n$, (31) can be expressed as follows:

$$i_m = \frac{2(C_{pri} + C_{str} + C_{sec}/n^2)V_{DD,1}}{t_{vr}} = \frac{2C_{sw}V_{DD,1}}{t_{vr}}, \tag{32}$$

being $C_{sw}$ the equivalent parasitic capacitance involved in the ZVS process, referred to the primary side. If turn-on ZVS is to be achieved by means of the magnetizing current, the following requirement can be obtained by applying the boundary in (30) to (32):

$$i_m(ZVS) \geq \frac{4C_{sw}V_{DD,1}f_{sw}}{1-k}, \tag{33}$$

where $i_m(ZVS)$ is the magnetizing current when the zero-voltage switching process takes place. When $i_m$ fails to fulfill this specification, the full soft-switching event cannot be reached in the available discontinuity time $t_{DCM}$. Therefore,

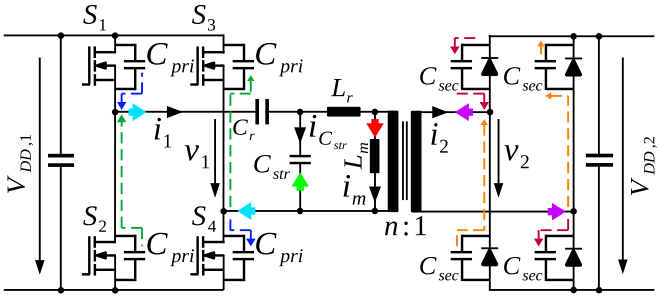



Fig. 6. Current flow during state 3, including parasitic elements, when $S_1$ and $S_4$ switch off, and $S_2$ and $S_3$ are to be switched on.

iZVS takes place in the primary converter, as shown in Fig. 4 (b). The obtained requirement is the conventional specification in the literature for turn-on ZVS in $LLC$ converters under DCM.

It is important to note that even if this requirement is satisfied, the complete soft-switching of the primary might not be achieved. The reason is that the initial condition of state 3 for the secondary devices is different from the primary devices: $v_{DS,1} = 0$ while $v'_{KA,5} = V_{C_r}/2$, as it is obtained in (10), in Section II-2. At the end of state 3 (beginning of state 4), $v'_{KA,5} = V'_{DD,2}$, while $v_{DS,1} = V_{DD,1} - V_{C_r}/2$.

*3) Second requirement for the magnetizing current:* The specification to consummate ZVS in the primary in state 4 can be deduced from $i_1$, which is the current that transfers the charge in the primary devices. Once the secondary converter completely switches, $L_m$ becomes clamped to $-V'_{DD,2}$ and all the magnetizing current flows through the secondary. Hence, the dc component of $i_1$ is zero during state 4, while it has an ac component result of $C_{pri} + C_{str}$ resonating with $L_r$. The transfer of the charge must be carried out by the remaining energy stored in $L_r$, which is related to $i_m$. Solving the circuit in Fig. 5 (e), the following expression is obtained:

$$i_1 = -L_r(C_{pri} + C_{str})\frac{d^2 i_1}{dt^2} \Rightarrow$$
$$i_1 = I_{1p,s4} cos\left(\frac{t}{\sqrt{L_r(C_{pri} + C_{str})}} + \theta_{s4}\right), \quad (34)$$

where $I_{1p,s4}$ is the peak value of the parasitic resonant current in the primary during state 4, and $\theta_{s4}$ the phase. These two numbers can be obtained considering the initial conditions of $i_1$ and $v_1$ in state 4, resulting in:

$$i_1 = i_m(ZVS)\frac{C_{pri}}{C_{sw}} cos\left(\frac{t}{\sqrt{L_r(C_{pri} + C_{str})}}\right). \quad (35)$$

The peak value of the resonant component of $v_{DS,1}$ must reach $V_{C_r}/2$ in order to achieve ZVS. This means that the amplitude of $v_1$, which can be expressed as:

$$V_{1,r} = L_r\frac{C_{pri} + C_{str}}{C_{pri}}\frac{I_{1p,s4}}{\sqrt{L_r(C_{pri} + C_{str})}} \Rightarrow$$
$$V_{1,r} = i_m(ZVS)\frac{\sqrt{L_r(C_{pri} + C_{str})}}{C_{sw}}, \quad (36)$$

must be at least $V_{C_r}$, leading to the second boundary for the magnetizing current:

$$i_m(ZVS) \geq V_{C_r}\frac{C_{sw}}{\sqrt{L_r(C_{pri} + C_{str})}}. \quad (37)$$

Introducing the expression of $V_{C_r}$ in (18) into (37), the second specification for the magnetizing current becomes:

$$i_m(ZVS) \geq \frac{P\pi^2 f_{sw} C_{sw}}{V_{DD,1} k^2}\sqrt{\frac{L_r}{(C_{pri} + C_{str})}}. \quad (38)$$

If $i_m(ZVS)$ is large enough, so it is the peak of the resonant current $i_1$ in state 4, and $v_{DS,1}$ can reach $V_{DD,1}$ and turn-on ZVS is accomplished. Otherwise, $v_{DS,1}, v_{DS,4}$ oscillate with a mean value of $V_{DD,1} - V_{C_r}/2$ while $v_{DS,2}, v_{DS,3}$ do so with a mean value of $V_{C_r}/2$ until the dead time is over. Then, the primary devices are hard switched for the remaining voltage, as shown in Fig. 4 (c). As a consequence, the turn on is iZVS.

It is worth mentioning that if $i_m(ZVS)$ is below the first or conventional requirement, neither the primary nor the secondary converter achieve soft-switching [see the iZVS example of Fig. 4 (b)]. In case that $i_m(ZVS)$ fulfills the first requirement, but not the second one, the secondary converter completes the soft-switching in state 3. However, the primary cannot accomplish it in state 4 [see the iZVS example of Fig. 4 (c)]. Finally, when $i_m(ZVS)$ is larger than both requirements, turn-on ZVS is accomplished in the primary converter, as shown in Fig. 4 (d).

*4) Required dead time:* The dead time defined in the primary converter must be so the full voltage soft-transition can be achieved. Therefore, it must fulfill that:

$$t_{dead} \geq t_{vr} + t_{d,off} - t_{d,on}, \quad (39)$$

regarding the effect of the turn-off delay $t_{d,off}$ and turn-on delay $t_{d,on}$ of the transistors. Then, $t_{vr}$ can be calculated through the following expression:

$$t_{vr} = 8C_{sw}L_m f_{sw}, \quad (40)$$

which is easy to use in the design process. The turn-off and turn-on delay times can be obtained, respectively, by state-of-the-art expressions as [46]:

$$t_{d,off} = R_G(C_{GD} + C_{GS})ln\left(\frac{V_{G,on} - V_{G,off}}{V_{G,th} - V_{G,off}}\right),$$
$$t_{d,on} = R_G(C_{GD} + C_{GS})ln\left(\frac{V_{G,on} - V_{G,off}}{V_{G,on} - V_{G,th}}\right), \quad (41)$$

where $R_G$ is the gate resistance, $C_{GD}$ and $C_{GS}$ are the Miller and the gate-to-source parasitic capacitances of the primary switches, respectively, $V_{G,on}$ and $V_{G,off}$ are the gate turn-on and turn-off voltages, and $V_{G,th}$ is the threshold voltage of the primary devices.

### C. No-channel turn-off switching

While MOSFET lossless turn-on in the primary converter is achieved if $i_m$ fulfills (33) and (38), the complementary MOSFET turn-off may take place with losses, because part of $i_m$ may flow through its channel. This can be seen attending to the circuit for one switching cell in Fig. 7 (a), and considering a conventional, hard-switching turn-off, such as the one presented in Fig. 7 (b). The analysis is performed assuming that $S_i$ turns off, and $S_j$ turns on afterwards.

During $t_{vr}$, when the voltage is switched between $S_i$ and $S_j$, the total drain current $i_{D,i}$ through the MOSFET which is turned off is divided. One part of this current, $i_{D0,i}$, flows through the channel of the MOSFET and causes power losses, since $v_{DS} > 0$. The other part charges the output capacitance, $C_{oss} = C_{GD} + C_{DS}$, which is noted as $C_{pri}$ in the primary devices. If the channel is put out before $S_i$ begins to block voltage, i.e., before $v_{DS,i} > 0$, it results in $i_{D0,i} \approx 0$. This can be seen as a no-channel turn-off of the transistor. Thus, the energy loss in the turn-off is $E_{off,i} \approx 0$ [46].

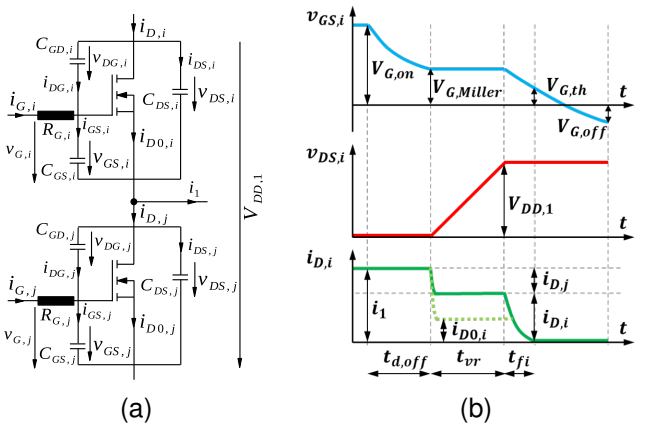



Fig. 7. (a) Single switching cell with MOSFET model. (b) Main waveforms during the conventional turn-off process of $S_i$.

As can be deduced from Fig. 7 (a):

$$i_1 = i_{D,i} - i_{D,j}, \tag{42}$$

where:

$$i_{D,i} = i_{D0,i} + i_{DS,i} + i_{DG,i}, \tag{43}$$

$$i_{D,j} = i_{DS,j} + i_{DG,j}. \tag{44}$$

In addition, the drain-to-source voltages of $S_i$ and $S_j$ fulfill that:

$$v_{DS,i} + v_{DS,j} = V_{DD,1} \Rightarrow \frac{dv_{DS,i}}{dt} + \frac{dv_{DS,j}}{dt} = 0., \tag{45}$$

and, during $t_{vr}$:

$$\frac{dv_{DS}}{dt} = \frac{dv_{DG}}{dt} + \frac{dv_{GS}}{dt} \approx \frac{dv_{DG}}{dt} \Rightarrow \frac{i_{DS}}{C_{DS}} \approx \frac{i_{DG}}{C_{GD}}. \tag{46}$$

The gate current can then be expressed as follows:

$$i_{G,i} = -i_{DG,i} + i_{GS,i} \approx -i_{DG,i}. \tag{47}$$

The goal is to achieve null current through the channel thanks to reducing the gate-to-source voltage of the MOSFET so $v_{GS} < V_{G,th}$ before the voltage switching begins. The gate resistance can be defined as:

$$R_G = \frac{V_{G,off} - v_{GS,i}}{i_{G,i}}, \tag{48}$$

where it must be noted that $i_{G,i}$ is negative in the turn-off process. The gate resistance must fulfill an upper boundary, so the switching process is quick enough in order to achieve $v_{GS,i} < V_{G,th}$ and hence, a lossless turn-off.

Considering (42)–(44) with $i_{D0,i} = 0$, the primary current during the zero-loss switching is:

$$i_1 = i_{DS,i} + i_{DG,i} - i_{DS,j} - i_{DG,j}, \tag{49}$$

which, considering (45) and (46), becomes:

$$i_1 = 2i_{DS,i} + 2i_{DG,i} = 2i_{DG,i}\left(\frac{C_{DS}}{C_{GD}} + 1\right). \tag{50}$$

Then, regarding (47), the primary current can be expressed by means of the gate current:

$$i_1 = -2i_{G,i}\left(\frac{C_{DS}}{C_{GD}} + 1\right) = -2i_{G,i}\frac{C_{pri}}{C_{GD}}, \tag{51}$$

where $C_{GD}$ is the Miller parasitic capacitance of the primary switches. Since the parasitic capacitances of the switches are not constant during the switching process, all the capacitances considered in these calculations are their respective charge-equivalent values, calculated over a voltage transition of $V_{DD,1}$ [25].

As depicted in Fig. 6 and described in Section IV-B, $i_1$ is a fraction of $i_m$ during the switching event. The primary current can be expressed as a function of the magnetizing current by calculating the share of the current according to the parasitic capacitances involved, which are $C_{pri}, C_{str}$ and $C_{sec}$. The resulting expression for the primary current is obtained as:

$$i_1 = \frac{i_m(ZVS)C_{pri}}{C_{pri} + C_{str} + C_{sec}/n^2} = i_m(ZVS)\frac{C_{pri}}{C_{sw}}, \tag{52}$$

which is convenient since it allows to continue with the design variable $i_m(ZVS)$. If (51) and (52) are put in common, the gate current under ZLS is obtained as:

$$i_{G,i} = -i_m(ZVS)\frac{C_{GD}}{2C_{sw}}. \tag{53}$$

Finally, (48) is particularized to the conditions imposed by ZLS, which are $v_{GS,i} < V_{G,th}$ for the gate-to-source voltage and (53) for the gate current. As a result, the limit of the total gate resistance for the lossless turn-off is:

$$R_{G,lim} = \frac{(V_{G,th} - V_{G,off})2C_{sw}}{i_m(ZVS)C_{GD}}. \tag{54}$$

It must be noted that $R_G = R_{G,int} + R_{G,ext}$, where $R_{G,int}$ is the internal gate resistance of each primary switch, and $R_{G,ext}$ is its external gate resistance. $R_{G,ext}$ is the only component of the gate resistance that can be freely selected during the design of the converter. Therefore, the boundary for lossless turn-off can be obtained for $R_{G,ext}$ as:

$$R_{G,ext} < R_{G,ext,lim} = R_{G,lim} - R_{G,int} \Rightarrow$$
$$R_{G,ext} < \frac{(V_{G,th} - V_{G,off})2C_{sw}}{i_m(ZVS)C_{GD}} - R_{G,int}. \tag{55}$$

As can be deduced from the obtained boundary for $R_{G,ext}$, the larger the current during the switching process, the lower the gate resistance limit that allows to achieve lossless, no-channel turn-off. Under the proposed ZLS, only a share of the magnetizing current is in charge of the switching process in the primary devices. As a consequence, the requirement in (55) can be easily satisfied. In order to illustrate the differences between conventional and lossless turn-off, simulation results are depicted in Fig. 8 with (a) $R_{G,ext} > R_{G,ext,lim}$, and (b) $R_{G,ext} < R_{G,ext,lim}$. As can be seen, in the first case there is current $i_{D0,i}$ through the channel when $S_i$ turns off and is blocking an increasing voltage $v_{DS,i} \rightarrow V_{DD,1}$. Therefore, there are turn-off losses in $S_i$, as represented with hatched areas in Fig. 8 (a). On the other hand, when the obtained specification for $R_{G,ext}$ is fulfilled as in Fig. 8 (b), $i_{D0,i} = 0$, and $S_i$ turns off with no losses.

Summarizing, the operation of the $LLC$ resonant converter under the proposed DCM-ZLS is for a fixed switching frequency, and neither control nor sensors are needed. The

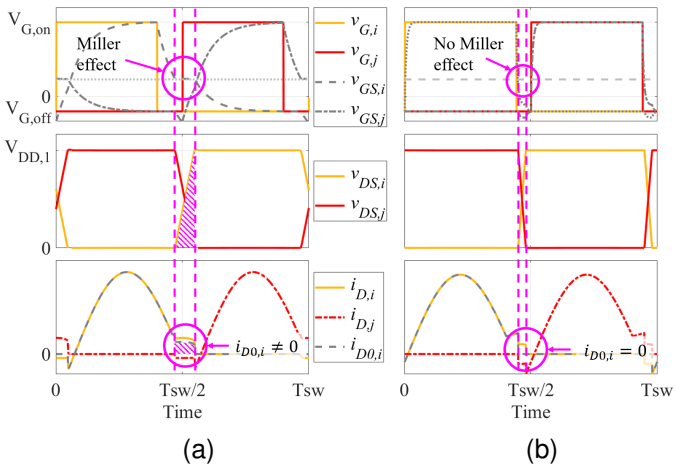



Fig. 8. Turn-off process of switch $S_i$. (a) Conventional turn-off, $R_{G,ext} > R_{G,ext,lim}$. (b) No-channel turn-off, $R_{G,ext} < R_{G,ext,lim}$.

voltage gain is fixed and independent of load, and lossless switching is accomplished by a proper design of a set of the converter parameters. Four requirements must be satisfied: two of them, (1) and (19), in order to ensure DCM; a lower boundary for the magnetizing current, which is the most demanding of (33) and (38), for lossless turn on; and an upper boundary for the external gate resistance of the primary switches, obtained in (55), to achieve lossless turn-off.

## V. Design Procedure of the Resonant Converter for DCM-ZLS

The design of the resonant converter comprises of the following design variables: switching-to-resonant frequency ratio $k$, magnetizing inductance $L_m$, dead time $t_{dead}$, series resonant inductance $L_r$, series resonant capacitor $C_r$, and external gate resistance $R_{G,ext}$, which are conditioned by the obtained requirements to operate under zero-loss switching. In this section, a step-by-step design procedure is presented and applied to an existing 18-kW test bench, which main characteristics are shown in Table I. The proposed design methodology can be easily followed with the help of the flow chart in Fig. 9 and the descriptions of the steps, even if the designer skips the principles of DCM-ZLS in the previous sections. The results of each step in the design procedure are presented in Table II.

TABLE I
Input Characteristics of the Test Bench

| Parameter | Value |
|---|---|
| Rated active power $P$ | 18 kW |
| Switching frequency $f_{sw}$ | 200 kHz |
| Max. input dc voltage $V_{DD,1_{max}}$ | 600 V |
| Transformer turns ratio | 0.8:1.0 |
| Primary switches | FF6MR12W2M1_B11 |
| Secondary switches | DDB2U20N12W1RF_B11 |
| Gate turn-on voltage $V_{G,on}$ | 15 V |
| Gate turn-off voltage $V_{G,off}$ | -3 V |
| Gate threshold voltage $V_{G,th}$ | 3.45 V |
| Internal gate resistance $R_{G,int}$ | 0.5 Ω |

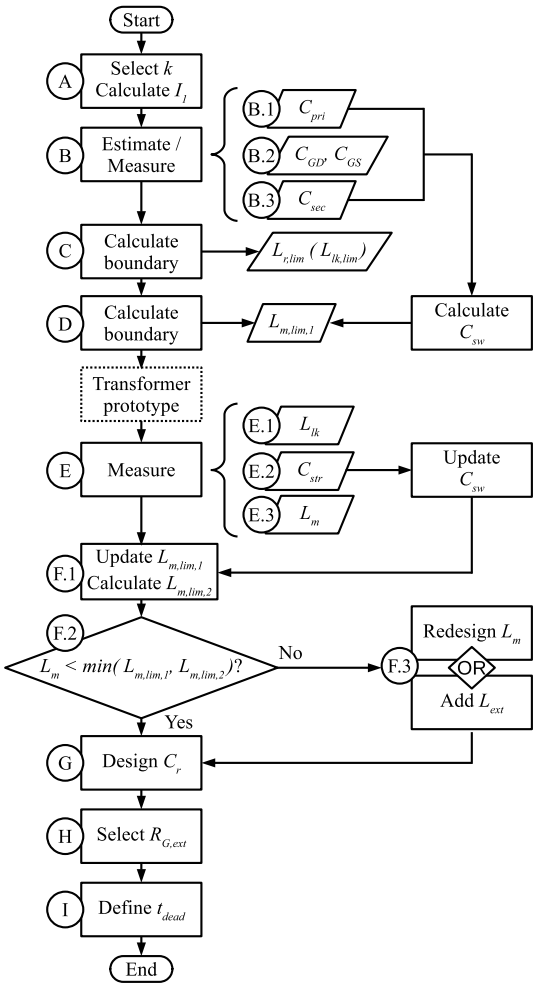



Fig. 9. Flow chart of the proposed design procedure for DCM-ZLS.

### A. Selection of $k$ and estimation of rated $I_1$

The parameter $k$, defined in (2), is paramount in the ZLS resonant converter, for it links conduction and switching of the semiconductors. The rms value of the current intensity in the switches and HF tank depends on $k$, as expressed in (3). It can be deduced that the closer $k$ to unity, the lower $I_1$ for a given delivered power, and thus lower conduction losses. However, if $k \to 1$, the discontinuity time $t_{DCM}$ is reduced and this can lead to an excessive magnetizing current requirement to achieve turn-on ZVS, as shown in (33). As a result, the selection of $k$ is under the criterion of the designer. In this application example, $k$ = 0.75 is defined. Hence, in the design of the HF transformer $I_1$ = 38 Arms can be considered for rated power $P$ = 18 kW.

### B. Characterization of the parasitic capacitances of the semiconductors

The parasitic capacitances that must be characterized in the design stage of the converter under ZLS are $C_{str}$, $C_{pri}$ and $C_{sec}$. The first one is the stray capacitance of the transformer and thus, it is not known beforehand. In a first stage of the design, $C_{sw} \approx C_{pri} + C_{sec}/n^2$ can be assumed.

*1) Characterization of $C_{pri}$:* It is deduced from the measurements on the primary converter with an inductive load. In this test, large enough dead time is set to allow complete charge/discharge of $C_{pri}$, as in ZLS. In this switching process, the primary ac current $i_1$ and the primary ac voltage $v_1$ are related by means of the capacitor equation. In one switching cell of the primary, the capacitance of one MOSFET is charged and the complementary is discharged simultaneously. Thus, integration of $i_1$ during the voltage switching, as depicted in the hatched area of Fig. 10, leads to obtain twice $Q_{pri}$. Then, $C_{pri}$ is calculated as:

$$i_1 = 2i_{Coss} = -\frac{dv_1}{dt}C_{pri} \Rightarrow$$
$$C_{pri} = \frac{\int_t^{t+t_{vr}} i_1\, dt}{v_1(t) - v_1(t+t_{vr})} = \frac{2Q_{pri}}{2V_{DD,1}}. \quad (56)$$

Alternatively, it can be measured at small signal with an impedance analyzer, or obtain it from the manufacturer.

*2) Characterization of $C_{GD}$ and $C_{GS}$:* The Miller capacitance of the primary switches is needed to calculate the limit of $R_{G,ext}$. It is also necessary, together with $C_{GS}$, to estimate $t_{d,off}$ and $t_{d,on}$. Both parasitic capacitances can be obtained through measurements with an impedance analyzer, or from the datasheet. In this paper, $C_{GD}$ and $C_{GS}$ are obtained from the manufacturer.

*3) Characterization of $C_{sec}$:* The parasitic capacitance of the diodes can be obtained from the datasheet, or measured straightforward by means of an impedance analyzer with a dc voltage bias, as it is conducted in this application.

The primary converter of the test bench comprises of two FF6MR12W2M1_B11 SiC MOSFET modules, one per switching cell of the full bridge. It has been reutilized from a higher rated power application. As a result, the primary switches are overdimensioned for the current 18-kW application, which enables to study the ZLS in a system with large output parasitic capacitances. The secondary converter comprises of two SiC diodes modules DDB2U20N12W1RF_B11 in parallel. The values of $C_{pri}$, $C_{GD}$, $C_{GS}$ and $C_{sec}$ can be seen in Table II.

It must be noted that $C_{pri}$ and $C_{sec}$ are charge-equivalent output parasitic capacitances and thus, voltage-dependent parameters. As a result, if $V_{DD,1}$ varies during the operation of the converter, the worst-case scenario must be considered regarding $C_{sw}$ for the design boundaries that are obtained in the following steps. For the magnetizing inductance and the time $t_{vr}$, which is used to set the dead time, it is the minimum $V_{DD,1}$, which means the maximum value of $C_{sw}$. For the external gate resistance, it is the maximum $V_{DD,1}$. Nevertheless, it is obtained that for $V_{DD,1} \geq 400V$, the charge-equivalent capacitances $C_{pri}$ and $C_{sec}$ of the devices used in the test bench can be assumed constant.

### C. Design boundary of the series resonant inductance

The requirement to ensure DCM is initially defined as $V_{C_r} < 2V_{DD,1}$ in (11). Then, this is transformed into a limit for the active power $P$, as expressed in (19). Nevertheless, the rated power of the converter is typically an input in the design process, so $P$ is fixed while the series resonant inductance is a design variable. Therefore, the requirement to ensure DCM becomes a boundary of $L_r$. Additionally to the DCM condition, $V_{C_r} < V_{DD,1}$ is desirable, so the slope of the magnetizing current is positive in (28), as mentioned in Section V-D. As can be seen, the upper limit of $V_{C_r}$ in this requirement is $V_{DD,1}$, while that for the DCM condition is $2V_{DD,1}$. As a consequence, the condition $V_{C_r} < V_{DD,1}$ implies a twice more restrictive limit for the resonant inductance $L_r$, which is derived by a simple rearrangement of (19) and dividing by two. The design limit of $L_r$ becomes:

$$L_r < L_{r,lim} = \frac{k^2 V_{DD,1}^2}{\pi^2 f_{sw} P}. \quad (57)$$

It must be noted that this is an upper boundary. As a consequence, it is possible to use the leakage inductance of the transformer as resonant inductor and thus, avoiding an external resonant inductor. From this point, it is assumed that the series inductance is $L_r = L_{lk}$. The value of $L_{lk,lim}$ in this example is presented in Table II. Since manufacturers can usually report a tolerance on $L_{lk}$ up to $\pm 20\%$, it is recommended to design the transformer with the minimum achievable leakage inductance or, at least, with a safety margin with respect to the theoretical $L_{lk,lim}$ that considers the aforementioned manufacturing tolerance.

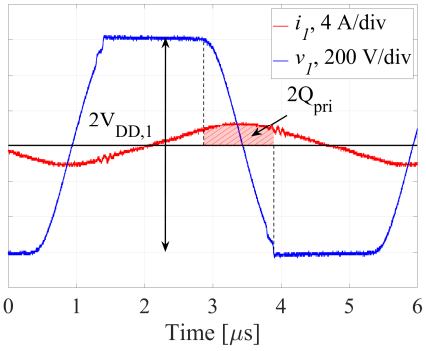



Fig. 10. Oscilloscope measurements to estimate $C_{pri}$.

### D. Design boundary of the magnetizing inductance

Two requirements have been obtained for the magnetizing current. Introducing the expression for $i_m(ZVS)$ in (29) into (33) and (38), respectively, the following upper boundaries for $L_m$ to achieve turn-on ZVS are obtained:

$$L_m \leq L_{m,lim,1} = \frac{(1-k)k}{16 C_{sw} f_{sw}^2}, \quad (58)$$

$$L_m \leq L_{m,lim,2} = \frac{V_{DD,1}^2 k^3}{4P\pi^2 C_{sw} f_{sw}^2} \sqrt{\frac{C_{pri} + C_{str}}{L_{lk}}}. \quad (59)$$

For the first design of the HF transformer, the manufacturer can consider only the specification in (58). The effect of $C_{str}$ can be neglected initially, thus assuming $C_{sw} \approx C_{pri} + C_{sec}/n^2$. The initial requirement $L_{m,lim,1}$ for this application is presented in Table II.

As can be deduced from the obtained boundaries (57), (58) and (59), the design of the transformer should aim to minimize $L_{lk}$ and $C_{str}$.

### E. Characterization of the HF transformer

It is key to characterize the transformer experimentally by means of the short- and open-circuit tests, since its parameters play a paramount role in the achievement of DCM-ZLS, especially $L_{lk}$ and $L_m$. Both inductances can be subjected of manufacturing tolerances that affect the design. Thus, it is essential to check their actual values and proceed according to the following steps.

*1) Measurement of $L_{lk}$:* The leakage inductance is measured by means of the short-circuit test, resulting in 1.3 $\mu$H.

*2) Characterization of $C_{str}$:* The stray capacitance can be obtained from the open-circuit test on the transformer, following the procedure described in [47]. Once $C_{str}$ is known, the equivalent parasitic capacitance of the system can be computed as $C_{sw} = C_{pri} + C_{sec}/n^2 + C_{str} = 3.53$ nF.

*3) Measurement of $L_m$:* The magnetizing inductance of the transformer is measured by means of the open-circuit test. The measured value is $L_m = 282\ \mu$H.

### F. Verify the adequate design of the magnetizing inductance

Once $C_{str}$, $L_m$ and $L_{lk}$ are known, the next steps are to be followed:

*1) Update the specifications for $L_m$:* The updated upper boundaries are $L_{m,lim,1}$ = 83 $\mu$H and $L_{m,lim,2}$ = 59 $\mu$H. In this design, the second requirement is the most demanding one.

*2) Check $L_m$:* The test bench that is used to illustrate the design procedure already implements a HF transformer, which has not been designed attending to the obtained specifications. As a consequence, $L_m$ is too large. In this case, the designer can choose whether to redesign the magnetizing inductance of the transformer to meet the most restrictive specification, or to add an external inductance. If the latter is selected, apply the following step.

*3) Implement $L_{ext}$ (only if necessary):* The external inductor must satisfy that the equivalent parallel inductance is $L_{p,eq} = L_m \mathbin{/\!/} L_{ext} < min(L_{m,lim,1}, L_{m,lim,2})$. The selected $L_{ext}$ and the resulting $L_{p,eq}$ are included in Table II.

### G. Design of the series resonant capacitor

The resonant capacitance $C_r$ can be calculated through (17), substituting $L_r$ by $L_{lk}$, since no external resonant inductor is implemented. The design value of $C_r$ is shown in Table II.

The resonant capacitor can also be affected by manufacturing tolerances, although normally narrower than those of the transformer inductances. Typical values are $\pm$2.5%, $\pm$5%, $\pm$10%. In addition, the capacitance can be affected by temperature. For instance, in the implemented reference, the temperature coefficient is -200 ppm/ºC. The designer can consider the worst-case scenario, in order to guarantee the robustness of the design.

### H. Selection of the external gate resistance

The design boundary obtained in (55) can be reformulated to express it only by means of parameters and design variables as:

$$R_{G,ext} < R_{G,ext,lim} = \\ = \frac{(V_{G,th} - V_{G,off})8C_{sw}L_m f_{sw}}{C_{GD}V_{DD,1}k} - R_{G,int}, \quad (60)$$

where $L_m$ must be replaced by $L_{p,eq}$ if an external parallel inductor is implemented.

As shown in Table I, the turn-off voltage applied to the gate is $V_{G,off}$ = -3 V. For the gate threshold voltage $V_{G,th}$, the worst case scenario is considered, that is the minimum value provided by the datasheet of the MOSFET. The value of $R_{G,int}$ can also been obtained from the datasheet. Finally, $R_{G,ext,lim}$ is obtained, as depicted in Table II. As can be seen, this requirement can be easily satisfied. The external gate resistance already implemented in the test bench is the default value considered by the manufacturer, which is 1.8 $\Omega$. It is not necessary to modify $R_{G,ext}$, since it satisfies the boundary.

### I. Selection of the dead time

The designer can define the dead time by calculating first $t_{vr}$ by means of (40), and $t_{d,off}$ and $t_{d,on}$ through (41). Then, apply (39). Note that $L_m$ must be replaced by $L_{p,eq}$ in the estimation of $t_{vr}$ if an external parallel inductor is implemented.

As can be seen, the designer can set a fixed $t_{dead}$ that satisfies (39) for any operating condition of the converter, since none of the times involved depend on $P$ and $V_{DD,1}$. The estimated values of $t_{vr}$, $t_{d,off}$, and $t_{d,on}$ together with the corresponding dead time set in the test bench, are included in Table II.

TABLE II
RESULTS OF THE DESIGN PROCESS

| Step | Name | Type | Value |
|---|---|---|---|
| A | $k$ | Selected by designer | 0.75 |
| A | $I_1$ | Calculated | 38 Arms |
| B | $C_{pri}$ | Measured/Datasheet | 1.86 nF |
| B | $C_{GD}$ | Measured/Datasheet | 0.18 nF |
| B | $C_{GS}$ | Measured/Datasheet | 15 nF |
| B | $C_{sec}$ | Measured/Datasheet | 0.96 nF |
| C | $L_{lk,lim}$ | Design upper boundary | 5.7 $\mu$H |
| D | $L_{m,lim,1}$ | Design upper boundary | 87 $\mu$H |
| E | $L_{lk}$ | Measured | 1.3 $\mu$H |
| E | $C_{str}$ | Measured | 0.17 nF |
| E | $L_m$ | Measured | 282 $\mu$H |
| F | $L_{m,lim,1}$ | Design upper boundary, updated | 83 $\mu$H |
| F | $L_{m,lim,2}$ | Design upper boundary, updated | 59 $\mu$H |
| F | $L_{ext}$ | Selected by designer | 55 $\mu$H |
| F | $L_{p,eq}$ | Calculated | 46 $\mu$H |
| G | $C_r$ | Calculated | 270 nF |
| H | $R_{G,ext,lim}$ | Design upper boundary | 20.0 $\Omega$ |
| H | $R_{G,ext}$ | Selected by designer | 1.8 $\Omega$ |
| I | $t_{vr}$ | Calculated | 260 ns |
| I | $t_{d,off}$ | Calculated | 36 ns |
| I | $t_{d,on}$ | Calculated | 16 ns |
| I | $t_{dead}$ | Selected by designer | 288 ns |

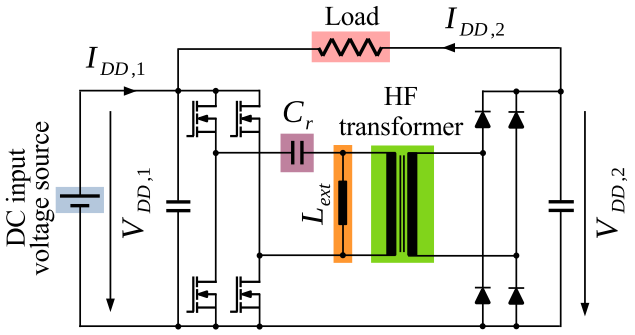



Fig. 11. Eschematic of the experimental setup.

## VI. Setup and Experimental Results

In order to validate the described operation of the resonant converter under DCM-ZLS, a set of experiments are conducted on a test bench. The input dc voltage, $V_{DD,1}$, is established by a dc power supply. The load is a bank of resistances. In order to operate the test bench in a power range of kW without dissipating all the output power in the resistances, a back-to-back setup is selected [48], as depicted in Fig. 11. Due to this arrangement, the power source only needs to provide the power dissipated by the converter and by the external load, which is a fraction of the power through the converter.

First, the deduced limits for the magnetizing inductance are verified, and the iZVS is compared to the ZLS based on the experimental results. The test bench is operated under DCM, and with $V_{DD,1} = 400$ V and $f_{sw} = 200$ kHz. Three different values of magnetizing inductance are used. The switching event for each scenario is presented in Fig. 12. In (a), the magnetizing inductance is that of the HF transformer, that is $L_m = 282\mu H$. No external inductance is added in parallel. This inductance is greater than $L_{m,lim,1}$. Therefore, the magnetizing current is too low, so the voltage cannot be switched completely during the discontinuous time and iZVS takes place in the semiconductor. As a result, there is a great $dv_{DS}/dt$ and an undesired resonance, with a voltage overshoot of 32% across the switch.

Then, in (b), an external inductance $L_{ext} = 110\mu H$ is connected in parallel to the transformer. The resulting parallel inductance is $L_{p,eq} = 79\mu H$, which is so $L_{m,lim,2} < L_{p,eq} < L_{m,lim,1}$. As can be observed, $v_{DS}$ is switched almost completely during $t_{vr}$, but the secondary ends its switching process first and there is not enough energy stored in $L_{lk}$ to finish the switching of the primary devices. Consequently, there is iZVS, although less critical than in the first scenario, since $L_{p,ext} < L_{m,lim,1}$ and is close to $L_{m,lim,2}$. Finally, an external inductance $L_{ext} = 55\mu H$ is added in the test depicted in (c), resulting in $L_{p,eq} < min(L_{m,lim,1}, L_{m,lim,2})$. The most demanding requirement for $L_m$ is satisfied and thus, ZVS is achieved.

From the conducted tests, it is demonstrated that the design of the HF transformer must satisfy the proposed boundaries $L_{m,lim,1}$ and $L_{m,lim,2}$ in order to ensure ZVS, so EMI and voltage overshoot in the semiconductors are avoided. It is worth mentioning that the measured $dv_{DS}/dt$ is 14.7 kV/$\mu$s in (a) and 2.5 kV/$\mu$s in (b), in both cases due to the forced

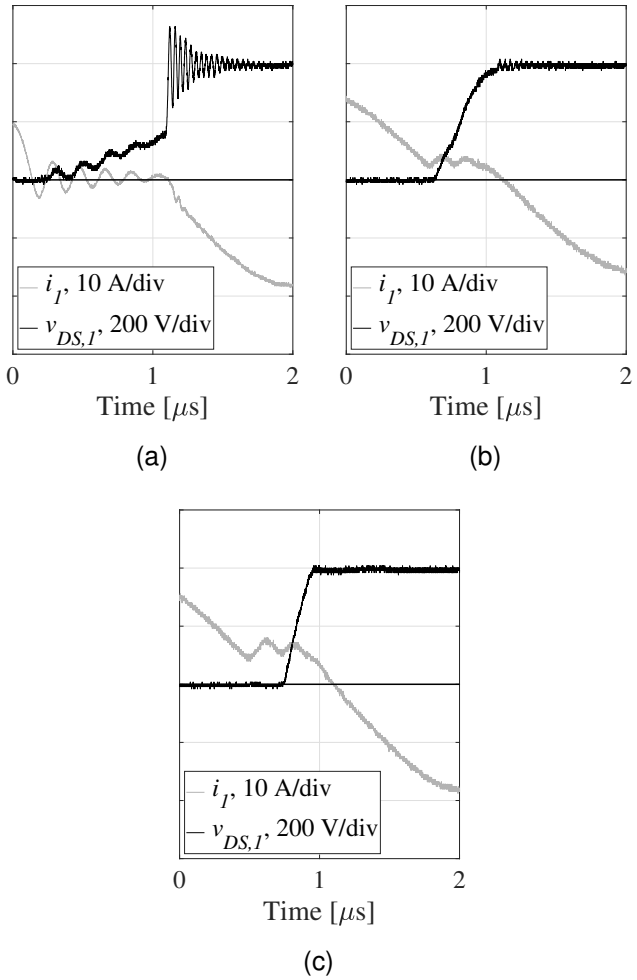
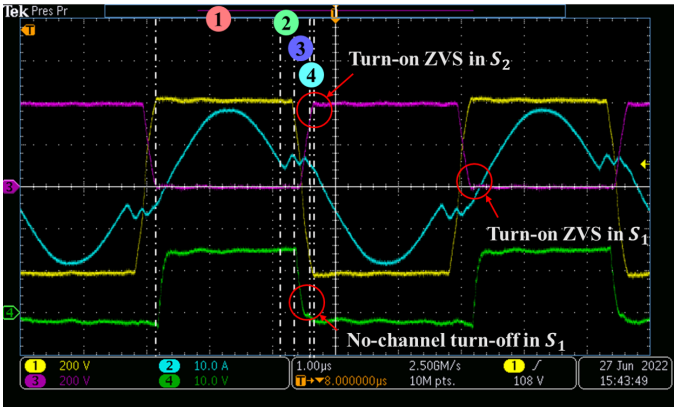



Fig. 12. Switching event in a SiC MOSFET of the test bench primary converter: (a) $L_{p,eq} = L_m > L_{m,lim,1}$. (b) $L_{m,lim,2} < L_{p,eq} < L_{m,lim,1}$. (c) $L_{p,eq} < L_{m,lim,2} < L_{m,lim,1}$.

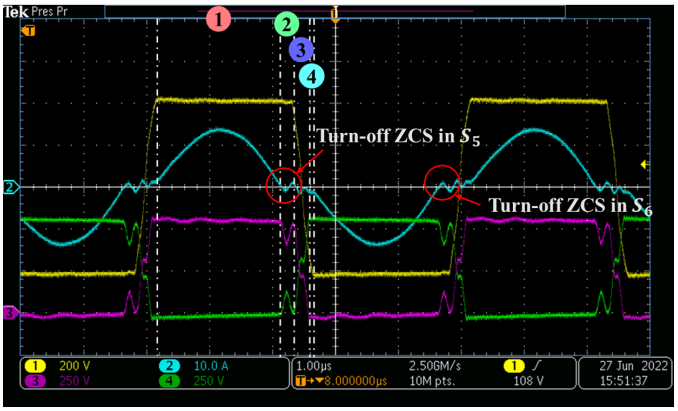
turn-on under iZVS, while in (c) the voltage is switched in a controlled manner with $dv_{DS}/dt = 1.8$ kV/$\mu$s.

Then, two more experimental tests are conducted on the test bench operating under DCM-ZLS. The characteristics of each one are summarized in Table III, including the dc input voltage, power, and external parallel inductor. The estimated $t_{vr}$ is also presented, together with the dead time set in the test bench, which is limited to steps of 32 ns. Additionally, for the sake of comparison with the estimated value, simulated and measured $t_{vr}$ are depicted. Test 1 is conducted at partial load and input voltage, while in Test 2 the converter is operated at rated $V_{DD,1}$ and rated power, 18 kW. The main waveforms in the primary and secondary sides for Test 1 are depicted in Fig. 13. The four conduction states theoretically analyzed in Section IV can be easily spotted. Additionally, the main waveforms in the primary and secondary sides of the test bench for Test 2 are shown in Fig. 14.

The correctness of the theoretical analysis conducted in this paper can be further verified by means of Fig. 15, which shows a zoom into the switching event of the test bench under DCM-ZLS in Test 2 (200 kHz, 600 V). In (a), the gate-to-source

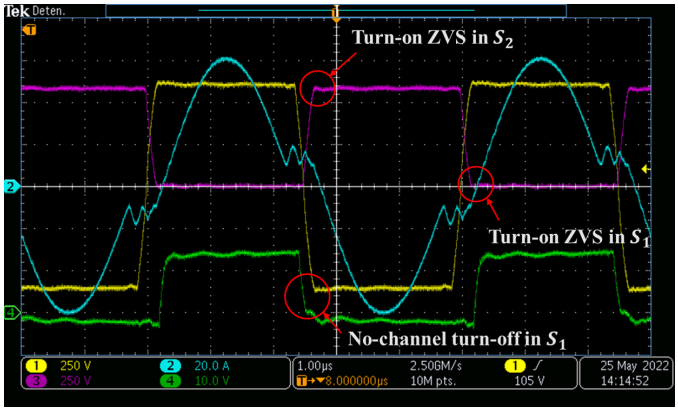



(a)

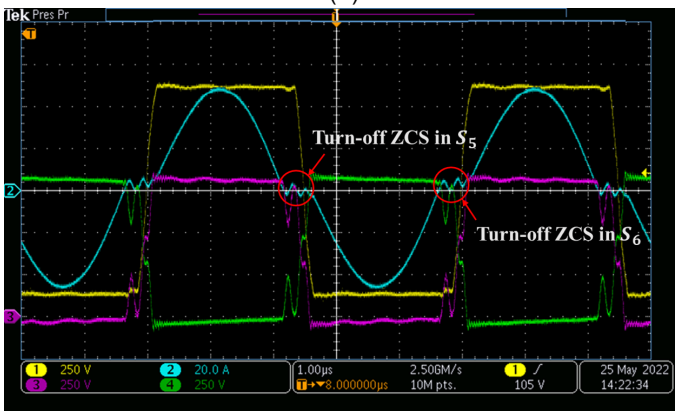



(b)

Fig. 13. Experimental results of Test 1: (a) Primary side. CH1: $v_1$. CH2: $i_1$. CH3: $v_{DS,1}$. CH4: $v_{GS,1}$. (b) Secondary side. CH1: $v_1$. CH2: $i_2$. CH3: $v_{KA,6}$. CH4: $v_{KA,5}$.




(a)




(b)

Fig. 14. Experimental results of Test 2: (a) Primary side. CH1: $v_1$. CH2: $i_1$. CH3: $v_{DS,1}$. CH4: $v_{GS,1}$. (b) Secondary side. CH1: $v_1$. CH2: $i_2$. CH3: $v_{KA,6}$. CH4: $v_{KA,5}$.

voltages of $S_1$ and $S_2$ are depicted, and in (b), the main voltage and current waveforms of the primary and secondary converters are represented.

The four conduction states can be easily identified. When $i'_2$ reaches zero, state 2 begins. All diodes of the secondary converter are turned off under ZCS. The average voltages of $S_5, S_8$, represented by $v'_{KA,5}$, become $V_{C_r}/2$, while the average voltages of $S_6, S_7$, represented by $v'_{KA,6}$, become $V_{DD,1} - V_{C_r}/2$, as obtained in (10). These average values are depicted in Fig. 15 (b) through dashed lines. As can be seen, the parasitic resonance between $L_{lk}$ and $C_{sec}/n^2$ is present during state 2 in $v'_{KA,5}$ and $v'_{KA,6}$, as discussed in Section IV. Then, $S_1$ is turned off [see $v_{GS,1}$ in Fig. 15 (a)], starting state 3. During this state, the parasitic resonance is between $L_{lk}$ and $(C_{pri} + C_{str})C_{sec}/n^2/(C_{pri} + C_{str} + C_{sec}/n^2)$.

Attending to $i'_2$, it becomes clear that its average value is not zero any more, for during state 3 the magnetizing current is shared by the primary and secondary devices to charge/discharge their parasitic capacitances. Then, when $v'_{KA,5}$ reaches $V_{DD,1}$ and $v'_{KA,6}$ reaches zero, the secondary ends its switching process, but before the primary converter does so, as predicted in the theoretical study of the $LLC$ converter under DCM-ZLS. Finally, the remaining energy in $L_{lk}$ is in charge of finishing the switching event in the primary during state 4, before the dead time is over.

As can be observed, the $LLC$ converter of the test bench is operating under DCM-ZLS in both experiments, regardless of the load condition, thanks to the proposed design procedure. In the primary, the switches are turned on under ZVS since their body diodes start to conduct before the transistors are turned on. Therefore, EMI are avoided in the switching, as can be seen in CH1 and CH3 of Fig. 13 (a) and Fig. 14 (a), and with more detail in the primary voltage $v_1$ in Fig. 15. The no-channel turn-off can be experimentally verified attending to the gate-to-source voltages $v_{GS,1}, v_{GS,2}$ in Fig. 15 (a), where no Miller effect takes place during the turn-off step, in accordance with the analytical model and the simulation results in Fig. 8. In the secondary, the resonant current becomes zero before the switching process begins, thus turning off the diodes under

TABLE III
CHARACTERISTICS OF THE EXPERIMENTAL TESTS

| Characteristic | Test 1 | Test 2 |
|---|---|---|
| $V_{DD,1}$ | 400 V | 600 V |
| $P$ | 3.8 kW | 18 kW |
| $L_{ext}$ | 55 $\mu$H | 55 $\mu$H |
| $t_{vr}$(analytical) | 260 ns | |
| $t_{dead}$ | 288 ns | |
| $t_{vr}$(simulation) | 267 ns | 293 ns |
| $t_{vr}$(experimental) | 224 ns | 247 ns |

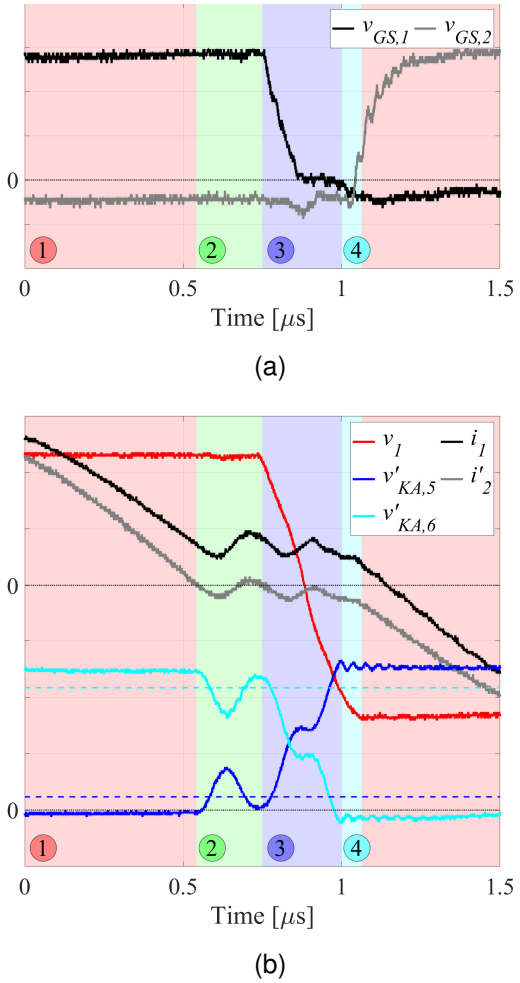



Fig. 15. Detail of the switching event in Test 2: (a) Gate voltages in the primary converter: $v_{GS,1}, v_{GS,2}$ (5 V/div). (b) Voltage waveforms $v_1, v'_{KA,5}, v'_{KA,6}$ (250 V/div), and current waveforms $i_1, i'_2$ (20 A/div).

ZCS.

Operating the $LLC$ converter under DCM-ZLS enables high-switching frequencies, as it is demonstrated in the conducted experiments, in which the test bench is switching at 200 kHz. The DCM-ZLS is ensured by design, and is independent of the delivered power, as shown with the partial-load and full-load tests. Moreover, the accurate estimation of $t_{vr}$, as shown in Table III, has allowed to set a proper dead time, which is not necessary to be adjusted during the operation of the converter.

## VII. Conclusion

The $LLC$ resonant converter is widely used in industrial applications where a fixed voltage gain is required, or where an additional power conversion stage is in charge of providing voltage regulation. The $LLC$ converter can be operated at fixed frequency under discontinuous conduction mode (DCM) to achieve soft-switching and fixed voltage gain for any load condition. This paper conducts first an in-depth analysis of DCM, which is conventionally used to achieve ZCS in both primary and secondary converters. However, as it is discussed in this article, ZCS is not free of losses and lead to undesired EMI. Taking advantage of DCM, zero-loss switching can be achieved. ZLS is the combination of turn-on ZVS and no-channel turn-off in the primary, together with ZCS in the secondary. A detailed analysis of the conduction states in the $LLC$ converter is presented, which enables to obtain the requirements for the magnetizing inductance and the gate resistance to accomplish lossless switching in the primary devices. Then, a step-by-step design procedure is proposed, which is applied to a 18-kW, 200-kHz test bench. Straightforward design expressions for the magnetizing inductance, the leakage inductance, the gate resistance and the dead time are provided. The resulting design according to the proposed methodology is tested in the test bench for two load conditions, including an experiment at rated voltage and power (600 V, 18 kW). The operation of the converter under DCM-ZLS is experimentally verified, showing soft-switching in both primary and secondary sides.

## References


[1] H. Dong, X. Xie, F. Mao, L. Zhang, and Y. He, "A novel primary-side regulation control scheme for ccm and dcm llc led driver based on "magnetizing current cancellation method"," *IEEE Transactions on Power Electronics*, vol. 35, no. 11, pp. 12 223–12 237, 2020.

[2] J. Ma, X. Wei, L. Hu, and J. Zhang, "Led driver based on boost circuit and llc converter," *IEEE Access*, vol. 6, pp. 49 588–49 600, 2018.

[3] D. Yu, X. Xie, and H. Dong, "A novel quasi-single-stage boost-llc ac/dc converter with integrated boost cells for achieving low bus voltage for led driver," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 4, pp. 4413–4424, 2022.

[4] Z. U. Zahid, Z. M. Dalala, R. Chen, B. Chen, and J.-S. Lai, "Design of bidirectional dc–dc resonant converter for vehicle-to-grid (v2g) applications," *IEEE Transactions on Transportation Electrification*, vol. 1, no. 3, pp. 232–244, 2015.

[5] C. Shi, H. Wang, S. Dusmez, and A. Khaligh, "A sic-based high-efficiency isolated onboard pev charger with ultrawide dc-link voltage range," *IEEE Transactions on Industry Applications*, vol. 53, no. 1, pp. 501–511, 2017.

[6] S. Zong, G. Fan, and X. Yang, "Double voltage rectification modulation for bidirectional dc/dc resonant converters for wide voltage range operation," *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 6510–6521, 2019.

[7] S. Srdic and S. Lukic, "Toward extreme fast charging: Challenges and opportunities in directly connecting to medium-voltage line," *IEEE Electrification Magazine*, vol. 7, no. 1, pp. 22–31, 2019.

[8] V. V. Reddy P., H. M. Suryawanshi, G. G. Talapur, and M. S. Ballal, "Optimized resonant converter by implementing shunt branch element as magnetizing inductance of transformer in electric vehicle chargers," *IEEE Transactions on Industry Applications*, vol. 55, no. 6, pp. 7471–7480, 2019.

[9] E. I. Pool-Mazun, J. J. Sandoval, P. N. Enjeti, and I. J. Pitel, "An integrated solid-state transformer with high-frequency isolation for ev fast-charging applications," *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, vol. 1, no. 1, pp. 46–56, 2020.

[10] C. Shen, H. Zhong, Y. Zhang, Y. Tang, and Y. Zhang, "Design method of 6-element boundary gain for llc resonant converter of electric vehicle," *IEEE Access*, vol. 8, pp. 183 090–183 100, 2020.

[11] C. Bai, B. Han, B.-H. Kwon, and M. Kim, "Highly efficient bidirectional series-resonant dc/dc converter over wide range of battery voltages," *IEEE Transactions on Power Electronics*, vol. 35, no. 4, pp. 3636–3650, 2020.

[12] R. Pandey and B. Singh, "A cuk converter and resonant llc converter based e-bike charger for wide output voltage variations," *IEEE Transactions on Industry Applications*, vol. 57, no. 3, pp. 2682–2691, 2021.

[13] J. Wu, S. Li, S.-C. Tan, and S. Y. R. Hui, "Fixed-frequency phase-shift modulated capacitor-clamped llc resonant converter for ev charging," *IEEE Transactions on Power Electronics*, vol. 37, no. 11, pp. 13 730–13 742, 2022.

[14] D. Cittanti, M. Gregorio, E. Vico, F. Mandrile, E. Armando, and R. Bojoi, "High-performance digital multiloop control of llc resonant converters for ev fast charging with lut-based feedforward and adaptive gain," *IEEE Transactions on Industry Applications*, vol. 58, no. 5, pp. 6266–6285, 2022.

[15] H. Hoffmann and B. Piepenbreier, "High voltage igbts and medium frequency transformer in dc-dc converters for railway applications," in *SPEEDAM 2010*, 2010, pp. 744–749.

[16] D. Dujic, C. Zhao, A. Mester, J. K. Steinke, M. Weiss, S. Lewdeni-Schmid, T. Chaudhuri, and P. Stefanutti, "Power electronic traction transformer-low voltage prototype," *IEEE Transactions on Power Electronics*, vol. 28, no. 12, pp. 5522–5534, 2013.

[17] C. Zhao, D. Dujic, A. Mester, J. K. Steinke, M. Weiss, S. Lewdeni-Schmid, T. Chaudhuri, and P. Stefanutti, "Power electronic traction transformer—medium voltage prototype," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 7, pp. 3257–3268, 2014.

[18] X. She, A. Q. Huang, and R. Burgos, "Review of solid-state transformer technologies and their application in power distribution systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 3, pp. 186–198, 2013.

[19] J. E. Huber and J. W. Kolar, "Applicability of solid-state transformers in today's and future distribution grids," *IEEE Transactions on Smart Grid*, vol. 10, no. 1, pp. 317–326, 2019.

[20] M. Rashidi, N. Altin, S. Ozdemir, A. Bani-Ahmed, M. Sabbah, F. Balali, and A. Nasiri, "Design and implementation of a llc resonant solid-state transformer," *IEEE Transactions on Industry Applications*, vol. 56, no. 4, pp. 3855–3864, 2020.

[21] T. Guillod, D. Rothmund, and J. W. Kolar, "Active magnetizing current splitting zvs modulation of a 7 kv/400 v dc transformer," *IEEE Transactions on Power Electronics*, vol. 35, no. 2, pp. 1293–1305, 2020.

[22] G. Ortiz, H. Uemura, D. Bortis, J. W. Kolar, and O. Apeldoorn, "Modeling of soft-switching losses of igbts in high-power high-efficiency dual-active-bridge dc/dc converters," *IEEE Transactions on Electron Devices*, vol. 60, no. 2, pp. 587–597, 2013.

[23] J. E. Huber, "Conceptualization and multi-objective analysis of multi-cell solid-state transformers," Ph.D. dissertation, ETH Zurich, Zurich, 2016.

[24] R. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Springer US, 2001.

[25] M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, "Zvs of power mosfets revisited," *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8063–8067, 2016.

[26] J. E. Huber, J. Miniböck, and J. W. Kolar, "Generic derivation of dynamic model for half-cycle dcm series resonant converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 4–7, 2018.

[27] J.-Y. Lee, Y.-S. Jeong, and B.-M. Han, "An isolated dc/dc converter using high-frequency unregulated *llc* resonant converter for fuel cell applications," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 7, pp. 2926–2934, 2011.

[28] R.-L. Lin and L.-H. Huang, "Efficiency improvement on llc resonant converter using integrated lclc resonant transformer," *IEEE Transactions on Industry Applications*, vol. 54, no. 2, pp. 1756–1764, 2018.

[29] C. Dincan, P. Kjaer, Y.-h. Chen, S. Munk-Nielsen, and C. L. Bak, "A high-power, medium-voltage, series-resonant converter for dc wind turbines," *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 7455–7465, 2018.

[30] G. Ning and W. Chen, "Asymmetric pulse frequency modulation with constant on-time for series resonant converter in high-voltage high-power applications," *IEEE Access*, vol. 7, pp. 176 971–176 981, 2019.

[31] F. Liu, G. Zhou, X. Ruan, S. Ji, Q. Zhao, and X. Zhang, "An input-series-output-parallel converter system exhibiting natural input-voltage sharing and output-current sharing," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 2, pp. 1166–1177, 2021.

[32] J. Huber, G. Ortiz, F. Krismer, N. Widmer, and J. W. Kolar, "$\eta$ - $\rho$ pareto optimization of bidirectional half-cycle discontinuous-conduction-mode series-resonant dc/dc converter with fixed voltage transfer ratio," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 1413–1420.

[33] W. Qin, N. Yu, Z. Zhou, X. Wu, and J. Zhang, "Active-clamp zvzcs resonant forward dc transformer (dcx) with load-adaptive on-time control," *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10 490–10 500, 2018.

[34] Y. Ren, M. Xu, J. Sun, and F. Lee, "A family of high power density unregulated bus converters," *IEEE Transactions on Power Electronics*, vol. 20, no. 5, pp. 1045–1054, 2005.

[35] J. E. Huber and J. W. Kolar, "Analysis and design of fixed voltage transfer ratio dc/dc converter cells for phase-modular solid-state transformers," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015, pp. 5021–5029.

[36] H. Xu, Z. Yin, Y. Zhao, and Y. Huang, "Accurate design of high-efficiency llc resonant converter with wide output voltage," *IEEE Access*, vol. 5, pp. 26 653–26 665, 2017.

[37] Z. Fang, J. Wang, R. Liu, L. Xiao, J. Zhang, G. Hu, and Q. Liu, "Energy feedback control of light-load voltage regulation for llc resonant converter," *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4807–4819, 2019.

[38] M. Li, Z. Ouyang, and M. A. E. Andersen, "High-frequency llc resonant converter with magnetic shunt integrated planar transformer," *IEEE Transactions on Power Electronics*, vol. 34, no. 3, pp. 2405–2415, 2019.

[39] G. Ortiz, M. G. Leibl, J. E. Huber, and J. W. Kolar, "Design and experimental testing of a resonant dc–dc converter for solid-state transformers," *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 7534–7542, 2017.

[40] L. Lindenmüller, R. Alvarez, P. Kleinichen, and S. Bernet, "Characterization of a 6.5 kv / 500a igbt module in a series resonant converter," in *2011 IEEE Energy Conversion Congress and Exposition*, 2011, pp. 4138–4143.

[41] H. Wen, J. Gong, X. Zhao, C.-S. Yeh, and J.-S. Lai, "Analysis of diode reverse recovery effect on zvs condition for gan-based llc resonant converter," *IEEE Transactions on Power Electronics*, vol. 34, no. 12, pp. 11 952–11 963, 2019.

[42] V. Vorperian and S. Cuk, "A complete dc analysis of the series resonant converter," in *1982 IEEE Power Electronics Specialists conference*, 1982, pp. 85–100.

[43] W. Ho and M. Pong, "Design and analysis of discontinuous mode series resonant converter," in *Proceedings of 1994 IEEE International Conference on Industrial Technology - ICIT '94*, 1994, pp. 486–489.

[44] C. Zucker, "Condenser problem," *American Journal of Physics*, vol. 23, no. 7, pp. 469–469, 1955.

[45] D. Elizondo, E. L. Barrios, and P. Sanchis, "Zero-loss switching in dc-dc series resonant converters under discontinuous conduction mode," in *2021 IEEE International Conference on Environment and Electrical Engineering and 2021 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I&CPS Europe)*, 2021, pp. 1–6.

[46] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. De Doncker, *Semiconductor Power Devices: Physics, Characteristics, Reliability*. Springer Berlin Heidelberg, 2011.

[47] H. Y. Lu, J. G. Zhu, and S. Hui, "Experimental determination of stray capacitances in high frequency transformers," *IEEE Transactions on Power Electronics*, vol. 18, no. 5, pp. 1105–1112, 2003.

[48] S. Lu, D. Kong, S. Xu, L. Luo, and S. Li, "A high-efficiency 80-kw split planar transformer for medium-voltage modular power conversion," *IEEE Transactions on Power Electronics*, vol. 37, no. 8, pp. 8762–8766, 2022.


**David Elizondo** (Student Member, IEEE) was born in Pamplona, Spain. He received the B.Sc. degree (Hons.) in electrical engineering and the M.Sc. degree (Hons.) in renewable energies and electrical engineering from the Public University of Navarre (UPNA), in 2017 and 2019, respectively, where he is currently pursuing the Ph. D. degree with a focus on the modeling, design and optimization of power converters for EV fast charging. He developed his master's thesis at Hochschule Osnabrück, Germany. In 2017, he joined the Electrical Engineering, Power Electronics and Renewable Energy Research Group, UPNA. For three months in 2022, he was an Academic Guest with the Power Electronics and Electrical Drives group, ISEA, Aachen. His research interests include EV fast-charging stations, resonant converters, and power inductors.

**Ernesto L. Barrios** (Member, IEEE) was born in Pamplona, Spain, in 1988. He received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from the Public University of Navarre, Pamplona, in 2009, 2012, and 2015, respectively. In 2011, he joined the Electrical Engineering, Power Electronics and Renewable Energy Research Group, Public University of Navarre, where he is currently an Associate Professor and a Researcher. For six months in 2016, he was an Academic Guest with the Power Electronic Systems Laboratory, ETH Zürich, Zürich, Switzerland. His research interests include high-frequency magnetics, power electronics, and renewable energies.

**Iñaki Larequi** was born in Pamplona, Spain. He received the M.Sc. degree in telecommunication engineering from the Public University of Navarre (UPNA) in 2001. For seven months, he developed his master´s thesis at the ENSERG (Grenoble, France), in collaboration with ST Microelectronics. He started his professional career as hardware design engineer in Agilent Technologies (Germany) and continued in CEMITEC Technological Centre (Spain). In 2017, he joined INGETEAM EV Chargers unit as lead hardware engineer for control and power electronics design. His main work has focused on EV fast-charging stations design, including high-power converters, analog sensing, digital control, and communications.

**Alfredo Ursúa** (Senior Member, IEEE) received B.Sc. (Hons.), M.Sc. (Hons.), and Ph.D. (Hons.) degrees in electrical engineering from the Public University of Navarre (UPNA), Pamplona, Spain, in 2001, 2004, and 2010, respectively. In 2002, he joined the Department of Electrical, Electronic and Communications Engineering where he is currently Associate Professor. He is also working with the Ingeper Research Group and with the Research Institute of Smart Cities of the UPNA. He is currently the Vice Dean of the Higher Technical School of Industrial and ICT Engineering and a member of the Steering Committee of the University Chair for Renewable Energies. He has been involved in more than 75 research projects both with public funding and in cooperation with industry and is the co-inventor of 7 patents. He has supervised 5 Ph.D. dissertations and coauthored more than 90 articles and contributions in international journals and conferences as well as 4 book chapters. His research interests include renewable energies, energy storage, hydrogen technologies, power electronics, and energy management. Dr. Ursúa was the recipient of the Extraordinary Doctoral Award in the fields of telecommunication technologies, bioengineering, and renewable energies, and the UPNA Research Award for the Best Technical Paper in 2013.

**Pablo Sanchis** (M'03-SM'12) received the M.Sc. degree in electrical engineering, the M.Sc. degree in management and business administration, and the Ph.D. degree in electrical engineering from the Public University of Navarre (UPNA), Pamplona, Spain, in 1994, 1995, and 2002, respectively. From 1996 to 1998, he was a Guest Researcher with the Delft University of Technology, The Netherlands. In 1998, he joined the Department of Electrical, Electronic and Communications Engineering, Public University of Navarre, where he is now a Full Professor. He is the Head of both the UPNA Chair for Renewable Energies and the Research Group in Electrical Engineering, Power Electronics, and Renewable Energies. He has been involved in more than 110 research projects both with public funding and in cooperation with industry and is the co-inventor of 14 patents. He has supervised 11 Ph.D. theses and coauthored around 160 articles and contributions in international journals and conferences as well as five book chapters (h-index of 38). His current research interests include renewable energies, power electronics, electric energy storage, electric mobility and hydrogen technologies. Dr. Sanchis received the UPNA Award for the Best Research Paper in 2013, the UPNA Award for Excellence in Teaching in 2017 and 2022, and the UPNA Award for Excellence in Research Career in 2022.