

Enhanced Single-Stage Folded Cascode OTA Suitable for Large Capacitive Loads

Antonio Lopez-Martin, *Senior Member, IEEE*, M. Pilar Garde, Jose M. Algueta, Carlos A. de la Cruz Blas, Ramon G. Carvajal, *Senior Member, IEEE*, and Jaime Ramirez-Angulo, *Fellow, IEEE*

Abstract— An enhanced single-stage folded cascode Operational Transconductance Amplifier (OTA) able to drive large capacitive loads is presented. Class AB operation is achieved by circuits that adaptively bias the input differential pair and the folding stage, which provide increased dynamic current boosting and gain-bandwidth product (GBW). Measurement results of a test chip prototype fabricated in a 0.5 μm CMOS process show an increase in slew rate and GBW by a factor of 30 and 15, respectively, versus the class A version using the same supply voltage and bias currents. Overhead in other performance metrics is small.

Index Terms— Amplifiers, Analog integrated circuits, CMOS integrated circuits, Class AB circuits.

I. INTRODUCTION

CLASS AB amplifiers are widely employed in applications requiring low power consumption since they can yield large dynamic currents not limited by the quiescent currents. Hence low static power consumption can be achieved without degrading dynamic performance. These amplifiers usually employ an adaptive bias circuit for the differential pair to get the required current boosting. Such adaptive circuits can provide very low quiescent currents in order to have very low static power dissipation. However, when a large differential input signal is applied, these adaptive bias circuits are able to provide large dynamic currents, with maximum swings larger than the quiescent current level.

Several proposals have been reported to provide class AB operation to classic amplifier topologies like telescopic and current mirror OTAs, e.g. [1]-[3]. However, achieving class AB operation in a folded cascode amplifier (Fig. 1(a)) is more complex. Adaptive biasing of the input pair is not effective by itself in this case since the bottom current sources at the folding stage limit the maximum output current. As these

current sources force the sum of currents through M_1 and M_{9c} to be $2I_{BIAS}$, and the same with the sum of currents through M_2 and M_{10c} , the maximum output current is $2I_{BIAS}$ regardless of the adaptive biasing circuit used for the input pair. Therefore, it is mandatory that these bias current sources also adapt to the input signal to achieve power efficiency. Thus, the conventional approach to enhance the performance of the folded-cascode amplifier is using multi-path schemes [4] or current recycling techniques [5-8], where these current sources are replaced by active current mirrors. However, these techniques have limited power efficiency since the active current mirrors employed lead to internal replication of large dynamic currents at the additional branches [3]. A simple modification of the conventional folded cascode OTA is proposed here which enhances the performance of the amplifier without this shortcoming.

II. PRINCIPLE OF OPERATION

Figure 1 shows the conventional (class A) folded cascode OTA (Fig. 1(a)) and the proposed Class AB OTA (Fig. 1(b)). The constant differential pair bias current source $2I_{BIAS}$ of Fig. 1(a) is replaced in Fig. 1(b) by an adaptive circuit to bias M_1 and M_2 . In addition, the current sources $2I_{BIAS}$ at the folding stage of Fig. 1(a) are replaced by another adaptive biasing circuit in Fig. 1(b), in order to avoid the limitation in output current described in the previous section. The adaptive bias techniques employed are described below.

A. Adaptive Biasing of the Input Pair

The adaptive biasing scheme chosen for the differential input pair is shown in Fig. 2(a) [3, 9]. It consists of two matched transistors M_1 and M_2 cross-coupled by two DC level shifters. In quiescent conditions $V_{SG1}^Q = V_{SG2}^Q = V_B$, so that transistors M_1 and M_2 have identical quiescent currents well controlled by the DC voltage V_B . If V_B is slightly larger than the MOS threshold voltage $|V_{TH}|$, very low static currents are generated. However, if for instance V_{IN+} decreases, the source voltage of M_1 drops by the same amount while the source voltage of M_2 remains constant. Hence, current in M_2 increases and current in M_1 decreases. These currents are not bounded by the quiescent current levels. Moreover, the full differential input signal is applied to each differential pair transistor whereas only half is applied in the conventional differential pair, thus doubling DC gain compared to Fig. 1(a).

Manuscript received November 1, 2016. This work has been supported by the Spanish Ministerio de Economía y Competitividad, grant TEC2013-47286-C3-2.

A. J. Lopez-Martin, M. P. Garde, J. M. Algueta and C. A. de la Cruz are with the Institute of Smart Cities, Public University of Navarra, 31006 Pamplona, Spain (e-mail: antonio.lopez@unavarra.es).

J. Ramirez-Angulo is with the Klipsch School of Electrical Engineering, New Mexico State University, Las Cruces, NM 88003-0001 USA (e-mail: jramirez@nmsu.edu).

R. G. Carvajal is with the Departamento de Ingeniería Electrónica, Escuela Superior de Ingenieros, Universidad de Sevilla. Avenida de los Descubrimientos, E-41092 Sevilla, Spain (e-mail: carvajal@gte.esi.us.es).

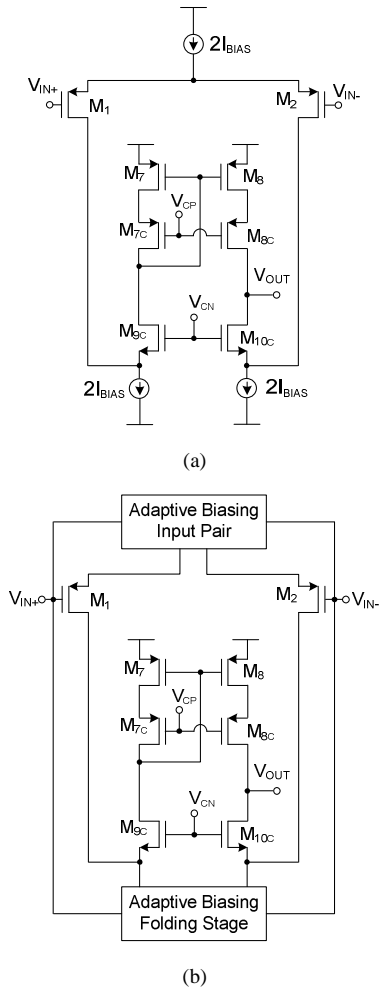


Fig. 1. (a) Class A folded cascode OTA (b) Class AB folded cascode OTA

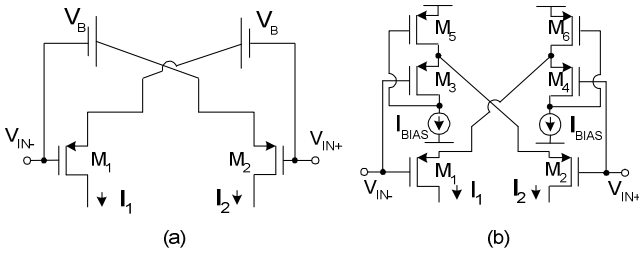


Fig. 2. Adaptive biasing of the differential input pair (a) Scheme (b) FVF implementation

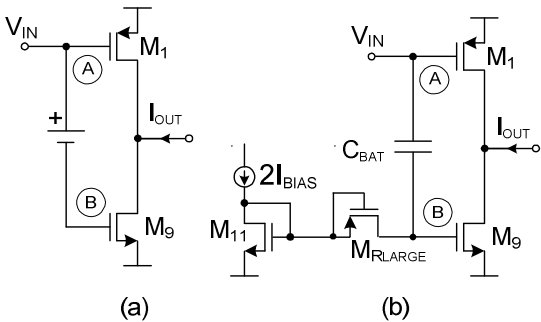


Fig. 3. Adaptive biasing of the folding stage (a) Scheme (b) QFG implementation

In order to implement the DC level shifters V_B in the scheme of Fig. 2(a), the Flipped Voltage Follower (FVF) [10] is employed, as shown in Fig. 2(b). Each FVF is made of two transistors (M_3, M_5 or M_4, M_6) and a current source I_{BIAS} . These FVFs feature low supply voltage requirements, simplicity, low output resistance, ability to source large currents and provide accurate quiescent current control. Quiescent current in M_1 and M_2 is the bias current I_{BIAS} of the FVFs assuming matched transistors M_1, M_2, M_3 and M_4 .

B. Adaptive Biasing of the Folding Stage

As mentioned before, the adaptive biasing of Fig. 2 would double DC gain (and GBW) of the folded cascode OTA but could not increase alone dynamic output currents, since currents in the output branches are limited by the current sources of the folding stage. To solve this issue these current sources are also adaptively biased in our proposal, by using Quasi-Floating Gate (QFG) transistors [11]. The idea is illustrated with the simple class AB output stage of Fig. 3(a).

Setting the DC level shift in Fig. 3(a) adequately, a well controlled quiescent current can be achieved, which can be low to reduce static power. When an input is applied, signal swing at node A is replicated at node B so that output currents are not limited by the quiescent current. Several proposals for the implementation of the DC level shift in Fig. 3(a) have been reported, such as using diode-connected transistors or resistors biased by DC currents. However, these solutions require extra quiescent power and may increase supply voltage requirements and reduce bandwidth. Besides, the resulting quiescent currents are often not accurately set and experience large process, voltage and temperature (PVT) variations.

Figure 3(b) shows an efficient implementation of this DC level shift avoiding these drawbacks, using a capacitor C_{BAT} and a large resistance pseudo-resistor M_{Rlarge} . In quiescent operation C_{BAT} has no effect and there is not current flowing through M_{Rlarge} , so the quiescent current in M_9 is accurately set to $2I_B$, regardless of process and thermal variations. Under dynamic conditions, voltage at node A is transferred to node B after attenuation by a factor $\alpha = C_{BAT}/(C_{BAT}+C_B)$ and a first-order RC high-pass filtering with a cutoff frequency $1/[2\pi R_{large}(C_{BAT}+C_B)]$, with R_{large} the large leakage resistance of the pseudo-resistor M_{Rlarge} and C_B the parasitic capacitance at node B. Since the value of R_{large} is extremely large, this cutoff frequency is typically < 1 Hz, so in practice only the DC component of voltage at node A is not transferred to node B. Note that this implementation of the floating battery does not require extra static power or supply voltage requirements. The extra silicon area is small as M_{Rlarge} is a minimum-size MOS transistor and C_{BAT} can be small (with the minimum value given by the lowest allowable α).

III. CIRCUIT IMPLEMENTATION

The class AB folded cascode OTA of Fig. 1(b) using the adaptive biasing schemes described is shown in Fig. 4. Note that the QFG transistors M_9 and M_{10} are not directly connected to the input signals. They re-use the FVFs to invert and scale

the input signals to fit the signal swing at the gates of M_9 - M_{10} and to avoid extra loading of the input terminals by the adaptive biasing of the folding stage.

In quiescent operation the circuit works like Fig. 1(a), with well controlled quiescent currents, since no current flows through the pseudo resistors M_{R1} and M_{R2} . For large positive $V_{ID}=V_{IN+}-V_{IN-}$, the gate voltage of M_5 decreases and that of M_6 increases. As described in Section II, since capacitors C_{BAT} cannot discharge rapidly due to the high resistive value of M_{R1} and M_{R2} , they act as floating batteries that decrease the gate voltage of M_{10} and increase that of M_9 . Hence a large output current is sourced to the load, yielding large positive Slew Rate SR_+ . Similarly, for negative V_{ID} the gate voltage of M_5 increases and that of M_6 decreases. As a consequence, the gate voltage of M_{10} increases and that of M_9 decreases, leading to a large output current sunk from the load that boosts SR_- .

A. Small-Signal Analysis

The adaptive biasing employed in Fig. 4 not only increases slew rate, it also significantly increases the transconductance G_m of the conventional OTA for the same bias current and transistor sizes. The transconductance of the conventional folded cascode OTA is

$$G_{mA}=g_{m1}=g_{m2} \quad (1)$$

while that of the OTA of Fig. 4 is

$$G_{mAB} = 2g_{m1} \left(1 + \alpha \frac{g_{m9}}{g_{m6}} \right) \quad (2)$$

with g_{mi} the transconductance gain of transistor M_i and $\alpha \approx C_{BAT}/(C_{BAT}+C_{gs9})$. Hence an increase of $2(1+\alpha g_{m9}/g_{m6})$ is achieved, where the factor 2 is due to the adaptive biasing circuit of the differential pair and the term $1+\alpha g_{m9}/g_{m6}$ corresponds to the adaptive current sources M_9 and M_{10} . This enhanced transconductance leads to the same increase in the GBW of the class AB OTA of Fig. 4 versus the conventional OTA of Fig. 1(a). The DC gain of the class AB OTA is also increased, but to a less extent since the output resistance R_{out} of the class AB OTA is also slightly decreased due to the nonzero output resistance of the FVFs.

Just like the conventional folded cascode OTA, the OTA of Fig. 4 features a dominant pole determined by the output resistance R_{out} and the load capacitance C_L , as well as a non-dominant pole corresponding to the source terminals of M_{9c} and M_{10c} . In addition, the circuit of Fig. 4 has an additional non-dominant pole introduced by the nodes corresponding to the gates of M_5 and M_6 . Since this pole is associated to PMOS devices, it may be at not very high frequencies. Moreover, reduction in the output resistance R_{out} also increases the frequency of the non-dominant pole. As a consequence, phase margin is reduced compared to the class A version. For this additional pole frequency to be at least 3 times the GBW, the required C_L is approximately

$$C_L > 6 \frac{g_{m1}}{g_{m5}} \left(1 + \alpha \frac{g_{m9}}{g_{m6}} \right) \cdot \left(C_{gs5} + C_b + \frac{C_{BAT} C_{gs10}}{C_{BAT} + C_{gs10}} \right) \quad (3)$$

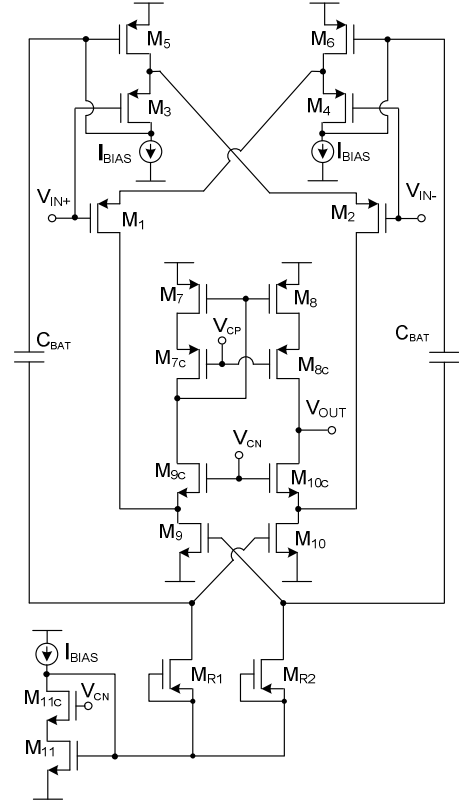


Fig. 4. Proposed class AB folded cascode OTA

where C_b is the bottom-plate to substrate capacitance of C_{BAT} . Hence, the circuit is amenable to drive relatively large load capacitances.

B. Slew Rate

The slew rate of the folded cascode OTA of Fig. 1(a) is

$$SR_{A+} = SR_{A-} = \frac{2I_B}{C_L} \quad (4)$$

since the maximum current sourced to the load of sunk from it is $2I_B$. Hence symmetrical positive and negative slew is provided but the maximum output current is limited by the bias current. The slew rate in the circuit of Fig. 4 is approximately

$$SR_{AB+} = SR_{AB-} = \frac{2I_B}{C_L} \left(1 + \alpha \sqrt{\frac{\beta_9}{\beta_6}} \right)^2 \quad (5)$$

with $\beta_i = \mu C_{ox}(W/L)_i$, evidencing the SR improvement achieved.

IV. MEASUREMENT RESULTS

Both the class A and class AB folded cascode OTA circuits of Fig. 1(a) and Fig. 4 were fabricated in a $0.5 \mu\text{m}$ CMOS test chip prototype. Figure 5 shows a microphotograph where the OTAs are enclosed by white rectangles. The transistor sizes employed are shown in Table I. Poly-poly capacitors C_{BAT} were used, with a value of 0.7 pF . Supply voltages were $\pm 1 \text{ V}$, and the bias current I_{BIAS} was $10 \mu\text{A}$. Cascode bias voltages

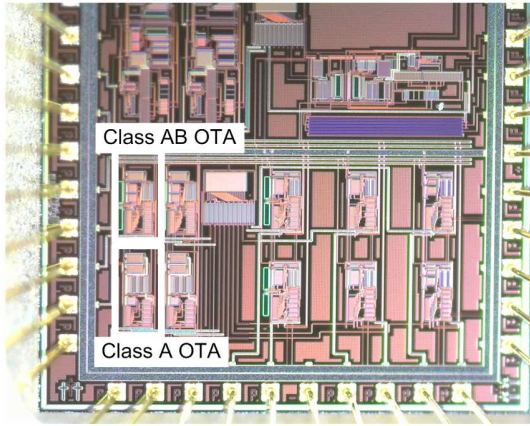


Fig. 5. Test chip microphotograph.

TABLE I - TRANSISTOR ASPECT RATIOS

Transistor	W/L ($\mu\text{m}/\mu\text{m}$)
M_1 - M_4	100/1
M_5 - M_6	9/0.6
M_7 - M_8	200/1
M_{7C} - M_{8C} , M_{9C} - M_{10C}	200/0.6
M_9 - M_{10}	120/0.6
M_{11}	60/0.6
M_{11C}	100/0.6
M_{R1} - M_{R2}	1.5/0.6

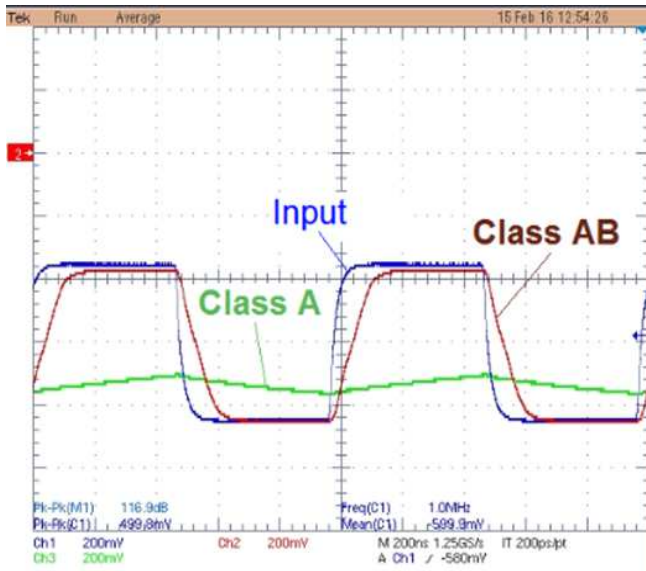


Fig. 6. Measured response of the class A and class AB folded cascode OTAs

V_{CP} and V_{CN} were set to -0.2 V and 0 V, respectively. An external load capacitor of 47 pF was used. Since the output was connected directly to a bonding pad and no external buffer was employed, the total load capacitance is increased by the pad, board and test probe capacitance. Its estimated value is of approximately 70 pF.

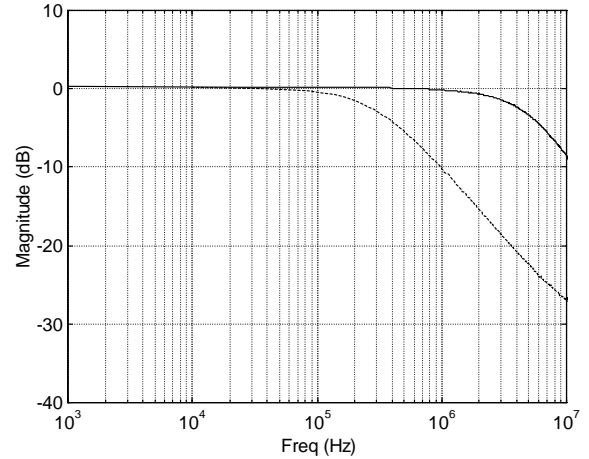


Fig. 7. Measured magnitude response of the class A OTA of Fig. 1(a) (dashed line) and the class AB OTA of Fig. 4 (solid line).

The transient response the OTAs was measured with the fabricated OTAs in unity gain configuration, and using a 1 MHz 0.5 V square wave at the input. Fig. 6 shows the measured output of both OTAs. Note the stable and faster settling of the proposed class AB OTA of Fig. 4. The SR_+ for the class A OTA is 0.32 V/ μs and for the proposed class AB OTA is 9.8 V/ μs , i.e., an increase factor of 30.6 is achieved for the same quiescent current and load capacitance. The expected increase factor from (5), with estimated $\alpha \approx 0.8$, was 36 .

The measured magnitude response of the OTAs as voltage followers is shown in Fig. 7. The cutoff frequency of the OTA of Fig. 4 is 4.75 MHz, and that of the OTA of Fig. 1(a) is 310 kHz. Due to the dominant pole design, these frequencies correspond approximately to the GBW of the OTAs. So an increase factor of 15.3 in GBW is observed experimentally. The expected value from (2) using $\alpha \approx 0.8$ was 12.2 .

A summary of the main measurement results for both OTAs is shown in Table II. Note that the settling time in the proposed OTA is <100 ns, while the conventional OTA is unable to settle for this input signal and load. Measured Total Harmonic Distortion (THD) is $<1\%$ for a 1 V_{pp} input sinusoid, whereas the conventional OTA shows a THD $>6\%$ due to settling limitations. The open-loop frequency response could not be measured directly due to the high gain. Simulation results for DC gain and phase margin are provided instead. Note that the increase in DC gain of the proposed OTA is 14.6 dB (i.e. a factor of 5.37), lower than the GBW increase due to the reduced output resistance. These results are in agreement with the theoretical analysis in Section III.A. The main drawback is the decrease in phase margin. The phase margin of the OTA of Fig. 1(a) drops to 79° at 4.75 MHz, so the OTA of Fig. 4 shows a degradation of 19° .

Concerning the noise level, it is even slightly lower in the proposed OTA due to the increased gain. However, static power increases a 50% by the bias current required for the FVFs, and silicon area is a 20% higher due to the capacitors C_{BAT} . If the width of M_3 and M_4 is made n times smaller than that of M_1 and M_2 , the required bias current for the FVF is also scaled by n , and the extra power would be just $50/n\%$.

Table II also includes a performance comparison with other proposed class AB amplifiers. To ease comparison, two conventional figures of merit (FOM) are included: $FOM_L = SR \cdot C_L / I_{supply} = I_{maxL} / I_{supply}$, where I_{supply} is the total current consumption, shows the large-signal current efficiency, and $FOM_S = 100 \cdot GBW \cdot C_L / I_{supply}$ (MHz·pF/μA) a small-signal speed/power ratio. Note that the proposed OTA compares favorably for both FOMs.

V. CONCLUSION

A class AB folded cascode OTA has been presented, based on two adaptive biasing circuits for the differential input pair and the folding stage. The use of FVFs and QFG transistors leads to a simple and compact implementation and does not require extra supply voltage. Measurement results show a significant increase in slew rate and fast settling, maintaining low noise and low static power consumption. The circuit can find application in low voltage low power switched capacitor circuits and in buffers requiring to drive large capacitive loads.

REFERENCES

- [1] K. de Langen and J.H. Huijsing, "Compact low-voltage power-efficient operational amplifier cells for VLSI," *IEEE J. Solid State Cir.*, vol. 33, no. 10, pp. 1482-1496, Oct. 1998.
- [2] M. R. Valero Bernal, S. Celma, N. Medrano and B. Calvo, "An ultralow-power low-voltage class-AB fully differential OpAmp for long-life autonomous portable equipment," *IEEE Trans. Cir. Syst. II*, vol. 59, no. 10, pp. 643-647, Oct. 2012.
- [3] A.J. Lopez-Martín, S. Baswa, J. Ramirez-Angulo and R. G. Carvajal, "Low-voltage Super Class AB CMOS OTA cells with very high slew rate and power efficiency," *IEEE J. Solid State Cir.*, vol. 40, no. 5, pp. 1068-1077, May 2005.
- [4] K. Nakamura and L.R. Carley, "An enhanced fully differential folded-cascode op amp," *IEEE J. Solid State Cir.*, vol. 27, no. 4, pp. 563-568, Apr. 1992.
- [5] R. Assaad and J. Silva-Martinez, "The recycling folded cascode: A general enhancement of the folded-cascode amplifier," *IEEE J. Solid State Cir.*, vol. 44, no. 9, pp. 2535-2542, Sep. 2009.
- [6] Y.-L. Li, K.-F. Han, X. Tan, N. Yan, and H. Min, "Transconductance enhancement method for operational transconductance amplifiers," *Electron. Lett.*, vol. 46, no. 19, pp.1330-1331, 2010.
- [7] Z. Yan, P.-I. Mak, and R. P. Martins, "Double recycling technique for folded-cascode OTA," *Analog Integr. Circ. Signal Proc.*, vol. 71, no. 1, pp. 137-141, 2012.
- [8] M. Yavari and T. Moosazadeh, "A single-stage operational amplifier with enhanced transconductance and slew rate for switched-capacitor circuits," *Analog Integr. Circ. Signal Proc.*, vol. 79, no. 3, pp. 589-598, Jun. 2014.
- [9] V. Peluso, P. Vancorenland, M. Steyaert, and W. Sansen, "900mV differential class AB OTA for switched opamp applications," *Electronics Letters*, vol. 33, no. 17, pp. 1455-1456, Aug. 1997.
- [10] R.G. Carvajal, J. Ramirez-Angulo, A. J. Lopez-Martin, A. Torralba, J.A. Galan, A. Carlosena, and F.M. Chavero, "The Flipped Voltage Follower: a useful cell for low-voltage low-power circuit design," *IEEE Trans. Cir. Syst. I*, vol. 52, no. 7, pp.1276-1291, Jul. 2005.
- [11] J. Ramirez-Angulo, A.J. Lopez-Martin, R.G. Carvajal, and F. Muñoz-Chavero, "Very low voltage analog signal processing based on Quasi Floating Gate transistors," *IEEE J. Solid State Cir.*, vol. 39, no. 3, pp. 434-442, Mar. 2003.
- [12] S. Chatterje, Y. Tsividis, and P. Kinget, "A 0.5-V bulk-input fully differential operational transconductance amplifier," in *Proc. ESSCIRC*, 2004, pp. 147-150.
- [13] L. Zuo and S. K. Islam, "Low-voltage bulk-driven operational amplifier with improved transconductance," *IEEE Trans. Cir. Syst. I*, vol. 60, no. 8, pp. 2084-2091, Aug. 2013.
- [14] P.R. Surkanti and P.M. Furth, "Converting a three-stage pseudoclass-AB amplifier to a true-class-AB amplifier," *IEEE Trans. Circuits Syst. II*, vol. 59, no. 4, pp. 229-233, Apr. 2012.
- [15] E. Cabrera-Bernal, S. Pennisi, A. D. Grasso, A. Torralba, and R. G. Carvajal, "0.7-V three-stage class-AB CMOS Operational Transconductance Amplifier," *IEEE Trans. Circuits Syst. I*, vol. 63, no. 11, pp. 1807-1815, Nov. 2016.
- [16] S. Sutula, M. Dei, L. Teres, and F. Serra-Graells, "Variable-mirror amplifier: A new family of process-independent class-AB single-stage OTAs for low-power SC circuits," *IEEE Trans. Circuits Syst. I*, vol. 63, no. 8, pp. 1101-1110, Aug. 2016.

TABLE II – SUMMARY OF MEASUREMENT RESULTS AND PERFORMANCE COMPARISON

Parameter	Class A OTA	Class AB OTA	[2]	[12]	[13]	[14]	[15]	[16]
CMOS process	0.5 μm	0.5 μm	0.18 μm	0.18 μm	0.35 μm	0.5 μm	0.18 μm	0.18 μm
Supply voltage	±1 V	±1 V	0.8 V	0.5 V	1 V	±1.25 V	0.7 V	1.8 V
Capacitive load	70 pF	70 pF	8 pF	20 pF	15 pF	25 pF	20 pF	200 pF
SR+	0.32 V/μs	9.8 V/μs	0.14 V/μs	2.89 V/μs	2.53 V/μs	2.7 V/μs	1.8 V/μs	74.1 V/μs
SR-	-0.28 V/μs	-7.6 V/μs	--	--	-1.37 V/μs	-3.3 V/μs	-3.8 V/μs	--
Pos. Settling	--	96ns	--	--	224 ns	--	1.3 μs	--
Neg. Settling	--	74ns	--	--	--	--	1 μs	--
THD	-24 dB @100kHz, 1V _{pp}	-41 dB @100kHz, 1V _{pp}	-52 dB @1kHz, 0.5V _{pp}	-40dB @0.4V _{pp}	--	-47.1 dB @2V _{pp}	-40.1 dB @250kHz, 0.4V _{pp}	--
DC gain (*)	69 dB	81.7 dB	51 dB	52 dB	88.3 dB	63.4 dB	57.5 dB	72 dB
PM (*)	89°	60°	60°	--	66.1°	83°	60°	50°
GBW	310 kHz	4.75 MHz	57 kHz	2.5 MHz	11.67 MHz	4.9 MHz	3 MHz	86.5 MHz
CMRR @DC	91 dB	78 dB	--	78 dB	40 dB	80 dB	19 dB	--
PSRR+ @DC	71 dB	72 dB	--	76 dB	40 dB	61.2 dB	52.1 dB	--
PSRR-@DC	79 dB	74 dB	--	--	--	--	66.4 dB	--
Eq. input noise @1MHz	128nV/√Hz	99 nV/√Hz	--	80 nV/√Hz	<60 nV/√Hz	--	100 nV/√Hz	--
Power	80 μW	120 μW	1.2 μW	110 μW	197 μW	437.5 μW	25.4 μW	11.9 mW
Area	0.020 mm ²	0.024 mm ²	0.057 mm ²	0.026 mm ²	0.157 mm ²	0.029 mm ²	0.020 mm ²	0.070 mm ²
FOM _L	0.56	11.42	0.74	0.26	0.19	6.4	1.54	2.24
FOM _S	75	554	30.4	227	88.9	70	165.3	261.7

(*) Simulation