E.T.S. de Ingeniería Industrial,
Informática y de Telecomunicación

Bobina de Tesla Conmutada

Grado en Ingeniería Eléctrica y Electrónica

Trabajo Fin de Grado

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RESUMEN

El objetivo de este proyecto es la creación de una Bobina de Tesla Conmutada. Una Bobina de Tesla se trata de un trasformador resonante con núcleo de aire capaz de generar niveles de tensión extremadamente altos. El funcionamiento de una Bobina de Tesla radica en la excitación de un circuito RLC (Resistencia-Inductor-Capacidad) a su frecuencia asociada o frecuencia de resonancia, debido a este fenómeno de resonancia los niveles de tensión generados son extremadamente altos.

El dispositivo está basado en dos bobinas concéntricas llamadas bobina primaria compuesta por varias vueltas de un conductor generalmente cobre y una bobina secundaria compuesta por cientos e incluso miles de vueltas generalmente de cobre esmaltado, aunque también se pueden observar algunas de aluminio.

El objetivo es excitar al sistema secundario compuesto por un sistema RLC mediante la bobina primaria. En esta tipología de Bobinas de Tesla se logra este objetivo mediante el uso de semiconductores, en este caso IGBT´s para inducir una corriente al sistema secundario a su frecuencia asociada o de resonancia.

PALABRAS CLAVE

- Bobina de Tesla
- Bobina de Tesla Conmutada
- SSTC
- Resonancia
- Sistemas resonantes

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ABSTRACT

The goal of this Project is the implementation of a Solid State Tesla Coil. A Tesla Coil is an air-cored resonant transformer capable of generating extremely high voltage. The key concept of a Tesla Coil is its resonant property, where a RLC (Resistor-Inductor-Capacitor) resonant circuit is energized at its resonant frequency, developing very high voltages.

The device consists of two concentric coils called primary coil, which consists of a few turns of wire, copper is generally used and a secondary coil, which consists of several hundreds to thousands of turns, bare copper wire is generally used, aluminum can also be used.

The goal is energize the secondary system which is a RLC circuit with the primary coil. In this typology of Tesla Coils we achieve it using semiconductors, IGBT´s here to induce a current to the secondary circuit at its resonant frequency.

KEY WORDS

- Tesla Coil
- Solid State Tesla Coil
- SSTC
- Resonance
- Resonant Systems

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1. Introducción

1.1 Contexto histórico

En la primavera de 1891 y continuando las investigaciones iniciales sobre voltaje y frecuencia de William Crookes, Nikola Tesla diseñó, construyó y patentó sus primeras bobinas que produjeron alto voltaje y alta frecuencia.

La primera bobina de Tesla estaba construida con una bobina primaria formada por 20 vueltas de cable cubierto por caucho separadas entre sí, los condensadores se realizaron mediante placas de un metal conductor sumergidas en aceite mineral, y la bobina secundaria estaba formada por 300 vueltas de cable cubierto de seda enrollado en un tubo de caucho y en sus extremos encajado en tubos de cristal o caucho.

El propósito de estas bobinas era de convertir y suplir energía eléctrica en una forma adaptada a la producción de ciertos nuevos fenómenos eléctricos que requerían cada vez corrientes de mayores frecuencias y potencial. Esta fue la primera aparición de una fuente de corriente RF (radio-frecuencia) capaz de excitar una antena para emitir potente radiación electromagnética.

Las bobinas posteriores fueron creadas generalmente por aficionados, tratándose de un transformador resonante con núcleo de aire, consiguiendo grandes tensiones. Estas bobinas perdieron el propósito con el que fueron creadas por Nikola Tesla y se dedicaron al espectáculo, generar largas chispas para el asombro del público.

La bobina de Tesla ha sufrido muchas variaciones a lo largo de su existencia, a continuación, se van a detallar los cambios sufridos con las diferentes versiones.

- **Spark Gap Tesla Coil (SGTC):** Esta tipología de bobinas se componen de un circuito primario formado por un transformador, generalmente de alta tensión, un circuito LC primario cuya frecuencia de resonancia sea similar a la del circuito LC secundario y un spark gap o explosor. Su funcionamiento radica en la carga del condensador, cuando dicha carga alcanza cierto potencial se activa el explosor cerrando el circuito LC y produciendo una corriente a su frecuencia de resonancia. Esta corriente se acopla en la bobina secundaria produciendo arcos eléctricos.

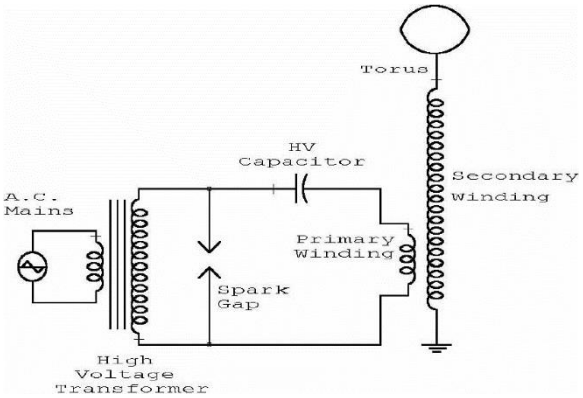


Fig1.Circuito bobina de Tesla por explosor

- **Vacuum Tube Tesla Coil (VTTC):** El funcionamiento es similar al anteriormente descrito salvo por un único cambio, el explosor se sustituye por un tubo de vacío, de este modo se puede controlar más fácilmente la tensión en la cual se cierra el circuito LC primario.

- **Solid State Tesla Coil (SSTC):** Con la aparición de semiconductores comerciales se idearon nuevos métodos de excitación de la bobina primaria y aparecieron las primeras bobinas de tesla conmutadas. El funcionamiento dejó de radicar en utilizar un circuito resonante primario y pasó a ser un sistema controlado de excitación de la bobina primaria a través de semiconductores como MOSFET´s o IGBT´s. Esta nueva tipología carece de condensador primario para la generación de esa corriente resonante.

1.2 Estado del arte

Dado que una bobina de Tesla es un dispositivo que genera grandes tensiones a RF se trata de un dispositivo peligroso para personas inexpertas, es por ello que no hay mucha oferta en el mercado de este tipo de dispositivos.

Se puede encontrar algo de variedad en pequeñas bobinas de Tesla. Nos centraremos en la opción de la empresa oneTesla . Esta empresa fue fundada a través de la conocida plataforma KickStarter por dos estudiantes del MIT (Massachusetts Institute of Technology) que ofrecen una pequeña opción para la compra y ensamblaje.

Una opción es el kit "TINYTESLA MUSICAL TESLA COIL KIT", se trata de una bobina de Tesla conmutada de muy baja potencia para principiantes con un ensamblaje muy sencillo e intuitivo. Ofrece una salida a interruptor con el objetivo de lograr reproducir música mediante la variación en el funcionamiento del interruptor.

Fig2.Producto tinytesla

Su precio final es de 219.99$ o 186.9€.

1.2 Motivación

La razón por la cual se decidió a la elaboración de este proyecto procede principalmente de la curiosidad, añadido al interés propio, en el diseño y construcción de proyectos generadores de alta tensión.

2. Objetivos

En este proyecto se diseñará y construirá una bobina de Tesla conmutada para obtener una primera experiencia con elementos generadores de alta tensión a alta frecuencia.

Dado que no se trata de un aparato de uso cotidiano, sus funciones se basan en el espectáculo y experimentación con alta tensión y alta frecuencia.

Los objetivos de este proyecto incluyen:

- Diseño y construcción de una bobina de Tesla conmutada auto-oscilante completamente funcional y semi-portable.
- Accesibilidad para modificar el funcionamiento de la bobina.

Para ello, la implementación del prototipo se divide en diferentes procesos de diseño, construcción y configuración a partir de los cuales se desarrollará el proyecto.

- Diseño hardware: La primera fase del proyecto consistirá en el diseño de los diferentes bloques que conforman el proyecto.
- Diseño y construcción de la PCB: Se realizará un diseño mediante una herramienta informática para su posterior construcción de la placa electrónica que controlará toda la bobina de Tesla conmutada.
- Prueba de funcionamiento de los diferentes bloques: Previo al ensamblaje de todos los componentes se probarán de manera independiente para comprobar su correcto funcionamiento o corregir los errores.
- Implementación del software del interruptor: Se desarrollará el programa que gobernará el funcionamiento de la bobina a modo de interruptor.
- Calibración de circuitos: Calibración de los diferentes circuitos para un funcionamiento óptimo.

3. Diseño Hardware

3.1. Introducción al funcionamiento y esquema principal

El funcionamiento de una bobina de Tesla conmutada (SSTC) es sencillo, se puede asemejar al funcionamiento de un convertidor de potencia cuya frecuencia de conmutación sea similar a la frecuencia de resonancia del circuito secundario. El circuito secundario se conforma de una bobina de cobre esmaltado generalmente un extremo se deberá de poner a tierra mientras que al otro habrá que asegurar una unión eléctrica con el toroide. El toroide se trata de una pieza con forma de donut de apariencia metálica cuyo objetivo es dar al sistema secundario una mayor capacitancia con respecto a tierra y así reducir su frecuencia de resonancia. El circuito secundario se puede resumir de la siguiente forma:

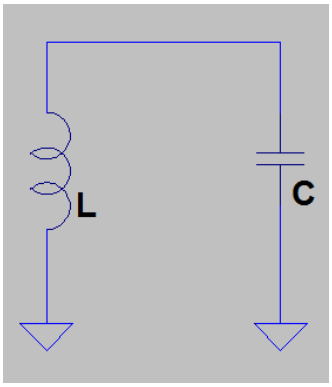


Fig3. Circuito secundario

Dicho sistema secundario llevará asociada una frecuencia de resonancia que estará relacionada con el producto de su inductancia (L) y su capacitancia (C) según la siguiente expresión:

$$f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{LC}}$$

El ratio entre la L y la C del sistema determinará el factor de calidad, el cual nos indicará como de ancha o de estrecha es la banda de resonancia. Este concepto puede ser entendido mejor asociándolo a un filtro paso-banda compuesto por una inductancia y una capacitancia, este factor de calidad nos indicará como de ancha es la banda de frecuencia en la cual el filtro no atenuará la señal.

El objetivo de estas bobinas de Tesla es encontrar la forma de conmutar el circuito primario a frecuencia de resonancia del secundario. La manera de conseguir este objetivo es inducir una onda cuadrada a través del primario mediante dispositivos semiconductores ya sea en configuración de medio puente o puente completo más conocido como puente en H. Se conseguirá mediante la rectificación de una fuente de potencia sinusoidal como puede ser la red eléctrica, una vez rectificada esta energía es almacenada en grandes condensadores y será el inversor el que se encargue de inducir una onda cuadrada AC a través del primario. El resultado de aplicar todo esto es una corriente sinusoidal a través de la bobina primaria por ser conmutado a frecuencia de resonancia del circuito secundario.

Para obtener la frecuencia de conmutación del inversor existen dos posibles opciones, la primera será con un generador externo de frecuencia y la segunda opción será la toma de una realimentación de la bobina secundaria que hará del sistema un sistema auto-resonante o auto-oscilante.

Cuando el sistema secundario es conmutado a su frecuencia de resonancia, una gran tensión se desarrolla a través de la bobina, si se continua alimentando al sistema a su frecuencia de resonancia esta tensión irá aumentando cada vez más produciendo una ionización en espacio circundante del toroide y eventualmente descargas al aire formando chispas o arcos.

3.2. Primer diseño

Como primer diseño y primera toma de contacto con las bobinas de Tesla conmutadas se ha partido de un diseño que ha demostrado su correcto funcionamiento:

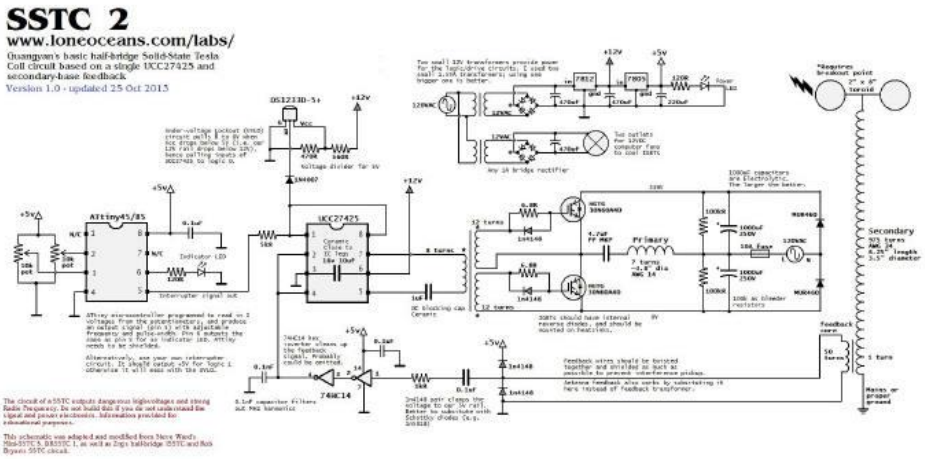


Fig4. Gunyan,G. (2005). Esquema general SSTC. Recuperado de http://www.loneoceans.com/labs/sstc2/

A partir de este esquema se expondrá y se detallará cada una de las decisiones tomadas para la realización del proyecto.

3.3. Componentes de una bobina de Tesla conmutada

Las partes que conforman una bobina de Tesla conmutada se pueden dividir en los siguientes grandes bloques:

- Sistemas resonantes: este sistema engloba la bobina secundaria y el toroide de aluminio, así como la bobina de excitación primaria. La bobina secundaria estará eléctricamente aislada del resto de circuitos.
- Bloque lógico: en este bloque convergen todos los elementos los cuales son necesarios para la correcta conmutación del inversor. En este bloque se generarán las señales necesarias para conmutar los semiconductores a la frecuencia deseada. Incluiremos el interruptor ya que debido a las altas exigencias de potencia y energía que dan como resultado la conmutación a tiempo completo del inversor, generalmente se añade un dispositivo capaz de interrumpir este modo continuo de funcionamiento con el fin de reducir energía consumida y excesos de temperatura en los semiconductores.
- Bloque inversor: en este bloque se encuentran todos los componentes de potencia necesarios para conmutar el inversor. Tendrá como objetivo conmutar dicha corriente a la frecuencia de resonancia del sistema secundario. En este bloque se engloba el inversor, rectificador, condensador de bus y adecuación de la red de potencia al sistema.

A continuación, se estudiará en detalle cada uno de estos bloques.

3.3.1. Sistemas Resonantes

3.3.1.1. Sistema Secundario

Para el diseño del sistema secundario le primera decisión a tomar es sobre que rango de frecuencia se desea que resuene, generalmente esta frecuencia se escoge conforme el tamaño deseado de la bobina. Para bobinas pequeñas el rango suele oscilar desde 500 kHz hasta pocos MHz en caso de no añadirle una capacidad con un toroide. Para el sistema se ha escogido una frecuencia de resonancia entre 200 y 250 kHz lo que corresponde a una bobina de tamaño medio. Todos los cálculos se han realizado mediante la herramienta 'Javatc3d' ofrecida por la web 'www.classictesla.com' en la cual introduciendo los datos necesarios se obtiene una simulación de las características del sistema. En este caso como ya se disponía de un toroide formado por conducto de aluminio flexible, una tubería de PVC a la cual se arrollaría la bobina secundaria y el alambre de cobre del laboratorio el cual era AWG 22. Con estos datos y con el objetivo de una frecuencia de resonancia cercana a 225 kHz se simularán diferentes valores de altura de la bobina secundaria y sus correspondientes vueltas. Esta frecuencia de resonancia no supondrá limitación a la hora de conmutar el inversor, se deberá escoger el rango de frecuencias en el que se desea trabajar ya que si se escogen unas frecuencias demasiado altas se puede tener problemas para la conmutación del inversor, por otro lado, si se escogen frecuencias más bajas el tamaño y precio de la bobina aumentan considerablemente.

En este diseño los datos de entrada serán los siguientes:

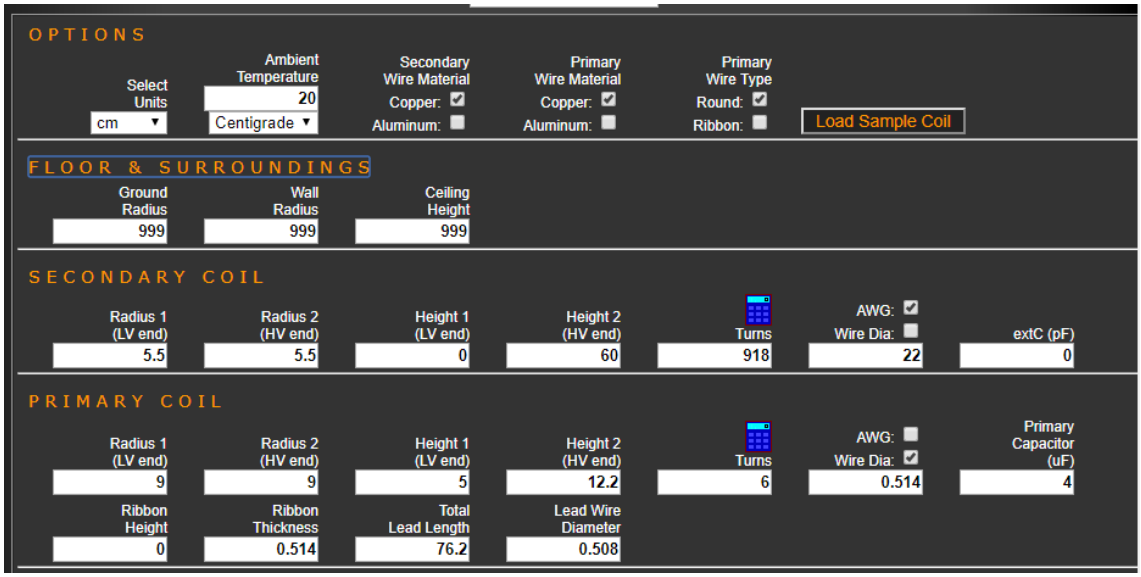


Fig5. Datos de entrada diseño bobina secundaria y primaria

Se debe señalar que la adición de un condensador en el circuito primario no se busca un efecto de resonancia, sino que su uso se debe a un elemento de seguridad para el inversor como bloqueador de corriente DC en caso de cortocircuito.

Esta herramienta también ofrece la utilidad de simulación de la capacidad aportada por el toroide metálico, dicho toroide se considera un dato de partida ya que el propósito era reutilizarlo.

Fig6. Datos del toroide

Con todos estos datos de entrada se obtiene un sistema con las siguientes características.

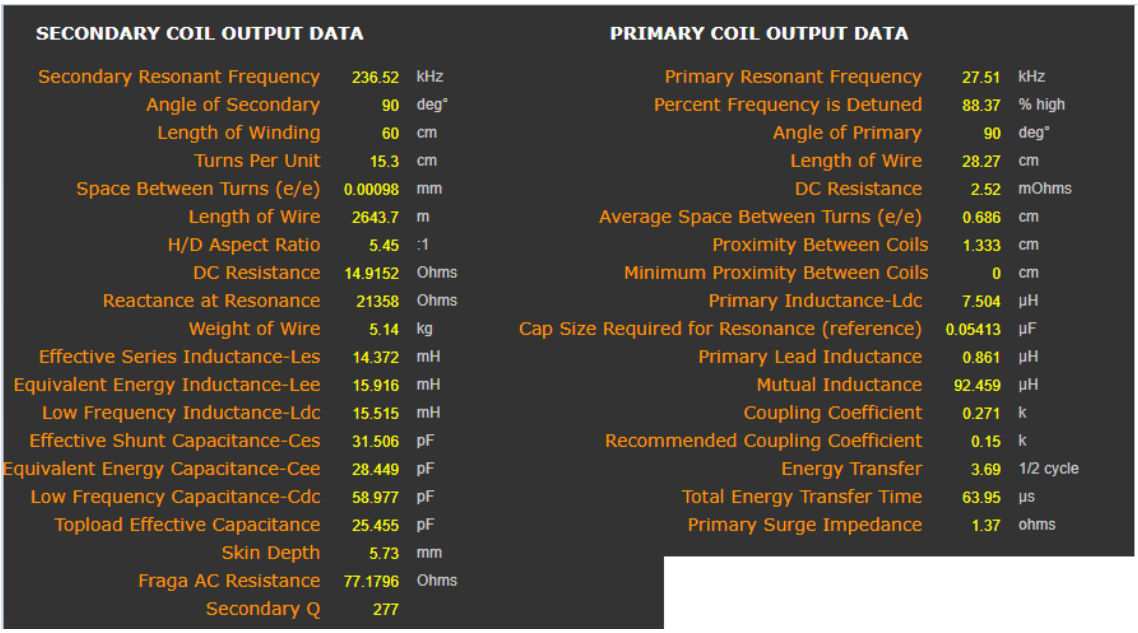


Fig7. Datos de salida sistema primario y secundario

Como se puede apreciar en la Fig7 se cumplen con los objetivos de diseño con una frecuencia de resonancia de 236.52 kHz.

Esta herramienta también ofrece la posibilidad de visualización de la bobina en 3D, para que el diseñador se haga una idea de la relación entre componentes y su distribución espacial.

Fig8. Simulación 3D bobina

A continuación, se muestra una fotografía del sistema secundario junto a la bobina de excitación primaria.

Fig9.Foto sistema secundario

Para complementar el aislamiento del conductor de cobre se le aplicará un esmalte no conductor. Existen varias opciones para este cometido: utilizar un esmalte diseñado para el aislamiento eléctrico o utilizar algún tipo de barniz para madera preferiblemente que sea a base de alguna composición de poliuretano. Puede parecer que la opción del esmalte pueda parecer la más lógica pero el uso de un barniz para madera resulta mucho más cómodo de utilizar, más rápido y más barato obteniendo un resultado similar.

3.3.1.2. Sistema Primario

La bobina primaria consta de unas pocas vueltas de un conductor de cobre (en este caso de sección 4 mm^2) arrolladas a una corta distancia de la bobina secundaria. El objetivo de este tipo de disposición del conductor es conseguir un buen factor de acoplamiento. Este factor se incrementará cuanto más cerca se disponga la bobina primaria de la secundaria, también variará según la geometría escogida. Este proyecto consta de una bobina primaria concéntrica a la bobina secundaria, de diámetro 18 cm y un total de 6 vueltas, con esas características el factor de acoplamiento obtenido es de 0.27. Un factor de acoplamiento muy alto provocará que salten chispas o arcos entre las espiras del circuito secundario. Se recomienda un factor de acoplamiento entre 0.15 y 0.3 si el hilo de cobre tiene suficiente aislamiento.

3.3.1.2.1. DC Block

Se acoplará en serie a la bobina primaria un condensador, este no tiene como objetivo provocar ningún tipo de resonancia, el propósito de este condensador será el bloqueo de una posible corriente de componente DC que potencialmente puede sobrecargar los transistores. La recomendación para escoger la capacidad de estos condensadores es de 1 a 10 uF generalmente de poliéster o de algún otro tipo de película plástica. En este proyecto se han dispuesto dos condensadores de 6.8 uF y 300 V en serie, obteniendo una capacidad de 3.4 uF y una tensión soportada de 600 V.

La reactancia aportada por este condensador al sistema primario vendrá definida por la capacidad de este condensador y la frecuencia de oscilación del sistema según la siguiente relación:

$$X_c = \frac{1}{wC} = \frac{1}{2\pi f_r C}$$

f_r: Frecuencia de resonancia del sistema

C: capacidad condensador DC block

Mediante un cálculo rápido se obtiene la impedancia que aporta al sistema primario con los siguientes datos de partida, f_r=236.52 kHz y C=3.4uF. La reactancia aportada por esta capacidad es de 0.2 Ω, una impedancia muy pequeña en comparación con la aportada por la bobina primaria que se estudiará a continuación.

A partir de este punto y explicado el propósito de este condensador se ignorará la reactancia aportada por el mismo para posteriores cálculos.

3.3.1.2.2. Bobina primaria

Como ya se ha mencionado la bobina primaria se compone de 6 vueltas de cable de 4 mm^2 y con un radio de 9 cm, la inductancia aportada por la bobina primaria es de 7.5 uH. Con este dato se calculará una estimación de la corriente que circulará por el puente. Primero se obtiene la impedancia que aporta la bobina a la frecuencia de funcionamiento según la siguiente expresión:

$$X_L = wL = 2\pi f_r L$$

f_r: Frecuencia de resonancia del sistema

L: inductancia de la bobina primaria

Con los datos ya expuestos se obtiene una impedancia inductiva de 11.14 Ω. Mediante esta impedancia se podrá estimar la corriente pico que circulará a través de la bobina. Con una tensión de bus de 325 V ($230*2^{1/2}$), es decir una onda cuadrada de 325 V pico. Con este valor y la impedancia de la bobina primaria se obtiene un pico en la corriente que circula por el puente de 29.19 Amperios. Este dato será utilizado como referencia en futuras operaciones y toma de decisiones.

3.3.2. Bloque lógico

En este apartado se expondrá los criterios de diseño en los cuales se ha basado la toma de decisiones respecto a este bloque de componentes. Todo este bloque se ha integrado en una PCB la cual también se explicará su diseño y construcción.

El objetivo de este bloque es generar las señales de disparo de los semiconductores para obtener una corriente sinusoidal a través del sistema primario a la frecuencia de resonancia del secundario. Para ello se dividirá el bloque en varios bloques más pequeños para conseguir razonar mejor su comportamiento. Se dividirá en los siguientes bloques:

- **Alimentación bloque lógico:** este bloque se destinará a la alimentación de toda la circuitería lógica, consta de una fuente de alimentación aislada, rectificadores, condensadores de almacenamiento de energía para la electrónica y reguladores para adaptar la tensión a la tensión de uso de los circuitos integrados.
- **Generador de frecuencia y filtrado:** este bloque se destinará a recuperar una pequeña parte de la corriente inducida en el sistema secundario para dar las órdenes de encendido y apagado a los drivers. En este bloque también se incluye el filtrado de la señal de realimentación para darle una entrada al driver acondicionada.
- **Driver:** este bloque es el que estará pondrá en contacto el bloque lógico o de señal y el bloque de potencia o inversor, incluye todos los elementos necesarios para una correcta conmutación del inversor.
- **Interruptor:** se engloba en el bloque lógico el interruptor para un funcionamiento discontinuo y que los elementos del inversor no estén sometidos a tanto estrés térmico.
- **Protección de circuitos electrónicos:** este bloque incluye un supervisor de tensión a modo de precaución, el funcionamiento de este bloque se explicará con detalle en su apartado correspondiente.

A continuación, se explicará cada uno de estos bloques.

3.3.2.1. Alimentación Bloque Lógico

El objetivo de este bloque es generar las señales de alimentación necesarias para el funcionamiento de la electrónica del proyecto. Se generará una señal de 12 V para la alimentación de la refrigeración de la caja, una línea de 12 V para el disparo del driver y una línea de 5 V para la operación de puertas lógicas y microprocesadores.

El esquema de alimentación se puede resumir mediante la siguiente imagen:

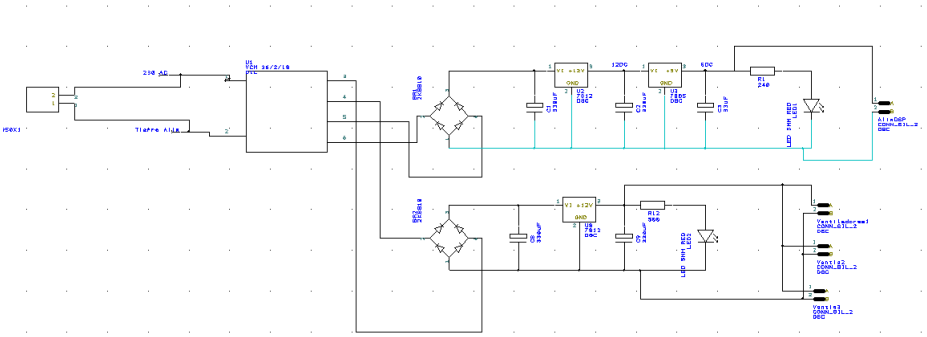


Fig10.Esquema alimentación PCB

Para la alimentación del bloque lógico se ha utilizado una fuente aislada con una relación de transformación de 230/18 ac. Esta fuente ofrece dos salidas independientes, una se utilizará para la alimentación de la refrigeración de la caja y la otra para toda la alimentación de la electrónica. El modelo elegido el de la marca Block VCM 36/2/18 pudiendo hacer una entrega de potencia máxima de 36 VA.

Fig11. Fuente de alimentación aislada Block VCM 36/2/18

Para la conexión de la tensión de alimentación de la fuente aislada se utilizarán clemas de conexión soldadas de dos entradas. Se ha escogido un terminal de rosca para PCB de 2 vías similar a este:

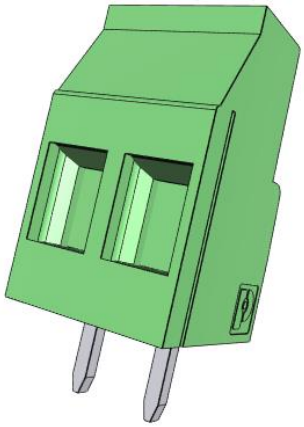


Fig12. Clema de conexión

El aislamiento eléctrico entre bornes de la clema debe ser suficiente para garantizar que no se creará una fuga de corriente entre sus terminales.

El puente rectificador de diodos para la rectificación de tensión para la placa electrónica es un rectificador en puente monofásico de la marca HY Electronic Corp y el modelo W10G.

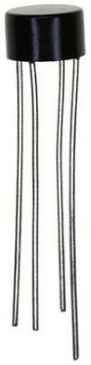


Fig13.Rectificador puente monofásico HY Electronic Corp W10G

Con el propósito de almacenamiento de energía y estabilizar tensiones se han dispuesto una serie de condensadores electrolíticos de 330 uF como el que se muestra a continuación.

Fig14. Condensador electrolítico PCB

Para la regulación y adaptación de tensión de los diferentes carriles se han utilizado reguladores de tensión lineal, de la gama de circuitos 78xx. En este proyecto se disponen de líneas a 12 V y a 5 V por lo que los reguladores utilizados son los 7812 y 7805 respectivamente.

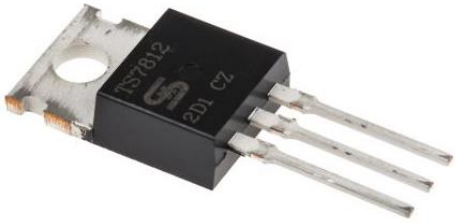


Fig15. Regulador de tensión lineal 12 V

Se han dispuesto una serie de LED´s para una comprobación visual de que los circuitos de alimentación proveen de las tensiones necesarias al resto de circuitos de la tarjeta, será necesario limitar la corriente por estos LED´s mediante el uso de resistencias.

Fig16. LED PCB

3.3.2.2. Generador de frecuencia y filtrado

El generador de frecuencia se basa en una realimentación del sistema secundario, se realiza mediante un pequeño transformador de corriente. Este transformador se compone de una ferrita apropiada para el uso a estas frecuencias a la cual se arrolla una vuelta de hilo de cobre de la bobina secundaria y cuarenta vueltas de las cuales sacaremos la referencia de frecuencia. Esta referencia deberá ser adecuada a los circuitos lógicos, mediante el uso de dos diodos se conseguirá adaptar esos niveles de tensión a nuestros railes de 0 a 5 voltios. Esta señal es filtrada, eliminando su componente DC y se adaptará mediante dos puertas NOT con tecnología Smith Trigger las cuales limpiarán la señal de armónicos de alta frecuencia y darán una salida cuadrada con un nivel de tensión apropiado al driver.

El núcleo escogido para esta aplicación es un anillo de ferrita EPCOS B64290L0632x830. Este núcleo resulta apropiado para aplicaciones a frecuencias cercanas a 200 kHz.

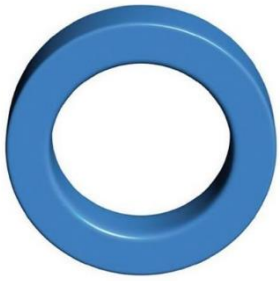


Fig17. Núcleo ferrita EPCOS B64290L0632x830

La característica más importante a la hora de elegir uno de estos núcleos es la propiedad de factor de inductancia (A_L) que dependerá del material del cual se componga el núcleo. El material elegido para este cometido es el N30 cuyo factor de inductancia A_L es de 4160 nH+-25% según la hoja de características del fabricante. De este factor dependerá la inductancia ofrecida por el núcleo según la siguiente expresión:

$$A_L = \frac{L}{N^2}$$

A_L: Factor de inductancia

L: Inductancia ofrecida por el núcleo

N: Número de vueltas de conductor arrolladas al núcleo

Estos núcleos son recomendados para aplicaciones de construcción de bobinas, transformadores, transformadores de impulso y transformadores de banda ancha.

Esta señal se acomodará a través de dos buffers inversores de la familia 74HC14, buffers inversores con báscula Smith para obtener una señal clara de conmutación en el driver.

Fig18. Buffer inversor Smith Trigger

Se implementa un condensador entre la salida del buffer y la entrada a los drivers con el fin de evitar disparos a muy alta frecuencia producidos por ruido ambiente.

3.3.2.3. Driver

Este circuito se encargará de dar las órdenes de disparo a los semiconductores. Se dividirá en dos subcircuitos, el circuito driver y el circuito de disparo del semiconductor. A continuación, se desarrollará cada uno de ellos.

3.3.2.3.1. Circuito Driver

Para este cometido se ha escogido un driver de la marca Texas Instruments el modelo UCC27425, se trata de una de las partes esenciales del proyecto, en las siguientes líneas se explicará la razón. Se han utilizado dos de estos drivers, cada uno conmutará una rama del puente en H. Este modelo es capaz de suministrar corrientes pico de 4.5 Amperios, suficiente para pequeños transistores.

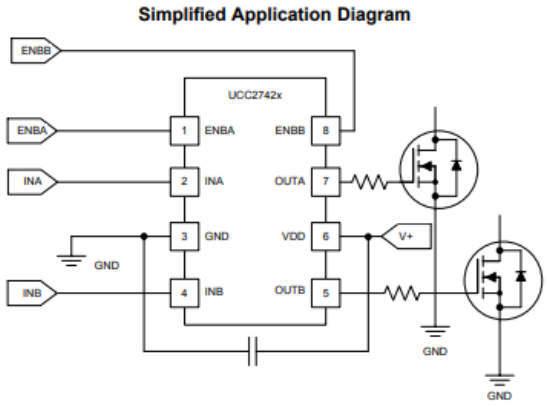


Fig19.Esquema Driver simplificado UCC27425

En las siguientes figuras se muestra el funcionamiento simplificado del driver así como su tabla de verdad.

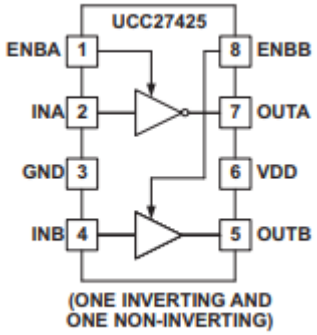


Fig20.Esquema funcionamiento driver UCC27425

		INPUTS (VIN_L, VIN_H)		UCC27425	
ENBA	ENBB	INA	INB	OUTA	OUTB
H	H	L	L	H	L
H	H	L	H	H	H
H	H	H	L	L	L
H	H	H	H	L	H
L	L	X	X	L	L

Fig21.Tabla de verdad driver UCC27425

A continuación se realizará la conexión del driver, para ello se establecerá el mismo potencial eléctrico entre sus entradas ENA y ENB de ambos drivers, de este modo con una única señal se podrá controlar el encendido y apagado de ambos drivers, esta señal provendrá del interruptor. Del mismo modo se establecerá el mismo potencial eléctrico entre las entradas INA e INB de ambos drivers para conseguir con una misma señal conmutar ambas ramas. En la siguiente imagen se muestran remarcados los estados de la tabla de verdad del driver en los cuales nos situaremos:

		INPUTS (VIN_L, VIN_H)		UCC27425	
ENBA	ENBB	INA	INB	OUTA	OUTB
H	H	L	L	H	L
H	H	L	H	H	H
H	H	H	L	L	L
H	H	H	H	L	H
L	L	X	X	L	L

Fig22.Tabla de estados deseados driver UCC27425

Mediante este método se obtiene una salida de +-12V con respecto a una de las salidas. Otro punto importante será disponer de condensadores de almacenamiento para suplir a los drivers durante la conmutación, los valores de estos condensadores pueden ir desde 15 uF hasta 100 uF. En la siguiente imagen se puede observar la conexión completa de los circuitos driver.

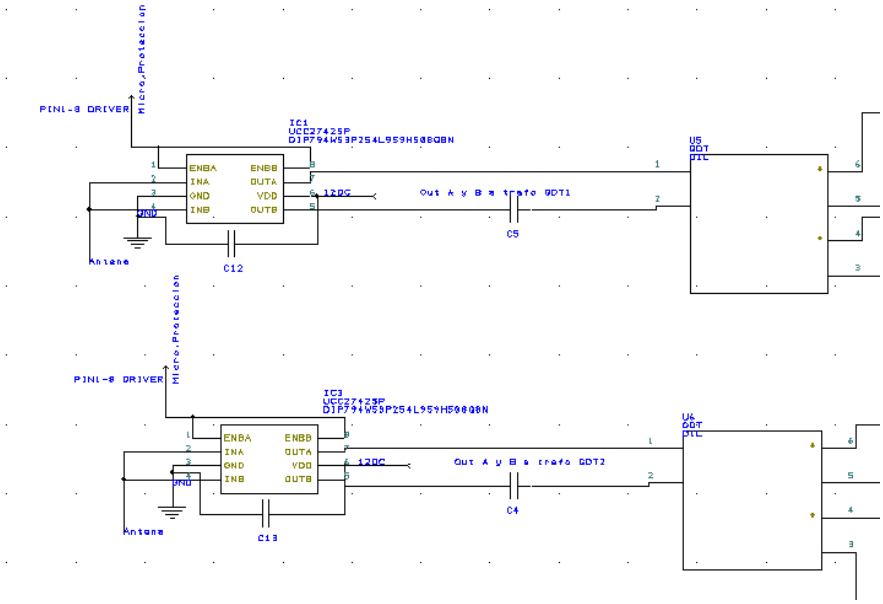


Fig23. Conexión drivers

Será necesario el aislamiento eléctrico del driver con respecto al circuito de potencia ya que no comparten el mismo potencial de referencia. Para realizar este cometido hay varias opciones disponibles como optoacopladores o transformadores. En este proyecto se ha optado por el aislamiento eléctrico mediante transformadores, estos transformadores reciben el nombre de GDT (*"Gate drive transformer"*). Del mismo modo que el circuito de realimentación de frecuencia se han utilizado dos ferritas. Estas ferritas se desconoce el modelo y características pero una buena opción para este uso son las anteriormente mencionadas para la realimentación de la bobina secundaria. Para asegurarnos la saturación de los transistores la relación entre las espiras del secundario y primario será cercana a 1.5, de este modo a la salida del transformador será de una tensión cercana a +-18 V respecto a la referencia tomada.

Se colocará un condensador en serie con el primario de manera similar a la bobina primaria con el objetivo de evitar corriente DC por el primario del transformador, este elemento se trata de un elemento de seguridad sin ninguna aplicación real en el

funcionamiento de la bobina, los valores de capacitancia para este condensador serán similares al condensador de la bobina primaria pero las tensiones que deberá soportar este son de 12 V.

3.3.2.3.2. Circuito disparo semiconductor

El objetivo de este circuito es conseguir un disparo suave de los elementos semiconductores del inversor. Para ello el disparo de cierre del semiconductor se produce a través de una resistencia de puerta o R_G, mientras que la apertura se produce a través de un diodo para hacerla lo más breve posible y disminuir las pérdidas por conmutación. La elección de la resistencia de puerta vendrá limitada por la corriente que pueda suministrar el driver, en este proyecto las resistencias de puerta son de 3.9 Ω. El esquema del circuito de disparo es el siguiente:

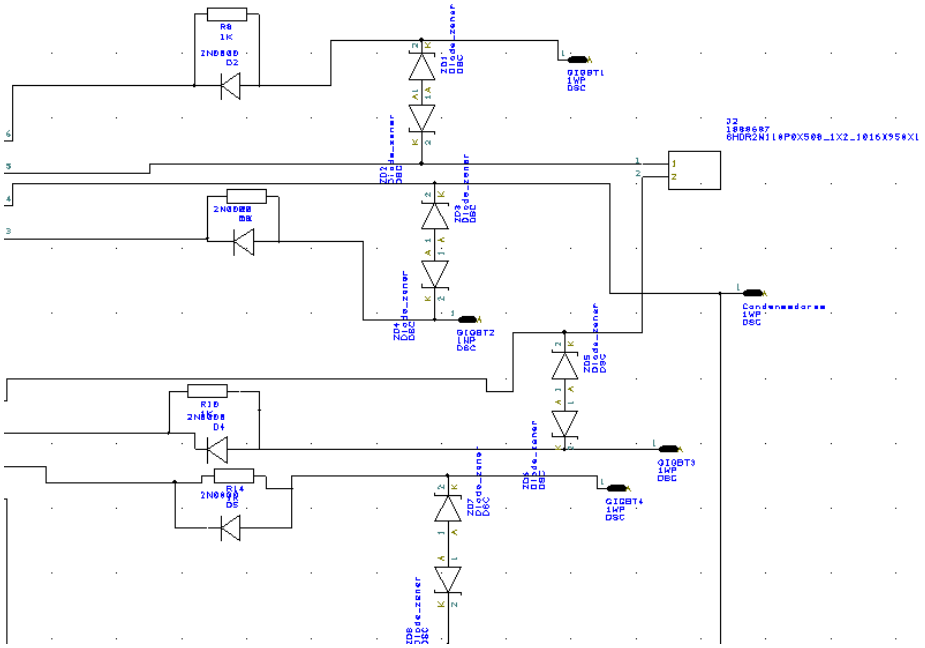


Fig24. Esquema disparo semiconductores

Se han dispuesto 2 diodos zener en antiserie con el fin de evitar sobretensiones entre puerta y emisor que puedan producir daños en el transistor, como se ha mencionado se han dispuesto con una topología antiserie, la suma entre la tensión de ruptura de un zener y la de polarización directa del otro no deben ser superiores a la máxima tensión entre puerta y emisor soportados por el transistor. Aunque no reflejado en el esquema también se han colocado resistencias entre la puerta y el emisor con el fin de evitar encendidos no deseados debidos a cargas parásitas.

3.3.2.4. Interruptor

Este dispositivo se encargará de interrumpir el funcionamiento continuo del inversor a través del driver. El objetivo de este bloque será generar una onda cuadrada de frecuencia

y ancho de pulso variable. Durante el periodo alto el inversor funcionará con normalidad y durante el periodo bajo el inversor cesará su funcionamiento. Esta operación se elabora mediante el uso de un microprocesador el cual mediante dos lecturas de entradas analógicas determinará la frecuencia y el ancho del pulso de la señal a enviar al pin "Eneable" del driver. En la siguiente imagen se muestra el esquema del bloque:

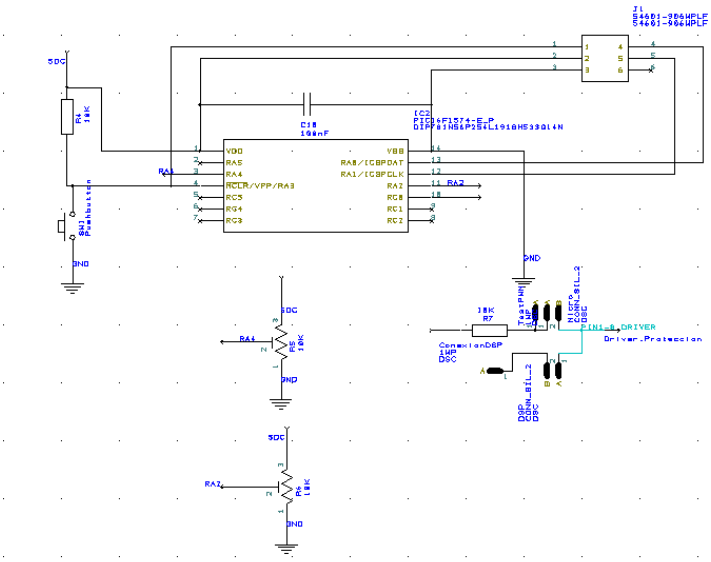
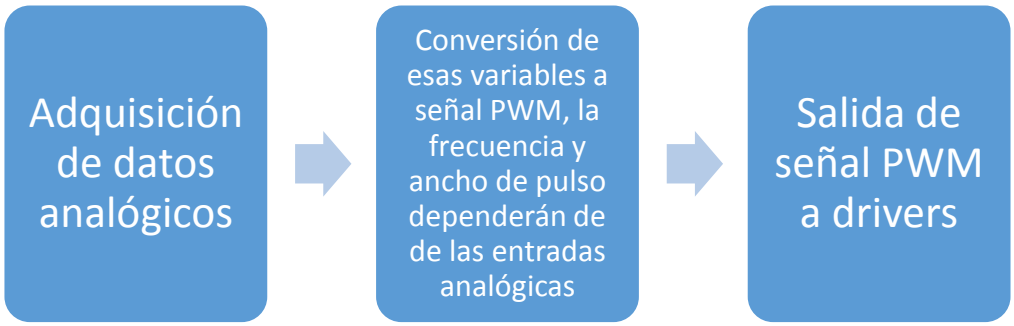


Fig25.Esquema microprocesador

El interruptor se ha realizado con un microprocesador de la marca Microchip y modelo PIC16F1575. Se trata de un microprocesador de 14 patillas con oscilador interno y suficiente memoria para albergar toda la programación necesaria para este cometido. El diagrama de flujo del programa es el siguiente:



El programa no podrá superar el ciclo de trabajo máximo del inversor calculado en el Anexo A.2 por lo que será necesario limitarlo.

3.3.2.5. Protección de circuitos electrónicos

El objetivo de este circuito es únicamente de protección del driver e inversor ante caídas de tensión en la tensión de alimentación del driver. Para asegurar que la tensión de disparo del driver es siempre a la cual se ha diseñado.

El circuito elegido para este cometido es un supervisor de tensión utilizado generalmente con microprocesadores, este circuito ante una caída de la alimentación produce un reset hasta que se reestablece la alimentación a unos valores mínimos. Se trata del circuito supervisor de tensión DS1233-5+.

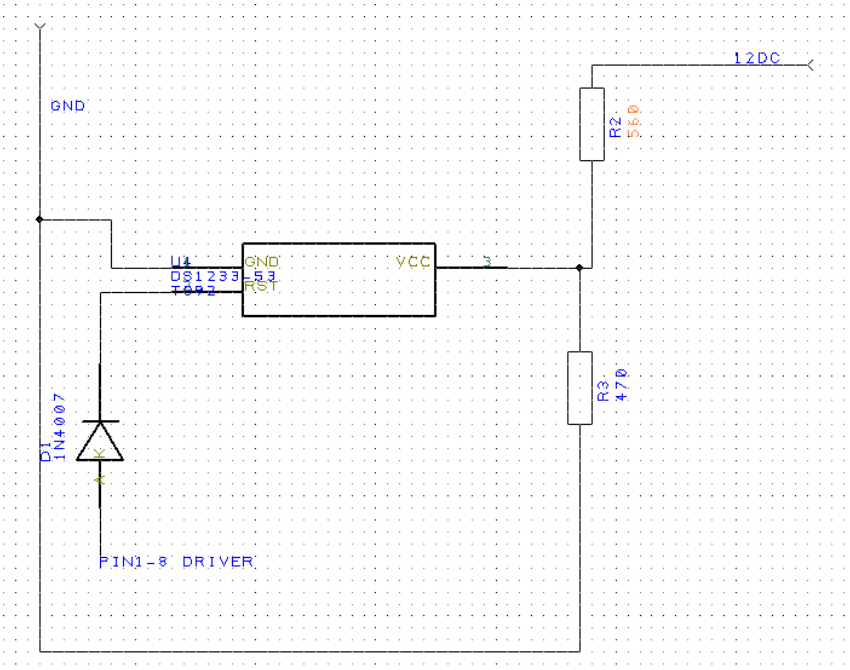


Fig26. Supervisor de tensión DS1233-5+

Dado que la línea que se quiere supervisar es la de alimentación del driver la tensión debe ser adaptada a la entrada del supervisor. La tensión máxima de entrada del supervisor es de 5.5 V por lo que mediante un simple divisor de tensión se adapta para su supervisión. El integrado activará la señal de reset cuando la tensión de alimentación sea menor de 4.65 V. Extrapolando este valor si la tensión del rail de 12 V cae a un valor menor 10.19 V la señal de reset se activará a 0 V provocando la parada de los circuitos driver.

3.3.3. Bloque inversor

Este bloque se puede subdividir en adaptación de la red de potencia, bus DC e inversor. En las siguientes líneas se explicará la toma de decisiones de estos componentes.

3.3.3.1. Adaptación de la red de potencia

El objetivo de este circuito es adaptar la tensión para el uso de la bobina, este circuito consiste en un puente rectificador de diodos y un limitador de corriente.

Para la elección del puente de diodos no se ha tomado ninguna consideración aparte de que sea capaz de soportar la tensión pico de la red (325V) y que la corriente que circula por él no sea mayor a la de su hoja de características.

Como limitador de corriente existen varias opciones en el mercado como relés, transistores o termistores. El objetivo de este dispositivo es limitar la corriente de entrada cuando el bus DC está descargado. En este proyecto como opción barata y sencilla se ha escogido un termistor de coeficiente negativo o NTC ("*Negative termistor coefficient"*). Este termistor se trata de una resistencia variable con la temperatura, conforme se calienta su resistencia DC va disminuyendo hasta dejarlo prácticamente despreciable. Las consideraciones para elegir este elemento son la corriente nominal en estado de carga que lo va a atravesar y la resistencia a temperatura ambiente que ofrece. Para evitar que al momento de conexión de la bobina actúen protecciones magnetotérmicas se ha escogido un termistor que a temperatura ambiente ofrece una resistencia de 20 Ω, con esta resistencia se limita la corriente demandada inicial a 11.55 A, suficientemente baja para que no actúe ninguna protección. El modelo elegido es Ametherm MS 32 20010, que ofrece una resistencia de 20 Ω y está preparado para una corriente nominal de 10 A.

Fig27. Termistor NTC Ametherm MS 32 20010

3.3.3.2. Bus DC

El objetivo de este elemento es el almacenaje de energía y estabilización de tensión para la conmutación del inversor. Las consideraciones con este elemento no son elevadas, la tensión máxima soportada debe ser mayor a la tensión de red rectificada. Como consideraciones añadidas, que su resistencia serie equivalente sea baja o ESR ("*Equivalent series resistance*") y su inductancia serie equivalente o ESL ("*Equivalent series* inductance") sea lo más pequeña posible.

Las rápidas conmutaciones del inversor producen sobretensiones entre el colector y emisor del transistor debido a inductancias parásitas por lo que la disposición espacial de este elemento debe ser lo más cerca del puente inversor a través de un bus laminado con el fin de reducir al máximo posible todas las inductancias parásitas.

Los condensadores de bus elegidos son condensadores electrolíticos de aluminio KEMET ALS70A122DF450 de 1.2 mF.

Fig28.Condensador bus DC KEMET ALS70A122DF450

3.3.3.3. Inversor

El inversor es elemento clave de todo el proyecto y al que más atención se ha de prestar. Existen varias modalidades de inversores principalmente medio puente o puente completo aunque hay algunas opciones más. En este proyecto se ha elegido el uso de un puente completo.

Para la elección de los elementos semiconductores las principales características serán la tensión máxima colector-emisor que deberán soportar, intensidad colector-emisor que los atravesará y frecuencia de conmutación. Para este proyecto los datos de diseño serán:

- Tensión nominal Colector-Emisor de 325 V
- Intensidad nominal 20.64 A (aproximación anteriormente calculada)
- Frecuencia de conmutación 235 kHz

Los transistores escogidos para este proyecto son de la marca Fairchild y modelo FGA60N65SMD. Se tratan de unos transistores IGBT que cumplen todas las características anteriormente citadas, a continuación se exponen las cualidades más interesantes y por qué han sido elegidos estos transistores:

- Tensión máxima Colector-Emisor: 650 V (a 25ºC)
- Corriente máxima Colector-Emisor: 120 A (a 25ºC)
- Corriente máxima Colector-Emisor: 60 A (a 100ºC)

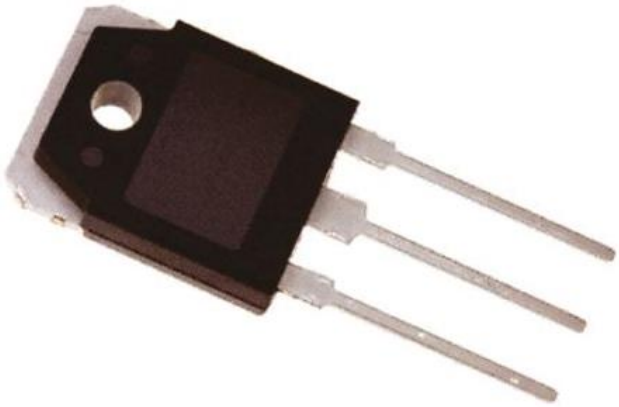


Fig29. IGBT FGA60N65SMD encapsulado TO-3PN

Estos transistores deberán ser puestos en un disipador de calor con el fin de evacuar las pérdidas generadas en la conmutación y conducción de corriente. Se deberá tener especial cuidado ya que con el fin de mejorar la evacuación de calor de estos transistores la tensión de la lámina metálica que hace contacto con el radiador no está aislada y comparte tensión con el colector. Se deberá poner una lámina aislante, ya sea de mica o plástica para aislar correctamente el transistor del disipador, en este caso se ha puesto una lámina plástica diseñada para tal efecto que ofrece una resistencia térmica aproximada de 0.5 ºC/W.

La posición de los transistores en el disipador se realizará con el objetivo de reducir todas las inductancias parásitas al mínimo.

El disipador elegido para la disipación de estas pérdidas en forma de calor es de la marca SEMIKRON, el modelo P38/300. Se trata de un disipador de aletas de aluminio verticales lacadas con un barniz negro con el fin de mejorar la disipación de calor por radiación. Es un disipador de 300x200x40 mm con una resistencia térmica dada por el fabricante de 0.28 K/W.

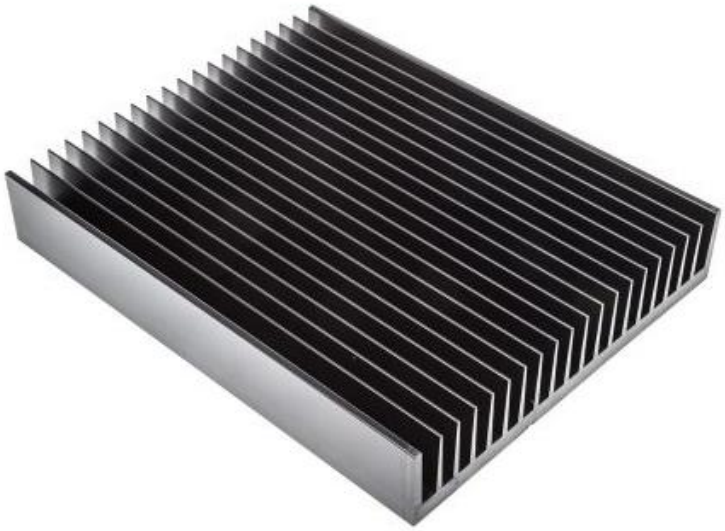


Fig30. Disipador de aluminio SEMIKRON P38/300

Los cálculos de potencia disipada así como el ciclo de trabajo máximo de operación de la bobina se adjuntarán en el Anexo A.1.

4. Diseño PCB

La construcción de este bloque se ha realizado mediante una PCB. El diseño de la PCB se desarrolla mediante el programa gratuito "DesignSpark", herramienta ofrecida por la empresa de componentes electrónicos "RS Componentes". Este programa facilita el diseño de PCB´s y mediante los archivos de salida GERBER la posibilidad de fabricación de las placas electrónicas.

En primer lugar se enumerarán los componentes para la construcción de la PCB.

4.1. Componentes PCB

- Fuente de alimentación aislada: Componente diseñado para la integración en PCB con una entrada de 230V y dos salidas a 18V con una capacidad de potencia máxima de 36 VA.

Fig31. Fuente de alimentación aislada Block VCM 36/2/18

- Rectificador de diodos: se trata de elementos de orificio pasante ideados para transformar la tensión ac a continua para su posterior regulación.

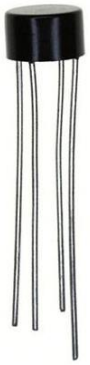


Fig32.Rectificador puente monofásico HY Electronic Corp W10G

- Regulador: circuito integrado de orificio pasante para la regulación de los niveles de tensión necesarios.

Fig33. Regulador de tensión lineal 12 V

- Condensadores electrolíticos: condensadores de orificio pasante para el almacenaje de energía y regulador de tensión.

Fig34. Condensador electrolítico PCB

- Circuitos integrados: Todos los circuitos integrados serán de orificio pasante y conexionados mediante zócalos adecuados. En este apartado se incluyen microprocesador, drivers y puertas lógicas. Mediante el uso de zócalos no se expone al circuito integrado a altas temperaturas que podrían dañarlo durante el proceso de soldadura.

Fig35. PIC16F1575

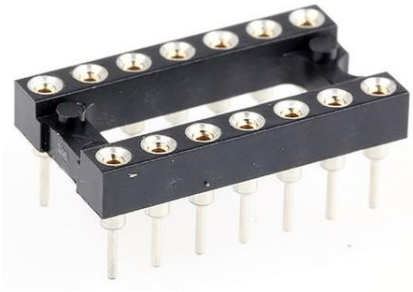


Fig36. Zócalo 14 pines

- Resistencias: Las resistencias serán todas de orificio pasante y de 0.5 y 0.25 W de potencia con un 5% de tolerancia.

Fig37. Resistencia 1/2 W

- Condensadores de desacoplo: Los condensadores para este cometido serán cerámicos de orificio pasante de 100 nF y dispuestos lo más cerca del integrado entre alimentación y tierra.

Fig38. Condensador cerámico PCB

- Potenciómetros: Se tratan de potenciómetros lineales giratorios de 3 pines con un recorrido de 3/4 de vuelta.

Fig39. Potenciómetro giratorio lineal PCB

- Pulsador: Para la función de reseteo del microprocesador se monta un pulsador de orificio pasante y 4 pines.

Fig40. Pulsador PCB

- Puerto RJ11: Para la programación del microprocesador es necesaria la conexión con el exterior, el conexionado del puerto RJ11 con el microprocesador se establece según el documento A.7.5.

Fig41. Conector hembra RJ11 PCB

- LED: Indicador visual del correcto funcionamiento de los circuitos de alimentación.

Fig42. Led Verde 5mm

- Conexión de circuitos externos: para la conexión de circuitos externos los elementos utilizados son clemas de conexión y pines macho para el testeo del funcionamiento de la PCB.

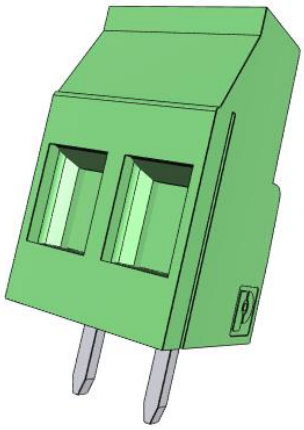


Fig43. Clema de conexión

Fig44. Pin macho PCB

4.2. Diseño de componentes de la PCB

Los componentes necesarios para la creación de la PCB se han obtenido mediante la aplicación "*rs components search engine*" ofrecida por la página web de componentes eléctricos "rs components".

El único componente que ha sido necesario crear ha sido la fuente de alimentación aislada 230/18 Vac. Para ello se ha creado un diseño esquemático con todas los pines accesibles del componente, se le ha asociado también una huella PCB que contiene tanto las medidas reales del componente como la posición de los pines de conexión.

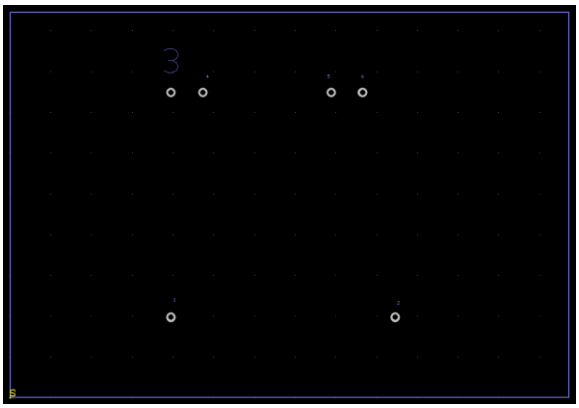


Fig45. Huella PCB VCM 36/2/18

Para el resto de componentes se ha utilizado la aplicación anteriormente descrita.

4.3. Especificaciones del diseño de la PCB

A continuación se describen los objetivos de diseño:

- Los Componentes serán de orificio pasante (DIP) por lo tanto se habrá de determinar el diámetro mínimo del agujero así como el área del pad para una correcta soldadura.
- La PCB se diseñará a una capa con el objetivo de reducir costes en su fabricación. En la capa superior se montarán los componentes y en la capa inferior se enrutarán las pistas necesarias entre ellos.
- Dado que la fabricación de la PCB se realiza mediante fresado de una capa de cobre completa se aprovechará para realizar las pistas lo más anchas posibles con el fin de mejorar la calidad de señales y reducir el tiempo de fabricación de la PCB.
- Se intentará minimizar el uso de vías, dado que el PCB es a una única capa en caso de utilizar vías se designará cono un agujero vacío al que posteriormente se le agregará un cable para la unión del circuito.
- Con el objetivo de supervisar diferentes señales se situarán puntos de test y conmutadores para aislar circuitos en caso de errores.
- En las regiones no ocupadas por pistas se añadirá un plano de masa para reducir interferencias y mejorar las conexiones de masa con los diferentes circuitos.

4.4. Diseño final PCB

Para el diseño final de la PCB se tendrá en cuenta la posición en la placa de componentes críticos como el puerto RJ-11 para la programación del microprocesador, fuente aislada, salidas a drivers y conexiones de referencia en los extremos de la placa para facilitar todo el conexionado.

Con todos los argumentos mencionados el resultado del diseño es el siguiente:

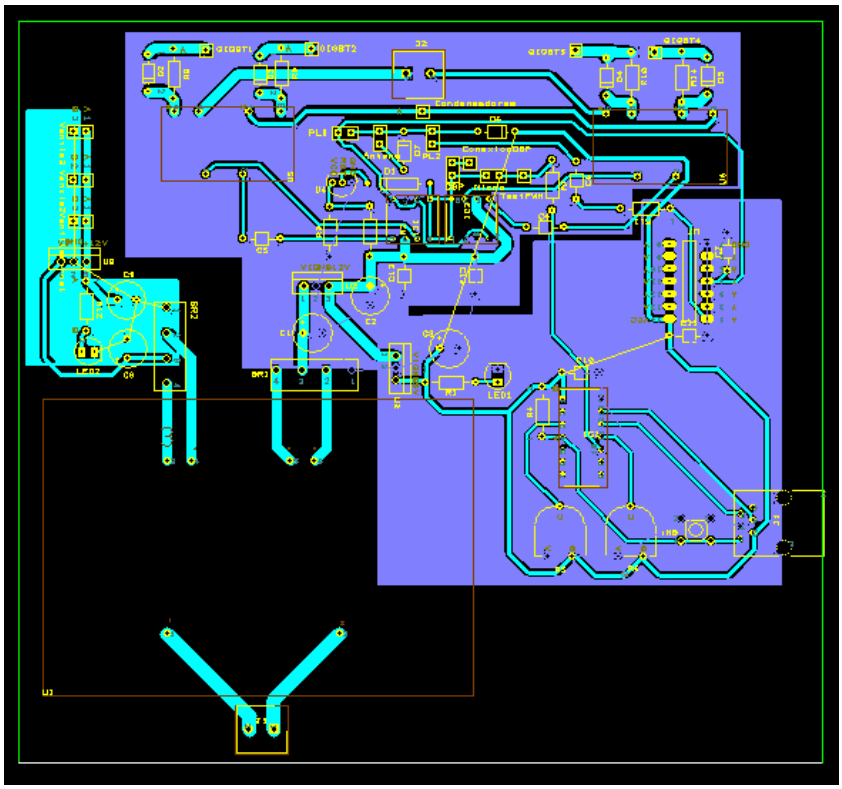


Fig46. PCB Control bobina

Como ya se ha comentado los elementos para una conexión externa se han dispuesto en los extremos de la PCB con el fin de facilitar conexiones.

4.5. Fabricación PCB

Una vez completado el diseño se exportan los archivos de fabricación o archivos GERBER para la fabricación de la PCB en la fresadora CNC de la universidad. La PCB se fresa a partir de una lámina de fibra de vidrio forrada con una lámina de cobre de 35 µm.

Una vez finalizada la fabricación se procede a poblar la PCB con los componentes con los cuales se ha diseñado, el resultado es el siguiente:

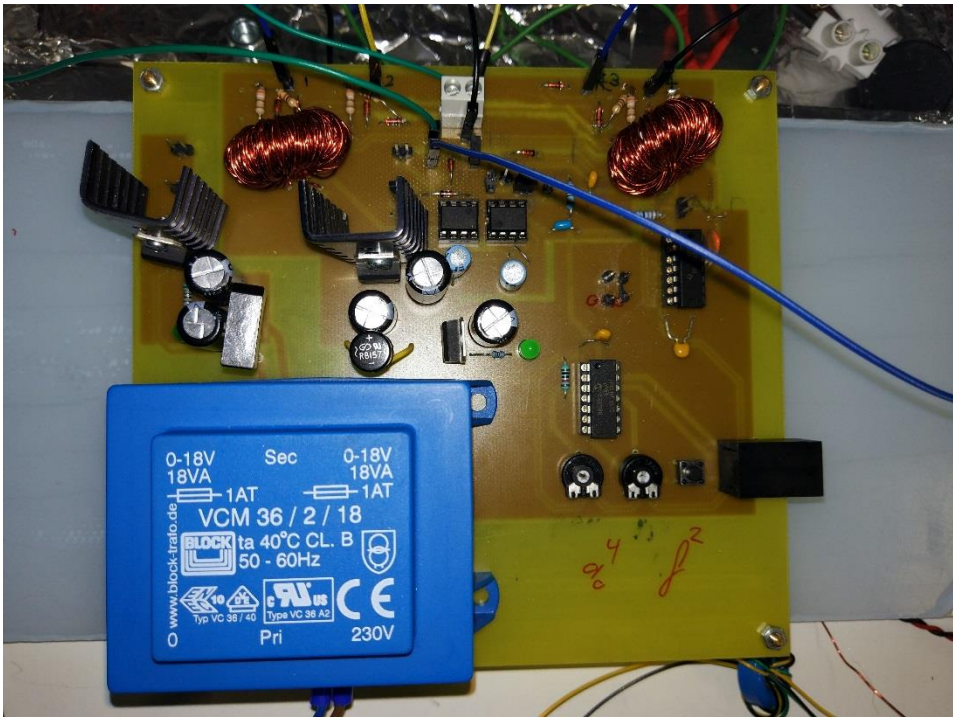


Fig47. PCB bobina poblada

5. Desarrollo e implementación del software

La programación del microprocesador que actuará como interruptor se realizará con el programa MPLABX v4.15. Se trata de un software de la marca "*Microchip*" que se utiliza para la programación de todo tipo de microprocesadores y microcontroladores fabricados por ellos.

El cuerpo del programa está compuesto por un bucle infinito el cual tomará las medidas analógicas necesarias cada ciclo con el fin de refrescar la salida.

Se ha añadido un pequeño offset de funcionamiento con el objetivo de descontinuar el funcionamiento de la bobina mediante software.

La programación completa podrá encontrarse en los anexos adjuntos.

El funcionamiento del programa lo define el siguiente diagrama de flujo:

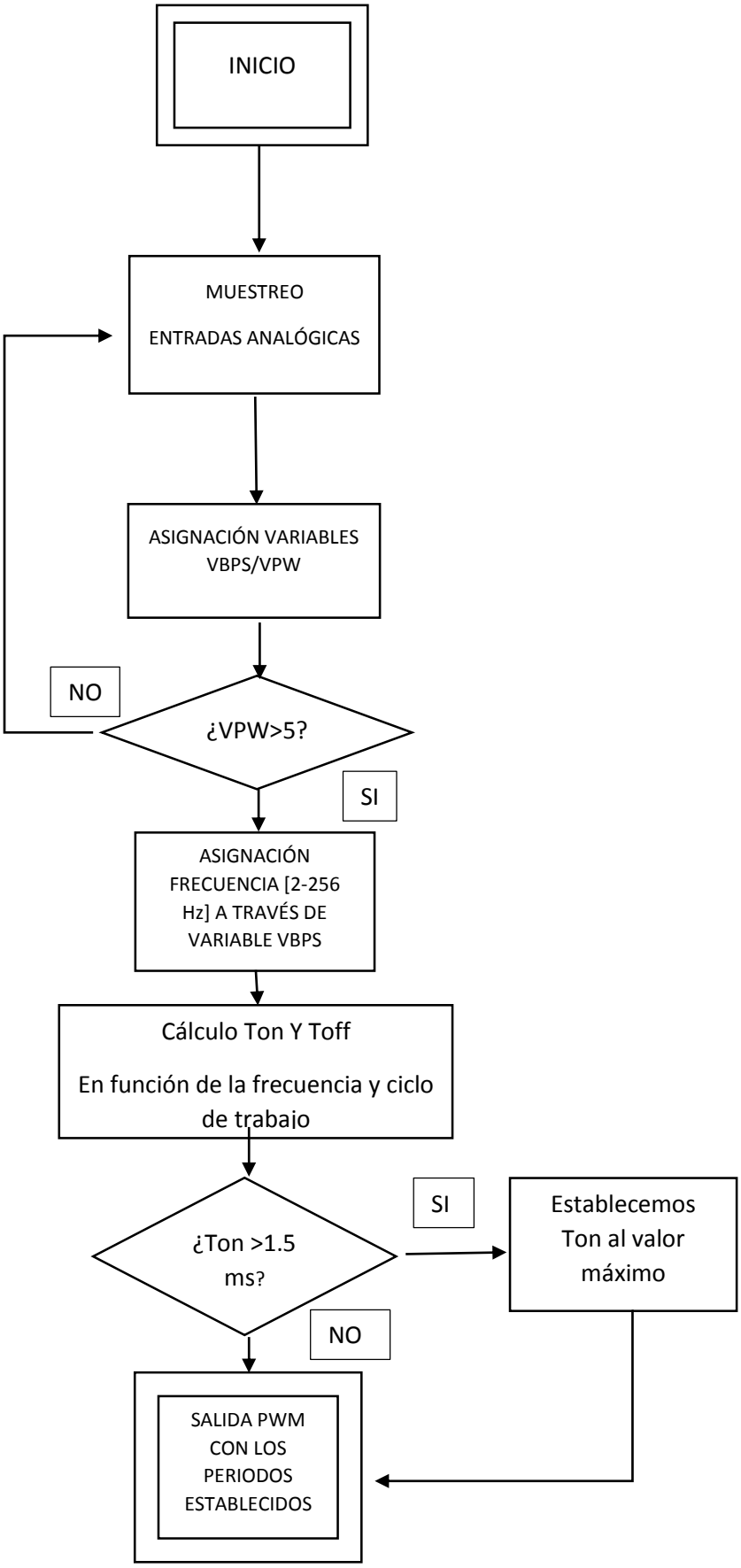


Fig48. Diagrama de flujo interruptor

6. Pruebas de funcionamiento

Con el fin de comprobar el correcto funcionamiento de los diferentes circuitos, se testearán de manera independiente previo ensamblaje final.

6.1. Driver e Interruptor

Con el objetivo de aclarar el funcionamiento del conjunto de driver e interruptor se adjunta la siguiente imagen. En ella se pueden observar dos frecuencias de onda muy diferenciadas, la menor corresponde al interruptor mientras que la mayor corresponde a la frecuencia de conmutación realimentada. La conmutación del inversor solo podrá darse mientras la señal del interruptor se encuentré en estado alto.

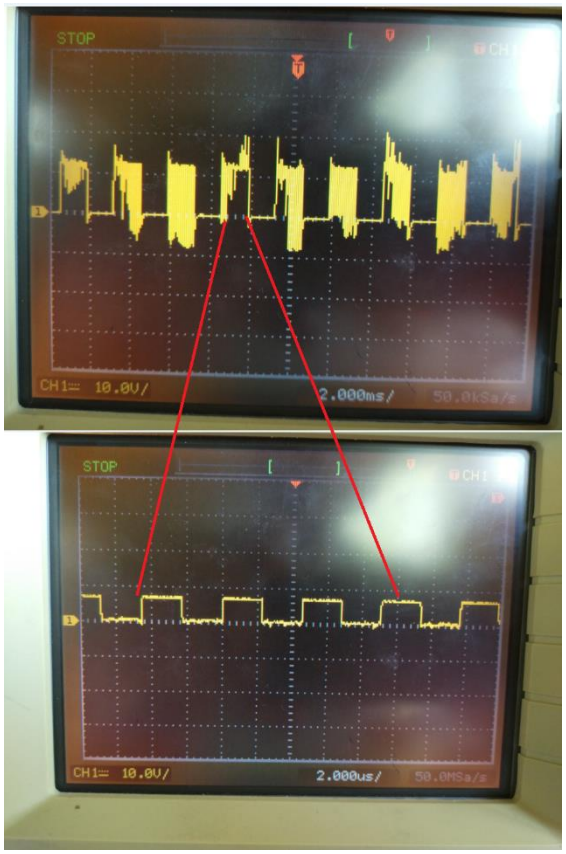


Fig49. Prueba de conmutación

6.2. Conmutación Inversor

A continuación se muestran las tensiones en la conmutación del inversor.

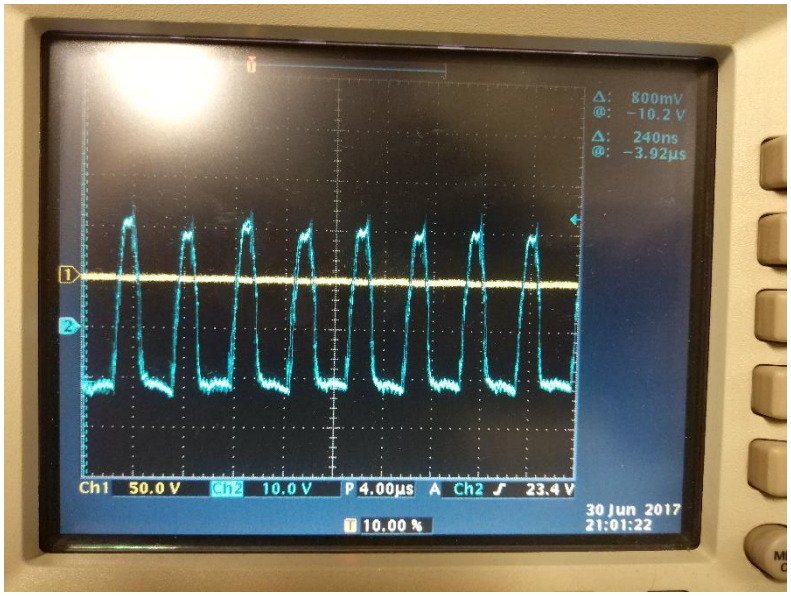


Fig50. Tensión de puerta conmutación inversor (V_{GE})

Se consigue la saturación del semicondutor a + 20 V mientras que la tensión de apertura se reduce a -10 V.

Para completar la visualización de señales del semiconductor se aporta una fotografía de las tensiones entre el colector y emisor conmutado a frecuencia de resonancia y con una tensión de bus de 60 V.

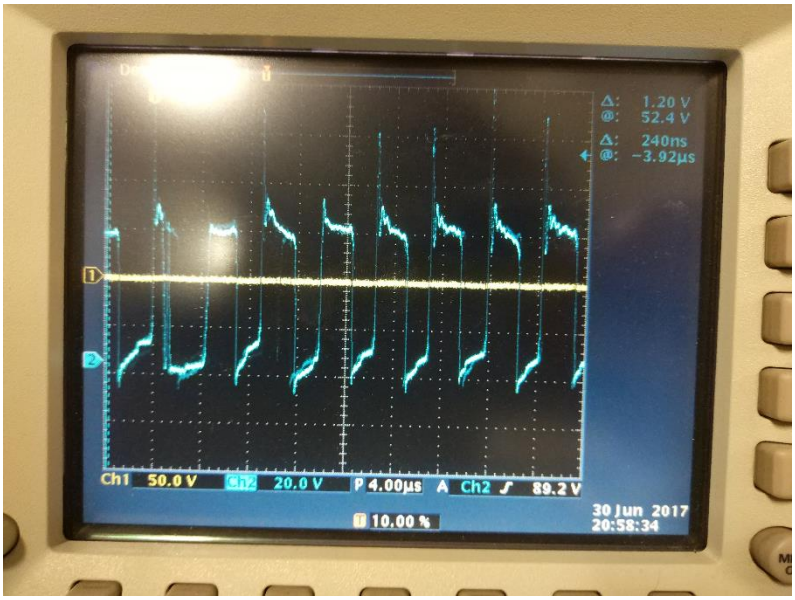


Fig51. Tensión colector-emisor durante la conmutación (V_{CE})

Se aprecia una clara sobretensión la cual es producida por la apertura del transistor y acentuada por la inductancia parásita del conductor que une el bus DC con el colector del transistor. Para intentar amortiguar esta sobretensión se ha diseñado un circuito “snubber” según el anexo A.3. Para evitar que el transistor no sufra sobretensiones que lo puedan dañar o destruir se han colocado unos diodos supresores de tensión entre el colector y emisor de cada transistor, estos diodos amortiguarán el pulso absorbiendo la energía

contenida en él, el modelo elegido es 1.5KE200A, se trataun diodo TVS unidireccional con una tensión residual máxima 274 V. Dos de ellos en serie evitarán que la tensión entre colector y emisor del semiconductor supere los 548 V manteniendo cierto margen de seguridad.

6.3. Funcionamiento Bobina

Con todos los sistemas operativos se procede a la comprobación del funcionamiento del conjunto de la bobina con una tensión DC aplicada directamente en bus de 60 V. Los resultados obtenidos han sido favorables, con unas descargas directas a un conductor conectado a tierra como se muestra a continuación:

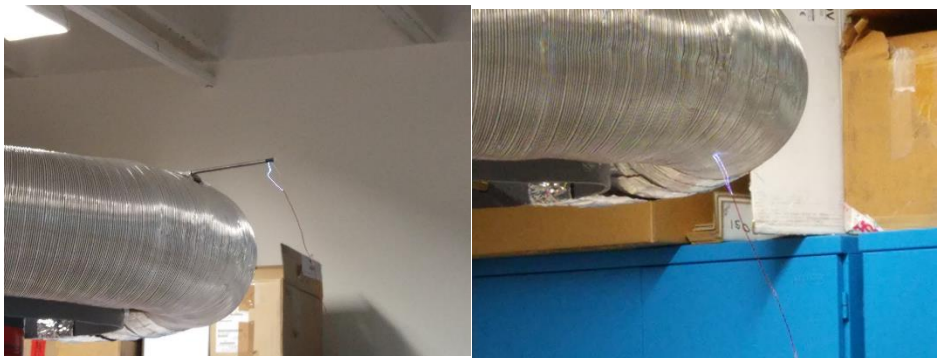


Fig52. Descargas eléctricas bobina 60 V

7. Conclusiones

A continuación se expondrán los objetivos cumplidos en cuanto al diseño y construcción durante la realización de este proyecto.

- Se ha realizado el diseño hardware de una bobina de Tesla conmutada con análisis de cada uno de sus componentes así como de su interacción.
- El diseño del esquema eléctrico de la electrónica ha sido diseñado y desarrollado mediante el software informático DesignSpark para su fabricación en PCB.
- Se ha implementado el diseño en una PCB y se han realizado los montajes y soldaduras para el correcto funcionamiento.
- Se ha conseguido la realimentación a partir de la bobina secundaria para realizar un sistema auto-oscilante.
- Se ha gobernado el control de la bobina mediante un microprocesador el cual tomará las decisiones necesarias para el correcto funcionamiento de la misma.
- Se ha realizado la calibración necesaria de los diferentes componentes para un funcionamiento óptimo.

8. Líneas futuras

Una vez terminado el proyecto, se plantean diferentes líneas para la mejora técnica del prototipo, partiendo del mismo prototipo o de una nueva versión.

8.1. Ampliación de funciones

El proyecto tiene margen de ampliación sobre todo en la funcionalidad de la bobina.

- Reproducción de música: Mediante el cambio del interruptor por un sistema controlador MIDI (Musical Instrument Digital Interface) o DSP (Digital Signal Processor) analizar una señal de música entrante y generar las señales necesarias para la operación de la bobina a la frecuencia de las diferentes notas musicales.
- Generar un sistema doblemente resonante: Mediante la introducción de un condensador primario conseguir que la frecuencia de resonancia del sistema primario y secundario sean similares. Con este cambio se consiguen bobinas mucho más potentes y con descargas mucho más prolongadas.
- Externalizar interruptor: Conseguir la variación del funcionamiento de la bobina mediante un sistema externo a ella operado a distancia de seguridad. La transmisión de este elemento a la bobina se realizará mediante fibra óptica para que el campo electromagnético producido en la operación de la bobina no afecte al correcto funcionamiento del interruptor.

8.2. Mejoras técnicas

En este apartado se discutirá las diferentes mejoras que se le pueden realizar al prototipo una vez construido con el objetivo de economizar el producto y producir mejoras técnicas.

- Construcción PCB de 4 capas: con el objetivo de reducir interferencias por el campo electromagnético creado por las descargas de la bobina secundaria. Se propone la transmisión por las pistas intermedias cubiertas por planos de alimentación y tierra para reducir la radiación absorbida y evitar interferencias.
- Construcción de la PCB con componentes SMD: La sustitución de los componentes de pontaje de orificio pasante por componentes superficiales reducirá el tamaño de la PCB con el consiguiente ahorro económico y tiempo de fabricación.
- Caja metálica: Con el objetivo de evitar interferencias, en próximos prototipos relacionados la caja será metálica para una conexión firme a tierra.

9. Referencias bibliográficas

- https://es.wikipedia.org/wiki/Bobina_de_Tesla#Historia Consultada a día 15 de Mayo de 2018
- http://onetesla.com/products/kits/tinytesla-all/tinytesla-musical-tesla-coil-kit.html Consultada a día 20 de Mayo de 2018
- http://www.loneoceans.com/labs/sstc2/ Consultada a día 26 de Enero de 2018
- http://www.classictesla.com/java/javatc3d/javatc3d.html Consultada a día 26 de Enero de 2018
- Mohan, N., & Undeland, T., & Robbins, W. (2003). Power Electronics (Tercera edición). Estados Unidos: John Wiley & Sons, Inc.

ANEXOS

A.1 Cálculo de potencia disipada IGBT

En este apartado se calcularán las pérdidas producidas por los IGBT en la conmutación del inversor. Se calcula las pérdidas para el caso más desfavorable, con una temperatura del semiconductor de 175 ºC. Para ello se parten de los siguientes datos:

- V_{CE}=325 V
- I_{CE}=20.64 A
- F_{con}=235 kHz
- R_G=3.9 Ω

$$Potencia\ disipada\ conducción = CicloTrabajo * I * V_{CE_{sat(175\ ºC)}}$$

$$Potencia\ disipada\ conducción = 0.5 * 20.64\ A * 1.75\ V = 18\ W$$

$$Potencia\ disipada\ conmutación = (Energía\ encendido + Energía\ apagado) * F_{con}$$

$$E_{on} = E_{on_{ref(175\ ºC)}} * \left(\frac{V_{CE}}{V_{CE_{ref}}}\right)^{1.3} * \left(\frac{I_{CE}}{I_{CE_{ref}}}\right) * K_{RG_{ON}}$$

$$E_{on} = 2.08\ mJ * \left(\frac{325}{400}\right)^{1.3} * \left(\frac{20.64}{60}\right) * 1.05 = 0.5735\ mJ$$

$$E_{off} = E_{off_{ref(175\ ºC)}} * \left(\frac{V_{CE}}{V_{CE_{ref}}}\right)^{1.3} * \left(\frac{I_{CE}}{I_{CE_{ref}}}\right) * K_{RG_{off}}$$

$$E_{off} = 0.78\ mJ * \left(\frac{325}{400}\right)^{1.3} * \left(\frac{20.64}{60}\right) * 1.2 = 0.2458\ mJ$$

$$Potencia\ disipada\ conmutación = (0.5735\ mJ + 0.2458\ mJ) * 235000\ Hz = 192.53\ W$$

$$Potencia\ disipada\ total = 210.53\ W$$

$$La\ potencia\ total\ disipada\ por\ los\ 4\ IGBT\ será\ de\ 842\ W$$

A.2 Cálculo ciclo de trabajo máximo interruptor

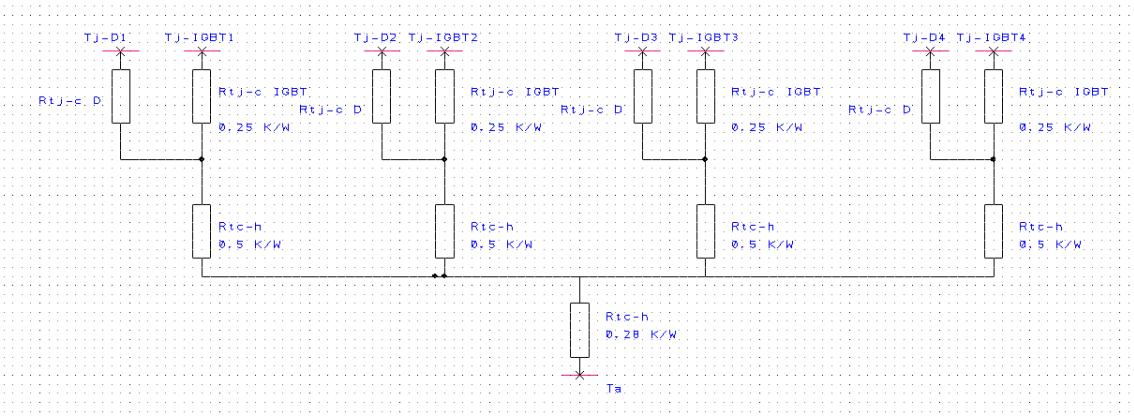


Fig53. Esquema térmico equivalente disipador

Con los siguientes datos de partida se calculará el ciclo de trabajo máximo al cual funcionará en interruptor:

- Temperatura ambiente 25 ºC
- Temperatura interior IGBT 175 ºC
- Potencia de pérdidas de cada IGBT= 211 W

$$T_h = T_a + D * Potencia\ disipada\ total * R_{T_{ha}}$$

$$T_c = T_h + D * Potencia\ disipada\ por\ IGBT * R_{T_{ch}}$$

$$T_{j_{igbt}} = T_c + D * Potencia\ disipada\ por\ IGBT * R_{T_{jc}}$$

T_h: *Temperatura disipador*

T_a: *Temperatura ambiente*

T_c: *Temperatura encapsulado IGBT*

$T_{j_{igbt}}$: *Temperatura unión IGBT*

$R_{T_{ha}}$: *Resistencia térmica disipador-entorno*

$R_{T_{ch}}$: *Resistencia térmica encapsulado-radiador*

$R_{T_{jc}}$: *Resistencia térmica unión-encapsulado*

D: ciclo de trabajo máximo de operación

$$T_{j_{igbt}} = 175\ ºC = 25\ ºC + D * 0.25\ \frac{ºC}{W} * 211W + D * 0.5\ \frac{ºC}{W} * 211W + D * 0.28 \frac{ºC}{W} * 842W$$

$$D = 0.38$$

A.3 Cálculo circuito snubber

Cálculo circuito snubber RC dispuesto entre colector y emisor de cada uno de los IGBT según el documento anexo 7.4.

$$f_{ring0} = \frac{1}{2\pi\sqrt{L_{LK} * C_{LK}}} = 5MHz$$

L_{LK}: Inductancia parásita del circuito

$$C_{LK}: Capacidad\ Colector - Emisor\ IGBT$$

f_{ring0}: Frecuencia de las oscilaciones entre colector y emisor en la conmutación

$$C_{LK} = \frac{C_{add}}{x^2 - 1}$$

C_{add}: Capacidad añadida para determinar la capacidad entre Colector-Emisor IGBT

x: Relación entre f_{ring0} y frecuencia de las oscilaciones con capacidad añadida

$$x = \frac{f_{ring0}}{f_{ring1}}$$

Con una capacidad añadida *C_{add}=3.3 nF* se obtienen unas oscilaciones (*f_{ring1})* a 3.47 MHz.

$$x = \frac{5MHz}{3.47MHz} = 1.44$$

$$C_{LK} = \frac{3.3\ nF}{1.44^2 - 1} = 3.066\ nF$$

$$L_{LK} = \frac{1}{\left(2\pi * f_{ring0}\right)^2 * C_{LK}} = 330.47\ nH$$

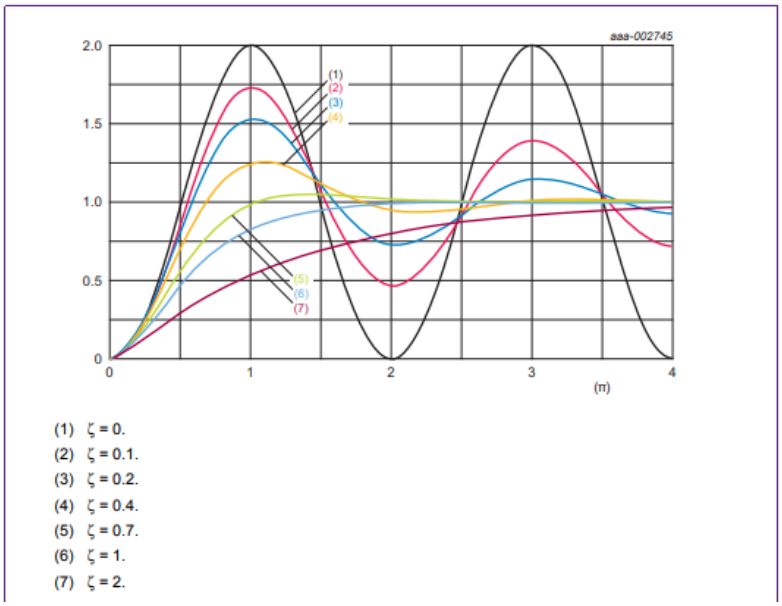


Fig54. Gráfica amortiguación snubber

Con un factor de amortiguamiento ξ=0.7

$$\xi = \frac{1}{2 * Rs} * \sqrt{\frac{L_{LK}}{C_{LK}}} \rightarrow Rs = 7.41\ \Omega$$

En algunos circuitos con la resistencia Rs será suficiente para amortiguar las oscilaciones producidas por la conmutación, sin embargo en la mayoría de circuitos inversores con una única resistencia se estaría cortocircuitando el transistor, es por ello que se añade una capacidad en serie con esta resistencia con el objetivo de evitar este efecto. La capacidad se diseña según la siguiente expresión.

$$C_S = \frac{1}{2\pi * f_{ring0} * R_S} = 4.29\ nF$$

A.4 BOM List (presupuesto)

			Sistema Secundario			
Nº	Cantidad	Unidades	Componente	Marca	Precio unitario (€)	Precio (€)
1	1	MT	Tubo PVC 110	Leroy Merlín	2,7	2,70
2	864	MT	Hilo Cobre Esmaltado AWG 22	Cetronic	0,011	9,50
3	1,72	MT	Conducto alumínio flexible 130mm	Novatub	4,07	7,00
4	2	MT	Varilla de latón roscada	Leroy Merlín	7,13	14,26
5	3	MT	Conductor aislado 750 V cobre 4 mm2	Sumidelec	0,4	1,20
6	1	UD	Plancha metacrilato 6 mm 500mm*500mm	Macoglass	12,39	12,39
7	2	UD	Condensador MKP 6,8 uF 300V	EPCOS	3,61	7,22

			Bloque Lógico			
Nº	Cantidad	Unidades	Componente	Marca	Precio unitario (€)	Precio (€)
8	1	UD	Fuente VCM 36/2/18	Block	21,63	21,63
9	1	UD	Regulador de tensión lineal L7805ACV	STMicroelectronics	0,29	0,29
10	2	UD	Regulador de tensión lineal L7812ACV	STMicroelectronics	1,1	2,2
11	5	UD	Condensador Electrolítico 330uF	RS Pro	0,05	0,25
12	2	UD	Indicador LED Verde	Kingbright	0,2	0,4
13	2	UD	Rectificador en puente monafásico 100 V	Vishay	0,564	1,128
14	2	UD	Terminal de rosca para PCB	Phoenix Contact	0,568	1,136
15	3	UD	Núcleo ferrita EPCOS B64290L0632x839	EPCOS	0,67	2,01
16	1	UD	Buffer Inversor Smith Trigger	Texas Instruments	0,395	0,395
17	2	UD	Driver UCC27425	Texas Instruments	1,996	3,992
18	2	UD	Condensador 47 uF 16 V	RS Pro	0,043	0,086
19	2	UD	Condensador cerámico multicapa 4.7 uF 50 V	Murata	1,154	2,308
20	1	UD	PIC16F1575	Microchip	1,164	1,164
21	2	UD	Potenciómetro PCB 10 kΩ			0
22	1	UD	Supervisor de tensión DS1233-5+	Maxim	1,4	1,4
23	3	UD	Condensador cerámico multicapa 0.1 uF 50 V	KEMET	0,2	0,6
24	8	UD	Diodo Zener 18 V 0.5 W	Nexperia	0,1	0,8
25	4	UD	Resistencia fija 3.9 Ω 1W	RS Pro	0,012	0,048

26	7	UD	Diodo Conmutación 1N4148	Taiwan Semiconductor	0,012	0,084
27	1	UD	Resistencia fija 1 kΩ 1W	RS Pro	0,012	0,012
28	1	UD	Resistencia fija 10 kΩ 1W	RS Pro	0,011	0,011
29	1	UD	Condensador Cerámico 100 pF	Murata	0,135	0,135

			Inversor			
Nº	Cantidad	Unidades	Componente	Marca	Precio unitario (€)	Precio (€)
30	4	UD	IGBT FGA60N65SMD	ON Semiconductor	3,85	15,40
31	2	UD	Condensador Aluminio 1.2 mF 450 V ALS70A122DF450	KEMET	19,13	38,26
32	1	UD	Rectificador monofásico 600 V 25 A KBPC2506	HY Electronic Corp	0,93	0,93
33	2	MT	Conductor aislado 750 V cobre 4 mm2	Sumidelec	0,4	0,80
34	1	UD	Termistor NTC MS 32 20010	Ametherm	3,7	3,70
35	1	UD	Disipador térmico Semikron P38/300A, 300 x 200 x 40mm	Semikron	69,45	69,45
36	8	UD	Diodo TVS Unidireccional 1.5KE200A 1500 W	STMicroelectronics	0,386	3,09

			Caja Madera			
Nº	Cantidad	Unidades	Componente	Marca	Precio unitario (€)	Precio (€)
37	1	UD	Recinto madera 390 x 300 x 300	Leroy Merlín	30,02	30,02
38	1	UD	Cinta adhesiva aluminio 50 x 50 m	3M	11,14	11,14
39	1	UD	Rollo papel albal cocina	Albal	2,23	2,23
40	1	UD	Conector IEC Macho 15 A 250 V	TE Connectivity	3,39	3,39
41	2	UD	Ventilador Axial 12 V	Sunon	2,94	5,88

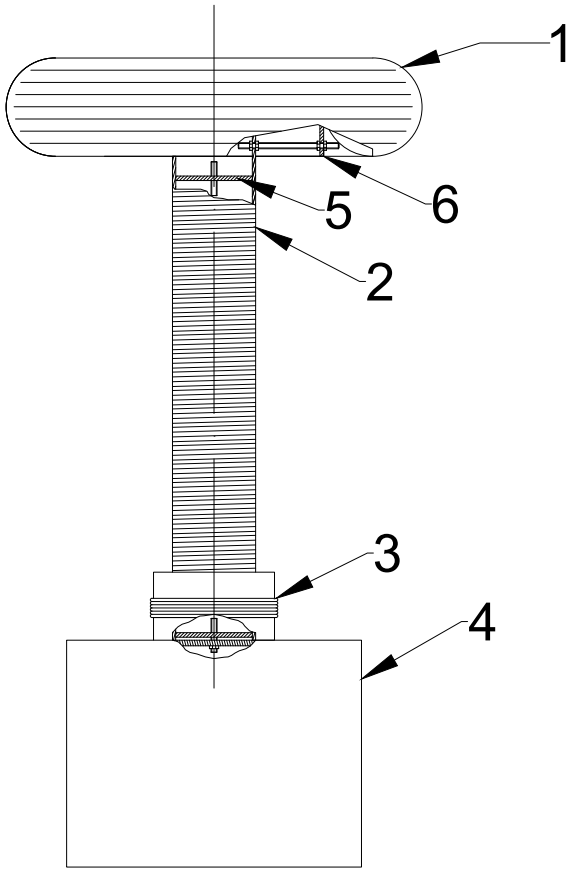
Presupuesto Ejecución Material (€)	278,64
IVA (21%)	58,51
Presupuesto Ejecución Material Total (€)	337,16

A.5 Programa Interruptor

```
/*
 * File:   newmain.c
 * Author: Ivan
 *
 * Created on 22 de marzo de 2018, 16:49
 */

// PIC16F1575 Configuration Bit Settings

// 'C' source line config statements

// CONFIG1
#pragma config FOSC = INTOSC    // Oscillator Selection Bits (INTOSC oscillator; I/O function on CLKIN pin)
#pragma config WDTE = OFF       // Watchdog Timer Enable (WDT disabled)
#pragma config PWRTE = OFF      // Power-up Timer Enable (PWRT disabled)
#pragma config MCLRE = ON       // MCLR Pin Function Select (MCLR/VPP pin function is MCLR)
#pragma config CP = OFF         // Flash Program Memory Code Protection (Program memory code protection is disabled)
#pragma config BOREN = ON       // Brown-out Reset Enable (Brown-out Reset enabled)
#pragma config CLKOUTEN = OFF   // Clock Out Enable (CLKOUT function is disabled. I/O or oscillator function on the CLKOUT pin)

// CONFIG2
#pragma config WRT = OFF        // Flash Memory Self-Write Protection (Write protection off)
#pragma config PPS1WAY = ON     // PPSLOCK bit One-Way Set Enable bit (PPSLOCKED Bit Can Be Cleared & Set Once)
#pragma config PLLEN = ON       // PLL Enable (4x PLL enabled)
#pragma config STVREN = ON      // Stack Overflow/Underflow Reset Enable (Stack Overflow or Underflow will cause a Reset)
#pragma config BORV = LO        // Brown-out Reset Voltage Selection (Brown-out Reset Voltage (Vbor), low trip point selected.)
#pragma config LPBOREN = OFF    // Low Power Brown-out Reset enable bit (LPBOR is disabled)
#pragma config LVP = OFF        // Low-Voltage Programming Enable (High-voltage on MCLR/VPP must be used for programming)

// #pragma config statements should precede project file includes.
// Use project enums instead of #define for ON and OFF.

#include <xc.h>
#include <math.h>
#define _XTAL_FREQ 32000000

//Declaracion de variables
int maxontime = 1500;//Maximo tiempo On en us
float duty = 0.1;//Maximo ciclo de trabajo
int offsetapagado = 5;//Numero de LSB para considerar la bobina apagada
int maxfreq;          //Uso futuro

//Inicio variables a usar
unsigned long int ontime = 0;//us en alto de la señal PWM
unsigned long int offtime = 0;//us en bajo de la señal PWM
int freq;//insertare la frecuencia correspondiente a partir de variables analógicas
unsigned long int period;//inverso de frecuencia

int vpw;//guardaremos el ancho del pulso en 10 bits
int vbps;//Guardaremos la frecuencia o beeps per second en 10 bits
int i;//Variable auxiliar que se utilizará en los bucles delay
```

```
void main(void) {
    //Configuracion de registros
    OSCCON = 0b11110000;//Frecuencia del Oscilador interno de 32 MHz
TRISA = 0b00011100;//RA2 y RA4 como entradas analogicas
ANSELA = 0b00010100;//RA4 y RA2 como entrada analógica, se deberá multiplexar el CAD
TRISC = 0b00000000;//RC0 como salida en este caso digital
ADCON1 = 0b11110000;//Configuración del CAD selección de modo de guardado de datos de conversión
while(1){
    //Lectura de entradas analogicas
    ADCON0 = 0b00001101;//Establezco la entrada a consultar en este caso RA4 o AN3
    __delay_us(40);//Espero para posibles rebotes y una conversion nitida
    ADCON0bits.GO=1;//Una vez cargado el condensador del circuito S&H empiezo la conversión
    while(ADCON0bits.GO==1);//Espero hasta que acabe el conversor y se active el bit DONE a 0
    vpw = 256*ADRESH + ADRESL - offsetapagado;//Asigno la variable ancho de pulso

    ADCON0 = 0b00001001;//Establezco la entrada a consultar en este caso RA2 o AN2
    __delay_us(40);//Espero para posibles rebotes y una conversion nitida,mirar bien
    ADCON0bits.GO=1;
    while(ADCON0bits.GO==1);
    vbps = 256*ADRESH + ADRESL;//Asigno la variable frecuencia

    ADCON0bits.ADON=0;//Apago conversor hasta siguiente ciclo


    if (vpw<0)      //En caso de queres apagar la bobina usar el potenciometro de ancho de pulso, pequeño offset por imperfecciones del p
    {LATC = 0b00000000;
    __delay_us(40);
    }
    else
    {
        //asigno frecuencia
        freq = 1+(vbps+4)/4;//Escala de 2 a 256 HZ
        ontime = (vpw*duty/1018)*(1000000/freq);//Establezco el ton del pùlso en us en funcion de frecuencia y ciclo de trabajo
        period = (1000000/freq);//Establezco el periodo total de la señal en us
        if(ontime>=maxontime)
        {ontime = maxontime;//En caso de ontime supere al tiempo maximo se reduce al maximo
        }
        offtime = period - ontime;//tiempo en off en us
        LATC = 0b00000001;//Salida RC0 a 1 durante el ton

        ontime=ontime/10; //Escalo el tiempo para reducir en número de ciclos de bucle
        offtime=offtime/10;
        i=0;
        while(i<ontime) //Bucle señal PWM en alto
        {//__delay(1);
        i++;
        __delay_us(10);
        }

        LATC = 0b00000000;//Salida RC0 a 0 durante el toff
        i=0;
        while(i<offtime)    //Bucle señal PWM en bajo
        {//__delay(1);
        i++;
        __delay_us(10);
        }
    }
    }
    }
```

Fig55. Programa microprocesador



PIEZA	DESCRIPCIÓN	UNIDADES
1	TOROIDE ALUMINIO	1
2	BOBINA SECUNDARIA	1
3	BOBINA PRIMARIA	1
4	RECINTO CONTENEDOR	1
5	AMARRES BOBINA SECUNDARIA	2
6	AMARRE TOROIDE	1

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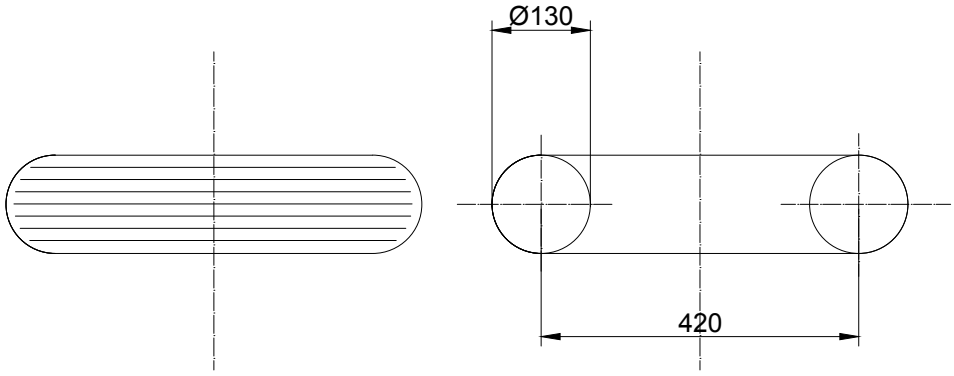
PROYECTO: **BOBINA DE TESLA CONMUTADA**		REALIZADO: **GARNICA ARCE,IVÁN**
		FIRMA:

PLANO:	FECHA:	ESCALA:	Nº PLANO:
PLANO GENERAL COMPONENTES	31/5/2018	1:10	1

1



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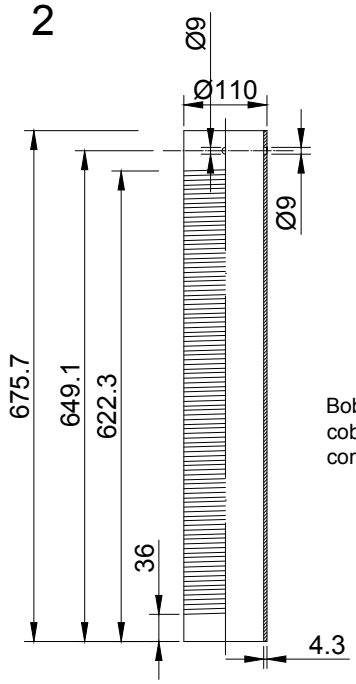

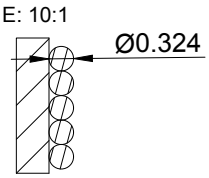

Bobinado secundario compuesto por cobre esmaltado AWG 22. La bobina la componen 980 vueltas

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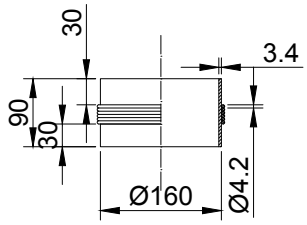
PROYECTO: **BOBINA DE TESLA CONMUTADA**		REALIZADO: **GARNICA ARCE,IVÁN**
		FIRMA:

PLANO:	FECHA:	ESCALA:	Nº PLANO:
PLANO TOROIDE Y BOBINA SECUNDARIA	31/5/2018	1:10	2

3



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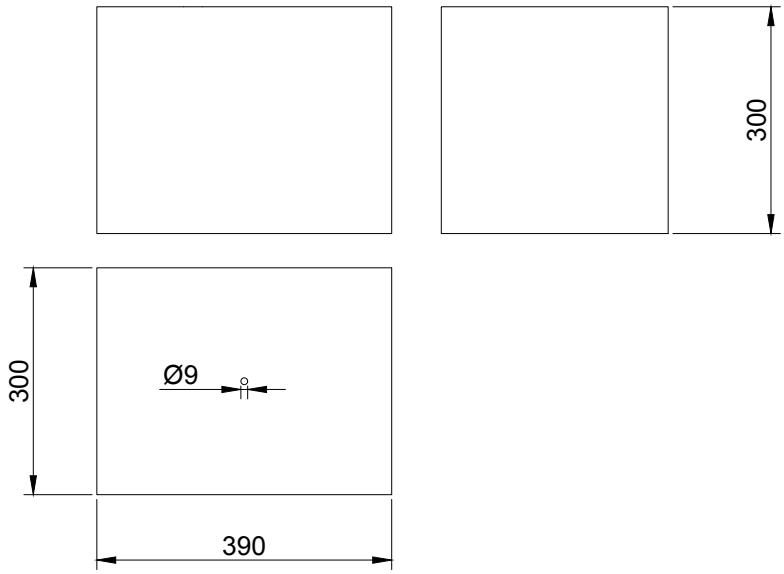

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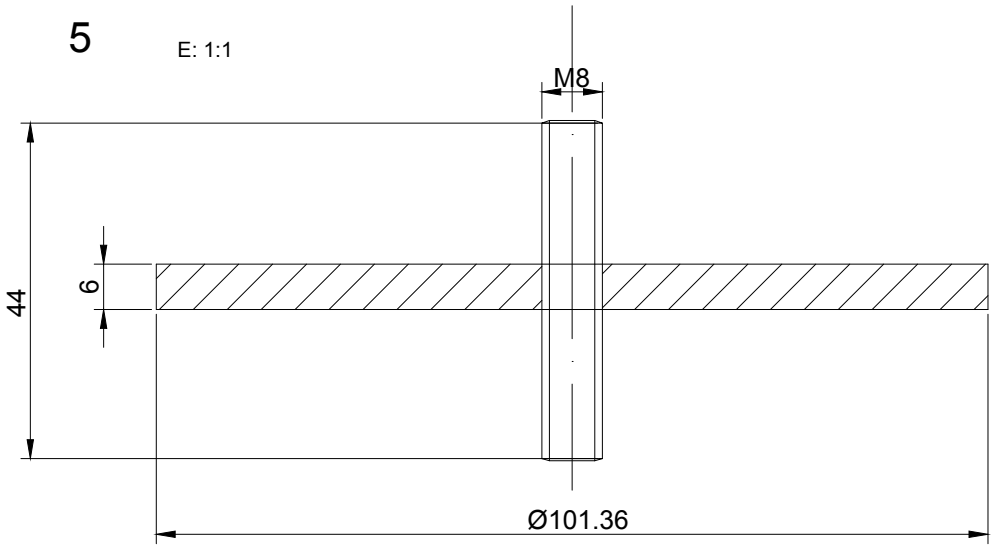
PROYECTO: **BOBINA DE TESLA CONMUTADA**		REALIZADO: **GARNICA ARCE,IVÁN**
		FIRMA:
PLANO: **PLANO BOBINA PRIMARIA Y CONTENEDOR**		FECHA: 31/5/2018 / ESCALA: 1:10 / Nº PLANO: 3

5 E: 1:1



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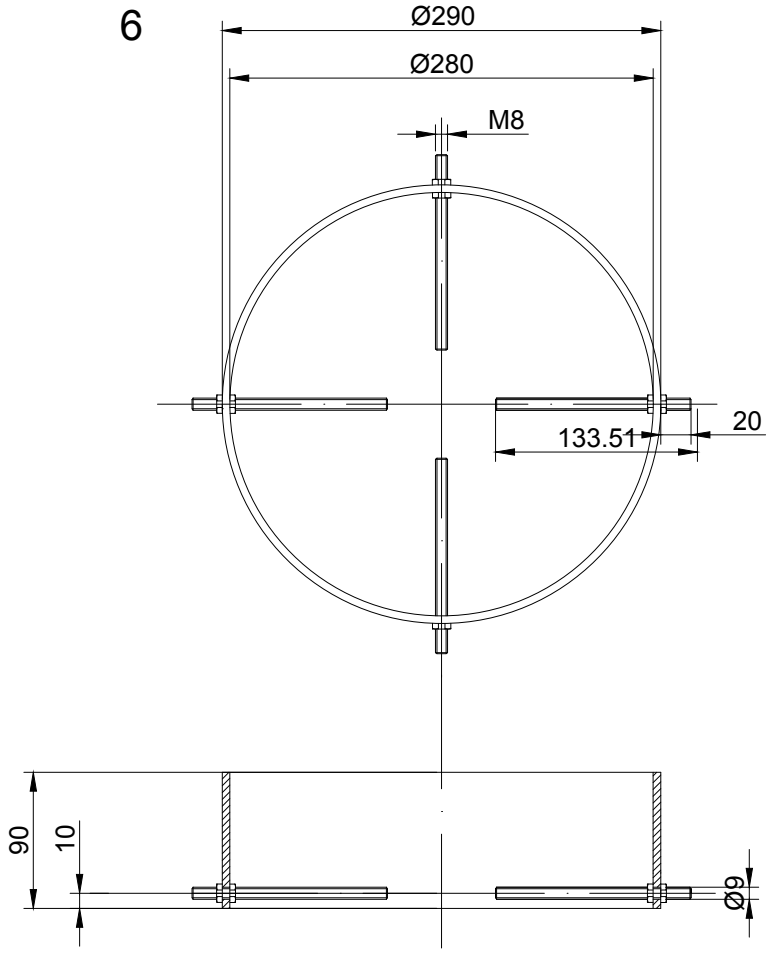

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PROYECTO: **BOBINA DE TESLA CONMUTADA**		REALIZADO: **GARNICA ARCE,IVÁN**
		FIRMA:

PLANO:	FECHA:	ESCALA:	Nº PLANO:
PLANO AMARRES BOBINA Y TOROIDE	31/5/2018	1:5	4

FAIRCHILD SEMICONDUCTOR®

October 2013

FGA60N65SMD
650 V, 60 A Field Stop IGBT

Features

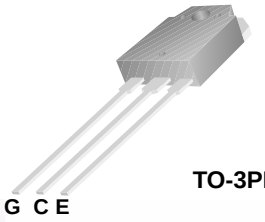
- Maximum Junction Temperature : $T_J = 175^oC$
- Positive Temperature Co-efficient for Easy Parallel Operating
- High Current Capability
- Low Saturation Voltage: $V_{CE(sat)}$ = 1.9 V(Typ.) @ I_C = 60 A
- Fast Switching : E_{OFF} = 7.5 uJ/A
- Tighten Parameter Distribution
- RoHS Compliant

Applications

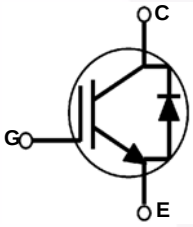
- Solar Inverter, UPS, Welder, PFC, Telecom, ESS

General Description

Using novel field stop IGBT technology, Fairchild's new series of field stop 2nd generation IGBTs offer the optimum performance for solar inverter, UPS, welder, telecom, ESS and PFC applications where low conduction and switching losses are essential.



TO-3PN



Absolute Maximum Ratings

Symbol	Description		Ratings	Unit
V_{CES}	Collector to Emitter Voltage		650	V
V_{GES}	Gate to Emitter Voltage		± 20	V
	Transient Gate to Emitter Voltage		± 30	V
I_C	Collector Current	@ $T_C = 25^oC$	120	A
	Collector Current	@ $T_C = 100^oC$	60	A
$I_{CM\ (1)}$	Pulsed Collector Current		180	A
I_F	Diode Forward Current	@ $T_C = 25^oC$	60	A
	Diode Forward Current	@ $T_C = 100^oC$	30	A
$I_{FM\ (1)}$	Pulsed Diode Maximum Forward Current		180	A
P_D	Maximum Power Dissipation	@ $T_C = 25^oC$	600	W
	Maximum Power Dissipation	@ $T_C = 100^oC$	300	W
T_J	Operating Junction Temperature		-55 to +175	^oC
T_{stg}	Storage Temperature Range		-55 to +175	^oC
T_L	Maximum Lead Temp. for soldering Purposes, 1/8" from case for 5 seconds		300	^oC

Notes:
1: Repetitive rating: Pulse width limited by max. junction temperature

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JC}$(IGBT)	Thermal Resistance, Junction to Case	-	0.25	$^oC/W$
$R_{\theta JC}$(Diode)	Thermal Resistance, Junction to Case	-	1.1	$^oC/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	-	40	$^oC/W$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FGA60N65SMD	FGA60N65SMD	TO-3PN	-	-	30

Electrical Characteristics of the IGBT T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{CES}	Collector to Emitter Breakdown Voltage	V_{GE} = 0V, I_C = 250μA	650	-	-	V
$\frac{\Delta BV_{CES}}{\Delta T_J}$	Temperature Coefficient of Breakdown Voltage	V_{GE} = 0V, I_C = 250μA	-	0.6	-	$V/^oC$
I_{CES}	Collector Cut-Off Current	V_{CE} = V_{CES}, V_{GE} = 0V	-	-	250	μA
I_{GES}	G-E Leakage Current	V_{GE} = V_{GES}, V_{CE} = 0V	-	-	±400	nA
On Characteristics						
$V_{GE(th)}$	G-E Threshold Voltage	I_C = 250μA, V_{CE} = V_{GE}	3.5	4.5	6.0	V
$V_{CE(sat)}$	Collector to Emitter Saturation Voltage	I_C = 60A, V_{GE} = 15V	-	1.9	2.5	V
		I_C = 60A, V_{GE} = 15V, T_C = 175°C	-	2.1	-	V
Dynamic Characteristics						
C_{ies}	Input Capacitance	V_{CE} = 30V, V_{GE} = 0V, f = 1MHz	-	2915	-	pF
C_{oes}	Output Capacitance		-	270	-	pF
C_{res}	Reverse Transfer Capacitance		-	85	-	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{CC} = 400V, I_C = 60A, R_G = 3Ω, V_{GE} = 15V, Inductive Load, T_C = 25°C	-	18	27	ns
t_r	Rise Time		-	47	70	ns
$t_{d(off)}$	Turn-Off Delay Time		-	104	146	ns
t_f	Fall Time		-	50	68	ns
E_{on}	Turn-On Switching Loss		-	1.54	2.31	mJ
E_{off}	Turn-Off Switching Loss		-	0.45	0.60	mJ
E_{ts}	Total Switching Loss		-	1.99	2.91	mJ
$t_{d(on)}$	Turn-On Delay Time	V_{CC} = 400V, I_C = 60A, R_G = 3Ω, V_{GE} = 15V, Inductive Load, T_C = 175°C	-	18	-	ns
t_r	Rise Time		-	41	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	115	-	ns
t_f	Fall Time		-	48	-	ns
E_{on}	Turn-On Switching Loss		-	2.08	-	mJ
E_{off}	Turn-Off Switching Loss		-	0.78	-	mJ
E_{ts}	Total Switching Loss		-	2.86	-	mJ

Electrical Characteristics of the IGBT (Continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max	Unit
Q_g	Total Gate Charge	V_{CE} = 400V, I_C = 60A, V_{GE} = 15V	-	189	284	nC
Q_{ge}	Gate to Emitter Charge		-	20	30	nC
Q_{gc}	Gate to Collector Charge		-	91	137	nC

Electrical Characteristics of the Diode T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Min.	Typ.	Max	Unit
V_{FM}	Diode Forward Voltage	I_F = 30A	T_C = 25°C	-	2.1	2.6	V
			T_C = 175°C	-	1.7	-	
E_{rec}	Reverse Recovery Energy	I_F =30A, dI_F/dt = 200A/µs	T_C = 175°C	-	127	-	uJ
t_{rr}	Diode Reverse Recovery Time		T_C = 25°C	-	47	-	ns
			T_C = 175°C	-	212	-	
Q_{rr}	Diode Reverse Recovery Charge		T_C = 25°C	-	87	-	nC
			T_C = 175°C	-	933	-	

Typical Performance Characteristics

Figure 1. Typical Output Characteristics

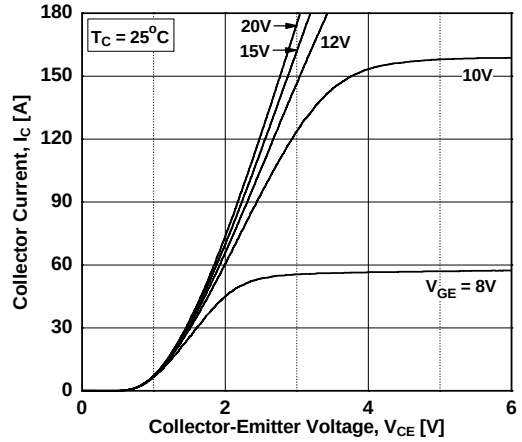


Figure 2. Typical Output Characteristics

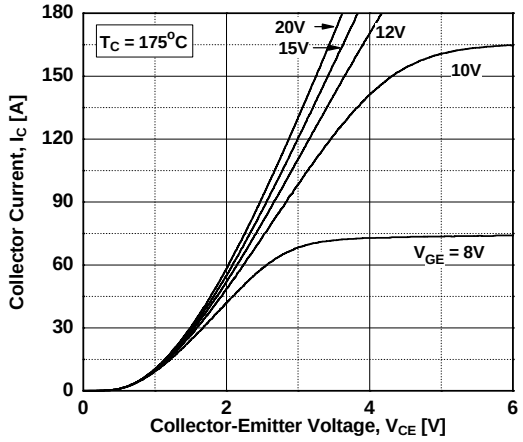


Figure 3. Typical Saturation Voltage Characteristics

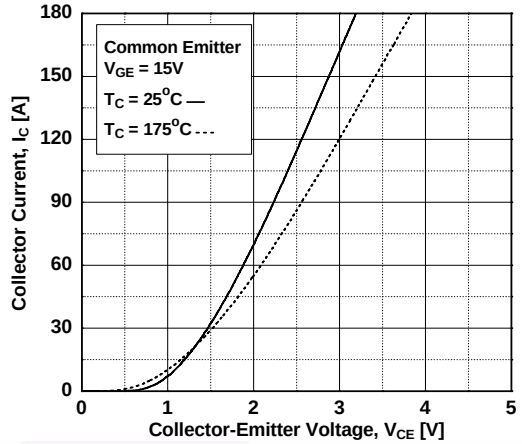


Figure 4. Saturation Voltage vs. Case Temperature at Variant Current Level

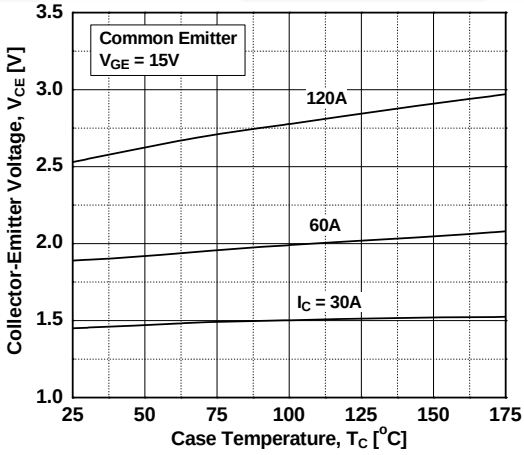


Figure 5. Saturation Voltage vs. V_{GE}

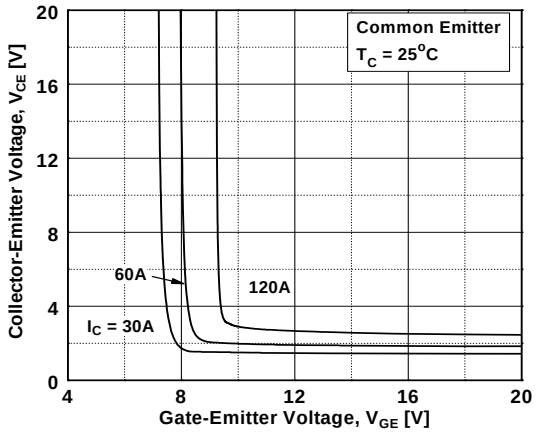
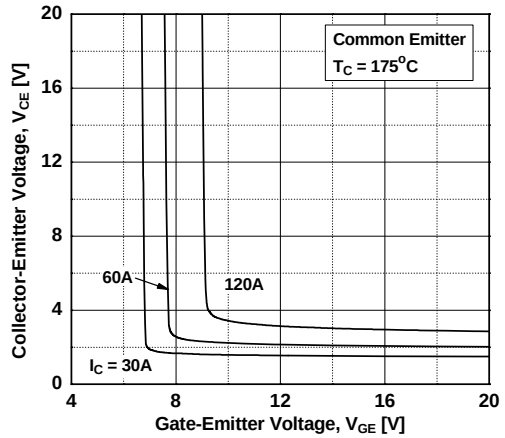


Figure 6. Saturation Voltage vs. V_{GE}



Typical Performance Characteristics

Figure 7. Capacitance Characteristics

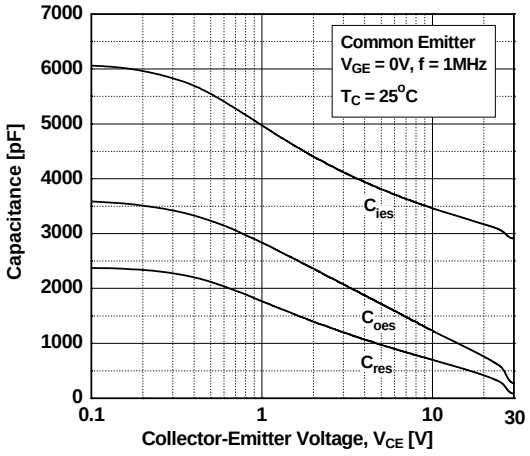


Figure 8. Gate charge Characteristics

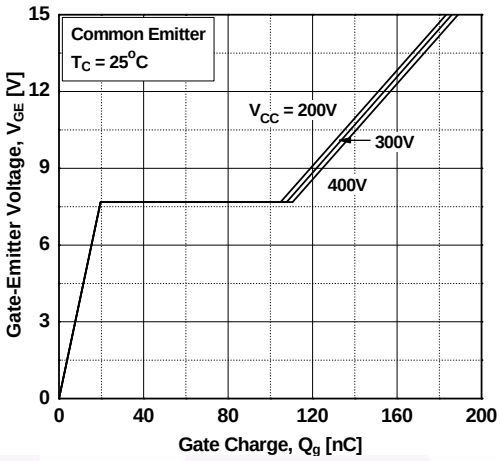


Figure 9. Turn-on Characteristics vs. Gate Resistance

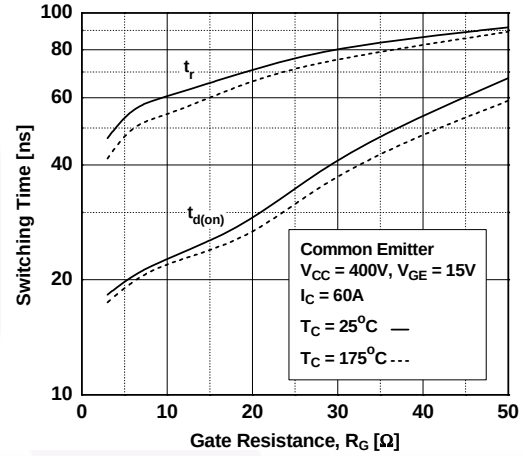


Figure 9. Turn-off Characteristics vs. Gate Resistance

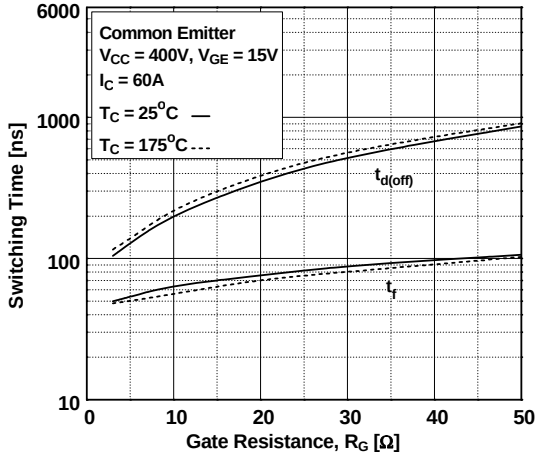


Figure 11. Switching Loss vs. Gate Resistance

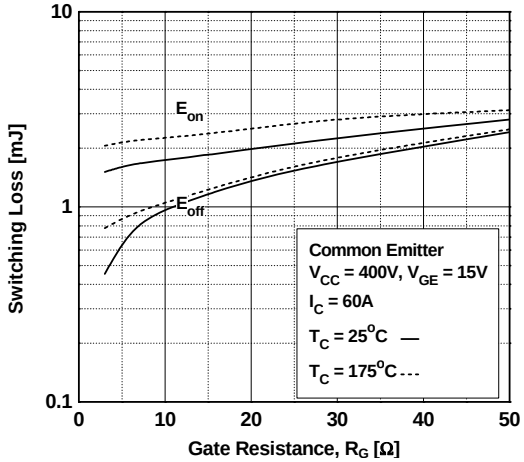
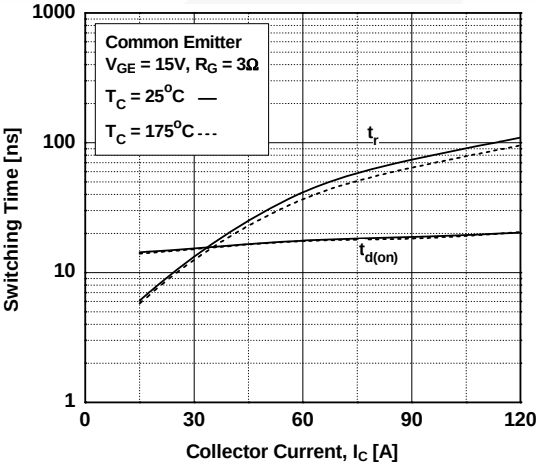


Figure 12. Turn-on Characteristics vs. Collector Current



Typical Performance Characteristics

Figure 13. Turn-off Characteristics vs. Collector Current

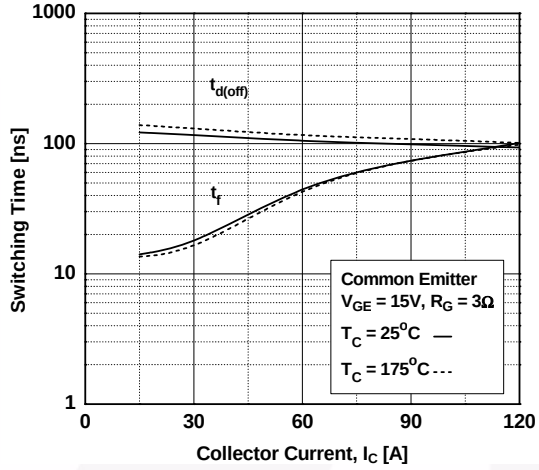


Figure 14. Switching Loss vs.. Collector Current

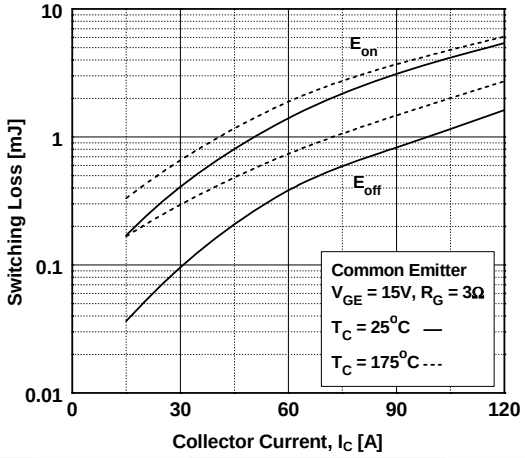


Figure 15. Load Current Vs. Frequency

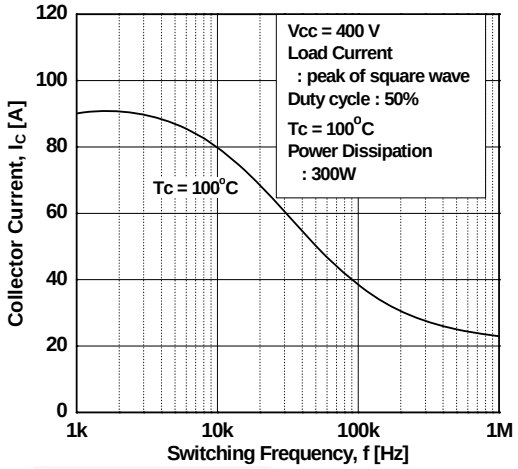


Figure 16. SOA Characteristics

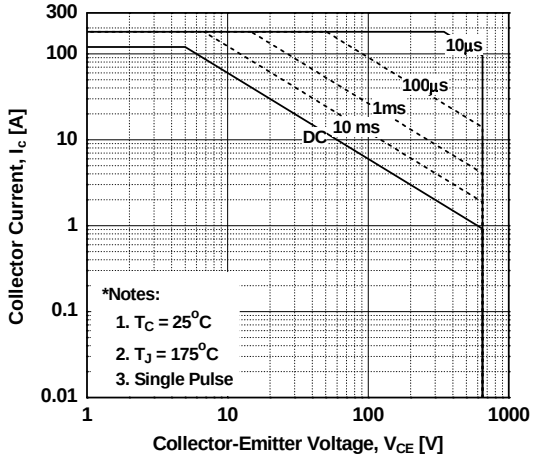


Figure 17. Forward Characteristics

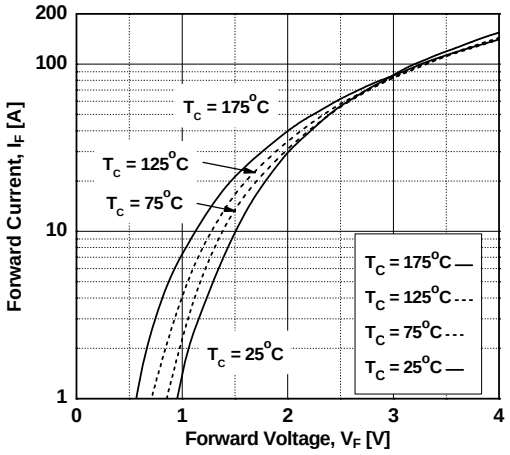
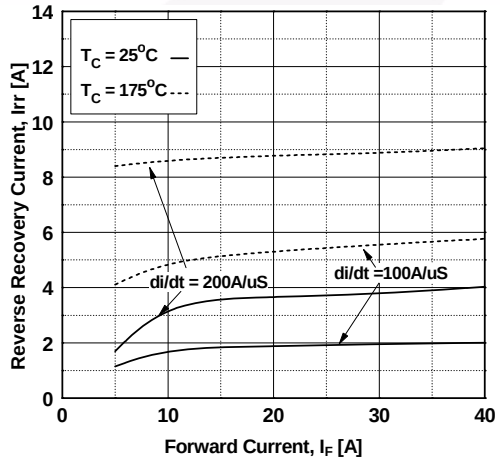


Figure 18. Reverse Recovery Current



Typical Performance Characteristics

Figure 19. Reverse Recovery Time

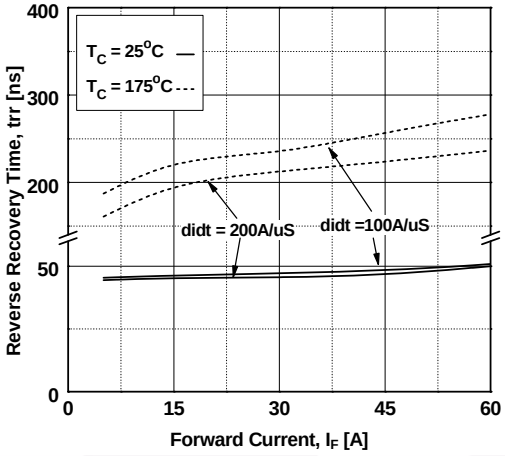


Figure 20. Stored Charge

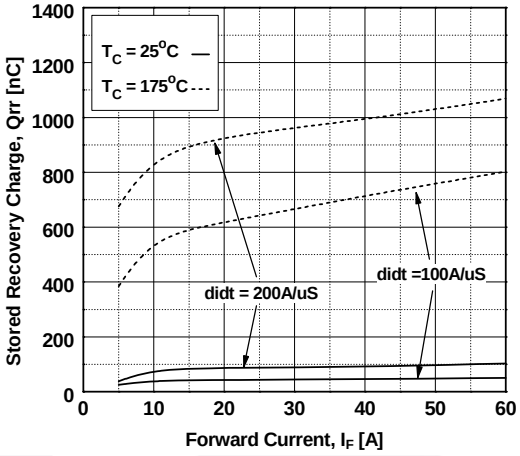


Figure 21.Transient Thermal Impedance of IGBT

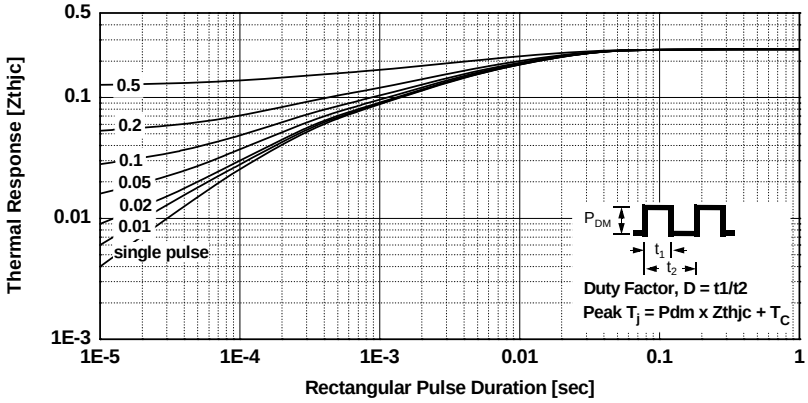
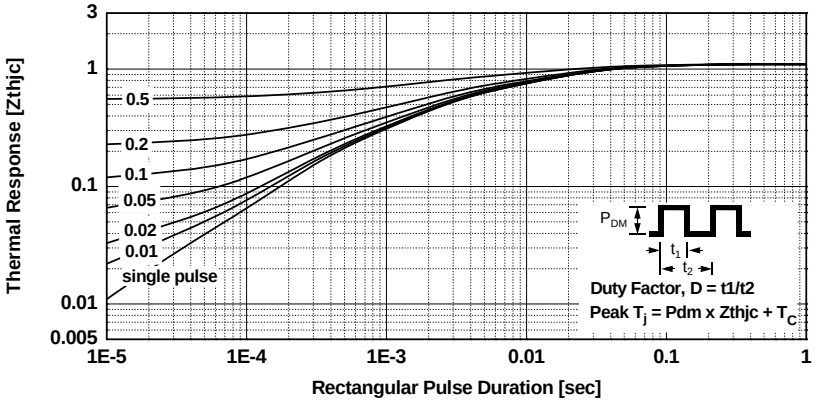


Figure22.TransientThermalImpedanceofDiode



Mechanical Dimensions

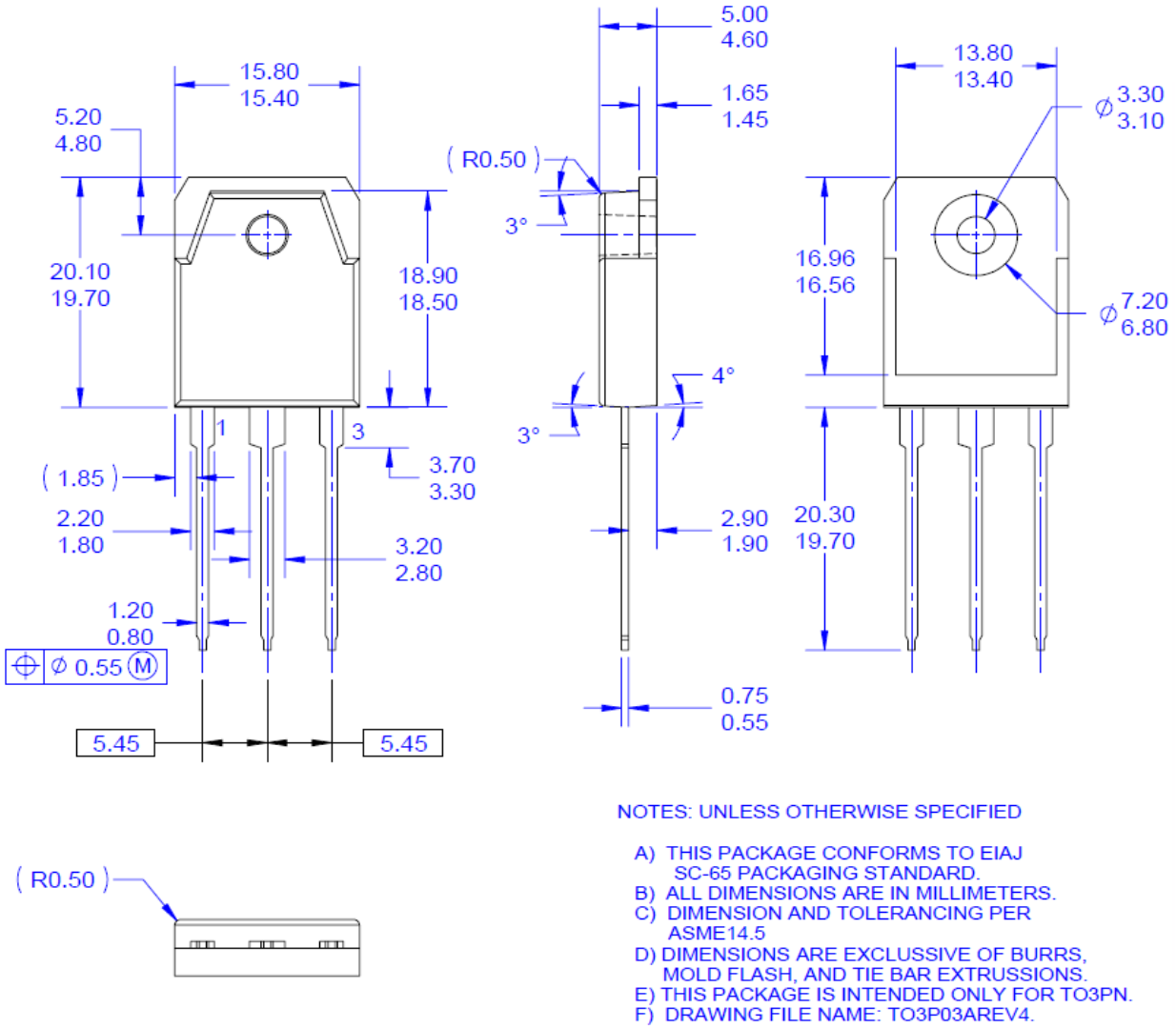


Figure 20. TO-3P 3L - 3LD, T03, PLASTIC, EIAJ SC-65

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Dimensions in Millimeters

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I66

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FGA60N65SMD

UCC2742x Dual 4-A High Speed Low-Side MOSFET Drivers With Enable

1 Features

- Industry-Standard Pin-Out
- Enable Functions for Each Driver
- High Current Drive Capability of ±4 A
- Unique BiPolar and CMOS True Drive Output Stage Provides High Current at MOSFET Miller Thresholds
- TTL/CMOS Compatible Inputs Independent of Supply Voltage
- 20-ns Typical Rise and 15-ns Typical Fall Times with 1.8-nF Load
- Typical Propagation Delay Times of 25 ns with Input Falling and 35 ns with Input Rising
- 4-V to 15-V Supply Voltage
- Dual Outputs Can Be Paralleled for Higher Drive Current
- Available in Thermally Enhanced MSOP PowerPAD™ Package
- Rated From –40°C to 125°C

2 Applications

- Switch Mode Power Supplies
- DC/DC Converters
- Motor Controllers
- Line Drivers
- Class D Switching Amplifiers

3 Description

The UCC2742x family of high-speed dual MOSFET drivers can deliver large peak currents into capacitive loads. Three standard logic options are offered – dual-inverting, dual-noninverting, and one-inverting and one-noninverting driver. The thermally enhanced 8-pin PowerPAD™ MSOP package (DGN) drastically lowers the thermal resistance to improve long-term reliability. It is also offered in the standard SOIC-8 (D) or PDIP-8 (P) packages.

Using a design that inherently minimizes shoot-through current, these drivers deliver 4A of current where it is needed most at the Miller plateau region during the MOSFET switching transition. A unique BiPolar and MOSFET hybrid output stage in parallel also allows efficient current sourcing and sinking at low supply voltages.

The UCC2742x provides enable (ENB) functions to have better control of the operation of the driver applications. ENBA and ENBB are implemented on pins 1 and 8 which were previously left unused in the industry standard pin-out. They are internally pulled up to V_{DD} for active high logic and can be left open for standard operation.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC27423 UCC27424 UCC27425	SOIC (8)	4.90 mm × 3.91 mm
	MSOP-PowerPAD (8)	3.00 mm × 3.00 mm
	PDIP (8)	9.81 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Diagram

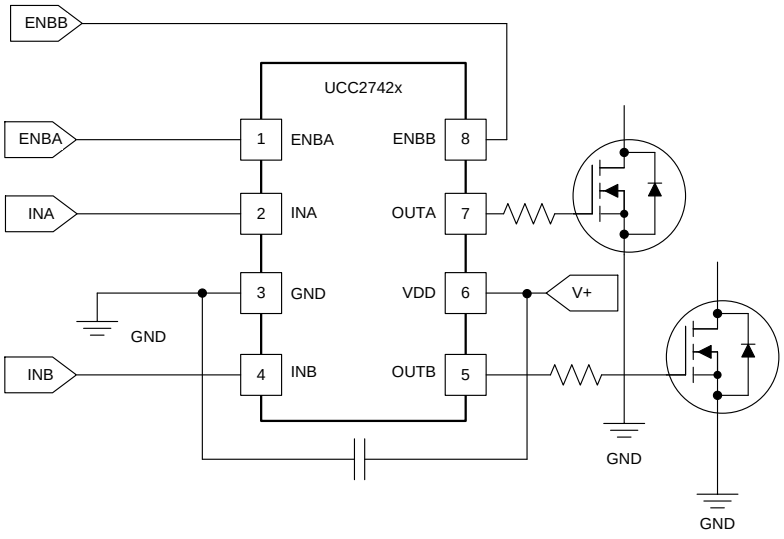


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (May 2013) to Revision E — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision C (July 2011) to Revision D — **Page**

- Added *Pin Functions* table note ... 3
- Added ABSOLUTE MAXIMUM RATINGS note ... 4
- Added additional ENABLE pin description. ... 12

Changes from Revision B (November 2004) to Revision C — **Page**

- Changed temperature rating. ... 1
- Changed ORDERING INFORMATION temperature range, three instances. ... 1
- Changed Output current (OUTA, OUTB) DC from 0.3 A to 0.2 A. ... 4
- Changed ELECTRICAL CHARACTERISTICS temperature rating. ... 5
- Changed Low-level output level from 40 mV max to 45 mV max. ... 5

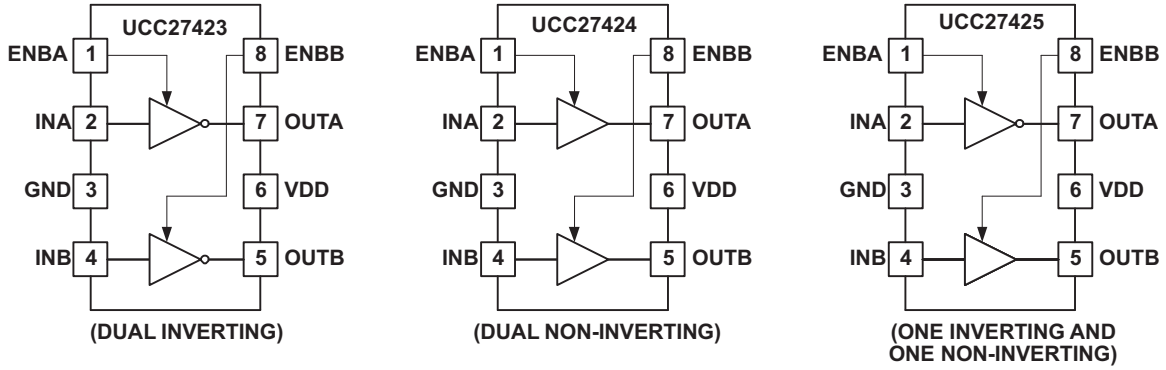
5 Device Comparison Table

OUTPUT CONFIGURATION	TEMPERATURE RANGE $T_A = T_J$	PACKAGED DEVICES		
		SOIC-8 (D)(1)	MSOP-8 PowerPAD (DGN)(2)	PDIP-8 (P)
Dual inverting	–40°C to 125°C	UCC27423D	UCC27423DGN	UCC27423P
Dual nonInverting	–40°C to 125°C	UCC27424D	UCC27424DGN	UCC27424P
One inverting, one noninverting	–40°C to 125°C	UCC27425D	UCC27425DGN	UCC27425P

(1) D (SOIC-8) and DGN (PowerPAD-MSOP) packages are available taped and reeled. Add R suffix to device type (e.g. UCC27423DR, UCC27424DGNR) to order quantities of 2,500 devices per reel for D or 1,000 devices per reel for DGN package.
(2) The PowerPAD™ is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate which is the ground of the device.

6 Pin Configuration and Functions

D Package, DGN Package, P Package
8-Pin SOIC, 8-Pln MSOP-PowerPAD, 8-Pin PDIP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ENBA	1	I	Enable input for the driver A with logic compatible threshold and hysteresis. The driver output can be enabled and disabled with this pin. It is internally pulled up to V_{DD} with 100 kΩ resistor for active high operation. The output state when the device is disabled will be low regardless of the input state.
ENBB	8	I	Enable input for the driver B with logic compatible threshold and hysteresis. The driver output can be enabled and disabled with this pin. It is internally pulled up to V_{DD} with 100 kΩ resistor for active high operation. The output state when the device is disabled will be low regardless of the input state.(1)
GND	3	—	Common ground: this ground should be connected very closely to the source of the power MOSFET which the driver is driving.
INA	2	I	Input A: input signal of the A driver which has logic compatible threshold and hysteresis. If not used, this input should be tied to either V_{DD} or GND. It should not be left floating.(1)
INB	4	I	Input B. Input signal of the A driver which has logic compatible threshold and hysteresis. If not used, this input should be tied to either V_{DD} or GND. It should not be left floating.
OUTA	7	O	Driver output A. The output stage is capable of providing 4A drive current to the gate of a power MOSFET.
OUTB	5	O	Driver output B. The output stage is capable of providing 4A drive current to the gate of a power MOSFET.
V_{DD}	6	I	Supply. Supply voltage and the power input connection for this device.

(1) Refer to *Detailed Description* for more details.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
V_{DD}	Supply voltage		–0.3	16	V
I_{OUT_DC}	Output current (OUTA, OUTB) DC			0.2	A
I_{OUT_PULSED}	Pulsed, (0.5 µs)			4.5	A
V_{IN}	Input voltage (INA, INB)		–5	6 or V_{DD} + 0.3 (whichever is larger)	V
	Enable voltage (ENBA, ENBB)		–0.3	6 or V_{DD} + 0.3 (whichever is larger)	V
	Power dissipation at T_A = 25°C	DGN package		3	W
		D package		650	mW
		P package		350	
T_J	Junction operating temperature		–55	150	°C
	Lead temperature (soldering, 10 s)			300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) When $V_{DD} \leq 6$ V, EN rating max value is 6 V; when $V_{DD} > 6$ V, EN rating max value is V_{DD} + 0.3 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4		15	V
INA and INB	Input voltage	–2		15	V
ENA and ENB	Enable voltage	0		15	V
T_J	Operating junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		UCC2742x			UNIT
		D (SOIC)	DGN (MSOP)	P (PDIP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.3	56.6	55.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.2	52.8	45.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.3	32.6	32.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.2	1.8	23.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	46.8	32.3	32.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	5.9	–	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

V_{DD} = 4.5 V to 15 V, T_A = –40°C to 125°C, T_A = T_J, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT (INA, INB)						
V_{IN_H}	Logic 1 input threshold		2			V
V_{IN_L}	Logic 0 input threshold				1	
	Input current	0 V ≤ V_{IN} ≤ V_{DD}	–10	0	10	µA
OUTPUT (OUTA, OUTB)						
	Output current	V_{DD} = 14 V (1)		4		A
V_{OH}	High-level output voltage	V_{OH} = V_{DD} – V_{OUT}, I_{OUT} = –10 mA		330	450	mV
V_{OL}	Low-level output level	I_{OUT} = 10 mA		22	45	
	Output resistance high	T_A = 25°C, I_{OUT} = –10 mA, V_{DD} = 14 V (2)	25	30	35	Ω
		T_A = full range, I_{OUT} = –10 mA, V_{DD} = 14 V (2)	18		45	
	Output resistance low	T_A = 25°C, I_{OUT} = 10 mA, V_{DD} = 14 V (2)	1.9	2.2	2.5	
		T_A = full range I_{OUT} = 10 mA, V_{DD} = 14 V (2)	1.2		4.0	
	Latch-up protection		500			mA
SWITCHING TIME						
t_r	Rise time (OUTA, OUTB)	C_{LOAD} = 1.8 nF		20	40	ns
t_f	Fall time (OUTA, OUTB)	C_{LOAD} = 1.8 nF		15	40	
t_{d1}	Delay, IN rising (IN to OUT)	C_{LOAD} = 1.8 nF		25	40	
t_{d2}	Delay, IN falling (IN to OUT)	C_{LOAD} = 1.8 nF		35	50	
ENABLE (ENBA, ENBB)						
V_{IN_H}	High-level input voltage	LO to HI transition	1.7	2.4	2.9	V
V_{IN_L}	Low-level input voltage	HI to LO transition	1.1	1.8	2.2	V
	Hysteresis		0.15	0.55	0.90	V
R_{ENB}	Enable impedance	V_{DD} = 14 V, ENB = GND	75	100	140	kΩ
t_{D3}	Propagation delay time (see Figure 2)	C_{LOAD} = 1.8 nF		30	60	ns
t_{D4}	Propagation delay time (see Figure 2)	C_{LOAD} = 1.8 nF		100	150	ns
OVERALL						
I_{DD}	UCC27423 Static operating current, V_{DD} = 15 V, ENBA = ENBB = 15 V	INA = 0 V, INB = 0 V		900	1350	µA
		INA = 0 V, INB = HIGH		750	1100	
		INA = HIGH, INB = 0 V		750	1100	
		INA = HIGH, INB = HIGH		600	900	
I_{DD}	UCC27424 Static operating current, V_{DD} = 15 V, ENBA = ENBB = 15 V	INA = 0 V, INB = 0 V		300	450	µA
		INA = 0 V, INB = HIGH		750	1100	
		INA = HIGH, INB = 0 V		750	1100	
		INA = HIGH, INB = HIGH		1200	1800	
I_{DD}	UCC27425 Static operating current, V_{DD} = 15 V, ENBA = ENBB = 15 V	INA = 0 V, INB = 0 V		600	900	µA
		INA = 0 V, INB = HIGH		1050	1600	
		INA = HIGH, INB = 0 V		450	700	
		INA = HIGH, INB = HIGH		900	1350	
I_{DD}	All disabled, V_{DD} = 15 V, ENBA = ENBB = 0 V	INA = 0 V, INB = 0 V		300	450	µA
		INA = 0 V, INB = HIGH		450	700	
		INA = HIGH, INB = 0 V		450	700	
		INA = HIGH, INB = HIGH		600	900	

(1) The pullup / pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The pulsed output current rating is the combined current from the bipolar and MOSFET transistors.
(2) The pullup / pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The output resistance is the Rds(on) of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

7.6 Dissipation Ratings

PACKAGE	SUFFIX	POWER RATING (mW) T_A = 70°C (1)	DERATING FACTOR ABOVE 70°C (mW/°C) (1)
SOIC-8	D	344–655 (2)	6.25–11.9 (2)
PDIP-8	P	500	9
MSOP (3)	DGN	1370	17.1

(1) 125°C operating junction temperature is used for power rating calculations
(2) The range of values indicates the effect of pc-board. These values are intended to give the system designer an indication of the best and worst case conditions. In general, the system designer should attempt to use larger traces on the pc-board where possible in order to spread the heat away form the device more effectively. For information on the PowerPAD™ package, refer to Technical Brief, *PowerPad Thermally Enhanced Package*, Texas Instruments (SLMA002) and Application Brief, *PowerPad Made Easy*, Texas Instruments (SLMA004).
(3) The PowerPAD™ is not directly connected to any leads of this package. However, it is electrically and thermally connected to the substrate which is the ground of the device.

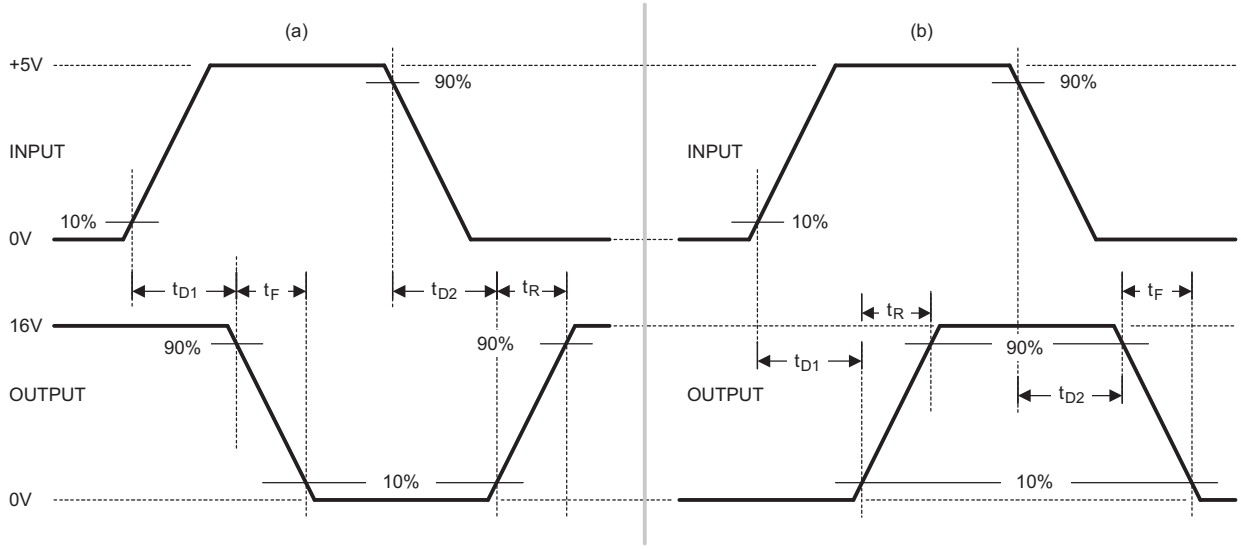
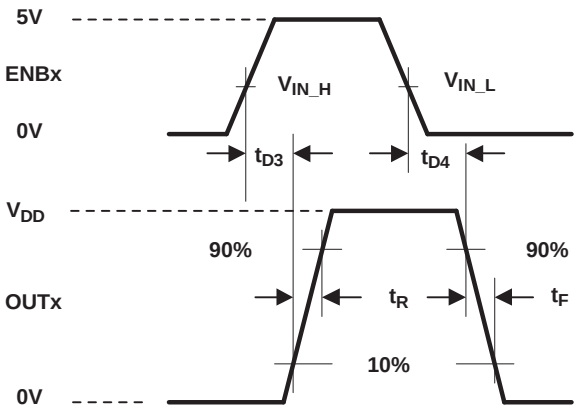


Figure 1. Switching Waveforms for (a) Inverting Driver and (b) Noninverting Driver



NOTE: The 10% and 90% thresholds depict the dynamics of the BiPolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

Figure 2. Switching Waveform for Enable to Output

7.7 Typical Characteristics

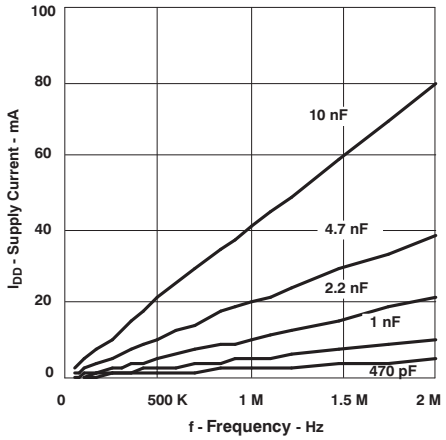


Figure 3. Supply Current vs Frequency (V_{DD} = 4.5 V)

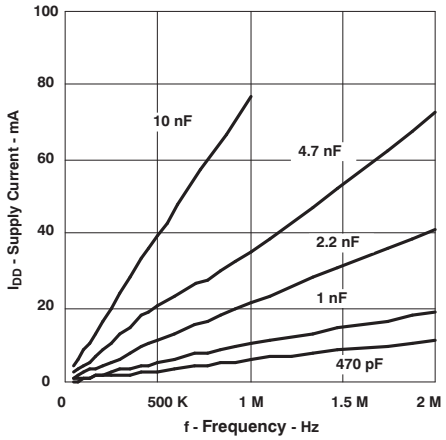


Figure 4. Supply Current vs Frequency (V_{DD} = 8.0 V)

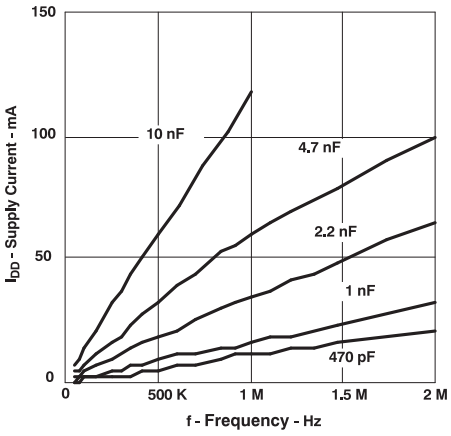


Figure 5. Supply Current vs Frequency (V_{DD} = 12 V)

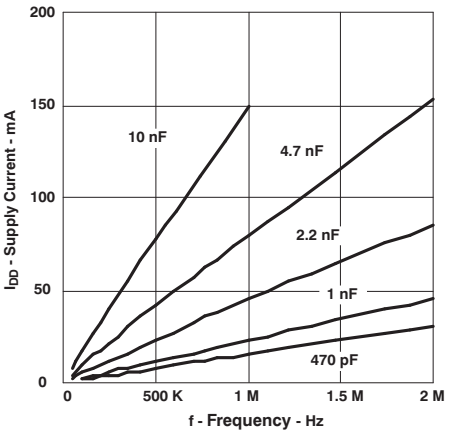


Figure 6. Supply Current vs Frequency (V_{DD} = 15 V)

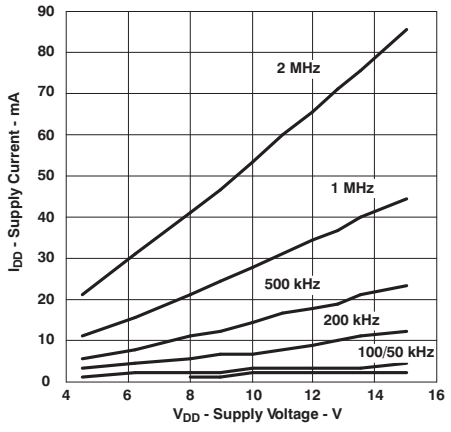


Figure 7. Supply Current vs Supply Voltage (C_{LOAD} = 2.2 nF)

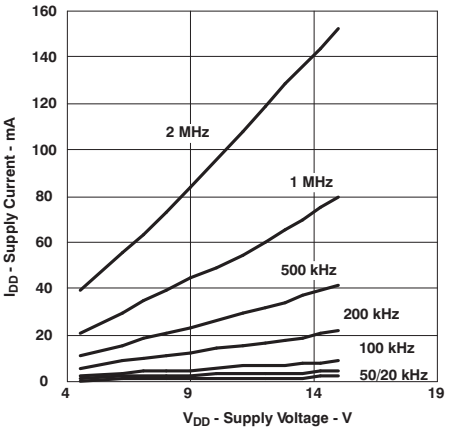


Figure 8. Supply Current vs Supply Voltage (C_{LOAD} = 4.7 nF)

Typical Characteristics (continued)

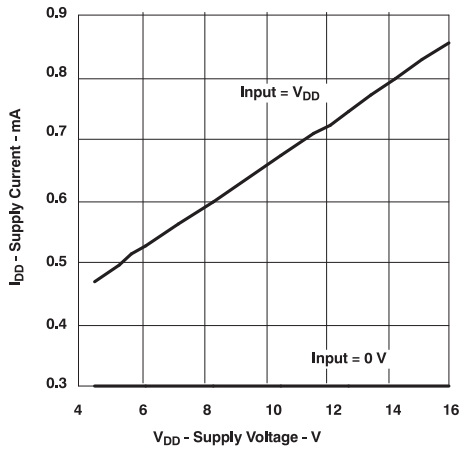


Figure 9. Supply Current vs Supply Voltage (UCC27423)

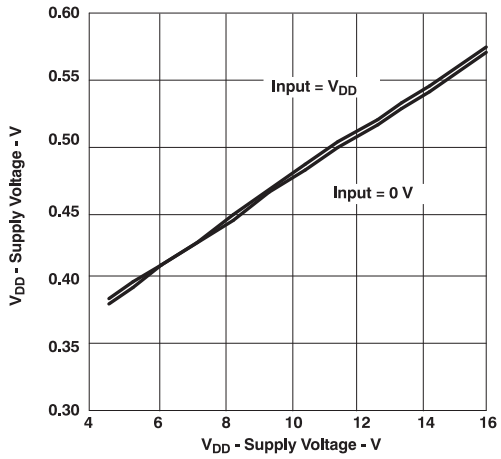


Figure 10. Supply Current vs Supply Voltage (UCC27424)

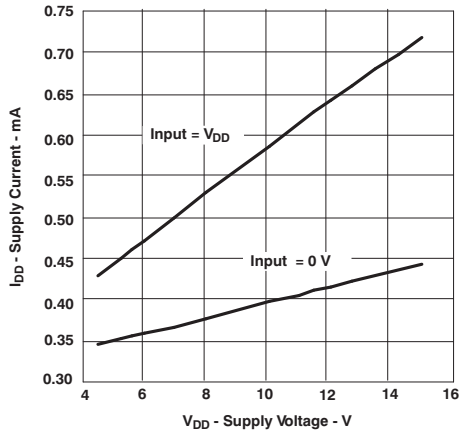


Figure 11. Supply Current vs Supply Voltage (UCC27425)

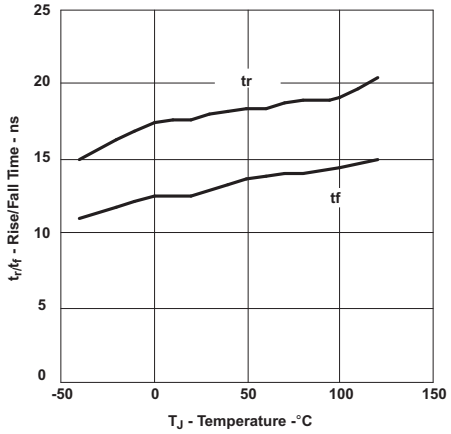


Figure 12. Rise Time and Fall Time vs Temperature (UCC27423)

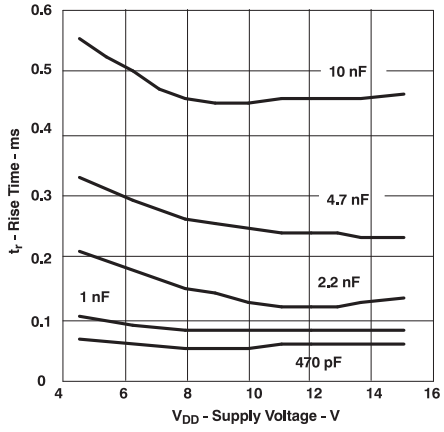


Figure 13. Rise Time vs Supply Voltage

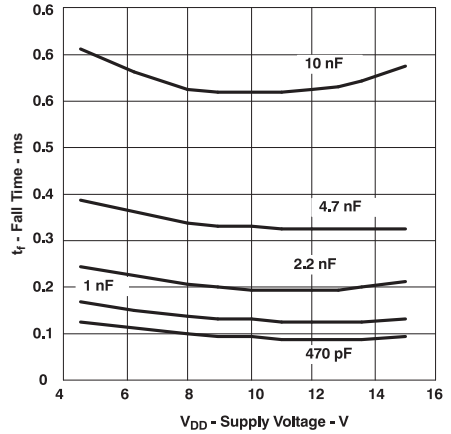


Figure 14. Fall Time vs Supply Voltage

Typical Characteristics (continued)

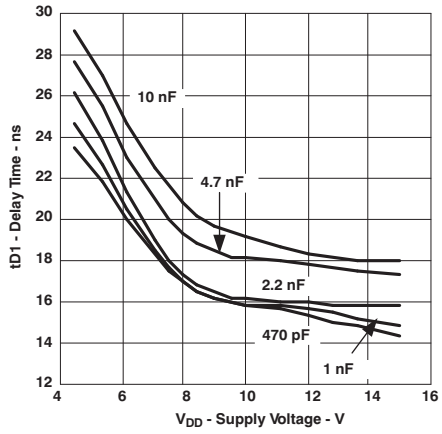


Figure 15. Delay Time (t_{D1}) vs Supply Voltage (UCC27423)

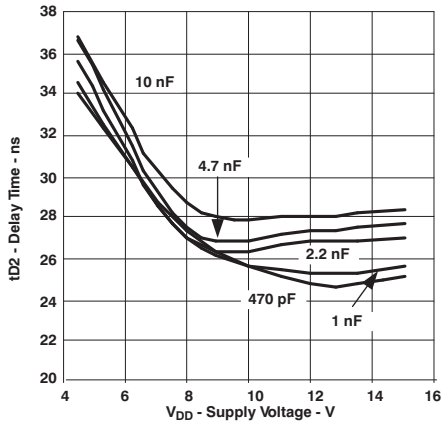


Figure 16. Delay Time (t_{D2}) vs Supply Voltage (UCC27423)

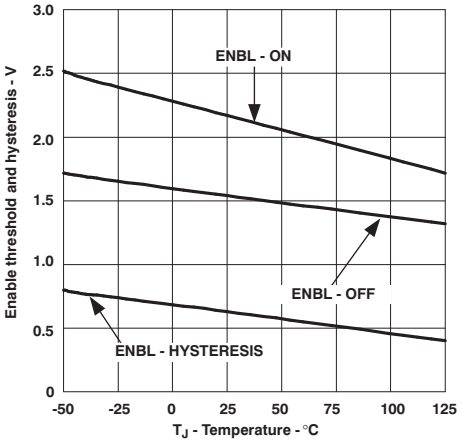


Figure 17. Enable Threshold and Hysteresis vs Temperature

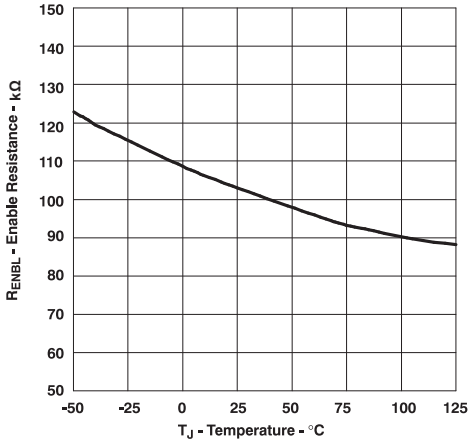


Figure 18. Enable Resistance vs Temperature

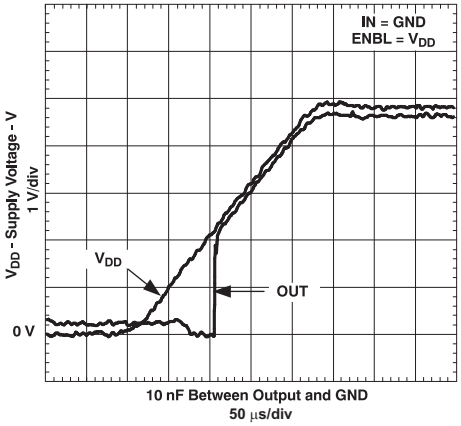


Figure 19. Output Behavior vs Supply Voltage (Inverting)

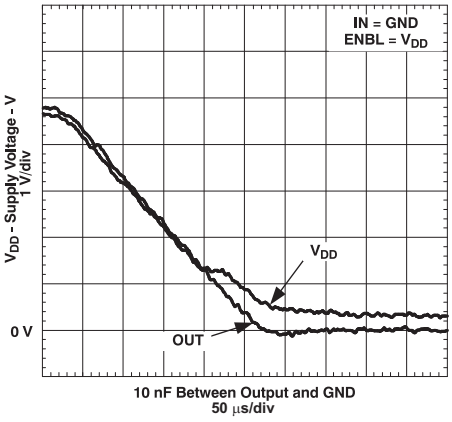


Figure 20. Output Behavior vs Supply Voltage (Inverting)

Typical Characteristics (continued)

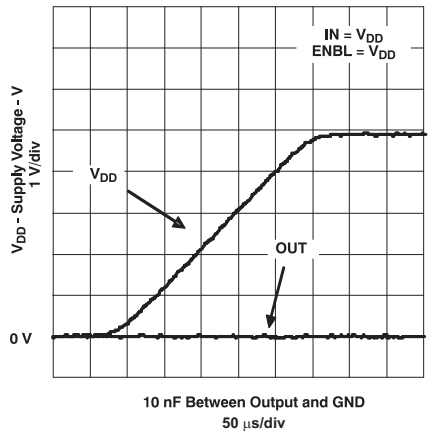


Figure 21. Output Behavior vs V_{DD} (Inverting)

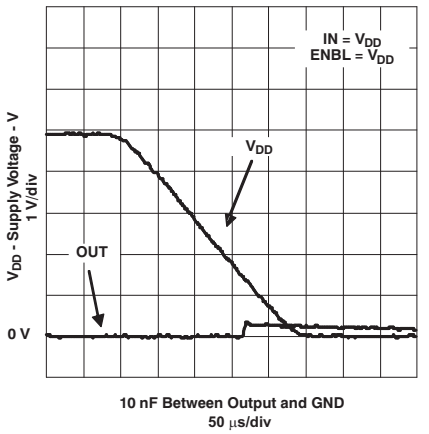


Figure 22. Output Behavior vs V_{DD} (Inverting)

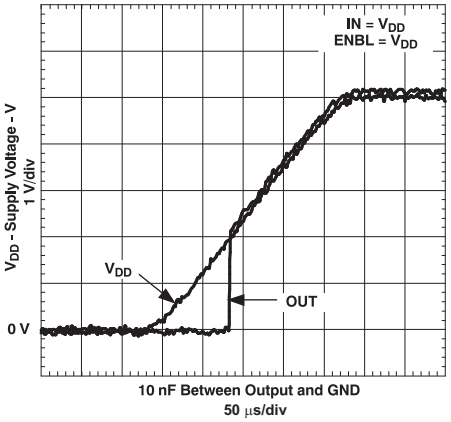


Figure 23. Output Behavior vs V_{DD} (Noninverting)

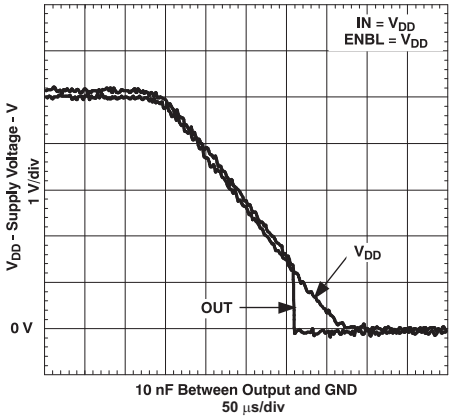


Figure 24. Output Behavior vs V_{DD} (Noninverting)

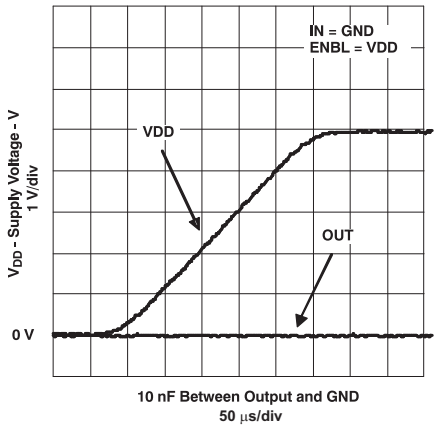


Figure 25. Output Behavior vs V_{DD} (Noninverting)

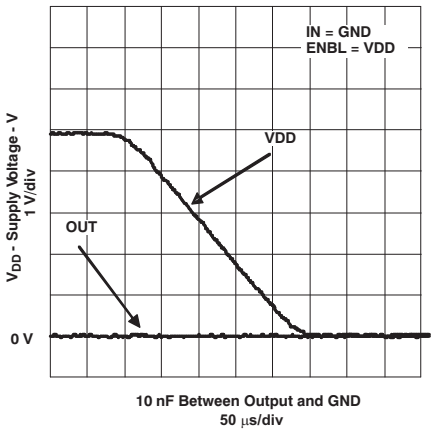


Figure 26. Output Behavior vs V_{DD} (Noninverting)

Typical Characteristics (continued)

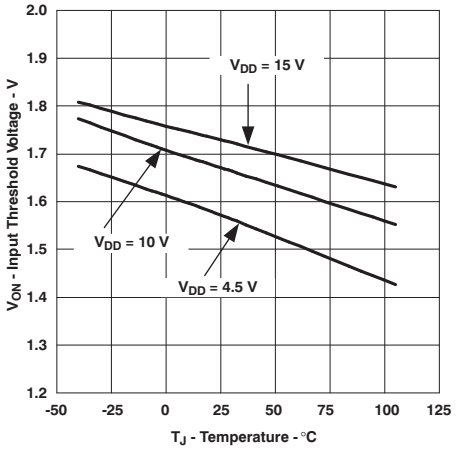


Figure 27. Input Threshold vs Temperature

8 Detailed Description

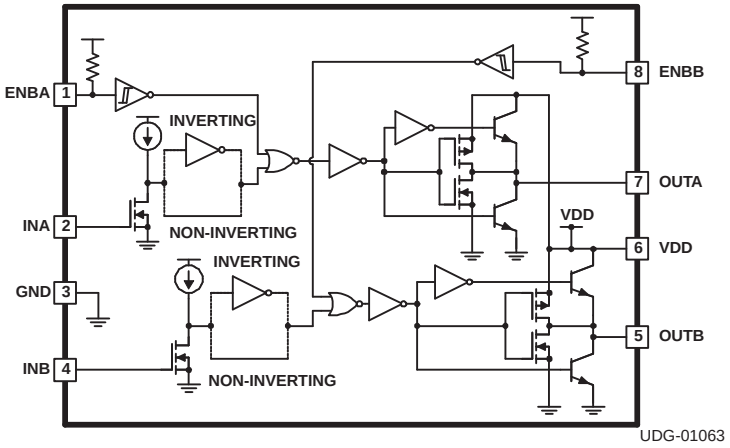
8.1 Overview

The UCC2742x family of high-speed dual MOSFET drivers can deliver large peak currents into capacitive loads. Three standard logic options are offered – dual-inverting, dual-noninverting and one-inverting and one-noninverting driver. The thermally enhanced 8-pin PowerPAD™ MSOP package (DGN) drastically lowers the thermal resistance to improve long-term reliability. It is also offered in the standard SOIC-8 (D) or PDIP-8 (P) packages. Using a design that inherently minimizes shoot-through current, these drivers deliver 4A of current where it is needed most at the Miller plateau region during the MOSFET switching transition. A unique Bipolar and MOSFET hybrid output stage in parallel also allows efficient current sourcing and sinking at low supply voltages. Table 1 highlights more details about UCC2742x.

Table 1. UCC2742x Features and Benefits

FEATURE	BENEFIT
1-ns (typ) delay matching between channels	Ease of paralleling outputs for higher (2 times) current capability, ease of driving parallel-power switches
Expanded V_{DD} operating range of 4 to 15 V	Flexibility in system design
Outputs enabled when enable pins (ENx) in floating condition	Pin-to-pin compatibility with the UCC27324 device from Texas Instruments and industry standard pinout, in designs where Pin 1 and Pin 8 are in floating condition
CMOS/TTL compatible input and enable threshold with wide hysteresis	Enhanced noise immunity, while retaining compatibility with microcontroller logic-level inputs signals (3.3 V, 5 V) optimized for digital power
Ability to handle –5 V_{DC} (max) at input pins (INA/B)	Increased robustness in noisy environments

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Enable

UCC2742x provides dual Enable inputs for improved control of each driver channel operation. The inputs incorporate logic compatible thresholds with hysteresis. They are internally pulled up to V_{DD} with 100kΩ resistor for active high operation. When ENBA and ENBB are driven high, the drivers are enabled and when ENBA and ENBB are low, the drivers are disabled. The default state of the Enable pin is to enable the driver and therefore can be left open for standard operation. However, if the enable pin is left open, it is recommended to terminate any PCB traces to be as short as possible to limit noise. If large noise is present due to non-optimal PCB layout, it is recommended to tie the Enable pin to Vcc or to add a filter capacitor (0.1 µF) to the Enable pin. The output states when the drivers are disabled is low regardless of the input state. See the truth table of Table 2 for the operation using enable logic.

Feature Description (continued)

Enable input are compatible with both logic signals and slow changing analog signals. They can be directly driven or a power-up delay can be programmed with a capacitor between ENBA, ENBB and AGND. ENBA and ENBB control input A and input B respectively.

8.3.2 Input Stage

The input thresholds have 3.3 V logic sensitivity over the full range of V_{DD} voltages; it is equally compatible with 0 to V_{DD} signals. The inputs of the UCC2742x driver family are designed to withstand 500-mA reverse current without damaging the IC for logic upset. The input stage of each driver should be driven by a signal with a short rise or fall time. This condition is satisfied in typical power supply applications where the input signals are provided by a PWM controller or logic gates with fast transition times (<200 ns). The input stages to the drivers function as a digital gate, and they are not intended for applications where a slow changing input voltage is used to generate a switching output when the logic threshold of the input section is reached. While this may not be harmful to the driver, the output of the driver may switch repeatedly at a high frequency.

Users should not attempt to shape the input signals to the driver in an attempt to slow down (or delay) the signal at the output. If limited rise or fall times to the power device is desired, an external resistance can be added between the output of the driver and the load device which is generally a power MOSFET gate. The external resistor may also help remove power dissipation from the device package, as discussed in the section on Thermal Considerations.

Importantly, input signal of the two channels, INA and INB, which has logic compatible threshold and hysteresis. If not used, INA and INB must be tied to either V_{DD} or GND; it must not be left floating.

8.3.3 Output Stage

Inverting output s of the UCC27423 and OUTA of the UCC27425 are intended to drive external P-channel MOSFETs. Noninverting outputs of the UCC27424 and OUTB of the UCC27425 are intended to drive external N-Channel MOSFETs. Each output stage is capable of supplying ±4 A peak current pulses and swings to both V_{DD} and GND. The pullup/pulldown circuits of the driver are constructed of bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{DS(on)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor. Each output stage also provides very low impedance to overshoot and undershoot due to the body diode of the external MOSFET. This means that in many cases, external-Schottky-clamp diodes are not required. The UCC2742x family delivers 4 A of gate drive where it is most needed during the MOSFET switching transition (at the Miller plateau region) providing improved efficiency gains. A unique Bipolar and MOSFET hybrid output stage in parallel also allows efficient current sourcing at low supply voltages.

8.4 Device Functional Modes

With V_{DD} power supply in the range of 4 V to 16 V, the output stage is dependent on the states of the HI and LI pins. Table 2 shows the UCC2742x truth table.

Table 2. Input/Output Logic

		INPUTS (VIN_L, VIN_H)		UCC27423		UCC27424		UCC27425	
ENBA	ENBB	INA	INB	OUTA	OUTB	OUTA	OUTB	OUTA	OUTB
H	H	L	L	H	H	L	L	H	L
H	H	L	H	H	L	L	H	H	H
H	H	H	L	L	H	H	L	L	L
H	H	H	H	L	L	H	H	L	H
L	L	X	X	L	L	L	L	L	L

Importantly, if INA and INB are not used, they must be tied to either V_{DD} or GND; it must not be left floating.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

High frequency power supplies often require high-speed, high-current drivers such as the UCC2742x family. A leading application is the need to provide a high power buffer stage between the PWM output of the control IC and the gates of the primary power MOSFET or IGBT switching devices. In other cases, the driver IC is utilized to drive the power device gates through a drive transformer. Synchronous rectification supplies also have the need to simultaneously drive multiple devices which can present an extremely large load to the control circuitry.

Driver ICs are utilized when it is not feasible to have the primary PWM regulator IC directly drive the switching devices for one or more reasons. The PWM IC may not have the brute drive capability required for the intended switching MOSFET, limiting the switching performance in the application. In other cases there may be a desire to minimize the effect of high frequency switching noise by placing the high current driver physically close to the load. Also, newer ICs that target the highest operating frequencies may not incorporate onboard gate drivers at all. Their PWM outputs are only intended to drive the high impedance input to a driver such as the UCC2742x. Finally, the control IC may be under thermal stress due to power dissipation, and an external driver can help by moving the heat from the controller to an external package.

9.2 Typical Application

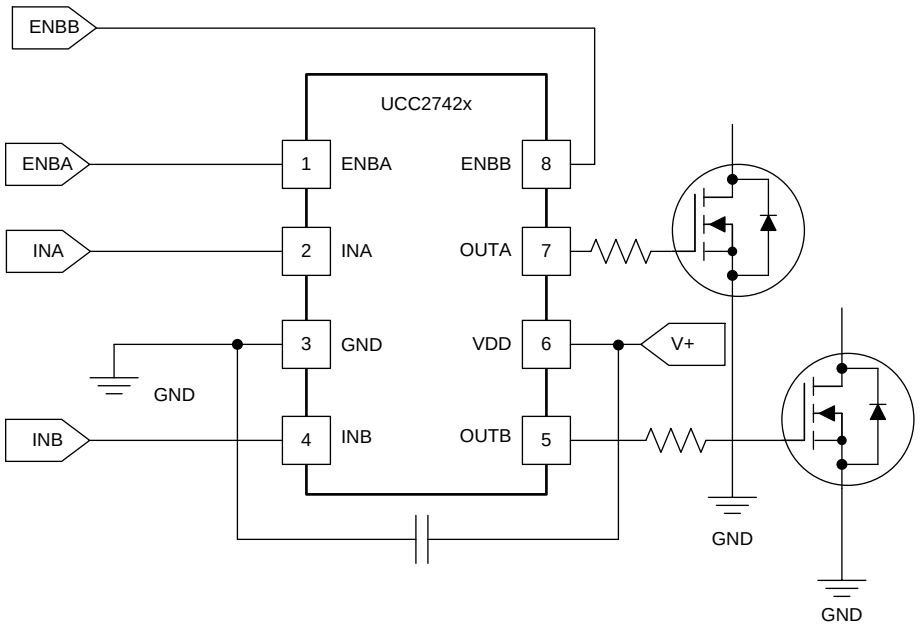


Figure 28. UCC2742x Driving Two Independent MOSFETs

9.2.1 Design Requirements

To select proper device from UCC2742x family, it is recommended to first check the appropriate logic for the outputs. UCC27423 has dual inverting outputs; UCC27424 has dual non-inverting outputs; UCC27425 has an inverting channel A and non-inverting channel B. Moreover, some considerations must be evaluated in order to make the most appropriate selection. Among these considerations are V_{DD}, drive current, and power dissipation.

Typical Application (continued)

9.2.2 Detailed Design Procedure

9.2.2.1 Source and Sink Capabilities During Miller Plateau

Large power MOSFETs present a large load to the control circuitry. Proper drive is required for efficient, reliable operation. The UCC2742x drivers have been optimized to provide maximum drive to a power MOSFET during the Miller plateau region of the switching transition. This interval occurs while the drain voltage is swinging between the voltage levels dictated by the power topology, requiring the charging and discharging of the drain-gate capacitance with current supplied or removed by the driver device.

Two circuits are used to test the current capabilities of the UCC2742x driver. In each case external circuitry is added to clamp the output near 5 V while the IC is sinking or sourcing current. An input pulse of 250 ns is applied at a frequency of 1 kHz in the proper polarity for the respective test. In each test there is a transient period where the current peaked up and then settled down to a steady-state value. The noted current measurements are made at a time of 200 ns after the input pulse is applied, after the initial transient.

The circuit in Figure 29 is used to verify the current sink capability when the output of the driver is clamped around 5V, a typical value of gate-source voltage during the Miller plateau region. The UCC2742x is found to sink 4.5 A at V_{DD} = 15 V and 4.28 A at V_{DD} = 12 V.

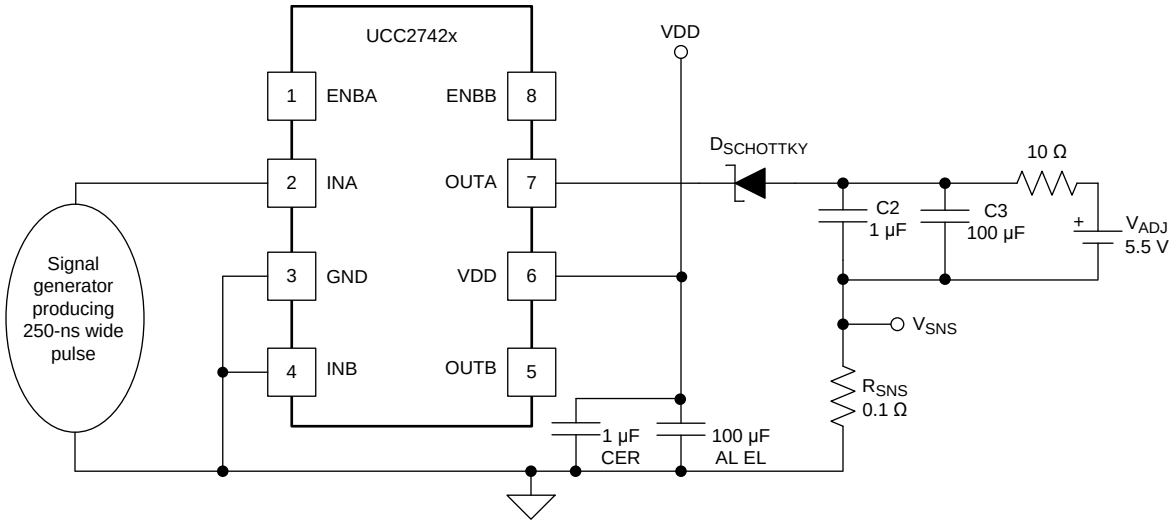


Figure 29. Current Sink Capability Test

The circuit show in Figure 30 is used to test the current source capability with the output clamped around 5 V with a string of Zener diodes. The UCC2742x is found to source 4.8 A at V_{DD} = 15 V and 3.7 A at V_{DD} = 12 V.

Typical Application (continued)

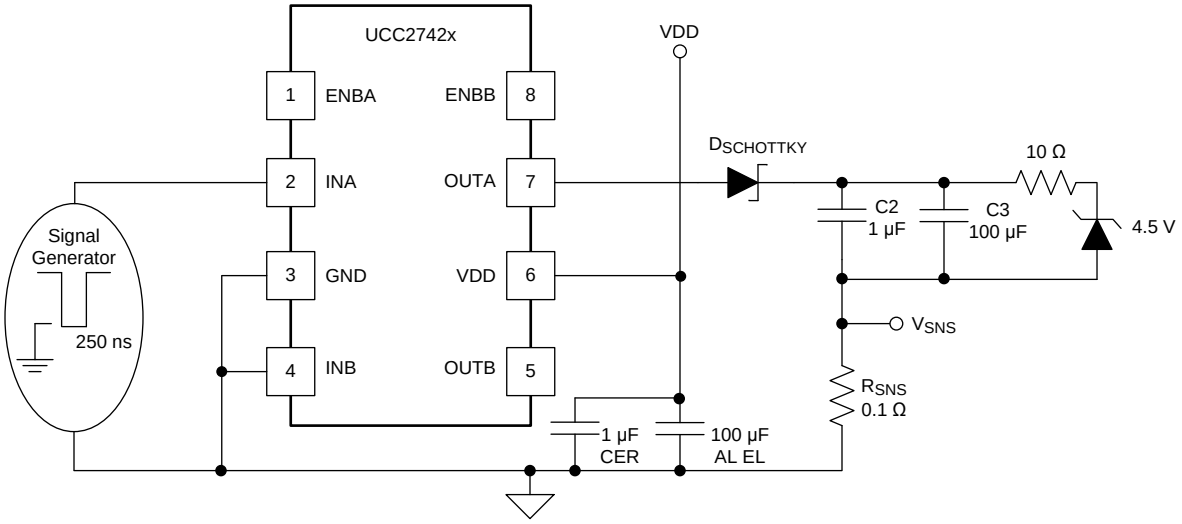


Figure 30. Current Source Capability Test

9.2.2.2 Parallel Outputs

The A and B drivers may be combined into a single driver by connecting the INA and INB inputs together and the OUTA and OUTB outputs together. Then, a single signal can control the paralleled combination as shown in Figure 31.

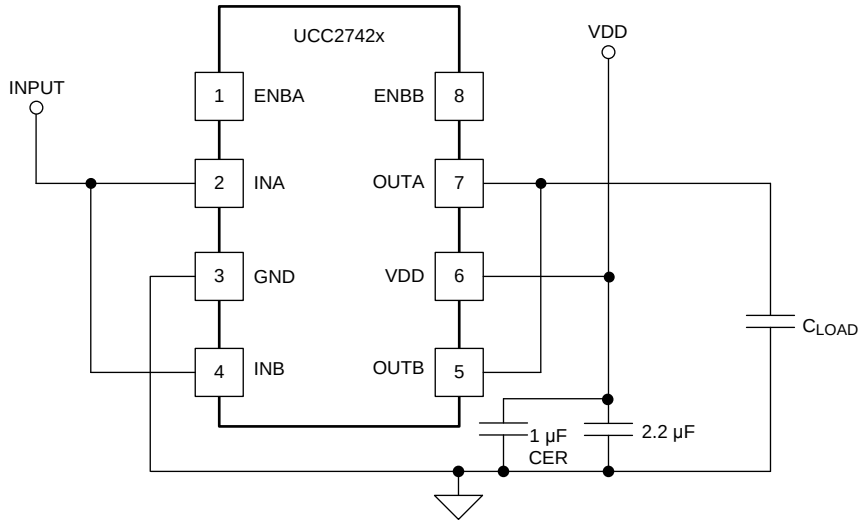


Figure 31. Parallel Operation of UCC27423 and UCC27424

Important consideration about paralleling two channels for UCC27423/4 include the INA and INB should be shorted in PCB layout as close to the device as possible, as well as for OUTA and OUTB, in which condition PCB layout parasitic mismatching between two channels could be minimized. The INA/B slope signal should be fast enough to avoid mismatched V_{IN_H} / V_{IN_L}, t_{d1} / t_{d2} between channel-A and channel-B. It is recommended to have input signal slope faster than 20 V/us.

Typical Application (continued)

9.2.2.3 V_{DD}

Although quiescent V_{DD} current is very low, total supply current will be higher, depending on OUTA and OUTB current and the programmed oscillator frequency. Total V_{DD} current is the sum of quiescent V_{DD} current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_g), average OUT current can be calculated from Equation 1.

$$I_{OUT} = Q_g \times f \quad (1)$$

where

- f = switching frequency

For the best high-speed circuit performance, two V_{DD} bypass capacitors are recommended to prevent noise problems. The use of surface mount components is highly recommended. A 0.1µF ceramic capacitor should be located closest to the V_{DD} to ground connection. In addition, a larger capacitor (such as 1µF) with relatively low ESR should be connected in parallel, to help deliver the high current peaks to the load. The parallel combination of capacitors should present a low impedance characteristic for the expected current levels in the driver application.

9.2.2.4 Drive Current and Power Requirements

The UCC2742x family of drivers are capable of delivering 4 A of current to a MOSFET gate for a period of several hundred nanoseconds. High peak current is required to turn the device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground. This repeats at the operating frequency of the power device. A MOSFET is used in this discussion because it is the most common type of switching device used in high frequency power conversion equipment.

References 1 and 2 in *Documentation Support* discuss the current required to drive a power MOSFET and other capacitive-input switching devices. Reference 2 in *Documentation Support* includes information on the previous generation of bipolar IC gate drivers.

When a driver IC is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by Equation 2.

$$E = \frac{1}{2}CV^2 \quad (2)$$

where

- C = load capacitor, and V = bias voltage (feeding the driver)

There is an equal amount of energy transferred to ground when the capacitor is discharged. This leads to a power loss given by Equation 3.

$$P = CV^2 \times f \quad (3)$$

where

- f = switching frequency

This power is dissipated in the resistive elements of the circuit. Thus, with no external resistor between the driver and gate, this power is dissipated inside the driver. Half of the total power is dissipated when the capacitor is charged, and the other half is dissipated when the capacitor is discharged. An actual example using the conditions of the previous gate drive waveform should help clarify this.

With V_{DD} = 12 V, C_{LOAD} = 10 nF, and f = 300 kHz, the power loss can be calculated as Equation 4.

$$P = 10\ nF \times (12\ V)^2 \times (300\ kHz) = 0.432\ W \quad (4)$$

With a 12 V supply, this would equate to a current of Equation 5.

$$I = \frac{P}{V} = \frac{0.432\ W}{12\ V} = 36\ mA \quad (5)$$

Typical Application (continued)

The actual current measured from the supply was 0.037A, and is very close to the predicted value. But, the I_{DD} current that is due to the IC internal consumption should be considered. With no load the IC current draw is 0.0027 A. Under this condition the output rise and fall times are faster than with a load. This could lead to an almost insignificant, yet measurable current due to cross-conduction in the output stages of the driver. However, these small current differences are buried in the high frequency switching spikes, and are beyond the measurement capabilities of a basic lab setup. The measured current with 10 nF load is reasonably close to that expected.

The switching load presented by a power MOSFET can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain of the device between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence $Q_g = C_{eff}V$ to provide the power loss in Equation 6.

$$P = C \times V^2 \times f = V \times Q_g \times f \quad (6)$$

This equation allows a power designer to calculate the bias power required to drive a specific MOSFET gate at a specific bias voltage.

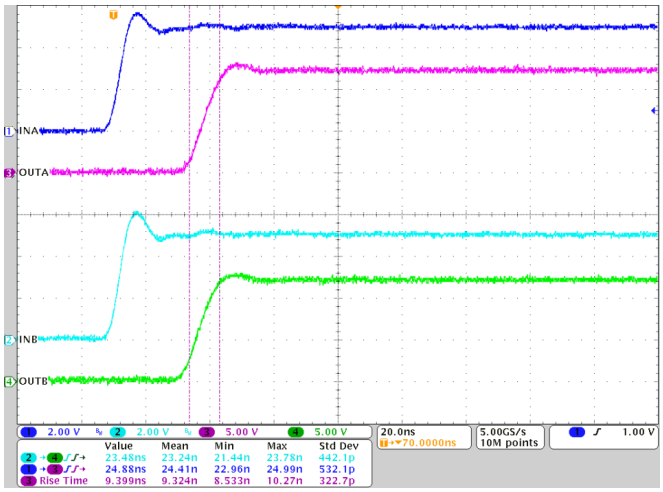
9.2.3 Application Curves

Figure 32 and Figure 33 shows rising/falling time and turn-on/off propagation delay testing waveform in room temperature for UCC27424, and waveform measurement data (see the bottom part of the waveform). Each channel, INA/INB/OUTA/OUTB, is labeled and displayed on the left hand of the waveforms.

The load capacitance testing condition is 1.8 nF, V_{DD} = 12 V, and f = 300 kHz.

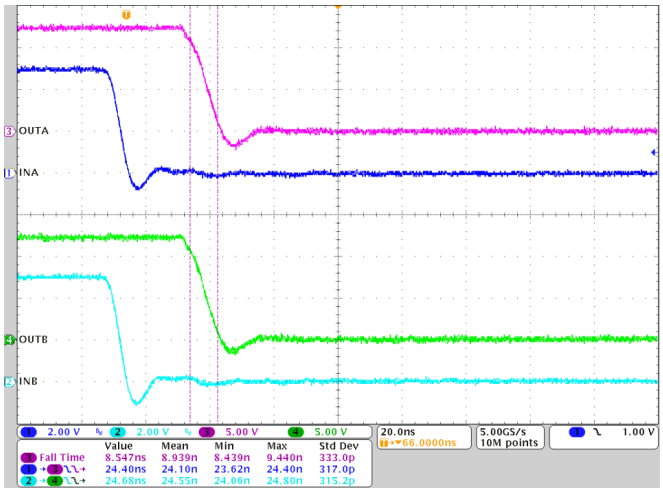
HI and LI share one same input from function generator, therefore, besides the propagation delay and rising/falling time, the difference of the propagation delay between HO and LO gives the propagation delay matching data.

Note the linear rise and fall edges of the switching waveforms. This is due to the constant output current characteristic of the driver as opposed to the resistive output impedance of traditional MOSFET-based gate drivers.



CL = 1.8 nF, V_{DD} = 12 V, f = 300 kHz

Figure 32. Rising Time and Turnon Propagation Delay



CL = 1.8 nF, V_{DD} = 12 V, f = 300 kHz

Figure 33. Falling Time and Turnoff Propagation Delay

10 Power Supply Recommendations

The recommended bias supply voltage range for UCC2742x is from 4 V to 15 V. The upper end of this range is driven by the 16 V absolute maximum voltage rating of the V_{DD}. It is recommended to keep proper margin to allow for transient voltage spikes.

A local bypass capacitor should be placed between the VDD and GND pins. And this capacitor should be located as close to the device as possible. A low ESR, ceramic surface mount capacitor is recommended. TI recommends using 2 capacitors across VDD and GND: a 100 nF ceramic surface-mount capacitor for high frequency filtering placed very close to VDD and GND pin, and another surface-mount capacitor, 220 nF to 10 µF, for IC bias requirements.

11 Layout

11.1 Layout Guidelines

Optimum performance of gate drivers cannot be achieved without taking due considerations during circuit board layout. The following points are emphasized:

1. Low ESR/ESL capacitors must be connected close to the IC between VDD and GND pins to support high peak currents drawn from VDD during the turn-on of the external MOSFETs.
2. Grounding considerations:
   - The first priority in designing grounding connections is to confine the high peak currents that charge and discharge the MOSFET gates to a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminals of the MOSFETs. The gate driver should be placed as close as possible to the MOSFETs.
   - Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver is connected to the other circuit nodes such as source of power MOSFET and ground of PWM controller at one, single point. The connected paths must be as short as possible to reduce inductance.
   - Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.
3. In noisy environments, tying inputs of an unused channel of the UCC2742x device to VDD or GND using short traces in order to ensure that the output is enabled and to prevent noise from causing malfunction in the output may be necessary.
4. Separate power traces and signal traces, such as output and input signals.

11.2 Layout Example

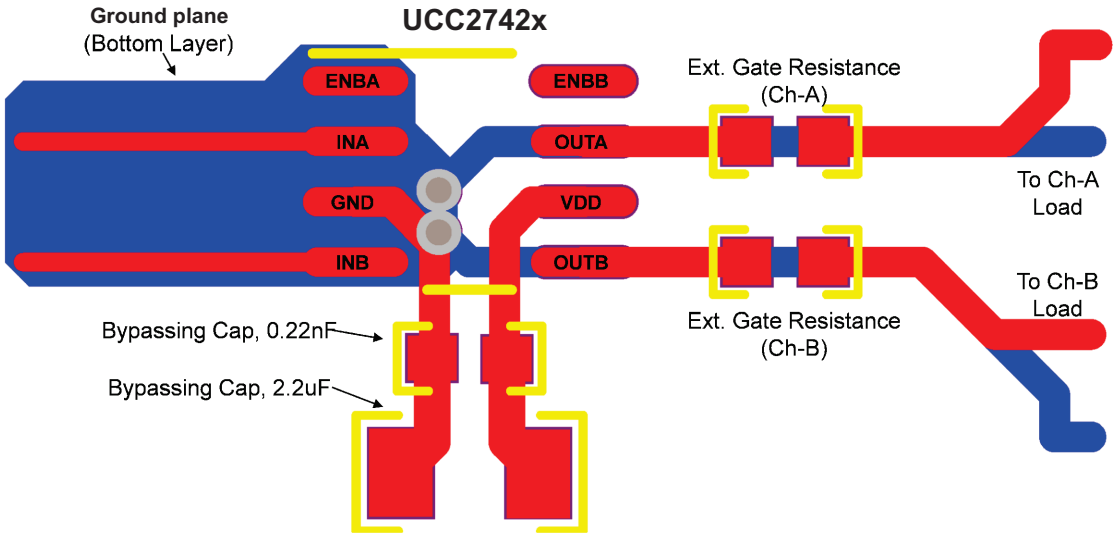


Figure 34. Recommended PCB Layout for UCC2742x

11.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the IC package. In order for a power driver to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The UCC2742x family of drivers is available in three different packages to cover a range of application requirements.

As shown in the power dissipation rating table, the SOIC-8 (D) and PDIP-8 (P) packages have a power rating of around 0.5 W with T_A = 70°C. This limit is imposed in conjunction with the power derating factor also given in *Dissipation Ratings*. Note that the power dissipation in our earlier example is 0.432W with a 10nF load, 12 V_{DD}, switched at 300kHz. Thus, only one load of this size could be driven using the D or P package, even if the two onboard drivers are paralleled. The difficulties with heat removal limit the drive available in the older packages.

The MSOP PowerPAD-8 (DGN) package significantly relieves this concern by offering an effective means of removing the heat from the semiconductor junction. As illustrated in Reference 3 of *Documentation Support*, the PowerPAD packages offer a leadframe die pad that is exposed at the base of the package. This pad is soldered to the copper on the PC board directly underneath the IC package, reducing the $R_{\theta JC(bot)}$ down to 5.9°C/W. Data is presented in Reference 3 of *Documentation Support* to show that the power dissipation can be quadrupled in the PowerPAD configuration when compared to the standard packages. The PC board must be designed with thermal lands and thermal vias to complete the heat removal subsystem, as summarized in Reference 4 of *Documentation Support*. This allows a significant improvement in heatsinking over that available in the D or P packages, and is shown to more than double the power capability of the D and P packages. Note that the PowerPAD™ is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate which is the ground of the device.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Related Products

PRODUCT	DESCRIPTION	PACKAGES
UCC37323 UCC37324 UCC37325	Dual 4-A Low-Side Drivers	MSOP-8 PowerPAD, SOIC-8, PDIP-8
UCC37321 UCC37322	Single 9-A Low-Side Driver with Enable	MSOP-8 PowerPAD, SOIC-8, PDIP-8
TPS2811 TPS2812 TPS2813	Dual 2-A Low-Side Drivers with Internal Regulator	TSSOP-8, SOIC-8, PDIP-8
TPS2814 TPS2815	Dual 2-A Low-Side Drivers with Two Inputs per Channel	TSSOP-8, SOIC-8, PDIP-8
TPS2816 TPS2817 TPS2818 TPS2819	Single 2-A Low-Side Driver with Internal Regulator	5-Pin SOT-23
TPS2828 TPS2829	Single 2-A Low-Side Driver	5-Pin SOT-23

12.2 Documentation Support

12.2.1 Related Documentation

- Power Supply Seminar SEM-1400 Topic 2: *Design And Application Guide For High Speed MOSFET Gate Drive Circuits*, by Laszlo Balogh, Texas Instruments (SLUP133).
- Application Note, *Practical Considerations in High Performance MOSFET, IGBT and MCT Gate Drive Circuits*, by Bill Andreycak, Texas Instruments (SLUA105)
- Technical Brief, *PowerPad Thermally Enhanced Package*, Texas Instruments (SLMA002)
- Application Brief, *PowerPAD Made Easy*, Texas Instruments (SLMA004)

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UCC27423	Click here	Click here	Click here	Click here	Click here
UCC27424	Click here	Click here	Click here	Click here	Click here
UCC27425	Click here	Click here	Click here	Click here	Click here

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27423D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	27423	Samples
UCC27423DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	27423	Samples
UCC27423DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	27423	Samples
UCC27423DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	27423	Samples
UCC27423DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	27423	Samples
UCC27423DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	27423	Samples
UCC27423P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 105	27423	Samples
UCC27424D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	27424	Samples
UCC27424DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	27424	Samples
UCC27424DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	27424	Samples
UCC27424DGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	27424	Samples
UCC27424DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	27424	Samples
UCC27424DGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	27424	Samples
UCC27424DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	27424	Samples
UCC27424DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	27424	Samples
UCC27424P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 105	27424	Samples
UCC27424PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 105	27424	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27425D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	27425	Samples
UCC27425DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	27425	Samples
UCC27425DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	27425	Samples
UCC27425DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	27425	Samples
UCC27425DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	27425	Samples
UCC27425DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	27425	Samples
UCC27425P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 105	27425	Samples
UCC27425PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 105	27425	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UCC27423, UCC27424, UCC27425 :

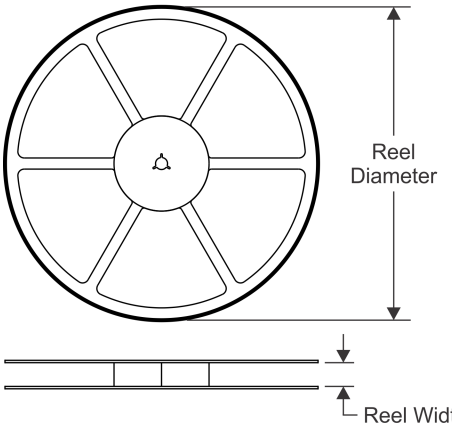
- Automotive: UCC27423-Q1, UCC27424-Q1, UCC27425-Q1
- Enhanced Product: UCC27423-EP, UCC27424-EP

NOTE: Qualified Version Definitions:

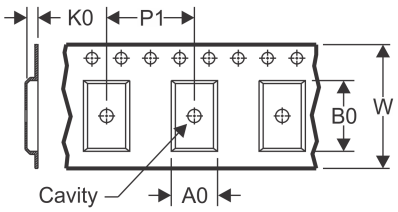
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

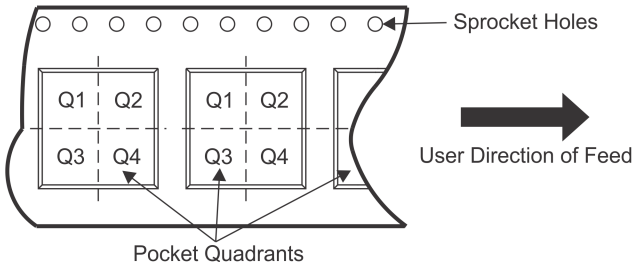


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

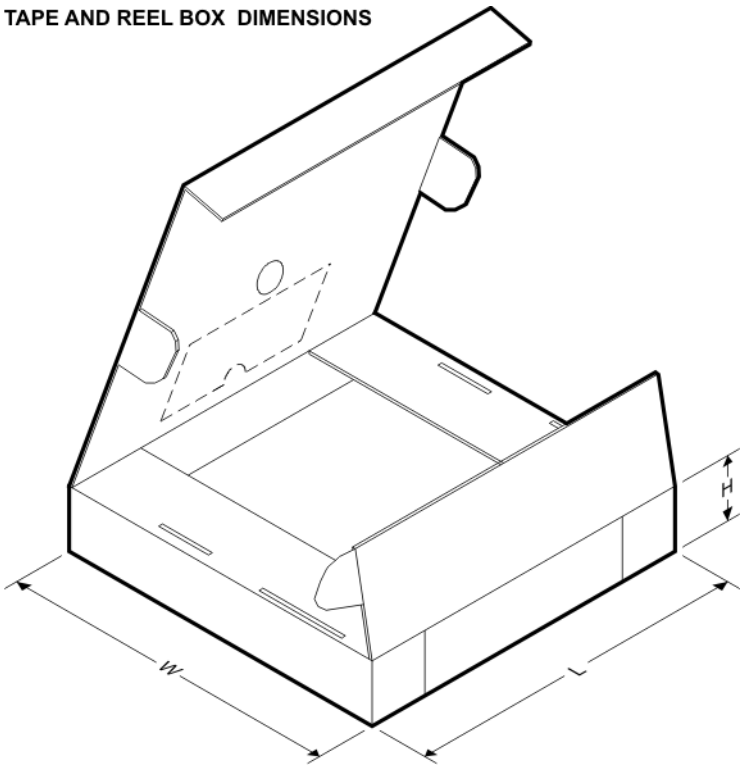
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27423DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27423DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27424DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27424DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27424DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27425DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27425DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

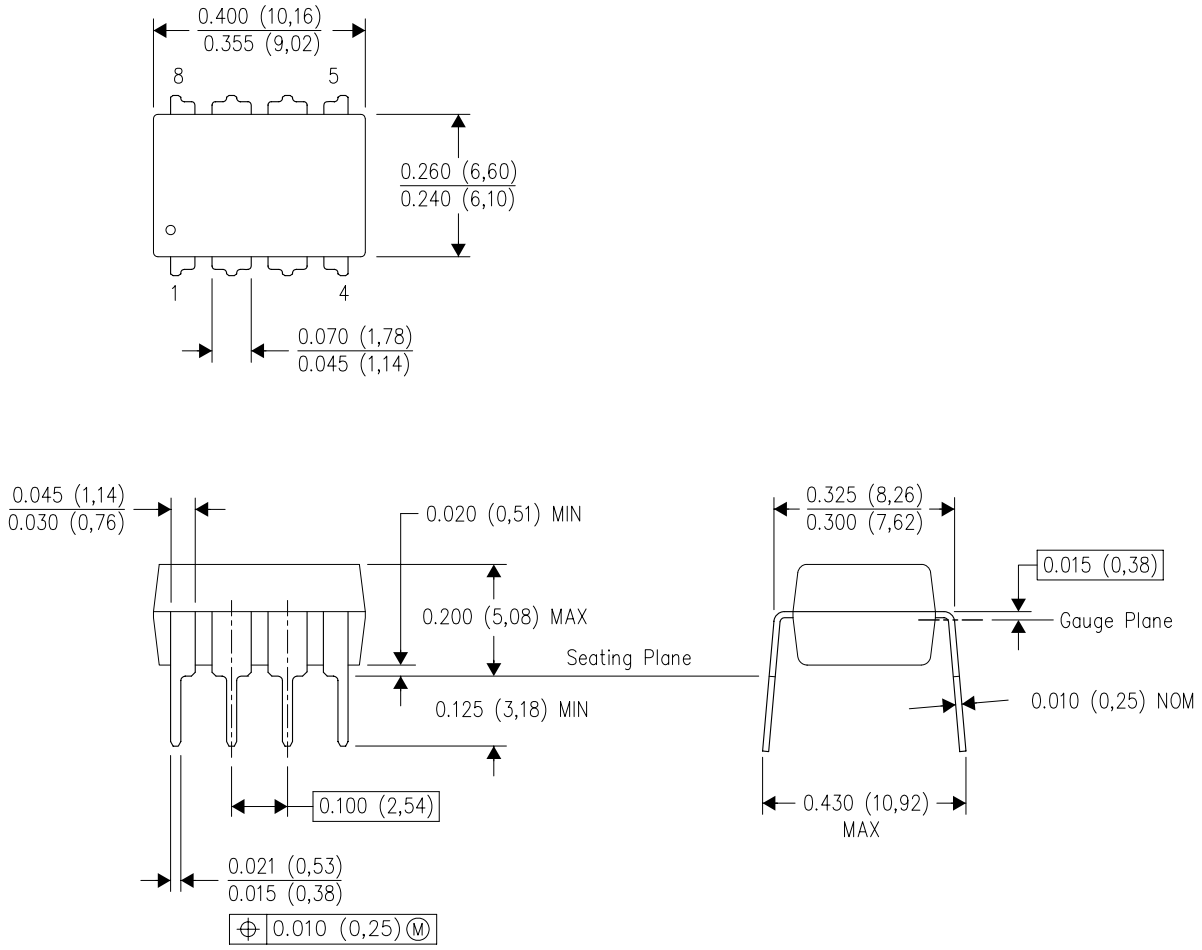
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

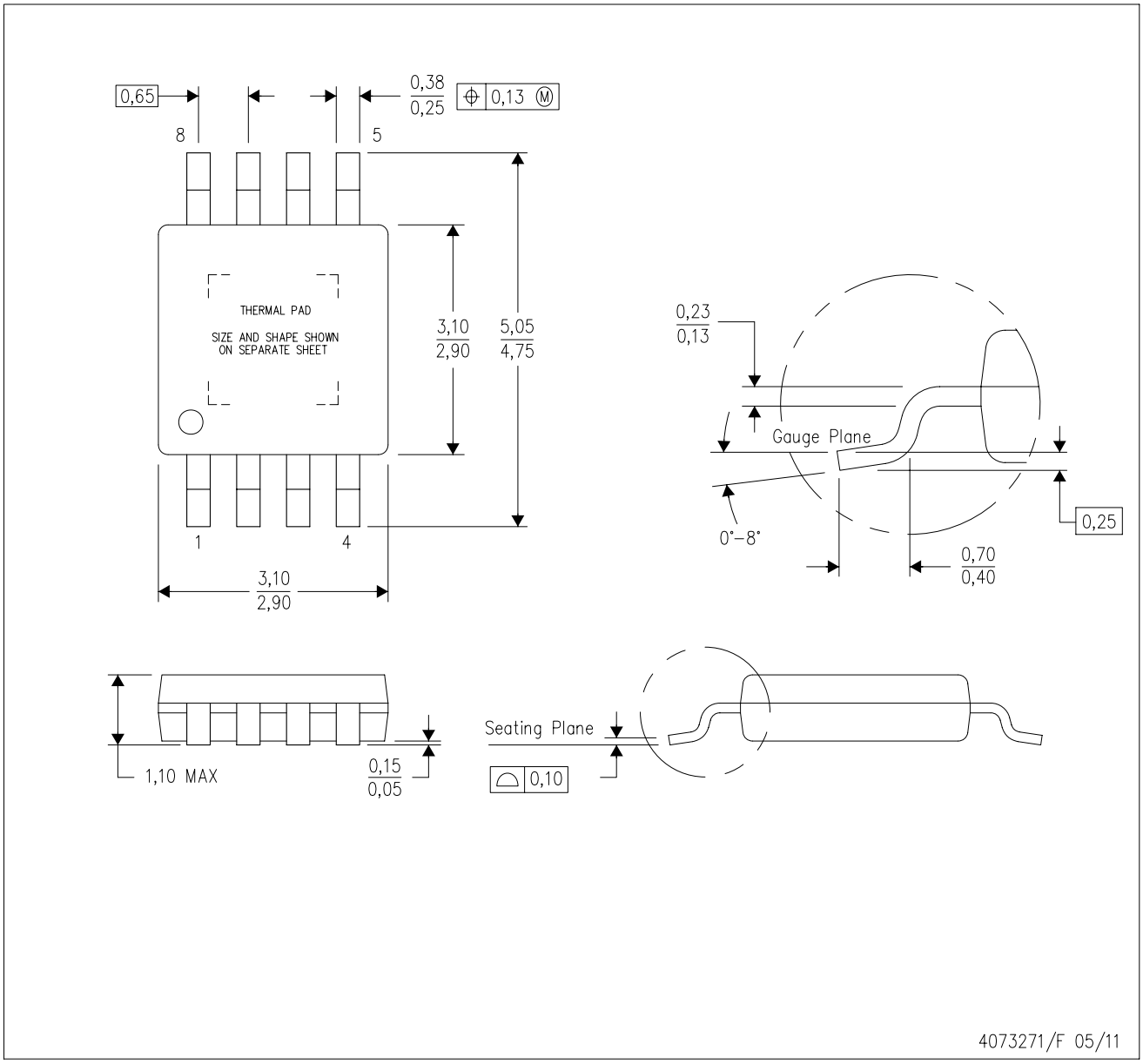
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27423DGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
UCC27423DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC27424DGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
UCC27424DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC27424DR	SOIC	D	8	2500	367.0	367.0	35.0
UCC27425DGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
UCC27425DR	SOIC	D	8	2500	340.5	338.1	20.6

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

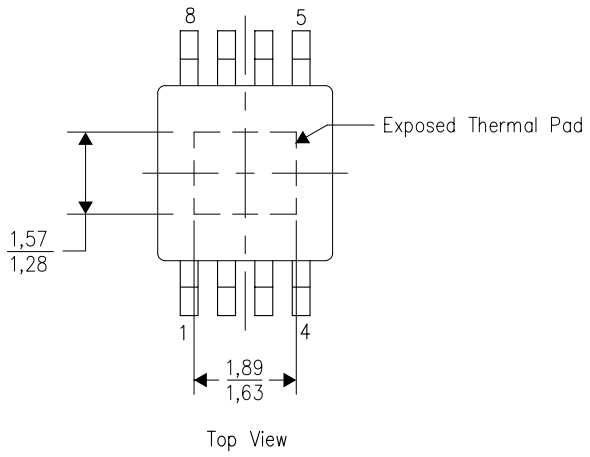
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

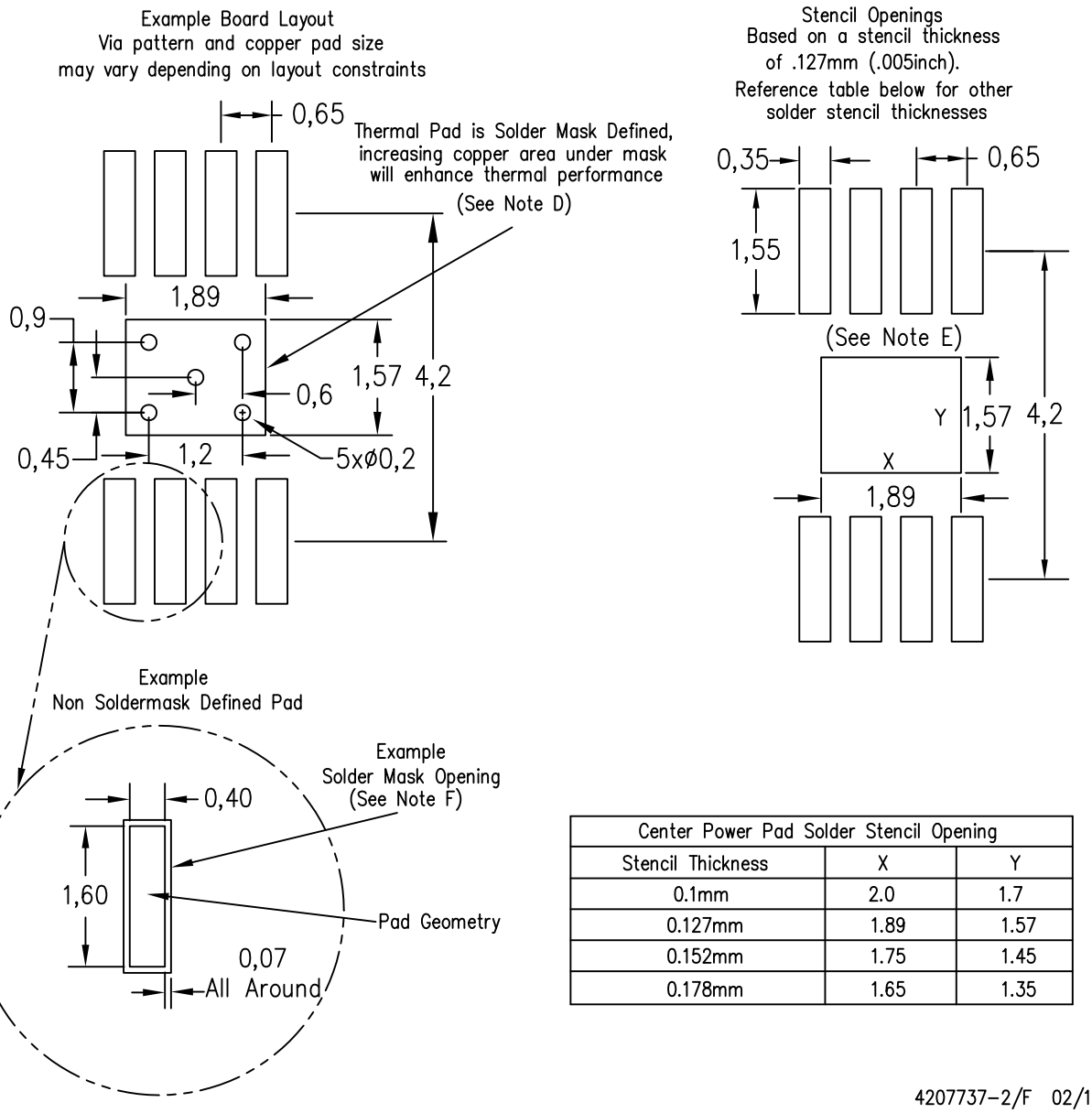
Exposed Thermal Pad Dimensions

4206323–2/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

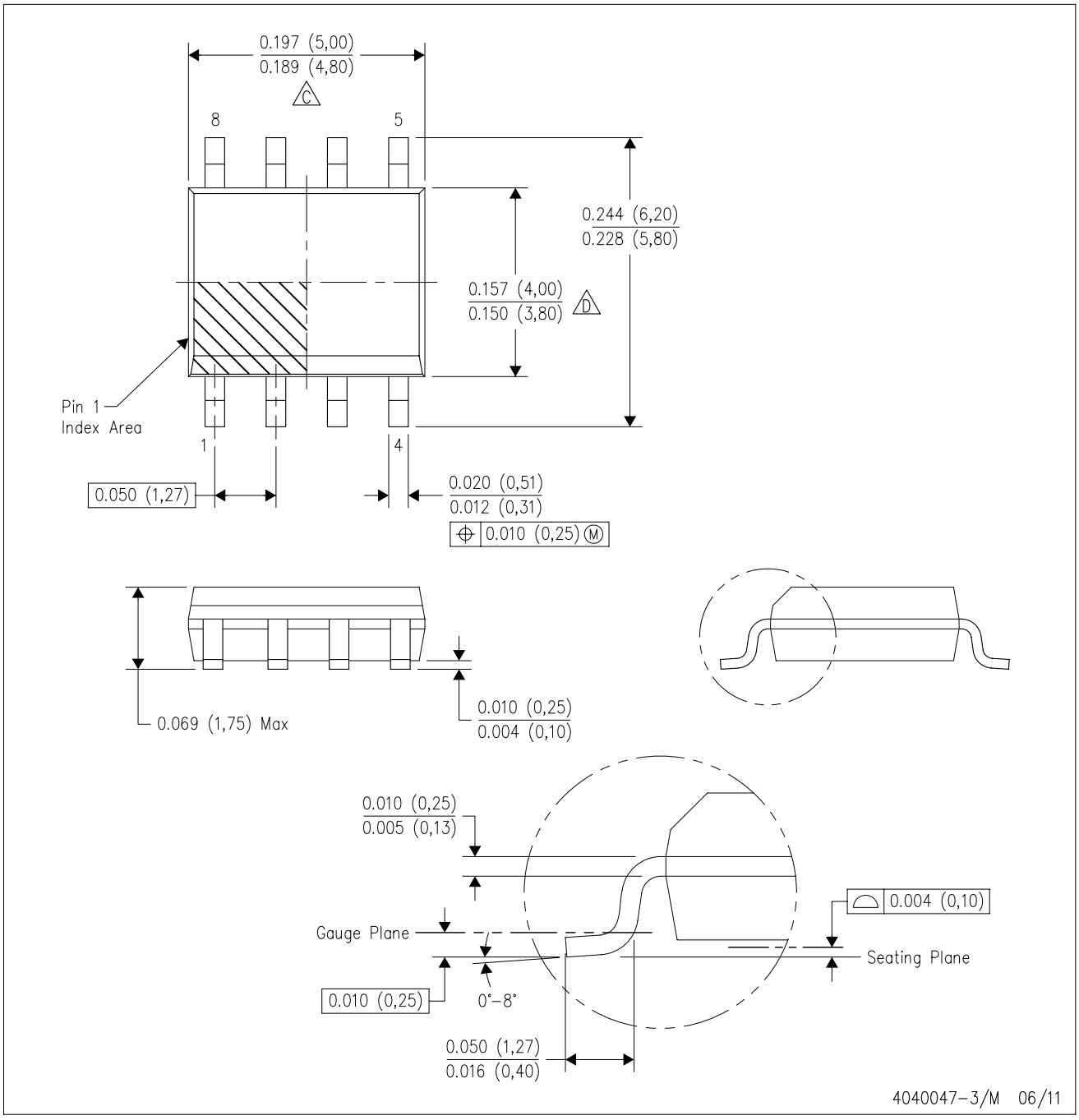


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

4207737–2/F 02/13

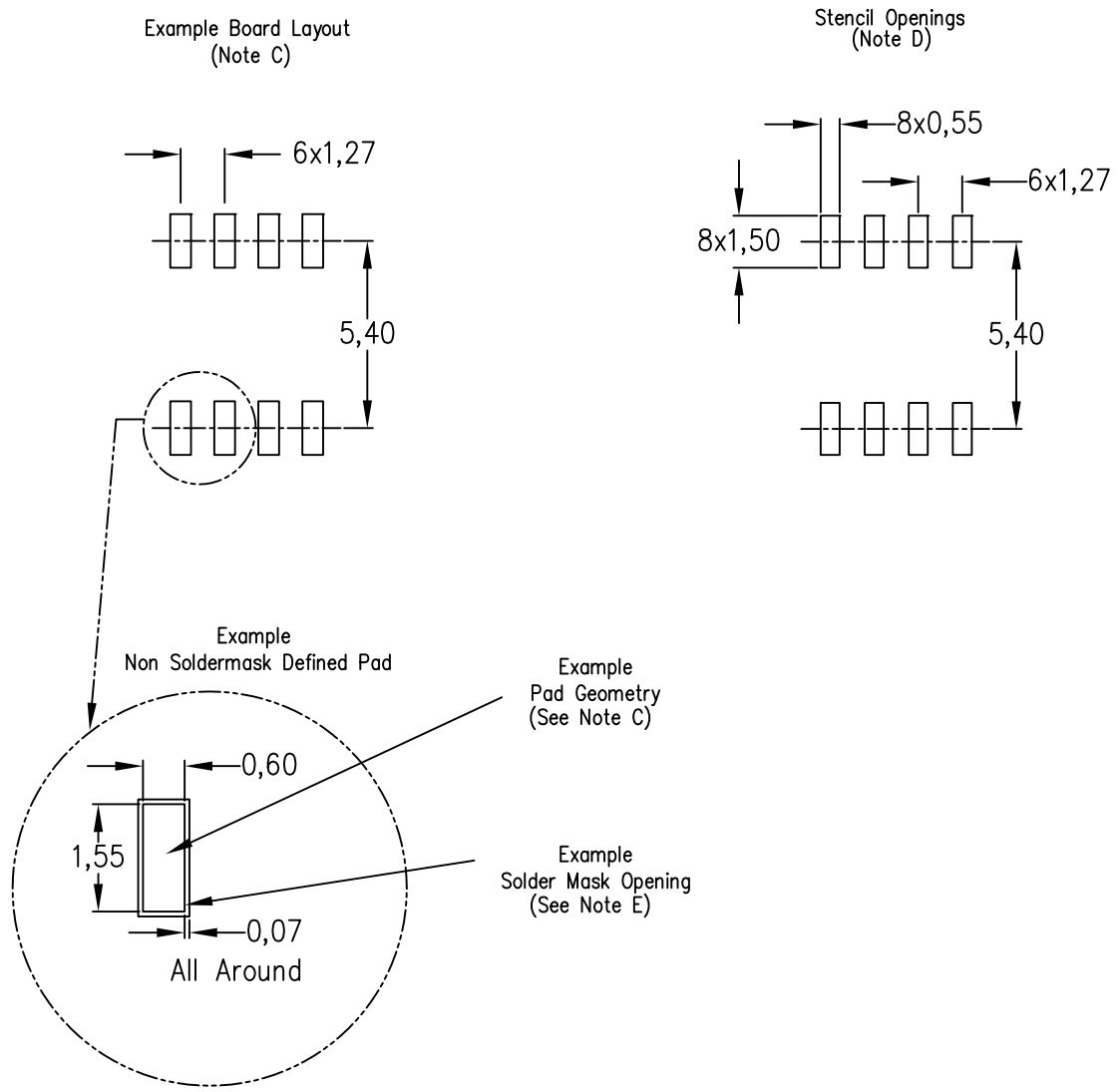
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Ferrites and accessories

Toroids (ring cores)
R 20.0 × 10.0 × 7.0

Series/Type: **B64290L0632**

Date: May 2017

EPCOS AG is a TDK Group Company.

■ Epoxy coating

R 20.0 × 10.0 × 7.00 (mm)
R 0.787 × 0.394 × 0.276 (inch)

Dimensions

d_a (mm)	d_i (mm)	Height (mm)	d_a (inch)	d_i (inch)	Height (inch)	
20.0 ±0.4	10.0 ±0.25	7.00 ±0.3	0.787 ±0.016	0.394 ±0.010	0.276 ±0.012	uncoated[1)]
21.2 max.	8.95 min.	8.1 max.	0.835 max.	0.352 min.	0.319 max.	coated

Characteristics and ordering codes

Material	A_L value nH	μ_i (approx.)	Ordering code	Magnetic characteristics				Approx. weight g
				$\Sigma l/A$ mm^{-1}	l_e mm	A_e mm^2	V_e mm^3	
N87	2130 ±25%	2200	B64290L0632X087	1.30	43.55	33.63	1465	7.6
N95	2600 ±25%	3000	B64290L0632X095					
N30	4160 ±25%	4300	B64290L0632X830					
T35	5000 ±25%	5100	B64290L0632X035					
T65	5050 ±30%	5200	B64290L0632X065					
T37	6280 ±25%	6500	B64290L0632X037					
T38	9740 ±30%	10000	B64290L0632X038					

N87: P_V (200 mT, 100 kHz, 100 °C) < 0.95 W/core
N95: P_V (200 mT, 100 kHz, 100 °C) < 0.8 W/core

1) On request.

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For detailed information see data book, chapter *"General - Definitions, 8.1"*.

Effects of core combination on A_L value

Stresses in the core affect not only the mechanical but also the magnetic properties. It is apparent that the initial permeability is dependent on the stress state of the core. The higher the stresses are in the core, the lower is the value for the initial permeability. Thus the embedding medium should have the greatest possible elasticity.

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Heating up

Ferrites can run hot during operation at higher flux densities and higher frequencies.

NiZn-materials

The magnetic properties of NiZn-materials can change irreversible in high magnetic fields.

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Processing remarks

The start of the winding process should be soft. Else the flanges may be destroyed.

- Too strong winding forces may blast the flanges or squeeze the tube that the cores can not be mounted any more.
- Too long soldering time at high temperature (>300 °C) may effect coplanarity or pin arrangement.
- Not following the processing notes for soldering of the J-leg terminals may cause solderability problems at the transformer because of pollution with Sn oxyde of the tin bath or burned insulation of the wire. For detailed information see chapter *"Processing notes"*, section 2.2.
- The dimensions of the hole arrangement have fixed values and should be understood as a recommendation for drilling the printed circuit board. For dimensioning the pins, the group of holes can only be seen under certain conditions, as they fit into the given hole arrangement. To avoid problems when mounting the transformer, the manufacturing tolerances for positioning the customers' drilling process must be considered by increasing the hole diameter.

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Symbols and terms

Symbol	Meaning	Unit
A	Cross section of coil	mm^2
A_e	Effective magnetic cross section	mm^2
A_L	Inductance factor; $A_L = L/N^2$	nH
A_{L1}	Minimum inductance at defined high saturation ($\triangleq \mu_a$)	nH
A_{min}	Minimum core cross section	mm^2
A_N	Winding cross section	mm^2
A_R	Resistance factor; $A_R = R_{Cu}/N^2$	$\mu\Omega = 10^{-6}\ \Omega$
B	RMS value of magnetic flux density	Vs/m^2, mT
ΔB	Flux density deviation	Vs/m^2, mT
$\hat{B}$	Peak value of magnetic flux density	Vs/m^2, mT
$\Delta\hat{B}$	Peak value of flux density deviation	Vs/m^2, mT
B_{DC}	DC magnetic flux density	Vs/m^2, mT
B_R	Remanent flux density	Vs/m^2, mT
B_S	Saturation magnetization	Vs/m^2, mT
C_0	Winding capacitance	F = As/V
CDF	Core distortion factor	$mm^{-4.5}$
DF	Relative disaccommodation coefficient $DF = d/\mu_i$	
d	Disaccommodation coefficient	
E_a	Activation energy	J
f	Frequency	s^{-1}, Hz
f_{cutoff}	Cut-off frequency	s^{-1}, Hz
f_{max}	Upper frequency limit	s^{-1}, Hz
f_{min}	Lower frequency limit	s^{-1}, Hz
f_r	Resonance frequency	s^{-1}, Hz
f_{Cu}	Copper filling factor	
g	Air gap	mm
H	RMS value of magnetic field strength	A/m
$\hat{H}$	Peak value of magnetic field strength	A/m
H_{DC}	DC field strength	A/m
H_c	Coercive field strength	A/m
h	Hysteresis coefficient of material	10^{-6} cm/A
$h/\mu_i{}^2$	Relative hysteresis coefficient	10^{-6} cm/A
I	RMS value of current	A
I_{DC}	Direct current	A
$\hat{I}$	Peak value of current	A
J	Polarization	Vs/m^2
k	Boltzmann constant	J/K
k_3	Third harmonic distortion	
k_{3c}	Circuit third harmonic distortion	
L	Inductance	H = Vs/A

Symbols and terms

Symbol	Meaning	Unit
$\Delta L/L$	Relative inductance change	H
L_0	Inductance of coil without core	H
L_H	Main inductance	H
L_p	Parallel inductance	H
L_{rev}	Reversible inductance	H
L_s	Series inductance	H
l_e	Effective magnetic path length	mm
l_N	Average length of turn	mm
N	Number of turns	
P_{Cu}	Copper (winding) losses	W
P_{trans}	Transferrable power	W
P_V	Relative core losses	mW/g
PF	Performance factor	
Q	Quality factor ($Q = \omega L/R_s = 1/\tan \delta_L$)	
R	Resistance	Ω
R_{Cu}	Copper (winding) resistance (f = 0)	Ω
R_h	Hysteresis loss resistance of a core	Ω
ΔR_h	R_h change	Ω
R_i	Internal resistance	Ω
R_p	Parallel loss resistance of a core	Ω
R_s	Series loss resistance of a core	Ω
R_{th}	Thermal resistance	K/W
R_V	Effective loss resistance of a core	Ω
s	Total air gap	mm
T	Temperature	°C
ΔT	Temperature difference	K
T_C	Curie temperature	°C
t	Time	s
t_v	Pulse duty factor	
$\tan \delta$	Loss factor	
$\tan \delta_L$	Loss factor of coil	
$\tan \delta_r$	(Residual) loss factor at $H \rightarrow 0$	
$\tan \delta_e$	Relative loss factor	
$\tan \delta_h$	Hysteresis loss factor	
$\tan \delta/\mu_i$	Relative loss factor of material at $H \rightarrow 0$	
U	RMS value of voltage	V
$\hat{U}$	Peak value of voltage	V
V_e	Effective magnetic volume	mm^3
Z	Complex impedance	Ω
Z_n	Normalized impedance $\lvert Z\rvert_n = \lvert Z\rvert / N^2 \times \varepsilon\ (l_e/A_e)$	Ω/mm

Ferrites and accessories

Symbols and terms

Symbol	Meaning	Unit
α	Temperature coefficient (TK)	1/K
α_F	Relative temperature coefficient of material	1/K
α_e	Temperature coefficient of effective permeability	1/K
ε_r	Relative permittivity	
Φ	Magnetic flux	Vs
η	Efficiency of a transformer	
η_B	Hysteresis material constant	mT^{-1}
η_i	Hysteresis core constant	$A^{-1}H^{-1/2}$
λ_s	Magnetostriction at saturation magnetization	
μ	Relative complex permeability	
μ_0	Magnetic field constant	Vs/Am
μ_a	Relative amplitude permeability	
μ_{app}	Relative apparent permeability	
μ_e	Relative effective permeability	
μ_i	Relative initial permeability	
μ_p'	Relative real (inductive) component of $\overline{\mu}$ (for parallel components)	
μ_p''	Relative imaginary (loss) component of $\overline{\mu}$ (for parallel components)	
μ_r	Relative permeability	
μ_{rev}	Relative reversible permeability	
μ_s'	Relative real (inductive) component of $\overline{\mu}$ (for series components)	
μ_s''	Relative imaginary (loss) component of $\overline{\mu}$ (for series components)	
μ_{tot}	Relative total permeability derived from the static magnetization curve	
ρ	Resistivity	Ωm^{-1}
$\Sigma l/A$	Magnetic form factor	mm^{-1}
τ_{Cu}	DC time constant $\tau_{Cu} = L/R_{Cu} = A_L/A_R$	s
ω	Angular frequency; $\omega = 2\ \Pi f$	s^{-1}

All dimensions are given in mm.

SMD Surface-mount device

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AN11160

Designing RC snubbers

Rev. 1 — 25 April 2012 Application note

Document information

Info	Content
Keywords	RC snubber, commutation, reverse recovery, leakage inductance, parasitic capacitance, RLC circuit and damping, MOSFET
Abstract	This document describes the design of a simple RC snubber circuit

Revision history

Rev	Date	Description
v.1	20120425	initial version

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1. Introduction

This document describes the design of a simple “RC snubber circuit”. The snubber is used to suppress high-frequency oscillations associated with reverse recovery effects in power semiconductor applications

2. Test circuit

The basic circuit is a half-bridge and shown in Figure 1.

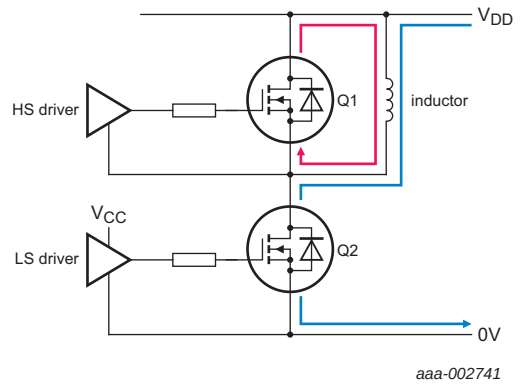


Fig 1. The half-bridge circuit

Q1 and Q2 are BUK761R6-40E devices. The inductor could also be connected to 0 V rather than V_{DD}.

Inductor current is established in the red loop; Q2 is off and current is flowing through Q1 body diode. When Q2 is turned on, current “commutates” to the blue loop and the reverse recovery effect occurs in Q1. We observe the effect of Q1 reverse recovery on the V_{DS} waveform of Q2; see Figure 2.

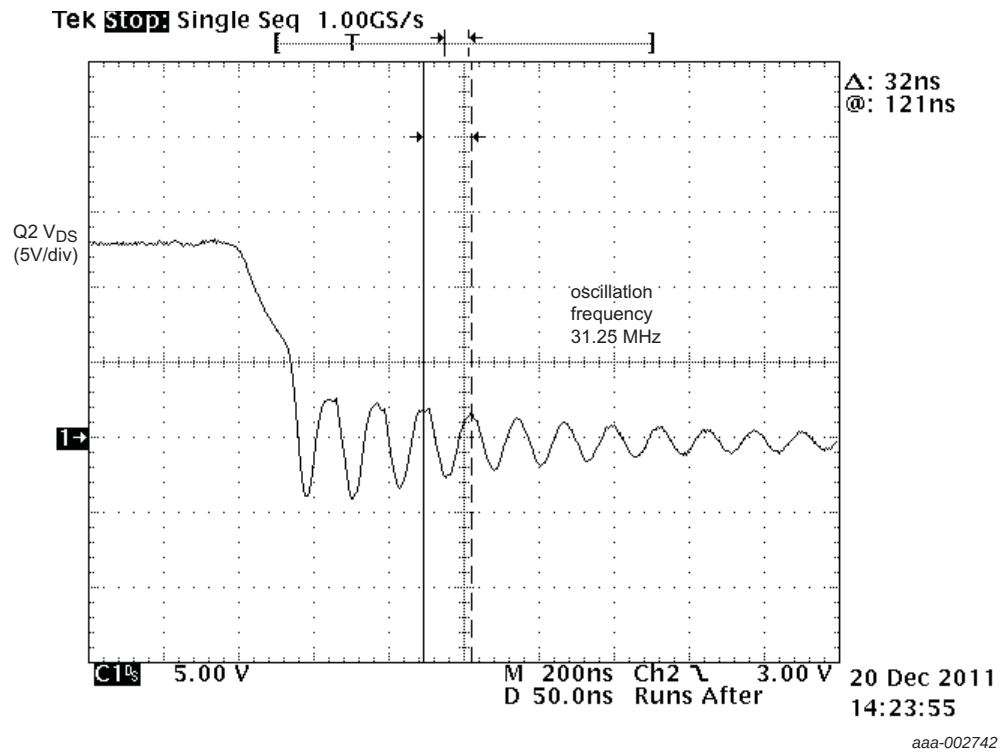


Fig 2. Reverse recovery-induced oscillation in Q2 V_{DS}

The equivalent circuit is shown in Figure 3.

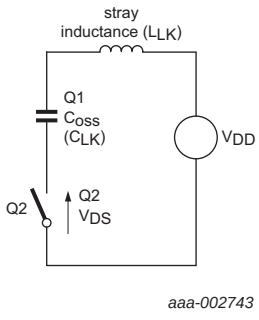


Fig 3. Equivalent circuit

We are primarily interested in the parasitic elements in the circuit:

- L_{LK} is the total stray or “leakage” inductance comprised of PCB trace inductance, device package inductance, etc.
- The parasitic capacitance C_{LK} is mainly due to C_{oss} of the upper (Q1) device.

Q2 is treated as a simple switch. The oscillation can be eliminated (snubbed) by placing an RC circuit across Q1 drain-source; see Figure 4

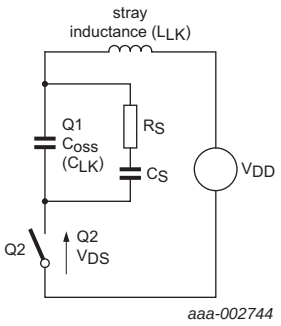


Fig 4. Equivalent circuit with snubber components R_S and C_S

3. Determining C_{LK} and L_{LK}

Before we can design the snubber, we must first determine C_{LK} and L_{LK}. We could attempt to measure C_{LK} and L_{LK} directly, but a more elegant method can be used. For this LC circuit, we know that:

$$f_{RING0} = \frac{1}{2\pi\sqrt{L_{LK}C_{LK}}} \quad (1)$$

where f_{RING0} is the frequency of oscillation without a snubber in place; see Figure 2. If we add an extra additional capacitor across Q1 (C_{add}), the initial oscillation frequency from f_{RING0} to f_{RING1} ($f_{RING1} < f_{RING0}$) will change. It can be shown that (see Section 7 "Appendix A; determining C_{LK} from C_{add}, f_{RING0} and f_{RING1}"):

$$C_{LK} = \frac{C_{add}}{x^2 - 1} \quad (2)$$

where:

$$x = \frac{f_{RING0}}{f_{RING1}} \quad (3)$$

So if we measure f_{RING0} (without C_{add}), then add a known C_{add} and measure f_{RING1}, we can determine C_{LK} and L_{LK} (two equations, two unknowns).

C_{add} = 3200 pF was added in circuit, and f_{RING1} found to be 22.2 MHz (f_{RING0} previously found to be 31.25 MHz; see Figure 2).

from Equation 3:

$$x = \frac{31.25}{22.2} = 1.41 \quad (4)$$

and from Equation 2:

$$C_{LK} = \frac{3200pF}{1.41^2 - 1} = 3239pF \quad (5)$$

Rearranging Equation 1:

$$L_{LK} = \frac{1}{(2\pi f_{RING0})^2 C_{LK}} \quad (6)$$

So with f_{RING0} = 31.25 MHz and C_{LK} = 3239 pF:

$$L_{LK} = \frac{1}{(2 \times \pi \times 3.125 \times 10^7)^2 \times 3.239 \times 10^{-9}} = 8.01 \times 10^{-9} H = 8.0nH \quad (7)$$

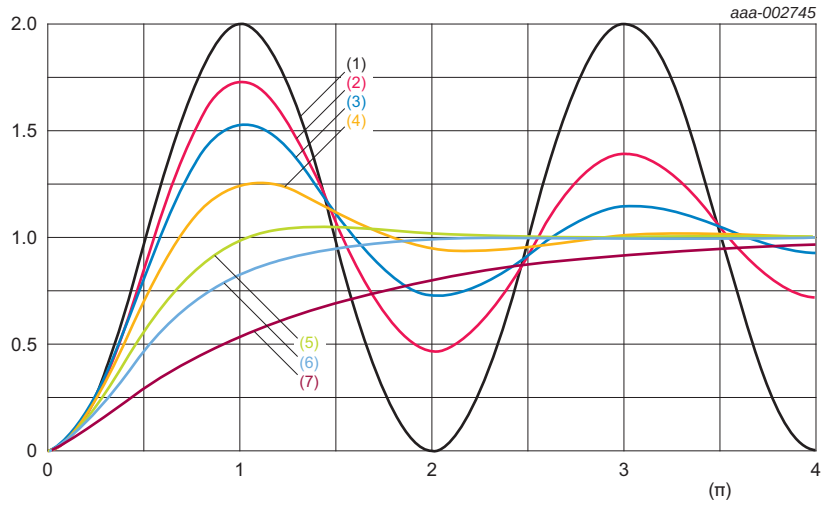
and with f_{RING1} = 22.2 MHz and (C_{LK} + C_{add}) = 3239 pF + 3200 pF = 6439 pF:

$$L_{LK} = \frac{1}{(2 \times \pi \times 2.22 \times 10^7)^2 \times 6.439 \times 10^{-9}} = 7.98 \times 10^{-9} H = 8.0nH \quad (8)$$

In other words, the calculated value of L_{LK} remains almost unchanged when we add the additional 3200 pF capacitance. This is a good sanity check of the method for determining C_{LK} and L_{LK}.

4. Designing the snubber - theory

If we replace C_S in Figure 4 with a short-circuit, then we simply have the classic RLC circuit found in text books. The response of this circuit to a step change in voltage (that is Q2 turning on) depends on the degree of damping (ζ or zeta) in the circuit; see Figure 5.



(1) ζ = 0.
(2) ζ = 0.1.
(3) ζ = 0.2.
(4) ζ = 0.4.
(5) ζ = 0.7.
(6) ζ = 1.
(7) ζ = 2.

Fig 5. Step response of an RLC circuit for various values of zeta (ζ)

In theory the circuit oscillates indefinitely if ζ = zero, although this is a practical impossibility as there is always some resistance in a real circuit. As ζ increases towards one, the oscillation becomes more damped that is, tends to decrease over time with an exponential decay envelope. This is an “underdamped” response. The case ζ = one is known as “critically damped” and is the point at which oscillation just ceases. For values of greater than one (overdamped), the response of the circuit becomes more sluggish with the waveform taking longer to reach its final value. There is therefore more than one possible degree of damping which we could build into a snubber, and choice of damping is therefore part of the snubber design process.

For this configuration of RLC circuit, the relationship between ζ, R_S, L_{LK} and C_{LK} is:

$$\varsigma = \left(\frac{1}{2R_S}\right)\sqrt{\frac{L_{LK}}{C_{LK}}} \tag{9}$$

The snubber capacitor C_S does not appear in Equation 9.

In some circuits, it is possible to damp the oscillations with R_S alone. However, in typical half-bridge circuits we cannot have a resistor mounted directly across Q1 drain source. If we did, then Q1 is permanently shorted by the resistor and the circuit as a whole would not function as required. The solution is therefore to put C_S in series with R_S, with the value of C_S chosen so as not to interfere with normal operation.

The snubber is a straightforward RC circuit whose cut-off frequency f_C is:

$$F_C = \frac{1}{2\pi R_S C_S} \tag{10}$$

Again, we must choose which value of f_C to be used, and there is no single correct answer to this question. The cut-off frequency of the snubber must be low enough to effectively short-circuit the undamped oscillation frequency f_{RING0}, but not so low as to present a significant conduction path at the operating frequency of the circuit (for example 100 kHz or whatever). A good starting point has been found to be $f_C = f_{RING0}$.

5. Designing the snubber - in practice

We now have sufficient information to design a snubber for the waveform shown in Figure 2. To recap:

C_{LK} = 3239 pF
L_{LK} = 8.0 nH
f_{RING0} = 31.25 MHz

$$\varsigma = \left(\frac{1}{2R_S}\right)\sqrt{\frac{L_{LK}}{C_{LK}}} \tag{11}$$

$$F_C = \frac{1}{2\pi R_S C_S} = f_{RING0} \tag{12}$$

The first task is to choose a value of damping (Figure 5). We have chosen ζ = 1, that is, critical damping. Rearranging Equation 11 we have:

$$R_S = \left(\frac{1}{2\zeta}\right)\sqrt{\frac{L_{LK}}{C_{LK}}} = \left(\frac{1}{2}\right)\sqrt{\frac{8.0\times10^{-9}}{3.239\times10^{-9}}} = 0.78\Omega \quad (13)$$

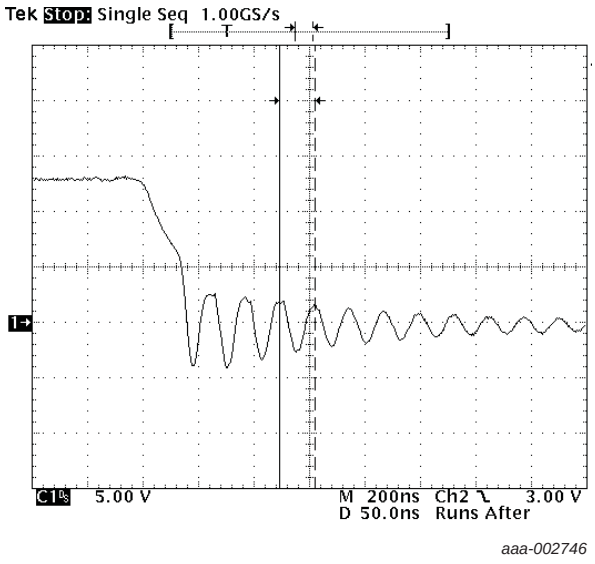
use $2 \times 1.5\ \Omega$ in parallel to give 0.75 Ω.

Rearranging Equation 12 we have:

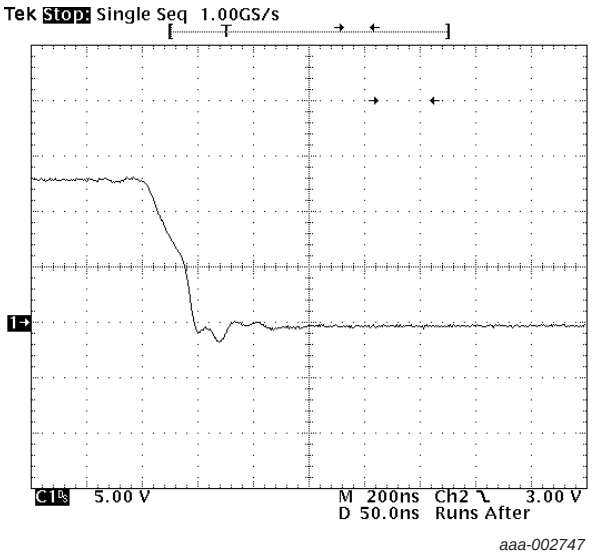
$$C_S = \frac{1}{2\pi R_S f_{RING0}} = \frac{1}{2\times\pi\times0.75\times3.125\times10^{7}} = 6.79nF \quad (14)$$

use 4.7 nF + 2.2 nF to give 6.9 nF.

The snubber was fitted across Q1 drain source. The resulting waveform is shown in Figure 6 together with the original (non-snubbed) waveform from Figure 2



a. Without snubber



b. With snubber

Vertical scale is 2 V/div.

Fig 6. Q2 V_{DS} waveform with and without snubber

As seen in Figure 6, the snubber has almost eliminated the ringing in the V_{DS} waveform. This technique could also be applied to the MOSFET in the Q2 position.

6. Summary

- Reverse recovery effects in power devices can induce high frequency oscillations in devices connected to them.
- A common technique for suppressing the oscillations is the use of an RC snubber.
- Design of an effective snubber requires the extraction of the circuit parasitic capacitance and inductance. A method has been demonstrated for doing this.
- The snubbed circuit has been shown to be a variation on the classic RLC circuit.

- A method of determining values of snubber components has been demonstrated. The method has been shown to work well, using the example of BUK761R6-40E MOSFETs

7. Appendix A; determining C_{LK} from C_{add}, f_{RING0} and f_{RING1}

We know that:

$$f_{RING0} = \frac{1}{2\pi\sqrt{L_{LK}C_{LK}}} \tag{15}$$

where f_{RING0} is the frequency of oscillation without a snubber in place and L_{LK} and C_{LK} are the parasitic inductances and capacitances respectively.

If we add capacitor C_{add} across Q1 drain-source, f_{RING0} is reduced by an amount “x” where:

$$\frac{f_{RING0}}{x} = \frac{1}{2\pi\sqrt{L_{LK}(C_{LK}+C_{add})}} \tag{16}$$

therefore

$$\frac{1}{2\pi\sqrt{L_{LK}C_{LK}}} = \frac{x}{2\pi\sqrt{L_{LK}(C_{LK}+C_{add})}} \tag{17}$$

$$\frac{1}{\sqrt{L_{LK}C_{LK}}} = \frac{x}{\sqrt{L_{LK}(C_{LK}+C_{add})}} \tag{18}$$

$$\sqrt{L_{LK}C_{LK}} = \frac{\sqrt{L_{LK}(C_{LK}+C_{add})}}{x} \tag{19}$$

$$C_{LK} = \frac{C_{LK}+C_{add}}{X^2} \tag{20}$$

$$C_{LK}x^2 - C_{LK} = C_{add} \tag{21}$$

$$C_{LK}(x^2-1) = C_{add} \tag{22}$$

$$C_{LK} = \frac{C_{add}}{x^2-1} \tag{23}$$

where:

$$x = \frac{f_{RING0}}{f_{RING1}} \tag{24}$$

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9. Contents

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For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 25 April 2012
Document identifier: AN11160

Using MPLAB® ICD 3

In-Circuit Debugger

1 Install the Latest Software

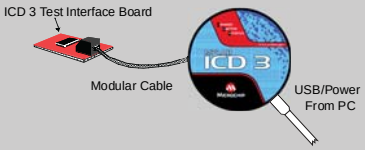
Install the MPLAB IDE software onto your PC using the MPLAB IDE CD-ROM or download the software from the MPLAB IDE page of the Microchip web site (www.microchip.com/MPLAB). Check the latest Release Notes for additional information.

2 Configure PC USB Communications

Connect MPLAB ICD 3 In-Circuit Debugger to a PC USB port via a USB cable. If the drivers do not install automatically, then install the drivers as instructed in: `C:\Program Files\Microchip\MPLAB IDE\ICD 3\Drivers\ddri.htm`.

Note: If a USB hub is used, the hub must be powered with its own power supply.

3 Use the ICD 3 Test Interface Board



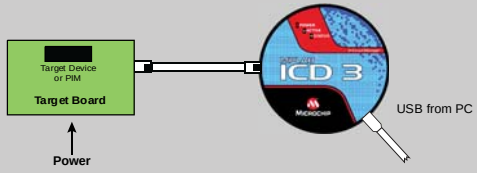
Use the supplied ICD 3 Test Interface Board to verify that the MPLAB ICD 3 is functioning properly:

1. Connect the ICD 3 Test Interface board to the debugger using the modular cable.
2. Ensure that "MPLAB ICD 3" is selected on either the Debugger or Programmer menu in MPLAB IDE.
3. From that menu, select "Settings", **Status** tab, then click on **Run ICD 3 Test Interface.** The status (pass/fail) is displayed in the Output window. If a pass message is displayed, the MPLAB ICD 3 is functioning properly.

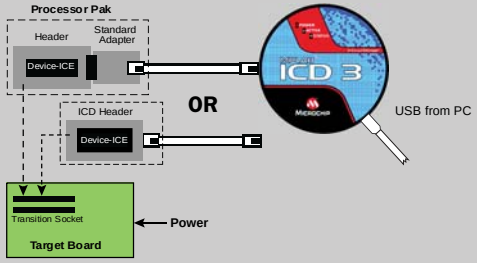
4 Connect to Target Device

1. Ensure the MPLAB ICD 3 is attached to the PC using the USB cable, if not already.
2. Remove the ICD 3 Test Interface Board and attach the modular cable between the debugger and target board.
3. Connect power to the target board.

Typical Debugger System – Device with on-board ICE circuitry



Alternate Debugger System Configuration Using an ICE Device



5 Build Your Project

1. Launch MPLAB IDE.
2. Load your project or use the Project Wizard to create a new one.
3. Build your project based on your configurations and options.
4. Attach the MPLAB ICD 3 to the PC using the USB cable.
5. Select the MPLAB ICD 3 as either a debugger (*Debugger>Select Tool*>ICD 3) or as a programmer (*Programmer>Select Programmer*>ICD 3).

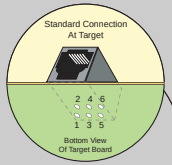
6 Program and Debug

1. Program your device.
2. As a programmer, MPLAB ICD 3 will automatically run your code. As a debugger, you can run, halt, single step and set breakpoints in your code.

ADDITIONAL INFORMATION

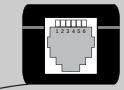
Circuitry and Connector Pinouts

Target Connector Pinout

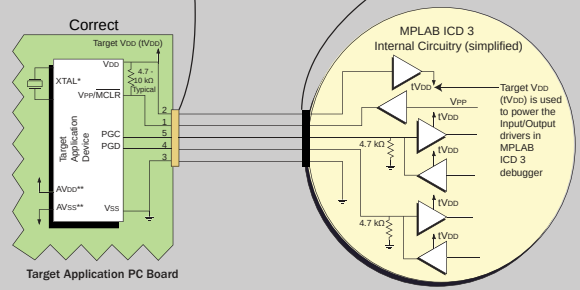


Modular Connector Pin	Microcontroller Pin
1	MCLR/VPP
2	VDD
3	Ground
4	PGD (ICSPDAT)
5	PGC (ICSPCLK)
6	PGM (LVP)

MPLAB ICD 3 RJ-11 Jack Pinout

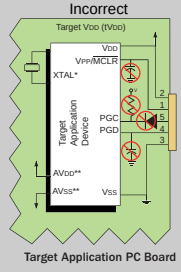


Pin	Signal
PGM	1
PGC	2
PGD	3
Ground	4
VDD	5
MCLR/VPP	6



*Target device must be running with an oscillator for the debugger to function as a debugger.
**If the device has AVDD and AVSS lines, they must be connected for the debugger to operate.

Target Circuit Design Precautions



- **Do not use greater than 100 µF capacitance on VDD** – depending on the overall load, it will prevent the target from powering quickly when MPLAB ICD 3 is the source of power.
- **Do not use capacitors on MCLR** – they will prevent fast transitions of VPP.
- **Do not use pull-ups on PGC/PGD** – they will divide the voltage levels since these lines have 4.7 kΩ pull-down resistors in MPLAB ICD 3.
- **Do not use multiplexing on PGC/PGD** – they are dedicated for communications to MPLAB ICD 3.
- **Do not use capacitors on PGC/PGD** – they will prevent fast transitions on data and clock lines during programming and debug communications.
- **Do not use diodes on PGC/PGD** – they will prevent bidirectional communication between MPLAB ICD 3 and the target PIC® MCU.

Recommended Settings

COMPONENT	SETTING
Oscillator	• OSC bits set properly • Running
Power	Supplied by target
WDT	Disabled (device dependent)
Code-Protect	Disabled
Table Read Protect	Disabled
LVP	Disabled
BOD	VDD > BOD VDD min
JTAG	Disabled
AVDD and AVSS	Must be connected
PGCx/PGDx	Proper channel selected, if applicable
Programming	VDD voltage levels meet programming specs

Note: See the *MPLAB ICD 3 User's Guide* for more component and setting information.

Reserved Resources

For information on reserved resources used by the debugger, see the MPLAB ICD 3 on-line help.

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MICROCHIP

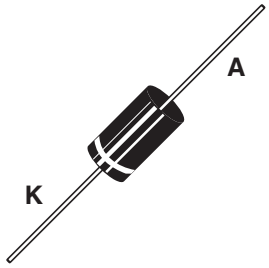
1.5KE

Transil™

Datasheet – production data

Features

- Peak pulse power: 1500 W (10/1000 µs)
- Breakdown voltage range:
  From 6.8 V to 440 V
- Uni and bidirectional types
- Low clamping factor
- Fast response time
- UL 497B file number: QVGQ2.E136224



DO-201

Description

Transil diodes provide high overvoltage protection by clamping action. Their instantaneous response to transient overvoltages makes them particularly suited to protect voltage sensitive devices such as MOS Technology and low voltage supplied IC's.

TM: Transil is a trademarks of STMicroelectronics.

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
P_{PP}	Peak pulse power dissipation (1)	$T_{j\ initial} = T_{amb}$	1500	W
P	Power dissipation on infinite heatsink	T_{amb} = 75 °C	5	W
I_{FSM}	Non repetitive surge peak forward current for unidirectional types	t_p = 10 ms $T_{j\ initial} = T_{amb}$	200	A
T_{stg}	Storage temperature range		-65 to + 175	°C
T_j	Maximum operating junction temperature		175	°C
T_L	Maximum lead temperature for soldering during 10s at 5mm from case.		230	°C

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

Table 2. Thermal parameter

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction to leads	20	°C/W
$R_{th(j-a)}$	Junction to ambient on printed circuit. L_{lead} = 10 mm	75	

Figure 1. Electrical characteristics - definitions

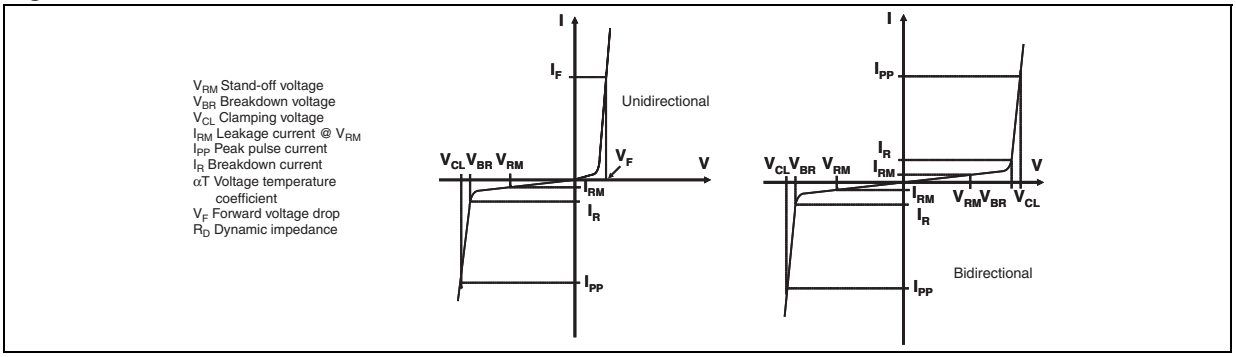


Table 3. Electrical characteristics - parameter values (T_{amb} = 25 °C)

Order code	I_{RM} @ V_{RM}		V_{BR} @ I_R(1)				V_{CL} @ I_{PP} 10/1000 µs		V_{CL} @ I_{PP} 8/20 µs		αT(2)	C(3)
	max.		max.	nom.	min.		max.		max.		max.	typ.
	µA	V	V	V	V	mA	V	A	V	A	10-4/ °C	pF
1.5KE6V8A/CA	1000	5.8	6.45	6.8	7.14	10	10.5	143	13.4	746	5.7	9500
1.5KE7V5A/CA	500	6.4	7.13	7.5	7.88	10	11.3	132	14.5	690	6.1	8500
1.5KE10A/CA	10	8.55	9.5	10	10.5	1	14.5	100	18.6	538	7.3	7000
1.5KE12A/CA	5	10.2	11.4	12	12.6	1	16.7	90	21.7	461	7.8	6000
1.5KE15A/CA	1	12.8	14.3	15	15.8	1	21.2	71	27.2	368	8.4	5000
1.5KE18A/CA	1	15.3	17.1	18	18.9	1	25.2	59.5	32.5	308	8.8	4300
1.5KE22A/CA	1	18.8	20.9	22	23.1	1	30.6	49	39.3	254	9.2	3700
1.5KE24A/CA	1	20.5	22.8	24	25.2	1	33.2	45	42.8	234	9.4	3500
1.5KE27A/CA	1	23.1	25.7	27	28.4	1	37.5	40	48.3	207	9.6	3200
1.5KE30A/CA	1	25.6	28.5	30	31.5	1	41.5	36	53.5	187	9.7	2900
1.5KE33A/CA	1	28.2	31.4	33	34.7	1	45.7	33	59.0	169	9.8	2700
1.5KE36A/CA	1	30.8	34.2	36	37.8	1	49.9	30	64.3	156	9.9	2500
1.5KE39A/CA	1	33.3	37.1	39	41.0	1	53.9	28	69.7	143	10.0	2400
1.5KE47A/CA	1	40.2	44.7	47	49.4	1	64.8	23.2	84	119	10.1	2050
1.5KE56A/CA	1	47.8	53.2	56	58.8	1	77	19.5	100	100	10.3	1800
1.5KE62A/CA	1	53.0	58.9	62	65.1	1	85	17.7	111	90	10.4	1700
1.5KE68A/CA	1	58.1	64.6	68	71.4	1	92	16.3	121	83	10.4	1550
1.5KE82A/CA	1	70.1	77.9	82	86.1	1	113	13.3	146	69	10.5	1350
1.5KE100A/CA	1	85.5	95.0	100	105	1	137	11	178	56	10.6	1150
1.5KE120A/CA	1	102	114	120	126	1	165	9.1	212	47	10.7	1000
1.5KE150A/CA	1	128	143	150	158	1	207	7.2	265	38	10.8	850
1.5KE180A/CA	1	154	171	180	189	1	246	6.1	317	31.5	10.8	725
1.5KE200A/CA	1	171	190	200	210	1	274	5.5	353	28	10.8	675
1.5KE220A/CA	1	188	209	220	231	1	328	4.6	388	26	10.8	625
1.5KE250A/CA	1	213	237	250	263	1	344	5.0	442	23	11	560
1.5KE300A/CA	1	256	285	300	315	1	414	5.0	529	19	11	500
1.5KE350A/CA	1	299	332	350	368	1	482	4.0	618	16	11	430
1.5KE400A/CA	1	342	380	400	420	1	548	4.0	706	14	11	390
1.5KE440A/CA	1	376	418	440	462	1	603	3.5	776	13	11	360

1. Pulse test: t_p < 50 ms (see *Figure 2*)
2. $\Delta V_{BR} = \alpha T \times (T_{amb} - 25) \times V_{BR}(25\ °C)$
3. V_R = 0 V, F = 1 MHz. For bidirectional types, capacitance value is divided by 2.

Figure 2. Pulse definition for electrical characteristics

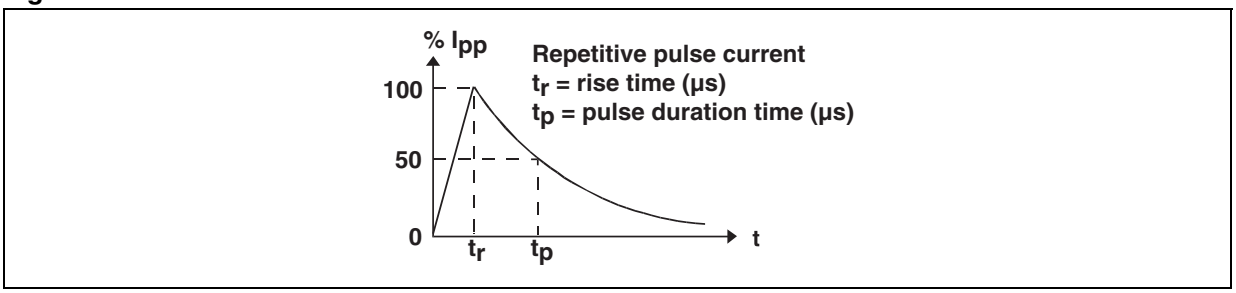


Figure 3. Peak pulse power dissipation versus initial junction temperature (printed circuit board)

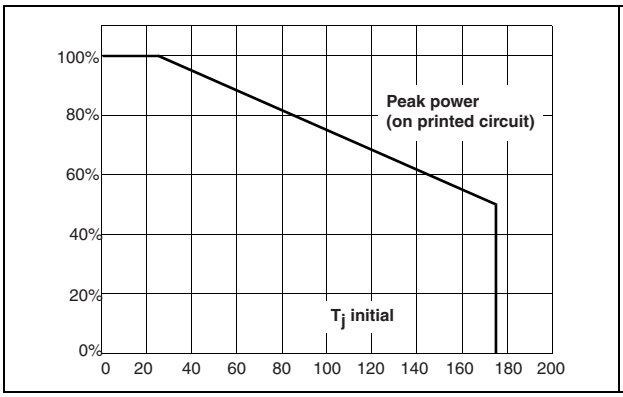


Figure 4. Peak pulse power versus exponential pulse duration

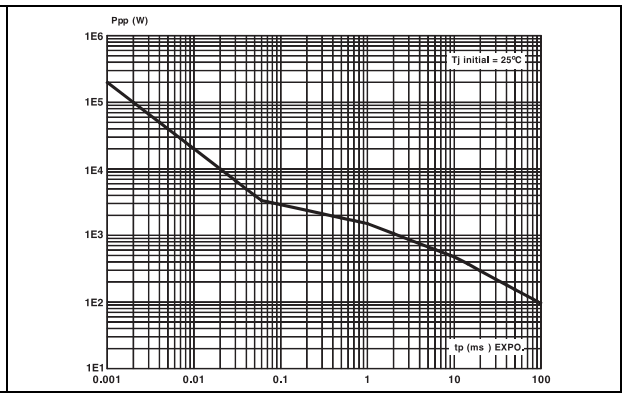


Figure 5. Clamping voltage versus peak pulse current

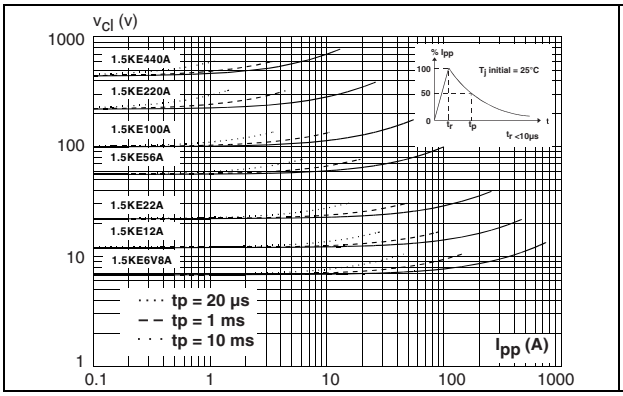
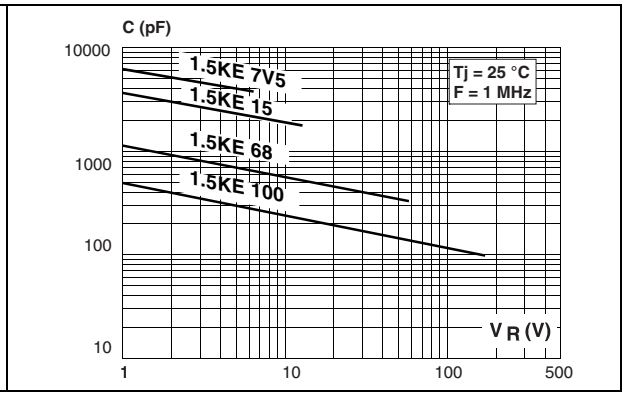


Figure 6. Capacitance versus reverse applied voltage for unidirectional types (typical values)



The curves of *Figure 5* are specified for a junction temperature of 25 °C before surge. The given results may be extrapolated for other junction temperatures by using the following formula:

$\Delta V_{BR} = \alpha T \times (Tamb - 25) \times V_{BR}$ (25 °C).

For intermediate voltages, extrapolate the given results.

Figure 7. Capacitance versus reverse applied voltage for bidirectional types (typical values)

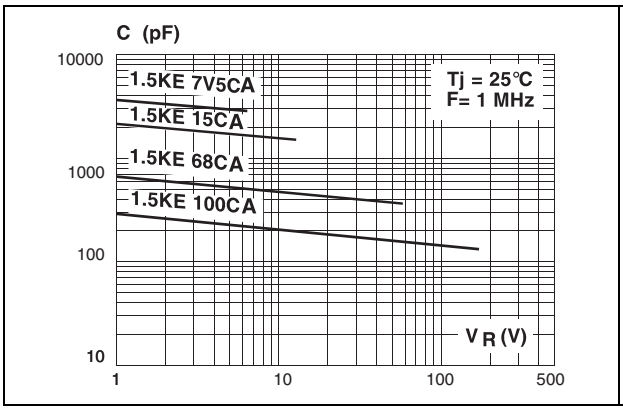


Figure 8. Peak forward voltage drop versus peak forward current (typical values for unidirectional types)

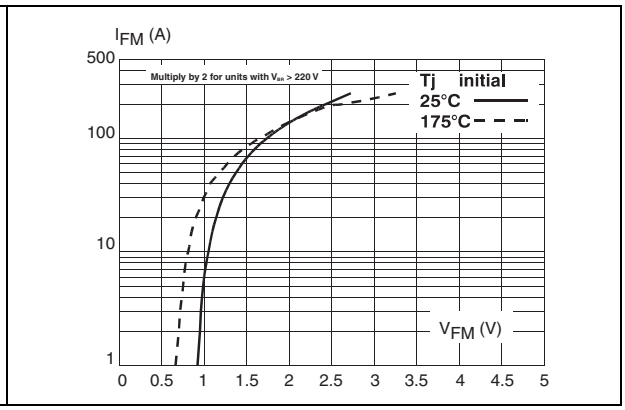


Figure 9. Transient thermal impedance junction-ambient versus pulse duration

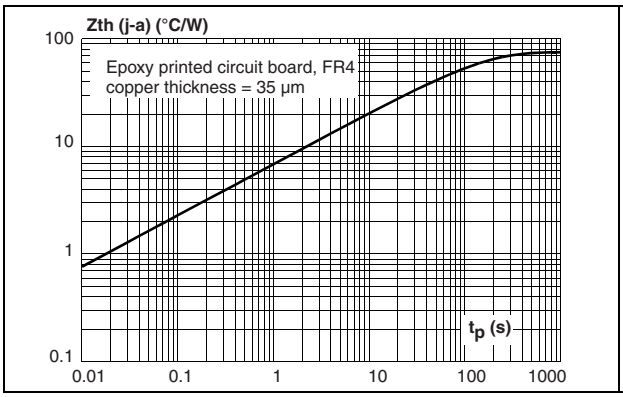
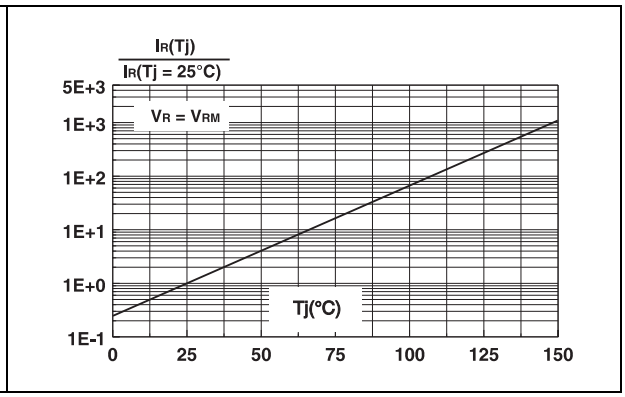
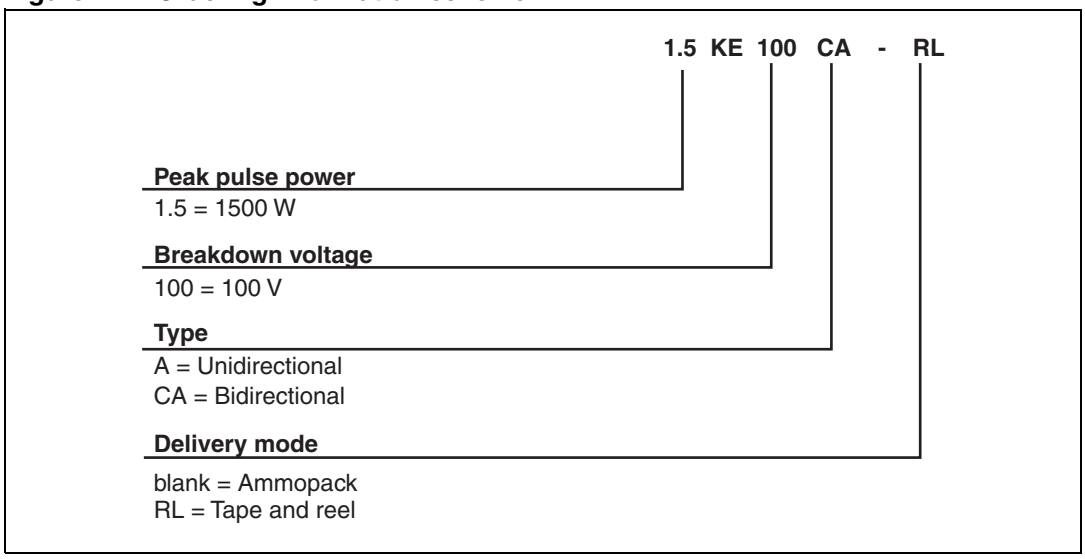


Figure 10. Relative variation of leakage current versus junction temperature



2 Ordering information scheme

Figure 11. Ordering information scheme

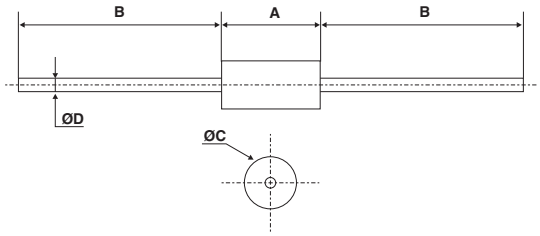


3 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 4. DO-201 dimensions



Ref.	dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	8.5	9.5	0.335	0.374
B	25.4		1	
Ø C	4.8	5.3	0.189	0.209
Ø D	0.96	1.06	0.038	0.042

Table 5. Marking

Order code	Marking[1]		Order code	Marking[1]	
1.5KE6V8A	1.5KE 6V8A	1.5KE6V8A	1.5KE6V8CA	1.5KE 6V8CA	1.5KE6V8CA
1.5KE7V5A	1.5KE 7V5A	1.5KE7V5A	1.5KE7V5CA	1.5KE 7V5CA	1.5KE7VCA5
1.5KE10A	1.5KE 10A	1.5KE10A	1.5KE10CA	1.5KE 10CA	1.5KE10CA
1.5KE12A	1.5KE 12A	1.5KE12A	1.5KE12CA	1.5KE 12CA	1.5KE12CA
1.5KE15A	1.5KE 15A	1.5KE15A	1.5KE15CA	1.5KE 15CA	1.5KE15CA
1.5KE18A	1.5KE 18A	1.5KE18A	1.5KE18CA	1.5KE 18CA	1.5KE18CA
1.5KE22A	1.5KE 22A	1.5KE22A	1.5KE22CA	1.5KE 22CA	1.5KE22CA
1.5KE24A	1.5KE 24A	1.5KE24A	1.5KE24CA	1.5KE 24CA	1.5KE24CA
1.5KE27A	1.5KE 27A	1.5KE27A	1.5KE27CA	1.5KE 27CA	1.5KE27CA
1.5KE30A	1.5KE 30A	1.5KE30A	1.5KE30CA	1.5KE 30CA	1.5KE30CA
1.5KE33A	1.5KE 33A	1.5KE33A	1.5KE33CA	1.5KE 33CA	1.5KE33CA
1.5KE36A	1.5KE 36A	1.5KE36A	1.5KE36CA	1.5KE 36CA	1.5KE36CA
1.5KE39A	1.5KE 39A	1.5KE39A	1.5KE39CA	1.5KE 39CA	1.5KE39CA
1.5KE47A	1.5KE 47A	1.5KE47A	1.5KE47CA	1.5KE 47CA	1.5KE47CA
1.5KE56A	1.5KE 56A	1.5KE56A	1.5KE56CA	1.5KE 56CA	1.5KE56CA
1.5KE62A	1.5KE 62A	1.5KE62A	1.5KE62CA	1.5KE 62CA	1.5KE62CA
1.5KE68A	1.5KE 68A	1.5KE68A	1.5KE68CA	1.5KE 68CA	1.5KE68CA
1.5KE82A	1.5KE 82A	1.5KE82A	1.5KE82CA	1.5KE 82CA	1.5KE82CA
1.5KE100A	1.5KE 100A	1.5KE100A	1.5KE100CA	1.5KE 100CA	1.5KE100CA
1.5KE120A	1.5KE 120A	1.5KE120A	1.5KE120CA	1.5KE 120CA	1.5KE120CA
1.5KE150A	1.5KE 150A	1.5KE150A	1.5KE150CA	1.5KE 150CA	1.5KE150CA
1.5KE180A	1.5KE 180A	1.5KE180A	1.5KE180CA	1.5KE 180CA	1.5KE180CA
1.5KE200A	1.5KE 200A	1.5KE200A	1.5KE200CA	1.5KE 200CA	1.5KE200CA
1.5KE220A	1.5KE 220A	1.5KE220A	1.5KE220CA	1.5KE 220CA	1.5KE220CA
1.5KE250A	1.5KE 250A	1.5KE250A	1.5KE250CA	1.5KE 250CA	1.5KE250CA
1.5KE300A	1.5KE 300A	1.5KE300A	1.5KE300CA	1.5KE 300CA	1.5KE300CA
1.5KE350A	1.5KE 350A	1.5KE350A	1.5KE350CA	1.5KE 350CA	1.5KE350CA
1.5KE400A	1.5KE 400A	1.5KE400A	1.5KE400CA	1.5KE 400CA	1.5KE400CA
1.5KE440A	1.5KE 440A	1.5KE440A	1.5KE440CA	1.5KE 440CA	1.5KE440CA

1. Marking with space is used to differentiate assembly location.

4 Ordering information

Table 6. Order codes

Order code	Marking	Package	Weight	Base qty	Delivery mode
1.5KExxxA/CA(1)	See *Table 5*	1.5KE	0.876g	1900	Tape and reel
				600	Ammopack

1. Where xxx is nominal value of V_{BR} and A or CA indicates unidirectional or bidirectional version. See *Table 3* for list of available devices and their order codes

5 Revision history

Table 7. Document revision history

Date	Revision	Changes
Feb -2002	3A	Last issue
12-Mar-2012	4	Added UL statement, *Table 5* and ordering information.

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