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Folded Cascode OTA with 5540 MHz·pF/mA FoM

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***Abstract*— A micropower single-stage folded cascode amplifier able to drive a wide range of capacitive loads is presented. It features class AB operation and includes power-efficient adaptive biasing techniques, which provide enhanced dynamic output current boosting and gain-bandwidth product (GBW). Phase lead compensation is used to improve phase margin and settling performance for low capacitive loads. Measurement results for a 0.5 µm CMOS process show a FoM of 5540 MHz·pF/mA, the highest one reported to date for a folded cascode amplifier to the authors' knowledge.**

***Keywords*— Folded Cascode, Amplifiers, Analog integrated circuits, CMOS integrated circuits, Adaptive Biasing, Class AB circuits.**

I. Introduction

Current and emerging portable and wearable applications (such as 4G/5G cellular networks, WSNs, or IoT scenarios) lead to a wide interest in low-power wireless electronic devices. Conciliating the increased performance that these technologies demand with the limited power coming from small batteries (or even from ambient energy scavenging) is a significant challenge. The Operational Transconductance Amplifier (OTA) is a critical analog building block and for many of these applications is the largest and most power consuming block [1].

The folded cascode (FC) is one of the most used OTAs in both single stage configuration and as the first stage of multi-stage topologies. This is due to its high gain and relatively large signal swing. The PMOS input version is often preferred due to its lower flicker noise, higher speed and suitable input common-mode level allowing NMOS-only switches in switched-capacitor (SC) circuits [1].

In conventional FC OTAs, the current sources used to bias the folding stage do not contribute to the OTA transconductance and limit the slew rate (SR). To overcome these issues, current recycling [1-4] or multipath techniques [5] have been proposed, replacing these current sources by active current mirrors. However, these approaches are not power efficient, as they create internal replicas of large dynamic currents at the additional branches [6]. Furthermore, the SR improvement is limited since SR is still proportional to the bias current. In this paper, a simple modification to the conventional FC OTA is presented which enhances performance avoiding these issues. A prior version was reported in [7] showing ability to drive in a power efficient manner large capacitive loads. In this paper a modification using lead compensation is proposed which allows preserving a large phase margin for lower capacitive loads.

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II. Principle of Operation

Figure 1(a) shows the schematic of a typical FC OTA. The GBW and SR of this circuit are:

$$GBW = \frac{g_{m1,2}}{2\pi C_L} \quad (1)$$

$$SR = \frac{I_{B2}}{C_L} \quad (2)$$

being $g_{m1,2}$ the small-signal transconductance of M_1 and M_2. Since the differential pair transistors are the only ones that contribute to the OTA transconductance, GBW is limited. As mentioned, a large percentage of power is used in the folding stage, without increasing its transconductance. In addition, the constant bias current I_{B2} of the folding stage limits the maximum output current, thus limiting the SR.

Fig. 1(b) shows the proposed Class AB OTA. Constant currents I_{B1} bias transistors M_3 and M_4, matched to M_1 and M_2, operating as DC level shifters [6]. The quiescent currents of M_1 and M_2 are set to I_{B1} by the resulting DC level shift. As the differential input voltage is applied to the gate and to the source of M_1 and M_2, the transconductance of the input differential pair is doubled.

Quasi-Floating Gate (QFG) techniques [8] are used to adaptively bias the folding stage. The gates of M_5 (M_{10}) and M_6 (M_9) are connected through floating capacitors C_{BAT}. High resistance devices (R_{large}) are obtained by using minimum-size transistors M_{R1} and M_{R2}. In quiescent operation, C_{BAT} is an open circuit so no current flows across M_{R1} and M_{R2}. Thus, the folding stages in Fig. 1(a) and Fig. 1(b) are equivalent without input signal. If a large positive input $V_{id}=V_{in+}-V_{in-}$ appears, there is a decrease in the gate voltage of M_5 and an increase in that of M_6. Due to the high resistive value of M_{R1} and M_{R2}, capacitors C_{BAT} do not discharge rapidly, behaving as floating batteries. This way, the gate voltage of M_{10} decreases and that of M_9

increases, yielding a large output current sourced to the load, which leads to a large positive Slew Rate SR_+. In a complementary way, a large output current is sunk from the load when negative V_{id} is applied, yielding a large SR_-. The GBW and SR of the circuit of Fig. 1(b) are:

$$GBW = \frac{2g_{m1,2}}{2\pi C_L}\left(1+\alpha\frac{g_{m9,10}}{g_{m5,6}}\right) \quad (3)$$

$$SR \approx \frac{I_{B2}}{C_L}\left(1+\alpha\sqrt{\frac{\beta_{9,10}}{\beta_{5,6}}}\right)^2 \quad (4)$$

with $\alpha \approx C_{BAT}/(C_{BAT}+C_{gs9,10})$ and β_i, the transconductance factor of transistor M_i, defined by $\beta_i=\mu C_{ox}(W/L)_i$.

2.A. Stability analysis

Both OTAs in Fig. 1 have a dominant pole $\omega_{p1} = -1/(R_{out}\, C_{out})$ at the output node and a non-dominant pole $\omega_{p2} \approx -g_{m9c}/C_1$ at the drain of M_1 and M_2, with $C_{out} \approx C_L$ and C_1 the capacitance at the drain of M_1, which is dominated by C_{gs9c}. Moreover, due to the additional signal path introduced in the proposed OTA, a new non-dominant pole $\omega_{p3} \approx -g_{m5}/(C_{gs5}+\alpha C_{gs10})$ is generated. It can be expected that $\omega_{p3} < \omega_{p2}$, because ω_{p3} is set by PMOS transistors and since $C_{gs5}+\alpha C_{gs10}$ is usually larger than C_{p9}. Therefore, the phase margin of the proposed OTA is smaller than the one of the conventional FC OTA. This leads to the need of relatively large C_L values, restricting the OTA applications.

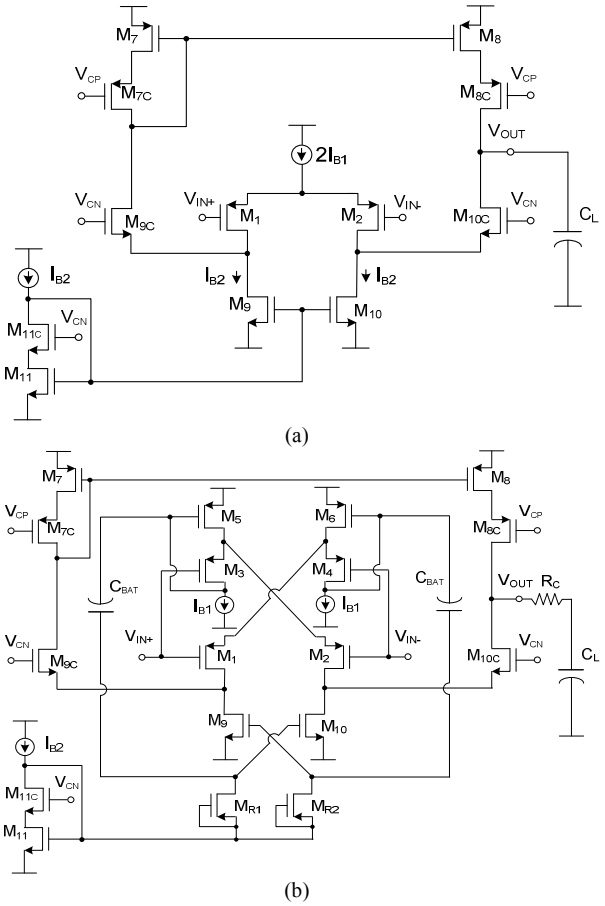

Fig. 1. (a) Conventional FC OTA (b) Proposed FC OTA.

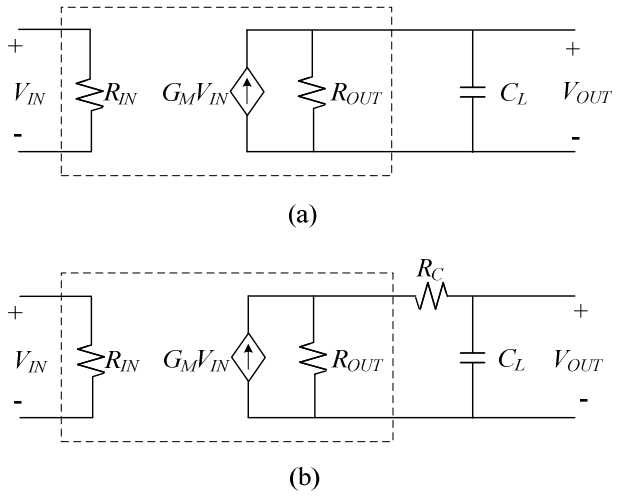

Fig. 2. Simplified AC model (a) Purely capacitive load (b) With lead compensation.

2.B. Lead compensation

To solve this issue, lead compensation at the output terminal is proposed, as shown in Fig. 1(b). This way, lower C_L values can be employed. To analyze the effect of the added resistor R_C, the basic single-pole AC model of the FC OTA shown in Fig. 2 will be used for simplicity. The transfer function of Fig. 2(a) is

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{G_m R_{out}}{1+sR_{out}C_L} \quad (5)$$

If a resistor R_C is placed in series with the capacitive load, as shown in Fig. 2(b), the transfer function $H(s)$ becomes:

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{G_m R_{out}(1+sR_C C_L)}{1+s(R_{out}+R_C)C_L} \quad (6)$$

Hence the lead resistance R_C creates a zero $\omega_z \approx -1/(R_C\, C_L)$ that can be placed at different locations to improve phase margin and settling performance [9]. The strategy followed here is to choose R_C in order to make ω_z slightly larger than the unity-gain frequency, leading to a phase lead equal to $\arctan(\omega_z/GBW)$ rads in the phase margin.

As it can be seen in (6), the output pole is modified by R_C, but if $R_C \ll R_{OUT}$, this variation can be neglected.

III. Measurement Results

A double-poly n-well CMOS process was used to fabricate the two circuits of Fig. 1. The nominal NMOS and PMOS threshold voltages are 0.67 V and –0.96 V, respectively. A photograph of the chip is shown in Fig. 3. The silicon area employed for the class A FC OTA of Fig. 1(a) was 0.020 mm^2 and that of the class AB OTA of Fig. 1(b) was 0.024 mm^2. This 20% increase is due to the poly-poly capacitors C_{BAT}, whose value was 700 fF. Table I shows the transistor sizes employed. Supply voltages were ±1 V, and the bias currents were $I_{B2}=2I_{B1}=20$ µA. Cascode bias voltages V_{CP} and V_{CN} were set to -0.2 V and 0 V, respectively.

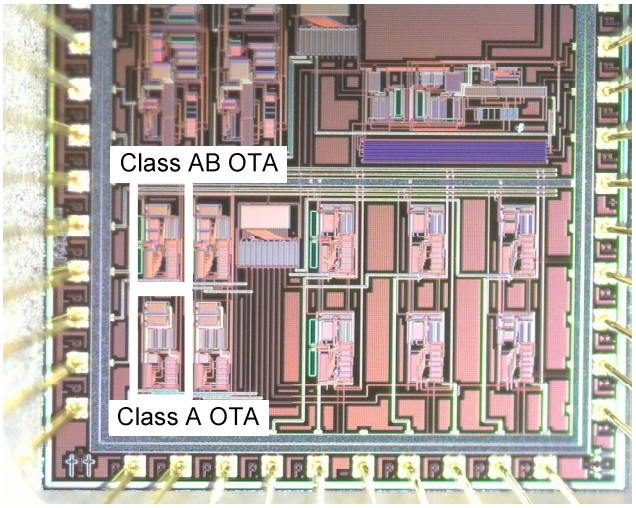

Fig. 3. Test chip microphotograph.

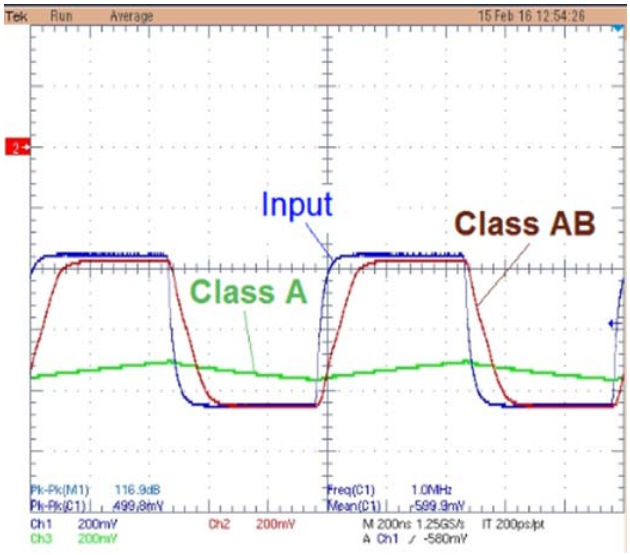

Fig. 4. Measured transient response for large C_L.

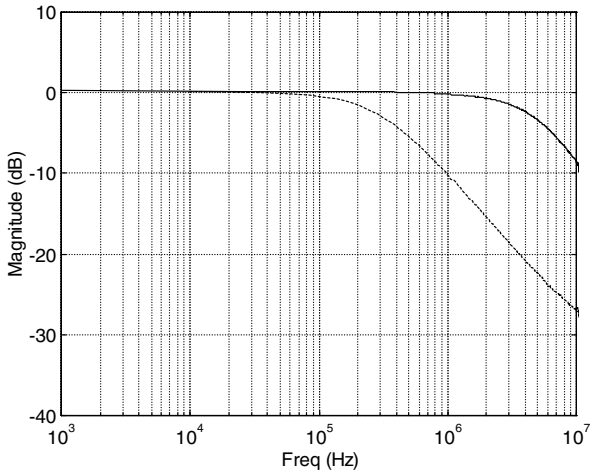

Fig. 5. Measured closed-loop magnitude response in buffer configuration.

TABLE I - TRANSISTOR ASPECT RATIOS

Transistor	W/L (μm/μm)
M_1-M_4	100/1
M_5-M_6	9/0.6
M_7-M_8	200/1
M_{7C}-M_{10C}	200/0.6
M_9-M_{11}	120/0.6
M_{11C}	100/0.6
M_{R1}-M_{R2}	1.5/0.6

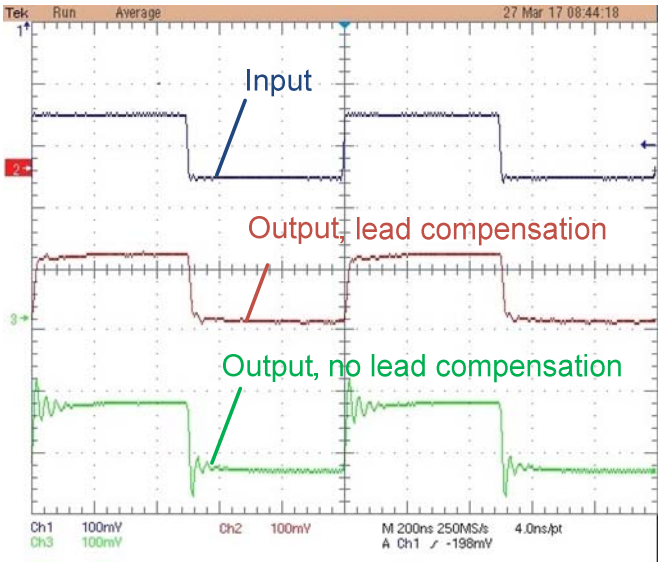

Fig. 6. Measured transient response without external C_L.

The measured transient response of the OTAs connected as voltage followers is shown in Fig. 4. Although the load capacitor used was C_L = 47 pF, if the capacitance of the measurement setup is considered, the overall estimated load capacitance is 70 pF. A 1 MHz 0.5 V periodic square wave with a -0.6 V DC component is employed as input signal. The measured *SR* for the class A FC OTA of Fig. 1(a) and for the proposed class AB FC OTA of Fig. 1(b) are 0.32 V/μs and 9.8 V/μs, respectively, which corresponds to an increase factor of 30.6 for the same biasing and load conditions. The theorectical enhancement from (4) and $\alpha \approx 0.8$, is a factor 36. The difference is mainly caused by the ideal MOS square law used for obtaining the approximate expression (4).

The frequency response of the voltage followers was also measured (Fig. 5) using a HP 89410A Vector Signal Analyzer. The same external load capacitor of 47 pF was used. The cutoff frequency of the OTA of Fig. 1(a) is 310 kHz, and that of Fig. 1(b) is 4.75 MHz. These values correspond approximately to the GBW of the OTAs because of the dominant pole design. Thus, an enhancement factor of 15.3 is observed. The theoretical improvement factor from (3) and $\alpha \approx 0.8$ is 12.2. The

difference may be partly due to the simple square law model employed to estimate the g_m values of the theoretical expression.

To assess the improvement provided by the lead compensation, Fig. 6 shows the measured transient response the proposed OTA of Fig. 1(b) in two different load conditions. The first one with the former C_L value of 47 pF. The second one corresponds to the absence of external load capacitor. In this latter case, the load capacitance is only that of the test setup, whose estimated value is of approximately 23 pF. The input signal applied is a 1 MHz 100 mV periodic square waveform with DC level of -200mV. Note that there is a significant ringing in the output waveform when no lead compensation is employed, which degrades settling performance. The inclusion of a lead resistance R_c of 772 Ω improves settling performance significantly, as the red line shows. The value of R_C was chosen as described in Section 2.B.

For noise measurements, an external amplifier with gain 22 was used to amplify noise, and its output was connected to a Keysight PXA N9030A signal analyzer. It was employed due to its improved displayed average noise level (DANL) vs the HP 89410A. The measured amplified noise spectrum using the OTA of Fig. 1(b) is shown in Fig. 7, yielding an integrated noise in 1 MHz of -66.2 dBmV. Eliminating the measured noise contribution of the external amplifier and test setup (which is assumed to be uncorrelated with the OTA noise), the equivalent input noise density of the OTA of Fig. 1(b) at 1 MHz is 35 nV/√Hz, and that of the FC OTA of Fig. 1(a) is 49 nV/√Hz. The lower input-referred noise of the proposed OTA is mainly attributed to its higher gain.

Table II summarizes the main measurement results for both OTAs, without using lead compensation and with an external load capacitor C_L=47 pF. As the FC OTA of Fig. 1(a) has settling limitations (as shown in Fig. 3), it features a large THD. The main drawback of the proposed OTA is the lower phase margin. The OTA in Fig. 1(b) presents a degradation of 19º comparing with that of Fig. 1(a). This degradation can be reduced if lead compensation is employed.

A comparison with other proposed class AB amplifiers is shown in Fig. 8. Two conventional Figures of Merit (FoM) are used: $FoM_1=SR\cdot C_L/I_{supply}=I_{maxL}/I_{supply}$, where I_{supply} is the total current consumption, which shows the large-signal current efficiency, and $FoM_2=GBW\cdot C_L/I_{supply}$ (MHz·pF/mA) a small-signal speed/power ratio. Note that the proposed OTA shows the highest FOM in both cases.

IV. Conclusion

An improved class AB folded cascode OTA has been presented. As measurement results show, a significant increase in slew rate and fast settling was achieved by applying adaptive biasing techniques at the current sources of the folding stage, keeping noise and static power consumption at low levels. Some possible application for this circuit are low voltage low power switched capacitor circuits and buffers with large capacitive load requirements.

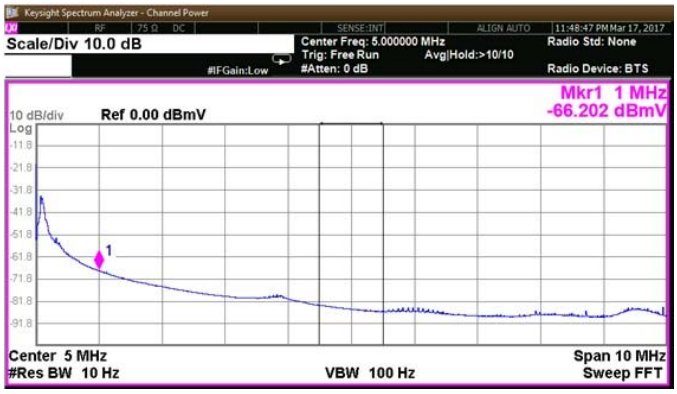

Fig. 7. Measured amplified noise spectrum of the buffer using OTA Fig. 1(b).

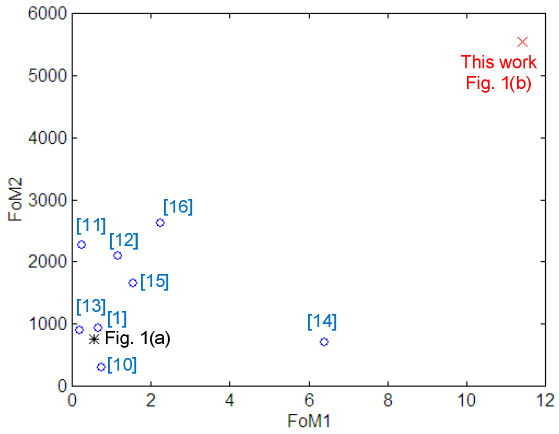

Fig. 8. Performance comparison.

TABLE II – SUMMARY OF MEASUREMENT RESULTS, R_C=0 Ω

Parameter	Class A OTA	Class AB OTA
CMOS process	0.5 µm	0.5 µm
Supply voltage	±1 V	±1 V
Capacitive load	70 pF	70 pF
SR+	0.32 V/µs	9.8 V/µs
SR-	-0.28 V/µs	-7.6 V/µs
Pos. Settling	--	96ns
Neg. Settling	--	74ns
THD @100kHz, $1V_{pp}$	-24 dB	-41 dB
DC gain (*)	69 dB	81.7 dB
PM (*)	89º	60º
GBW	310 kHz	4.75 MHz
CMRR @DC	91 dB	78 dB
PSRR+ @DC	71 dB	72 dB
PSRR-@DC	79 dB	74 dB
Input offset	11 mV	6 mV
Eq. input noise @1MHz	49 nV/√Hz	35 nV/√Hz
Power	80 µW	120 µW
Area	0.020 mm^2	0.024 mm^2

(*) Simulation

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