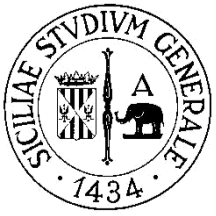

UNIVERSITÀ DEGLI STUDI DI CATANIA

Department of Electrical, Electronic and Computer Engineering

Master in Electronic Engineering

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DESIGN OF LOW POWER SUB-THRESHOLD TWO-STAGE CMOS OTAs USING DIFFERENT COMPENSATION TECHNIQUES

Final Master Thesis

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Academic Course 2017-2018

Dedicated to my

Father and Mother

Abstract – In this current final master thesis, different compensation techniques will be studied, simulated and compared in CMOS amplifiers. Specifically, these techniques will be applied in two-stage Operational Transconductance Amplifiers (OTAs). Due to the presence of both stages, the compensation techniques will be required to maintain the stability of the system. Another important aspect to consider is the inversion mode used. The circuit will be designed using the sub-threshold mode to obtain a low voltage-low power system. Using these compensation techniques with the transistors operating in the sub-threshold mode, two OTAs will be designed. One of them will be based in a Class-A amplifier, and the another in a Class-AB amplifier which uses the Quasi Floating-Gate (QFG) transistor technique. The objective is to compare them by some Figures of Merits (FOM), and relate them to different aspects of the system such as consumption, bandwidth, phase margin or slew rate. Finally, an optimal configuration will be found by these FOM.

Index terms – Analog CMOS integrated circuits, operational transconductance amplifier (OTA), sub-threshold, frequency compensation, two-stage amplifier, figure of merit (FOM), optimization, Class-A and Class-AB amplifiers, quasi floating-gate (QFG).

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NOMENCLATURE

ADC	Analog-to-Digital Conversion
BJT	Bipolar Junction Transistor
CBC	Current Buffer Compensation
CCVS	Current Controlled Voltage Source
CMOS	Complementary Metal-Oxide Semiconductor
DIBL	Drain-Induced Barrier Lowering
FET	Field-Effect Transistor
FOM	Figure of Merit
GBW	Gain Bandwidth product
L	Channel Length
MCNR	Miller Compensation with Nulling Resistor
MCPZC	Miller Compensation with Nulling Resistor and Pole-Zero Cancellation
MIFG	Multiple Input Floating Gate
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
NMOS	Negative-channel Metal-Oxide Semiconductor
OTA	Operational Transconductance Amplifier
PM	Phase Margin
PMOS	Positive-channel Metal-Oxide Semiconductor
QFG	Quasi Floating-Gate
SC	Switched-capacitor Circuit
SR	Slew Rate
VBC	Voltage Buffer Compensation
VDS	Drain-to-Source Voltage
$VDS_{,sat}$	Drain-to-Source Saturation Voltage
VGD	Gate-to-Drain Voltage
VGS	Gate-to-Source Voltage
W	Channel Width

1. INTRODUCTION

Low-voltage operation and optimized power designs of MOS transistors are required by modern wireless systems, portable battery-operated devices or trending concepts as the Internet of Things (IoT) in order to decrease the battery weight, size and to extend the lifetime. Even when the power is available in nonportable applications, the issue of low power design is becoming critical. So, as the size and density of chips continue to increase, the difficulty of dissipating the generated heat might add cost to the system or limit the functionality that can be provided. In analog circuits, reduction of the power dissipation while maintaining high operating speed is not as straightforward as in the digital case. In these and other applications, the Operational Transconductance Amplifiers (OTAs) are widely employed as active elements in switched-capacitor filters, data converters, sample and hold circuits, or as buffer amplifiers for driving large capacitive loads [20], [21].

These low voltage-low power constraints are mainly imposed on these OTA systems, which can be designed using different techniques to achieve these low voltage-low power requirements. One technique which is widely used to obtain a low power system consists in bias the transistors in the sub-threshold inversion mode, as alternative to the well-known strong inversion mode. In this mode, the transistor is biased with a gate-to-source voltage which is less than the threshold voltage. Through this condition, low channel currents are achieved, which imply a low power system with the counterpart of obtaining a low bandwidth [3]-[8]. Other example of these low voltage-low power techniques exploits the body terminal of MOS transistors to achieve high performance low voltage-low power analog circuits [22]. Finally, the simple but very effective technique to design low-voltage analog signal processing in MOS technologies is the Quasi Floating Gate (QFG) technique [9]-[11]. Other aspects which characterize an OTA is the class operation mode and the number of stages used. The Class-mode gives an indication of an amplifier characteristic, performance and consume. Examples of these classes which are widely used in analog design are the Class-A and Class-AB amplifiers. As it is known, Class-A circuits cannot achieve high performance requirements without significantly increasing their power consumption. When the Slew-Rate is the limiting factor of the design, a design strategy to overcome this drawback consists in designing the OTA by adopting Class-AB stages [9], [10], [20], [21]. In relation to the number of stages, it should be noted that the greater the number of stages is, the greater the gain of the system is. This is a very interesting option when a high gain system is required. If two or more stages are used, a compensation strategy must be included to maintain the stability of the system. In relation with this aspect, different compensation strategies can be adopted as the classic Miller compensation or more sophisticated buffer compensation strategies [14]-[16].

Considering all previous aspects, a family of sub-threshold two-stage CMOS OTAs have been designed. One of them is based in the Class-A and the another in the Class-AB, which uses the QFG technique to achieve this performance. For maintaining the stability of the systems, different compensation strategies have been used, which have been compared by an analytical figure of merit that expresses a tradeoff between gain-bandwidth product, load capacitance, and total transconductance for a given value of phase margin. Through this figure of merit, an optimal current stage relationship is searched which optimizes the performance of the system.

The project is organized as follows. In section 2, a review of the different inversion modes is detailed, with special emphasis in the sub-threshold mode. In section 3, the two-stage OTA topology is explained. The different compensation techniques are explained in Section 4. Then, in Section 5 the circuit simulations are done, which optimizations are shown in Section 6. All results are compared in Section 7. Finally, in Section 8 the conclusions and future research are described.

2. OPERATION OF MOS DEVICES AT DIFFERENT INVERSION LEVELS

The *Metal-Oxide-Semiconductor Field-Effect Transistor* (MOSFET) is a type of Field-Effect Transistor (FET), most commonly fabricated by the controlled oxidation of silicon. It has an insulated gate, whose voltage determines the conductivity of the device. This action of changing the conductivity with the amount of applied voltage can be used for amplifying or switching electronic signals. It should be noted that currently, the gate material is not a metal, is a layer of polysilicon. Similarly occurs with the oxide, that can be formed by different dielectric materials [1]. The name of metal and oxide are maintained by a classical sense.

The main advantage of the MOSFET is that it not requires almost input current to control the load current compared with a Bipolar Junction Transistor (BJT). In the *enhancement mode*, voltage applied to the gate terminal increases the conductivity of the device. In the *depletion mode*, voltage applied at the gate reduces the conductivity [1].

In relation to the terminals of a MOSFET device, it has four terminals: gate (G), source (S), drain (D) and bulk or body (B). This terminals performance as input, output or control terminal. The MOSFET device can be made by N-type or P-type semiconductors. In Fig. 1, a NMOS and a PMOS transistor can be shown with the different terminals. It is important to appreciate the symmetry of the devices and that they are complementary. For convenience, in a NMOS transistor the source is the terminal with the lowest voltage. In a PMOS transistor is the opposite, being the source the terminal which has the highest voltage. The performance of them are the same and the only thing that change is the sense of the currents and the polarity of the voltages. Since MOSFETs can be made with either P-type or N-type semiconductors, complementary pairs of MOS transistors can be integrated to make circuits with better performance, in the form of Complementary Metal-Oxide-Semiconductor (CMOS) circuits. This technique seeks to integrate both NMOS and PMOS transistors in the same substrate. In the same Fig. 1, a CMOS transistor can be shown.

In Table I, the electrical symbols of the NMOS and PMOS transistors can be checked. It is important to appreciate that the symbol can change depending on the applications. The generic symbol is the four terminals device, that is commonly used in analog circuits. This device can act as an enhancement mode transistor or a depletion mode transistor. Sometimes, the bulk terminal can be neglected because it is connected to the source terminal. This is very common in discrete devices or in digital circuits, and of course, in analog circuits.

MOSFET devices typically operate in their saturation regions. However, within the saturation region a device may be biased in the *strong inversion mode*, the *moderate inversion mode*, or the *weak/sub-threshold inversion mode*. These different modes are dependent on the *threshold voltage* (V_{TH}) applied to the transistor. It should be noted that a MOSFET device can also operate in the linear region and in these three different inversion modes. In weak inversion, the number of free carriers in the channel is small enough to lead a significant drift current. In this case, the diffusion current mechanism dominates. It should be noted that in this case, the MOSFET device operates more like a BJT. The gate-to-source voltage is near the threshold voltage and a very small channel current density exist in this situation. As gate-to-source voltage increases, more carriers are induced in the channel and drift current becomes more significant. In the moderate inversion mode, drift and diffusion components are comparable. Strong inversion is reached as the gate-to-source voltage increases to the point that drift current dominates the drain current [3].

Then, a comparative study of these three inversion modes is developed. First, the well-known strong inversion mode is studied. Then, the weak inversion mode is analyzed in detail which will be used in the present project. Finally, the moderate inversion mode is commented.

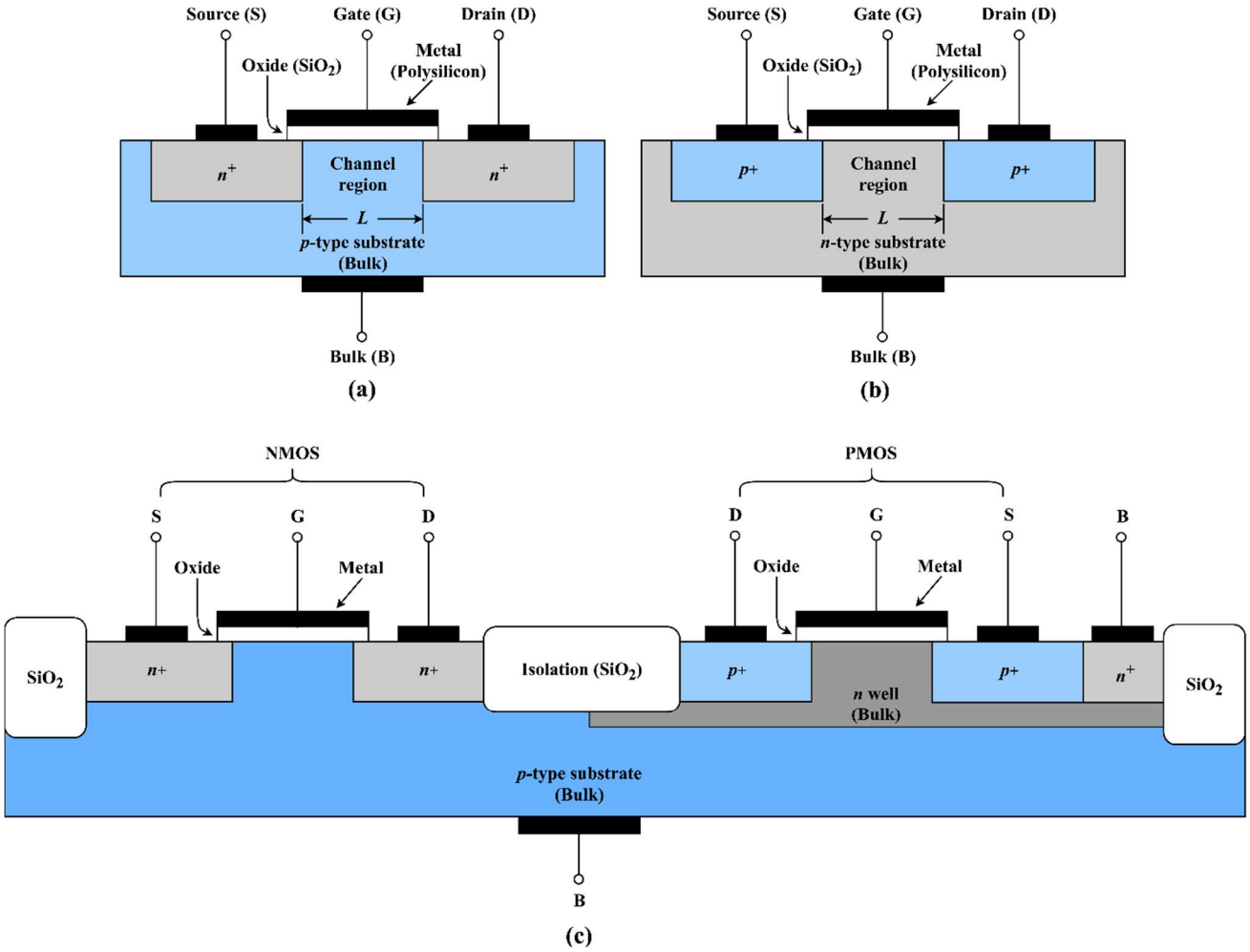
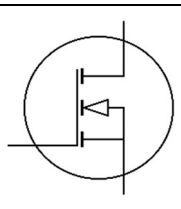
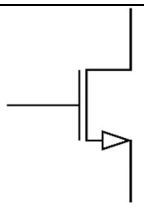
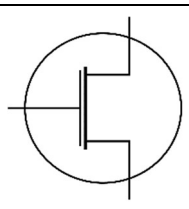
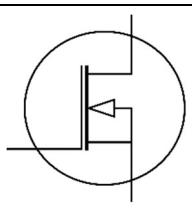
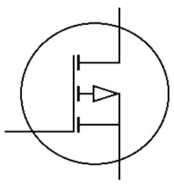
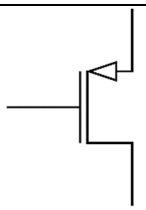
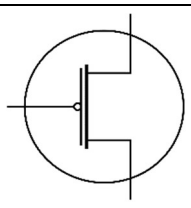
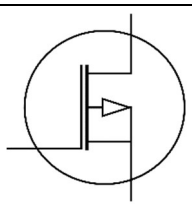


Fig. 1. Enhancement type MOSFET device. (a) NMOS transistor. (b) PMOS transistor. (c) CMOS transistor.

TABLE I
ELECTRICAL SYMBOLS FOR THE NMOS AND PMOS TRANSISTORS.

N-CHANNEL				
P-CHANNEL				
	MOSFET enh.	***MOSFET enh. (no bulk)***		***MOSFET dep.***

2.1. Strong Inversion Mode

The strong inversion mode is perhaps the most commonly used and the most popular in the main applications. That is why in the first electronic courses, the MOSFET device is studied in that configuration. When the device is analyzed in this mode, its three main operation regions in the enhancement mode are taught: *cut-off*, *linear* and *saturation*. In the cut-off region, the device acts like an open circuit, through which no current flows. In linear region, acts like a resistor controlled by voltage. Finally, in the saturation region, the device performance as a current source controlled by voltage.

These regions depend on the voltages V_G, V_D and V_S applied, which are the gate, drain and source voltage respectively. Combining these three voltages it can be obtained three different cases, which are shown in Table II.

TABLE II
DIFFERENT VOLTAGES IN THE TERMINALS OF A MOS TRANSISTOR.

Voltage gate-to-source	$V_{GS} = V_G - V_S$	(1)
Voltage gate-to-drain	$V_{GD} = V_G - V_D$	(2)
Voltage drain-to-source	$V_{DS} = V_D - V_S = V_{GS} - V_{GD}$	(3)

Other important values that influence in this operation mode are:

- V_{TH} or *Threshold voltage*: It is the minimum value of V_{GS} for create the channel between the drain and source.
- V_{OV} or *Effective/overdrive voltage*: It is the difference between V_{GS} and V_{TH}.

$$V_{OV} = V_{GS} - V_{TH} \tag{4}$$

- C_{ox} or *Oxide capacitance*: It is the capacitance between the gate and channel per area unit (F/m^2).

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{5}$$

where ε_{ox} is the permittivity of the SiO_2 and t_{ox} is the thickness of SiO_2 layer.

Considering the previous information, the different approximated equations that describe these three regions are shown in Table III. Additionally, in Fig. 2. can be checked the classic I_D-V_{DS} response of a MOSFET device. It should be noted that in the cut-off region, the V_{GS} is less than V_{TH}. On the contrary, in the linear and saturation region, the V_{GS} is much higher than V_{TH}. This condition is called strong inversion mode. It is appreciated the I_D-V_{DS} relationship in the linear region, turning the transistor in a resistor in which the current I_D is controlled by the voltage V_{DS} applied. For the case of the saturation region, there is no a I_D-V_{DS} relationship. In fact, the current I_D only depends on the square of the V_{GS}.

In a formal way, for the case of an NMOS transistor, when $V_{GS} > V_{TH}$, the electron density in the channel in thermal equilibrium is larger than the hole density in the bulk, $n > N_A$ where n is the number of free carriers and N_A is the doping concentration in a P-type semiconductor [2]. In the strong inversion mode, the main operation mechanism is the *drift current*.

TABLE III
DIFFERENT REGIONS IN THE STRONG INVERSION MODE.

Open circuit	***Cut-off***		
	$V_{GS} < V_{TH}$	$I_D = 0$	(6)
Strong inversion	***Linear***		
	$V_{GS} \gg V_{TH}, V_{DS} < V_{DS,sat} = V_{GS} - V_{TH}$	$I_D = \mu C_{ox} \frac{W}{L}(V_{GS} - V_{TH} - \frac{V_{DS}}{2})V_{DS}$	(7)
	Saturation		
	$V_{GS} \gg V_{TH}, V_{DS} \geq V_{DS,sat} = V_{GS} - V_{TH}$	$I_D = \mu C_{ox} \frac{W}{2L}(V_{GS} - V_{TH})^2$	(8)

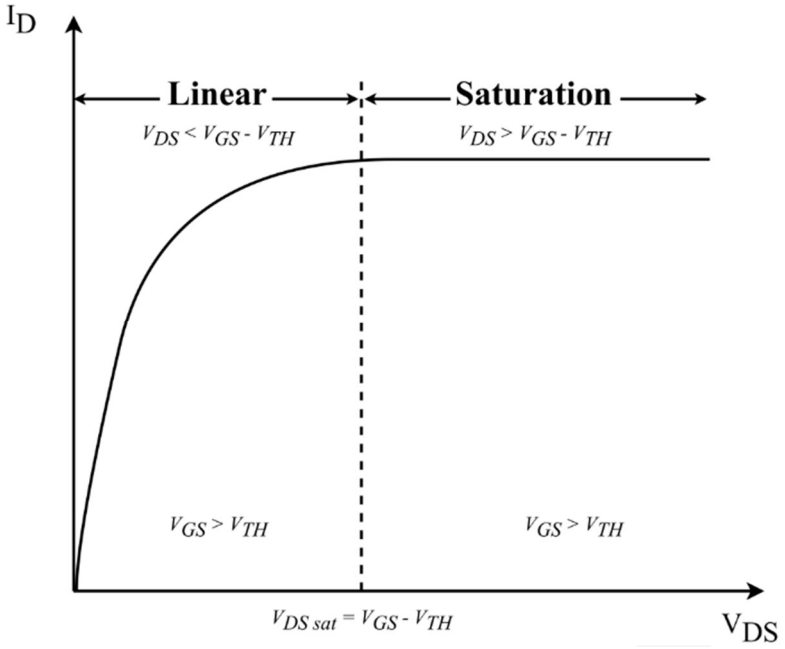


Fig. 2. V_{DS}-I_D response for a MOS transistor in strong inversion.

2.2. Weak and Sub-Threshold Inversion Mode

As has been said, the CMOS circuits usually have their transistors operating in the strong inversion mode. The condition to reach this mode is that $|V_{GS}| > |V_{TH}|$ and $|V_{DS}| > |V_{DS,sat}| = |V_{GS} - V_{TH}|$ in a NMOS or PMOS transistor, where V_{GS} and V_{DS} are the gate-to-source and drain-to-source voltage respectively, and V_{TH} is the threshold voltage. In this case, the main mechanism of working is the drift current. But there is another mode in a MOS transistor, that it is called sub-threshold or weak inversion mode. This mode is achieved when $|V_{GS}| < |V_{TH}|$. In this case, the drift current mechanism can be neglected, being the main mechanism the diffusion currents.

In the simplest model, the drain current is assumed to be zero when V_{GS} is less than the threshold voltage V_{TH} but it is true that there are currents that are flowing between the drain and source.

Let is imagine devices that may have widths that are 100 to 1000 times the length. In this case, the W/L ratio becomes very high. Since the drain current is proportional to this ratio, the drain current required for a practical analog design may be achieved by a value of V_{GS} that is only slightly higher or slightly lower than the threshold voltage. This low value of the overdrive voltage, named before as

V_{OV}, establishes the operation of the device in other alternative modes: the weak or sub-threshold inversion mode; and the moderate inversion mode. Surprisingly, operation below the strong inversion mode can result in advantages such as higher gain, less power dissipation, and less harmonic distortion [3]. The main advantages and disadvantages of the weak/sub-threshold inversion mode are shown in Table IV [4], [8].

> ***Commentary**: These advantages fit very well to the requirement of designing low voltage-low power circuits, and that is the reason why the sub-threshold mode has been considered in the current project.*

TABLE IV
ADVANTAGES AND DISADVANTAGES OF SUB-THRESHOLD MODE.

ADVANTAGES	***DISADVANTAGES***
Power dissipation is lower.	Lower bandwidth and lower slew-rate.
Voltage gain is constant in the operation region.	
Maximum transconductance efficiency (g_m/I_D).	Larger drain current mismatch.
Distortion of the output signal is reduced.[1]	
Better input-referred noise voltage.[2]	

It should be noted that the sub-threshold mode occurs with negative values of V_{OV} and the weak inversion mode with very low positive values of V_{OV}. Although they seem two different modes, the sub-threshold is included in the weak inversion mode. On the contrary, the moderate inversion occurs with low positive values of V_{OV} but higher than the weak inversion. For high values of V_{OV}, the transistor enters in the strong inversion mode.

It is well known that when the V_{GS} of a MOSFET transistor is reduced below V_{TH}, the channel current decreases approximately exponentially. In this mode, the channel current flows by diffusion and this current is a function of the inversion charge at the source and drain. For obtain the equation that describe the model, some assumptions are taken, according to [5]:

- The channel is sufficiently long so that the gradual channel approximation can be used and channel-length modulation effects are negligible.
- Generation currents in the drain, channel and source depletion regions are negligible; source and drain currents are then equal.
- The density of fast surface states and the fluctuations of surface potential are negligible.

Taking these assumptions, A. Vittoz rewrote in [5] an approximate expression developed by M. B. Barron for the weak inversion drain-to-source current in an NMOS transistor as follows:

$$I_D = \frac{W}{L}\mu {v_t}^2 \left(\frac{1}{2} q \varepsilon_S n_i\right)^{1/2} \cdot e^{-(3\Phi/2v_t)} \cdot \frac{e^{\Psi_S/v_t}}{(\Psi_S - v_t)^{1/2}} \cdot \left(e^{-(V_S/v_t)} - e^{-(V_D/v_t)}\right) \tag{9}$$

where

[1] The distortion of the output signal is less due to the voltage gain is constant in the operation region.
[2] The input-referred noise is better because it depends on $1/I_D$ value. In the strong inversion mode, it depends on $1/\sqrt{I_D}$. But it is must be considered that the total noise performance is worst in a sub-threshold system in comparison with a strong inversion system, because the current in a sub-threshold is less.

- W/L = aspect ratio of the transistor (width over length),
- μ = mobility of carriers in the channel,
- $v_t = kT/q$,
- ε_s = permittivity of Si,
- $\Phi = v_t \ln(N_B/n_i)$ is the bulk Fermi potential,
- N_B = constant bulk impurity concentration,
- n_i = intrinsic carrier concentration,
- Ψ_S = surface potential, constant along the channel in weak inversion,
- V_S = source voltage,
- V_D = drain voltage,
- V_G = gate voltage
- I_D = drain current.

It should be noted that this equation is valid for

$$4v_t + \Phi + V_S < \Psi_S < 2\Phi + V_S \tag{10}$$

The above equation (9) deserves a special mention because it is the basis of the formal mathematical description that defines the weak inversion mode. According to [5] and making some simplifications, (9) can be simplified as the well-known weak inversion equation (11)

$$I_D \approx I_{DO} \frac{W}{L} e^{\frac{V_{GS}-V_{TH}}{nv_t}} \left(1 - e^{-\frac{V_{DS}}{v_t}}\right) \tag{11}$$

where n is the slope factor (usually $1 < n < 2$), I_{DO} is the characteristic current, being both technology dependents, $v_t = kT/q \sim 26$ mV is the thermal voltage ($T = 300$ °K is the temperature in degrees Kelvin at room temperature, $k = 1.38\text{x}10^{-23}$ JK^{-1} is Boltzmann's constant and $q = 1.602\text{x}10^{-19}$ C is the charge of the electron), W/L is the aspect ratio of the transistor and V_{GS} (V_{DS}) is the gate-to-source (drain-to-source) voltage. It should be noted that (11) can be used in both NMOS and PMOS transistor. In (11), V_{TH} implicitly depends on V_{DS} through the Drain-Induced Barrier Lowering (DIBL) effect, as well as on V_{BS} through the body effect, where V_{BS} is the bulk-to-source voltage. At first order, this can be analytically expressed as [6]

$$V_{TH} = V_{TH0} - \lambda_{DS} V_{DS} - \lambda_{BS} V_{BS} \tag{12}$$

where V_{TH0} is the zero-bias threshold voltage (i.e. the value extrapolated under $V_{DS} = V_{BS} = 0$ V), whereas λ_{DS} and λ_{BS} are positive technology-dependent coefficients that determine the amount of threshold change with respect to V_{TH0} for assigned voltages V_{DS} and V_{BS} [6].

Then, simplified circuit models of MOS transistors are developed to better understand their behavior in weak inversion mode, as well as to permit paper-and-pencil circuit analysis. It will be discussed the large-signal models and the small-signal.

2.2.1. Simplified Large-Signal Transistor Models in Sub-Threshold

In the following, simplified circuit models of MOS in sub-threshold are derived under high and low values of V_{DS}.

Under "high" values of V_{DS} much greater than v_t (~100 mV), the last factor $(1 - e^{-V_{DS}/v_t})$ in (11) is close to unity, and the sub-threshold current of a MOS transistor is given by [6]

$$I_D \approx I_{DO}\frac{W}{L}e^{\frac{V_{GS}-V_{TH}}{nv_t}} \qquad \text{if } V_{DS} \gg v_t \tag{13}$$

With values of V_{DS} higher than 100 mV the transistor in the sub-threshold mode can be modelled like a *voltage-controlled current source*, as shown in Fig. 3(a).

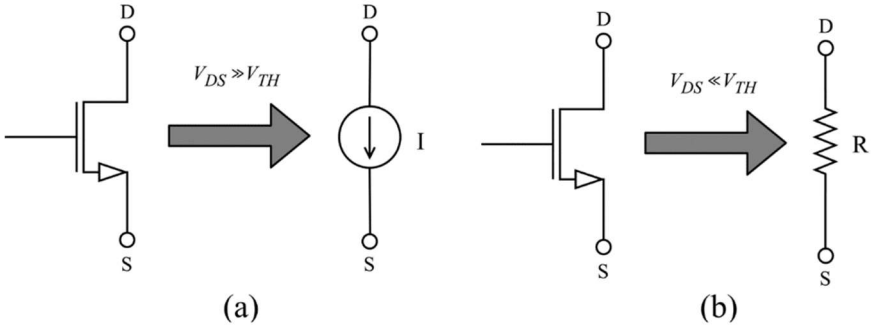


Fig. 3. (a) Equivalent large-signal MOS model for high V_{DS}. (b) Equivalent large-signal MOS model for low V_{DS}.

On the other hand, under "low" values of V_{DS} much lower than v_t (~25-30 mV), the last term $(1 - e^{-V_{DS}/v_t})$ in (11) can be expanded in Taylor series truncated to first order, obtaining [6]

$$I_D \approx I_{DO}\frac{W}{L}e^{\frac{V_{GS}-V_{TH}}{nv_t}}\frac{V_{DS}}{v_t} \qquad \text{if } V_{DS} \ll v_t \tag{14}$$

As can be seen in (14), a relation between I_D and V_{DS} can be stablished, so the drain-to-source current I_D is proportional to V_{DS}. In other words, the MOS transistor is equivalent to a *resistance* given by [6], which modelled can be show in Fig. 3(b).

$$R_{eq} = \frac{V_{DS}}{I_D} = \frac{v_t}{I_{DO}\frac{W}{L}e^{\frac{V_{GS}-V_{TH}}{nv_t}}} \qquad \text{if } V_{DS} \ll v_t \tag{15}$$

In conclusion, the MOS transistor in sub-threshold region can be modeled either as a current source for high values of (100 mV or more), or as a linear resistance given by for low values of (less than 25-30 mV).

2.2.2. Small-Signal Transistor Models in Sub-Threshold

From (11) and (12), the transconductance g_m, the drain-to-source resistance r_o, the substrate transconductance g_{mb}, and the intrinsic MOSFET DC gain ($A_{V0} = g_m r_o$) can be derived. These parameters are reported in Table V. The table also summarizes the values of g_m, r_o, g_{mb} and A_{V0} in the saturation region of strong inversion for establishing a comparison (in the expressions shown, $K = \mu C_{OX}$ is the process transconductance, λ is the channel length modulation coefficient and Φ_F is the strong inversion surface potential) [7].

In sub-threshold regime, g_m linearly depends on I_D, whereas it increases with $\sqrt{I_D}$ in strong inversion regime. This leads to a larger g_m/I_D ratio in sub-threshold mode, or similarly, the g_m value is larger in a sub-threshold MOSFET for a fixed I_D. The intrinsic MOSFET DC gain, A_{V0}, only depends on λ_{DS} in the sub-threshold mode [7].

In relation to the dynamic performance of a sub-threshold MOSFET, the intrinsic transition frequency f_{Ti} is evaluated. In Table V, the generic expression for f_{Ti} is given, where C_X is the gate input capacitance, given by the sum of the gate-to-source, gate-to-drain, and gate-to-body capacitances ($C_X = C_{GS} + C_{GD} + C_{GB}$). In (16i) and (16l), C_{OX} and C_d are the gate oxide capacitance and the depletion

region capacitance between gate and body per unit area, respectively. The intrinsic transition frequency linearly depends on I_D in the sub-threshold mode, whereas it depends on $\sqrt{I_D}$ in the strong inversion mode [7].

Finally, the noise performance is considered. In the sub-threshold mode, the MOSFET drain current exhibits a white noise part ($S_{iw} = 2qI_D$) caused by shot noise. The power spectral density of the input-referred noise voltage is given by the expressions shown in Table V. As shown, S_{vw} depends on $1/I_D$ and $1/\sqrt{I_D}$ in sub-threshold and strong inversion regions, respectively [7].

The equivalent small-signal MOS model for a high value of V_{DS} can be shown in Fig. 4. in which the g_m and r_o parameters can be shown.

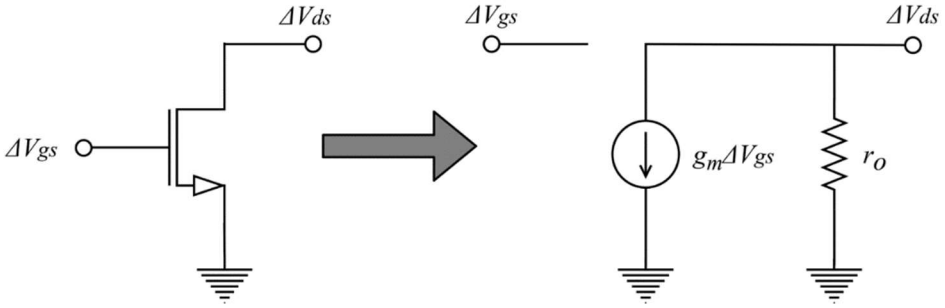


Fig. 4. Equivalent small-signal MOS model.

TABLE V
SMALL-SIGNAL MOSFET PARAMETERS (SATURATION REGION).

	SUB-THRESHOLD		***STRONG INVERSION***	
$g_m = \frac{\partial I_D}{\partial V_{GS}}$	$\frac{I_D}{nv_t}$	(16a)	$\sqrt{\frac{2KWI_D}{L}}$	(16b)
$r_o = \left[\frac{\partial I_D}{\partial V_{GS}}\right]^{-1}$	$\frac{nv_t}{\lambda_{DS} I_D}$	(16c)	$\frac{1}{\lambda I_D}$	(16d)
$g_{mb} = \frac{\partial I_D}{\partial V_{BS}}$	$\frac{\lambda_{BS} I_D}{nv_t}$	(16e)	$\frac{g_m \gamma}{2\sqrt{2\lvert\Phi_F\rvert + \lvert V_{SB}\rvert}}$	(16f)
$A_{VO} = g_m r_o$	$\frac{1}{\lambda_{DS}}$	(16g)	$\frac{1}{\lambda}\sqrt{\frac{2KW}{I_D L}}$	(16h)
$f_{Ti} = \frac{g_m}{2\pi C_X}$	$\frac{I_D}{nv_t}\frac{1}{WL}\frac{C_d + C_{OX}}{2\pi C_d C_{OX}}$	(16i)	$\sqrt{\frac{2KWI_D}{L}}\frac{3}{2WL}\frac{1}{2\pi C_{OX}}$	(16l)
$S_{VW} = \frac{S_{iW}}{{g_m}^2}$	$\frac{2qI_D}{{g_m}^2} = \frac{2q}{I_D}(nv_t)^2$	(16m)	$\frac{8kT}{3g_m} = \frac{8kT}{3}\sqrt{\frac{L}{2KWI_D}}$	(16n)

2.3. Moderate Inversion Mode

As V_{OV} continues to increase and more free carriers are induced in the channel, drift current becomes comparable to diffusion current, and both components contribute to drain current. At some point, V_{OV} reaches a value that leads to a drift current component of drain current exceeding the diffusion component sufficiently to render diffusion current negligible. Both components of current must be considered as V_{OV} ranges from about 20 mV up a value of [4]

$$V_{OV} \approx 2n\frac{kT}{q} = 2nv_t \tag{17}$$

Typically, *n* is between 1 and 2. This region is called the moderate inversion mode and exists for values of V_{OV} ranging from 20 mV up to about 80-220 mV. As V_{OV} is increased, the strong-inversion region is entered [4].

It should be noted that the moderate inversion mode acts like a bridge between the weak inversion and the strong inversion and there is not a well-defined mathematical model as both as the other inversion modes. The level of inversion can be approximately defined by the gate-to-source voltage. The lower end of the weak inversion mode is the subthreshold region that exists for values of V_{GS} less than v_t when positive drain current flows. As V_{GS} ranges from sub-threshold values up to about 20 mV above v_t, the device is in the weak inversion mode. From a value of 20 mV above v_t to a V_{GS} of approximately 80-220 mV the device operates in the moderate inversion region. Above this value of V_{GS}, drift current dominates and the device is in the strong inversion mode [4].

In the Fig. 5. the three different regions can be checked in function of the V_{OV} voltage. The Fig. 6. shows the I_D-V_{DS} characteristics for the device. The slope of a given curve is much less when the device operates at lower currents than the slope for curves at higher currents. This implies that r_o, the drain-to-source resistance, is considerably higher in the weak or moderate inversion region.

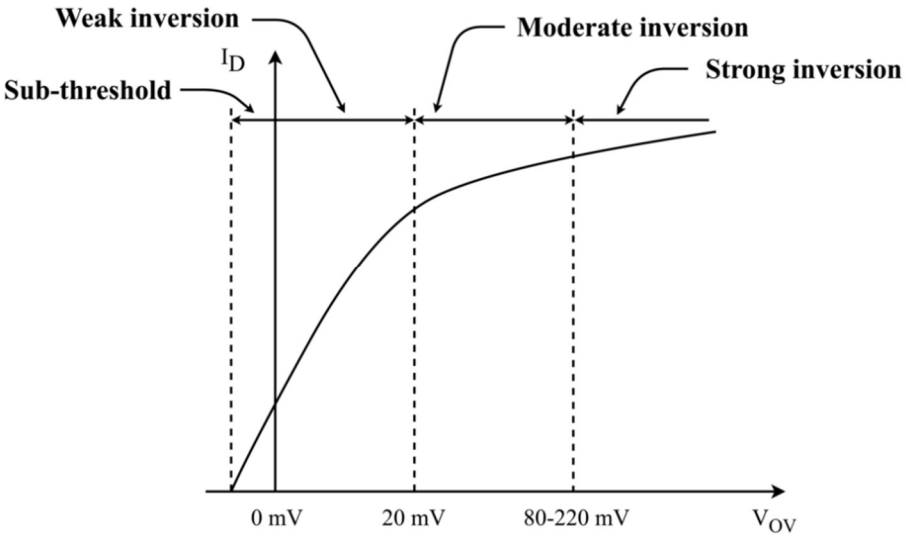


Fig. 5. Different inversion modes in function of V_{OV} voltage.

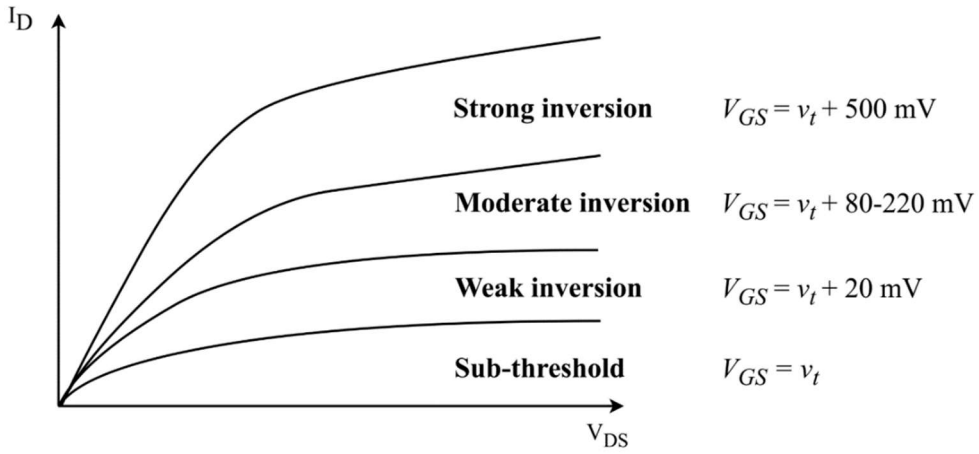


Fig. 6. V_{DS}-I_D characteristic of a MOS transistor operating in the three different inversion modes.

3. OTA CIRCUIT DESIGN

Once the different inversion modes have been described and chosen the sub-threshold as the design inversion mode, the next step consists in analyzing the circuit which will be studied, designed and simulated. This circuit has been proposed by [9], in which is designed using the strong inversion mode. In the current project, as has been said, the circuit will be designed using the sub-threshold mode because it is suitable for low power applications in which the bandwidth or the slew rate are not the most important requirements of the application.

The circuit will be based in a two-stage amplifier, in which the first stage will be consisted by a folded-cascode amplifier and the second stage in a Class-A/Class-AB. The Class-A output stage will be based in the classic common-source solution and the Class-AB in the Quasi Floating-Gate (QFG) transistor technique applied in the common-source scheme. It is important to say that due to the system has more than one stage, will be required a compensation technique for maintain the stability of the system. In Section 4, the different compensation techniques to be used will be explained. The block diagrams of the two different topologies are show in Fig. 7.

Then, the circuits will be explained in detailed. First, some basic concepts related with the OTA and the transconductor will be introduced. Then, the basic circuit stages of the OTA circuit will be explained, detailing each block. Then, some design techniques like the QFG technique and the Class-A/Class-AB amplifiers will be studied. Finally, the complete OTA topologies will be explained detailing the design procedure followed.

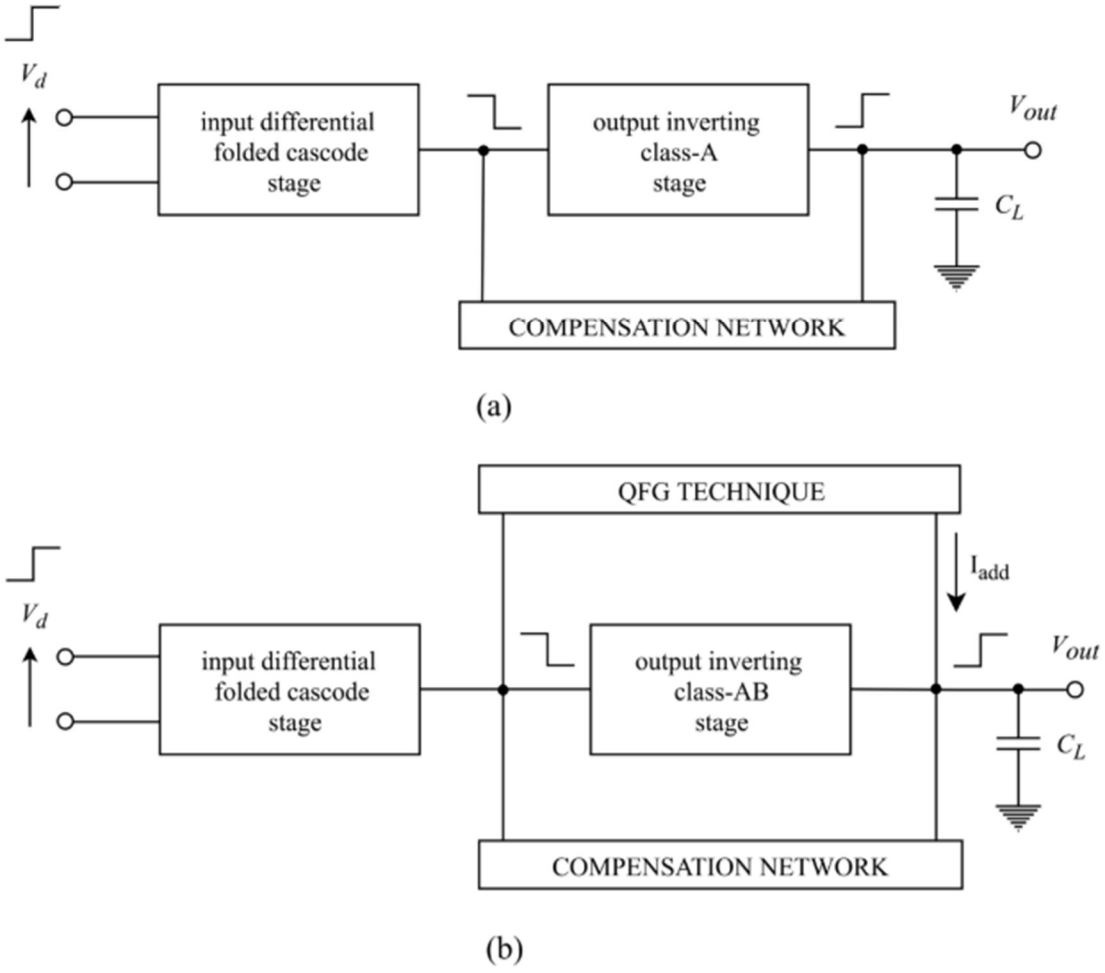


Fig. 7. (a) Schematic of the OTA Class-A type amplifier. (b) Schematic of OTA Class-AB type amplifier.

3.1. Definitions

A *voltage or current amplifier* is a device characterized for providing at its output the same parameter in its input (both voltage or current), but amplified with a gain relationship, whose relations can be consulted in (18) and (19)

$$V_{out} = A_V \cdot V_{in} \tag{18}$$

$$I_{out} = A_I \cdot I_{in} \tag{19}$$

where A_V is the voltage gain and A_I the current gain.

An *Operational Transconductance Amplifier or OTA* is a device which provides at its output a current proportional to its input voltage. In the ideal case, can be considered as a Current Controlled Voltage Source (CCVS), as (X) shows

$$I_{out} = G_m \cdot V_{in} \tag{20}$$

where G_m is the amplifier transconductance.

The main difference between the operational amplifier and the OTA is the output impedance. The first device presents a low output impedance, but the second presents large values. So, the operational amplifier can get high voltage gain values for low resistive loads, whereas that the OTA is used with capacitive loads or large resistive loads [10].

Taking account these concepts, can be deduced that an operational amplifier is an OTA follow by a *buffer*. The OTA, which output presents a large impedance value, provides an output current proportional to its input voltage, and an output voltage amplified respect to the input due the high voltage gain. The buffer copies that voltage from its input to its output, but changing from a high impedance terminal to a low terminal [10].

At this point, is important to comment an important difference. The OTA has been defined like a CCVS, but this behavior is only valid for a narrow input voltage range. An OTA provides a high transconductance, that is it, a high slope in the curve I_{out}-V_{in}, but within a narrow input range. If a linear application is required with a wider input range, it is necessary to linearize the I_{out}-V_{in} response. This circuit is called *Linear OTA or Transconductor*. It is true that in the literature the transconductor concept is used in the same way as the OTA concept, but they are not the same. In conclusion, an OTA presents a high gain transconductance value in a narrow input range and the transconductor presents a wider input linearized range with a lower transconductance value. In the Fig. 8., the I_{out}-V_{in} responses for both devices are shown, as well as the electrical symbols which define them [10].

With respect to the applications of both devices, the immediate application of an OTA, followed by a buffer, is the operational amplifier implementation. In this way, a high gain value is obtained, as well as a low output impedance. The reason for employing an OTA instead of a transconductor is the interest of getting a high transconductance value instead of a linear performance in a wide input range. Other applications are Switched-capacitor Circuits (SC) or Analog-to-Digital Converters (ADCs) [10].

In relation to the transconductor, the main application is the filter continuous-time design, like the G_m-C filters. Other applications can be the design of analog multipliers or the implementation of automatic gain control blocks [10].

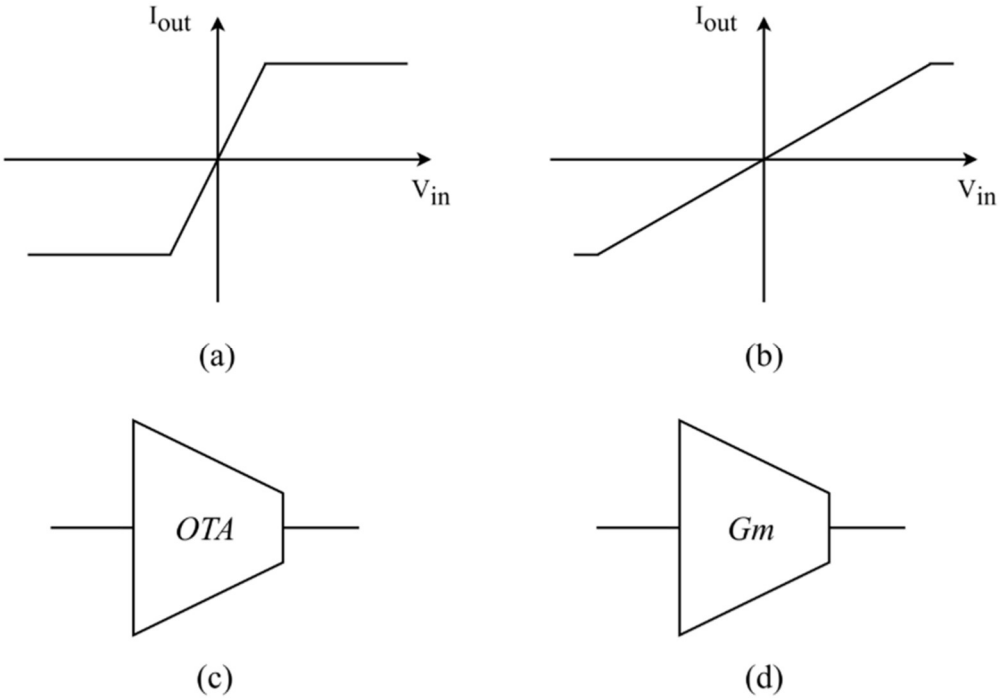


Fig. 8. (a) OTA I_{out}-V_{in} relation. (b) Transconductor I_{out}-V_{in} RELATION. (c) OTA symbol. (d) Transconductor symbol.

> ***Commentary**: In the current project, an OTA device will be designed because it is not required a linear application. This OTA will be designed using the sub-threshold mode already mentioned.*

3.2. Basic Circuit Stages

Once the OTA has been introduced, the next step consists in define its basic building stages. The OTA has two stages, as well as current mirrors which polarize these stages. The first stage consists in a folded-cascode amplifier and the second stage in a common-source amplifier. Then, these different circuits will be explained, including the current mirror stage previously cited.

3.2.1. Folded-Cascode Differential Amplifier

The first OTA stage consists in the well-mentioned *folded-cascode amplifier*. In this case, is a differential-input single-ended output design, which is formed by two sub-stages and by the transistors M_1-M_8, which topology can be seen in Fig. 9. The first sub-stage, formed by M_1 and M_2, is a *p*-channel differential pair, which output feeds the second sub-stage, known as the cascode topology and formed by M_3-M_8. Together, they form the folded-cascode amplifier. This topology is adequate to extend the input common-mode range down to negative rail and to reduce the flicker noise contribute. Observe that due to the low signal swing required at the output of the input stage, this is the only that can tolerate partial cascoding (M_3-M_6, while NMOS active load M_7-M_8 is a simple current mirror) [8].

The basic idea of the folded-cascode topology consist in apply cascode transistors to the input differential-input pair but using transistors opposite in type from those used in the input stage. For example, the differential-input pair transistors consisting of M_1 and M_2 are *p*-channel transistors in Fig. 9., whereas the cascode transistors M_5 and M_6 are *n*-channel transistors. This arrangement of opposite-type transistors allows the output of this single gain-stage amplifier to be taken at the same bias-voltage levels as the input signals. It should be mentioned that even though a folded-cascode amplifier is basically a single gain stage, its gain can be quite reasonable. Such a high gain occurs because the gain is determined by the product of the input transconductance and the output impedance, and the output

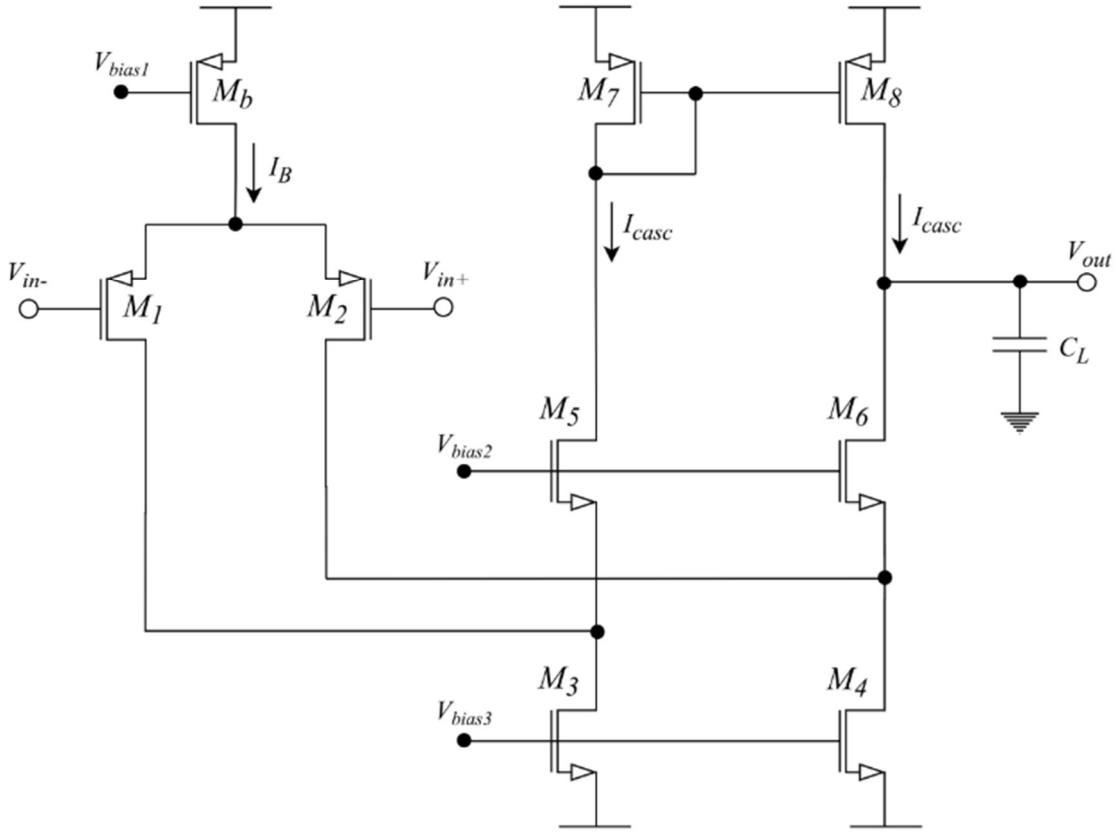


Fig. 9. Folded-Cascode amplifier.

impedance is quite high due to the use of cascode techniques. In the topology, differential-input to single-ended conversion is realized by the current mirror, composed by M_7 and M_8 [12]. The principal properties of this topology are reported in Table VI and some design expressions in Table VII, according to [12], [13].

***Commentary**: This topology is adequate in the design of low-voltage low-power analog integrated circuits due to the opposite-type transistors allows the output of this single gain-stage amplifier to be taken at the same bias-voltage levels as the input signals. Due to this, in the current project, a low-voltage low-power system will be designed, which advantageous characteristics justify its use.*

TABLE VI
FOLDED-CASCODE MAIN CHARACTERISTICS.

FOLDED-CASCODE CHARACTERISTICS	
Low-voltage low-power suitable design.	High gain.
High output resistance.	Good common-mode range.

3.2.2. Common-Source Amplifier

The second stage consists in the classic *common-source amplifier with active load*. In Fig. 10. this topology can be seen. This common-source topology is the most popular gain stage, especially when high input impedance is desired.

Here, a *p*-channel common-source amplifier has a *n*-channel active load, which is biased for drive the transistor. By using an active load, a high-impedance output load can be realized without using excessively large resistors or a large power-supply voltage. The use of an active load takes advantage

TABLE VII
FOLDED-CASCODE DESIGN EQUATIONS.

ESPECIFICATION	*DESIGN EQUATION*	
Gain (A_v)	$A_v \approx -g_{m1,2}R_{out}$	(21a)
Output resistance (R_{out})	$R_{out} = r_{o8}$	(21b)
Gain-bandwidth product (GBW)	$GBW = \frac{gm_{1,2}}{2\pi C_{out}}$ $C_{out} = C_{db6} + C_{db8} + C_L \approx C_L$	(21c)
Slew Rate (SR)	$SR = \frac{I_B}{C_L}$	(21d)
Power Consumption (P_{POWER})	$P_{POWER} = (V_{DD} + V_{SS})(I_B + 2I_{casc})$	(21e)

of the nonlinear, large-signal transistor current-voltage relationship to provide large small-signal resistances without large DC voltage drops [12]. In Table VIII some design expressions are reported, according to [12].

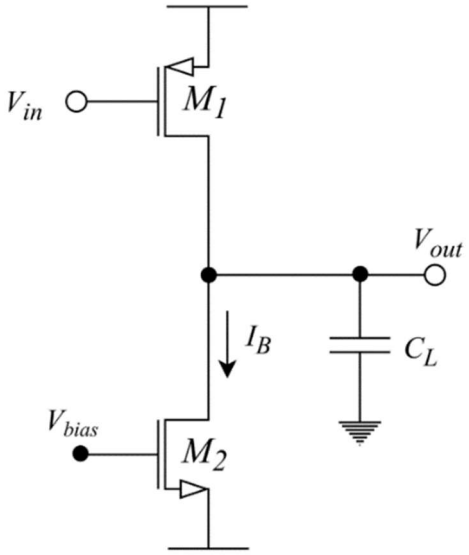


Fig. 10. Common-Source amplifier.

3.2.3. Current Mirrors

As seen, the first and the second stages need to be biased for achieve their performance. This bias activity is carried out by a *current mirror* network. An ideal current mirror is a two-port circuit that accepts an input current and produces an output current $I_{out} = I_{in}$. Since current sensing is best done with a low resistance, the ideal current source will have zero input resistance and a high output resistance. In this way, the ideal current mirror faithfully reproduces the input current regardless of the source and load impedances to which it is connected [12].

The current mirror network used in the current project is shown in Fig. 11. in which the *p*-channel transistor for implement it is used. It is assumed that all transistors are in the saturation region, or that is the same, the drain-to-source voltage V_{DS} must be greater than V_{OV}, as seen previously. If the finite

TABLE VIII
COMMON-SOURCE DESIGN EQUATIONS.

ESPECIFICATION	*DESIGN EQUATION*	
Gain (A_v)	$A_v \approx -g_{m1}R_{out}$	(22a)
Output resistance (R_{out})	$R_{out} = r_{o1}\|\|r_{o2}$	(22b)
Gain-bandwidth product (GBW)	$GBW = \frac{gm_1}{2\pi C_{out}}$ $C_{out} = C_{db1} + C_{db2} + C_{gd2} + C_L \approx C_L$	(22c)
Slew Rate (SR)	$SR = \frac{I_B}{C_L}$	(22d)
Power Consumption (P_{POWER})	$P_{POWER} = (V_{DD} + V_{SS})I_B$	(22e)

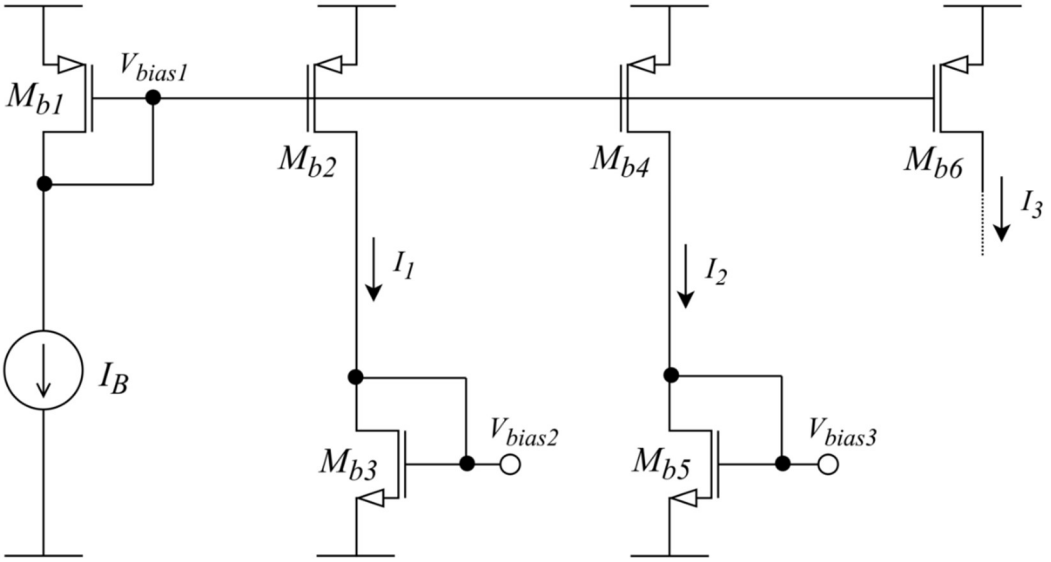


Fig. 11. Current mirror bias network.

small-signal drain-to-source impedances of the transistors are ignored, and it is assumed that the transistors are the same size, will have the same current since they both have the same gate-to-source voltage V_{GS}. However, when finite drain-to-source impedance is considered, whichever transistor has a larger drain source voltage will also have a larger current [12]. In (23) the equation that demonstrates the current mirror performance can be seen.

$$\frac{I_1}{I_B} = \frac{(W/L)_2}{(W/L)_1} \quad \frac{I_2}{I_B} = \frac{(W/L)_4}{(W/L)_1} \quad \frac{I_3}{I_B} = \frac{(W/L)_6}{(W/L)_1} \tag{23}$$

where I_B is the current bias, $I_{1\text{-}2\text{-}3}$ the current mirror copy, and W/L the transistor aspect ratio.

The currents I_1 and I_2 generate in the *n*-channel transistors a voltage bias V_{bias} which drive the folded cascode stage and the common source stage. The current I_3 biases the differential pair. Subsequently, these aspects will be extensively explained in the OTA design procedure.

A more accurate expression can be checked in (24), in which the dependence on the channel length modulation λ and the V_{DS} in included,

$$\frac{I_1}{I_B}=\frac{(W/L)_2}{(W/L)_1}\frac{(1+\lambda V_{DS2})}{(1+\lambda V_{DS1})} \quad \frac{I_2}{I_B}=\frac{(W/L)_4}{(W/L)_1}\frac{(1+\lambda V_{DS3})}{(1+\lambda V_{DS1})} \quad \frac{I_3}{I_B}=\frac{(W/L)_6}{(W/L)_1}\frac{(1+\lambda V_{DS6})}{(1+\lambda V_{DS1})}$$
$$\lambda \approx \frac{\Delta L}{V_E L} \tag{24}$$

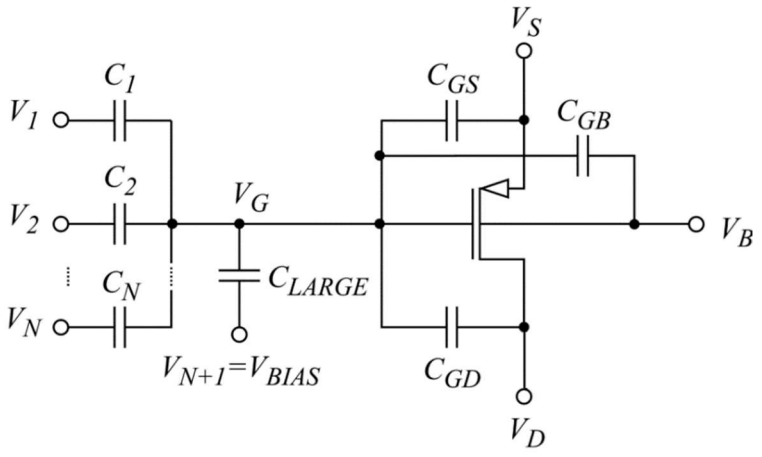
where I_B is the current bias, $I_{1\text{-}2\text{-}3}$ the current mirror copy, W/L the transistor aspect ratio, V_{DSi} is the i-th transistor drain-to-source voltage, λ the channel length modulation coefficient, L the transistor length and V_E is a technology parameter, similar in concept to the Early Voltage for BJTs. These equations demonstrate that a better current copy performance is achieved if a bigger V_{DS} or L is configurated.

3.3. Design Techniques

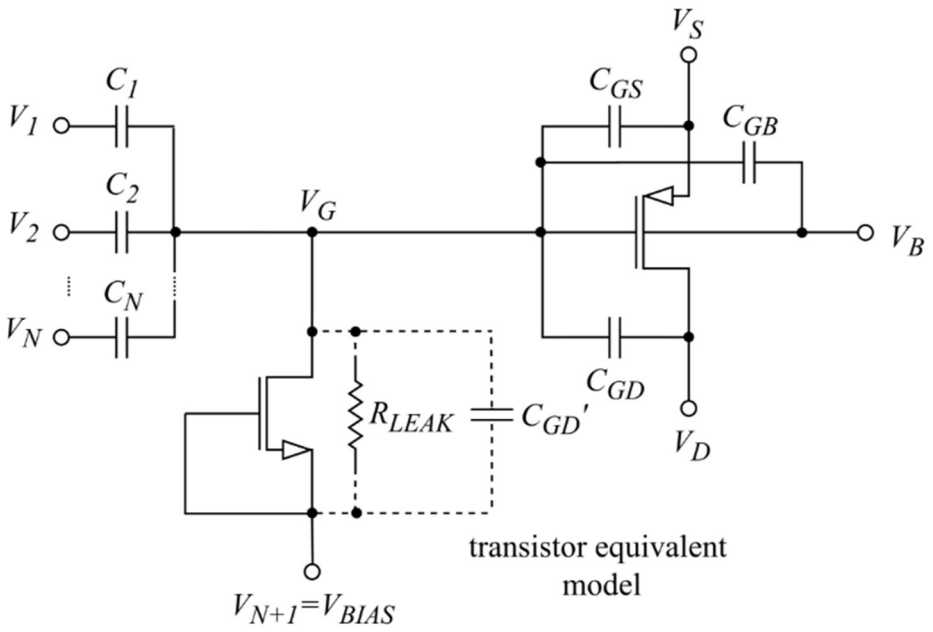
Then, some design techniques which improve the OTA performance will be introduced. Specifically, the technique of the Quasi Floating-Gate transistor will be studied, as well as the difference between the Class-A/Class-AB amplifier stages.

3.3.1. Quasi Floating-Gate Transistor

The Quasi Floating-Gate (QFG) transistor is a low-voltage low-power analog design technique in which circuits the supply voltages are decreased and get closed to the MOS transistor threshold voltage. This technique seeks to improve the performance of analog circuits during the transitory response. It is based in the Multiple Input Floating-Gate (MIFG) transistor, in which technique a weighted averaging of the inputs accurately controlled by capacitance ratios can be obtained, which is the basic operating principle. Nevertheless, issues often encountered in MIFG structures, such as the initial charge trapped in the floating-gates or the gain-bandwidth product degradation, are not present in QFG configurations [11]. The difference between the two techniques for a PMOS transistor can be seen in Fig. 12. and the equations that describe the model can be consulted in Table IX.



(a)



(b)

Fig. 12. (a) Multiple Input Floating-Gate (MIFG) *p*-channel transistor equivalent circuit. (b) Quasi Floating-Gate (QFG) *p*-channel transistor equivalent circuit.

TABLE IX
MIFG-QFG VOLTAGE GATE EQUATIONS.

MIFG
$V_G = \frac{C_{LARGE}}{C_T} V_{BIAS} + \frac{1}{C_T}\left(\sum_{k=1}^{N} C_k V_k + C_{GS}V_S + C_{GD}V_D + C_{GB}V_B\right)$ $C_T = \sum_{k=1}^{N} C_k + C_{GS} + C_{GD} + C_{GB}$ (25a)   where C_k is the k-th coupled input capacitor
QFG
$V_G = V_{BIAS} + \frac{sR_{leak}}{1 + sR_{leak}C_T}\left(\sum_{k=1}^{N} C_k V_k + C_{GS}V_S + C_{GD}V_D + C_{GB}V_B\right)$ $C_T = \sum_{k=1}^{N} C_k + C_{GS} + C_{GD} + C_{GB} + C'_{GD}$ (25b)   where C_k is the k-th coupled input capacitor

It is necessary to comment the disadvantages of the MIFG to justify the use of the QFG technique in the current project, according to [10]:

- The problem of the initial *charge trapped* in the transistor gate terminal. It is necessary to eliminate it using techniques like different metal contacts levels in the layout, to discharge the gate in the deposition of the metal layers, but leave it floating again after the process of etching. Finally, after the manufacturing, the gate will be floating without the charge trapped.
- The couple capacitor C_{LARGE} dimension is very large so the total area necessary to manufacture the circuit will be increased.
- Due the large size of C_{LARGE} in the differential input, the gain-bandwidth is decreased.

These problems can be solved using a resistor with a large value (R_{leak}), connecting the floating-gate to the DC polarization voltage instead of using the C_{LARGE} capacitor. With this configuration, the QFG transistor is obtained, as can be seen in Fig. 12(b) As in the MIFG case, the input terminals are capacitively coupled to the quasi-gloating gate but in this case, the DC gate voltage is fixed by a resistor instead a large capacitor. In practice, this resistor can be implemented using a NMOS minimum size transistor in the cut-off region in which not current flows through, and which can be got shorting the gate and source terminals. This is a very important aspect because implies a reduction of the total area in comparison with the C_{LARGE} capacitor [10].

From (25b), can be deduced that the inputs suffer a high-pass filtering with a cut-off frequency of $1/(2\pi R_{leak}C_T)$, which can take very low values. So that, even for very low frequency signals, the expression (25b) is a weighted sum of the input voltages determined by the relationships between capacities, plus some parasitic terms [10].

In the QFG transistors, the R_{leak} resistor establishes a DC voltage at the gate of the transistor equal to the DC voltage that has been applied to its terminal, and on it, overlaps the AC voltage of the expression (25b) produced by the other inputs. In this way, the gate voltage may be less than the negative supply voltage, which is quite common when the circuit is powered with voltages below 1V. This is not a problem while the potential difference between the voltage and the supply voltage is less than the voltage that causes the *p-n* junction between the body and the source of the NMOS transistor which it has been implemented R_{leak}. To control this problem, accurate ratios between the coupling capacitors of the inputs must be elected [10].

A similar analysis can be done for a NMOS QFG transistor, in which the resistor is implemented using a PMOS transistor in the cut-off region.

3.3.2. Class-A / Class-AB Amplifiers

Another design technique to use which improves the performance of the circuit is the use of a *Class-AB* output stage instead of a *Class-A* stage. This Class-AB operation from Class-A is achieved using the already seen QFG transistor technique. In Fig. 13. the implementation of the Class-AB stage using the QFG technique can be seen. It should be noted that the Class-A amplifier is formed by the already seen common-source amplifier.

The use of the floating battery in the Class-AB stage in Fig. 13(a) allows the node B to follow the voltage variations of the node A, with a DC voltage difference of V_{bat}. In the absence of signal, the current is stablished by the node A voltage added to the DC voltage V_{bat}. However, in dynamic conditions, the node A signal variations are transferred to the node B, allowing that the output current is not limited by the current obtained in static conditions. In Fig. 13(b), this floating battery is implemented using the QFG technique, in which can be seen that the output current exists in absence

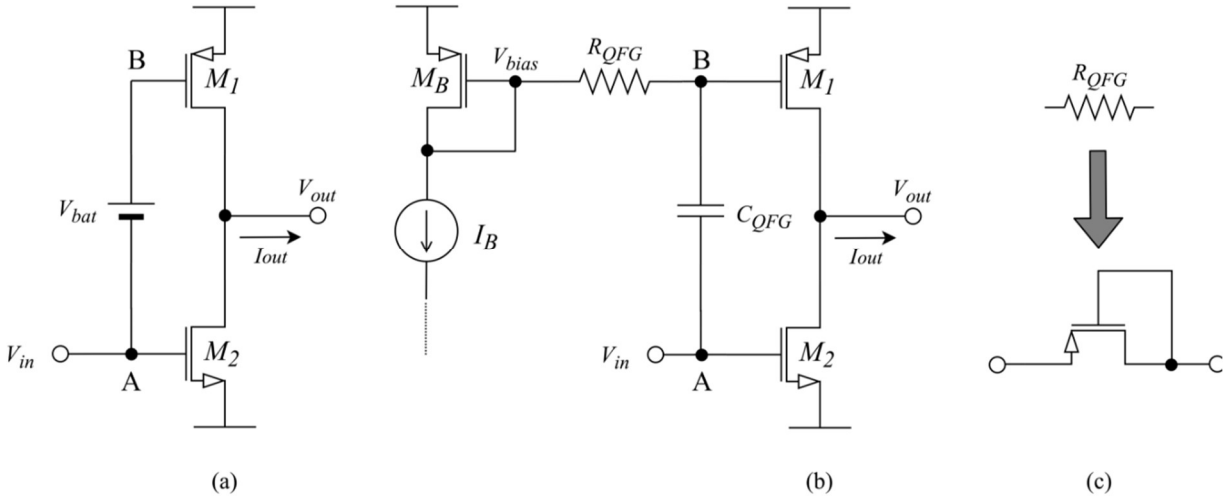


Fig. 13. Basic Class-AB stage. (a) Using floating battery. (b) Using the QFG transistor. (c) Implementation of the R_{QFG}.

of signal, which value is I_B. This is due to the fact that the capacitor acts like an open circuit and the current is fixed by the current mirror formed by the NMOS transistor. In dynamic conditions, the voltage of the node A is transferred to the node B as has been said. It should be noted the high pass filtered, which cut-off frequency is $1/(2\pi R_{QFG}C_{QFG})$. Due to the large resistor value, this cut-off frequency has a low value, so the filtered avoid that the DC voltage will be transferred from A to B. In Fig. 13(c), the implementation of this resistor using a minimum *W/L* transistor operating in the cut-off region can be checked [10].

The main advantage of the Class-AB configuration is the improvement of the *Slew-Rate* when the circuit operates in large-signal. In (26) the Slew-Rate expression can be seen,

$$SR_+ = \frac{I_{out}^{max}}{C_L} \tag{26}$$

where I_{out}^{max} is the maximum output current and C_L is the load capacitor.

If the system operation is in *small-signal*, the output voltage is low, so a big quantity of current for charge the capacitor is not required. This means that in these circumstances, although the current bias is low, the Slew-Rate parameter is not affected. Another approach for understanding the concept is that in small-signal, the capacitor acts like an open circuit [10]. In this case, the circuit performance is like the classic common-source class-A amplifier, so the Slew-Rate, as has been said, is not affected.

On the other hand, if the system operation is in *large-signal*, the quantity of current for charge the capacitor, for obtaining a large voltage output, is bigger. In this case the Slew-Rate is affected. The bigger the current output is, the faster the capacitor charge is, and the bigger the Slew-Rate parameter is. In the large-signal case, due to the dynamic characteristic, the QFG capacitor take part in the performance [10].

In the class-A circuits, the output current is limited by the current bias I_B, which is the maximum current to achieve. Hence, the maximum Slew-Rate value is $SR_{max} = I_B/C_L$. When the small-signal analysis is considered, it is not a problem because a good performance can be achieved with low bias currents. But in the large-signal analysis, large values of I_B should be fixed for achieve a greater Slew-Rate. This current bias increase, implies a power consume increment. Here implies the advantage of using a class-AB topology. In this circuits, the output current is not limited to I_B, in fact, can be bigger if a signal exists in the input. In this way, a large value of Slew-Rate can be achieved, which is important for the large-signal operation, but maintaining a low power consume due to the low value of the current bias [10].

In conclusion, for a better large-signal performance, a Class-AB topology can be used, in contrast with a class-A topology. With the Class-AB topology, the system speed is greater and the dynamic response improves with fast signal variations, or that is the same, high frequency components [10]. Additionally, the static power consume of a Class-AB amplifier is the same as a class-A amplifier.

3.4. OTA Design

Once the definition of the OTA has explained, the basic OTA circuit stages as well as some design techniques have been studied, the final step consists in design the final topologies using them. Two topologies have been design. One corresponds to a Class-A amplifier and the another to a Class-AB amplifier which uses the QFG transistor technique already studied. Then, these topologies will be shown, as well as the design procedure followed.

3.4.1. Circuit Topologies

In Fig. 14. the two OTA Class-A/Class-AB topologies can be seen. It is important to appreciate that they are similar except the QFG transistor technique included which converts the Class-A amplifier in a Class-AB topology. The different stages of the circuit are mentioned below, which have been studied previously:

- The first stage uses the transistors M_1, M_2, M_3, M_4, M_5, M_6, M_7 and M_8 forming a *folded-cascode circuit*. As seen, this topology fits very well in a low power system.
- In Fig. 14(a), the second stage is formed by M_9 and M_{10} in a *Class A* configuration.
- In Fig. 14(b), the second stage is formed by M_9 and M_{10} in a *Class AB* configuration, to get more current at the output of the system and to increment the slew rate parameter. This configuration is achieved using the QFG transistor technique, which is implemented with C_{QFG} and R_{QFG}.
- M_{b1}, M_{b2}, M_{b3}, M_{b4}, M_{b5} and M_{b6} are used as *current mirrors bias*.
- Between the nodes A and B, a *compensation network* is required for maintaining the stability of the system. In the current project, different compensation strategies will be used. This aspect will be threatened in Section 4.

The small-signal equivalent simplified model of the proposed two-stage OTAs is shown in Fig. 15., in which can be observed the transconductances of each stage, the QFG technique and the presence of the compensation network. In this model, g_{mi}, R_{oi} and C_{oi} are the i-th stage transconductance, resistance and equivalent output capacitance respectively, C_{QFG} is the QFG capacitor and R_{QFG} is the QFG resistor. It should be noted that g_{m1} can be the transconductance of M_1 or M_2 due to the symmetry of the circuit, g_{m9} is the transconductance of M_9 and g_{m10} is the transconductance of M_{10}. It is important to appreciate one detail. In the case of the class-A topology, the second stage transconductance is g_{m9}, but in the Class-AB topology is $g_{m9}+g_{m10}$. This shows how the QFG technique improves the performance of the system, increasing the output transconductance and therefore, the Slew-Rate. This transconductance increment is produced during dynamic conditions, that is it, when the input signal changes. In stationary state, the C_{QFG} behaves like an open circuit, and the g_{m10} transconductance does not affect the performance. One important aspect of the circuit is the knowledge of the different stage currents, I_i, associated to the stage transconductances, which in general are not equal to the stage bias currents. For the first stage the current I_1, associated with g_{m1}, is equal to half M_{b6} drain current, $I_{Mb6}/2$, but the first stage bias current, I_{B1}, is equal to $I_{B1} = I_{Mb6} + 2 \cdot I_{M5,6}$ (the bias contribution of the differential input and the bias contribution of the folded section). Besides, in the second stage, the current bias is equal to the stage current, that is it, $I_{B2} = I_2 = I_{M10}$.

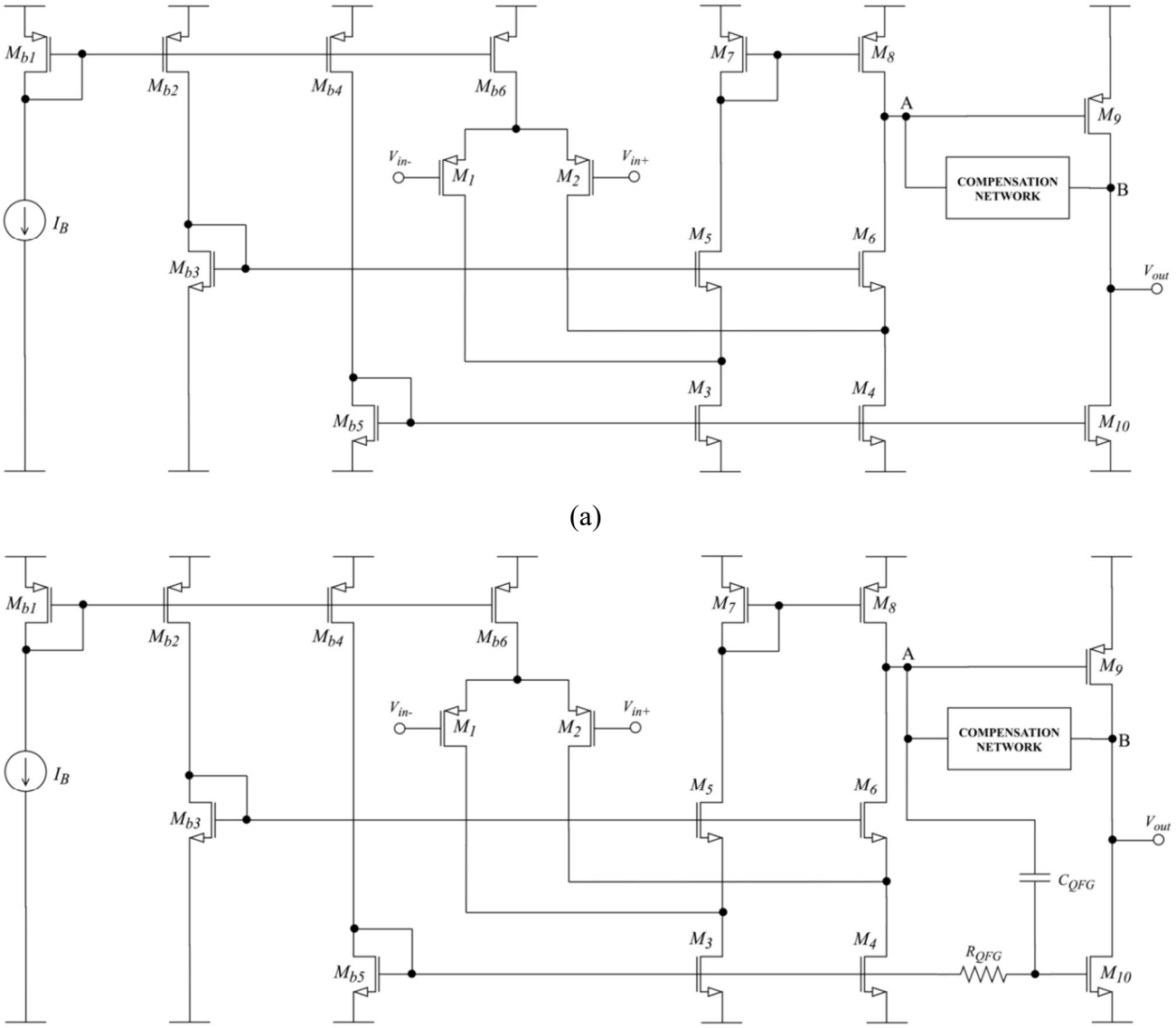
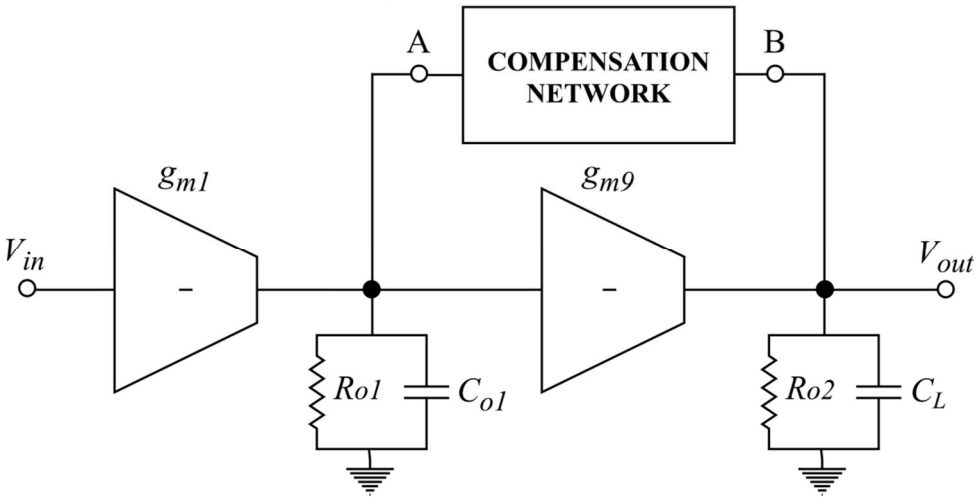
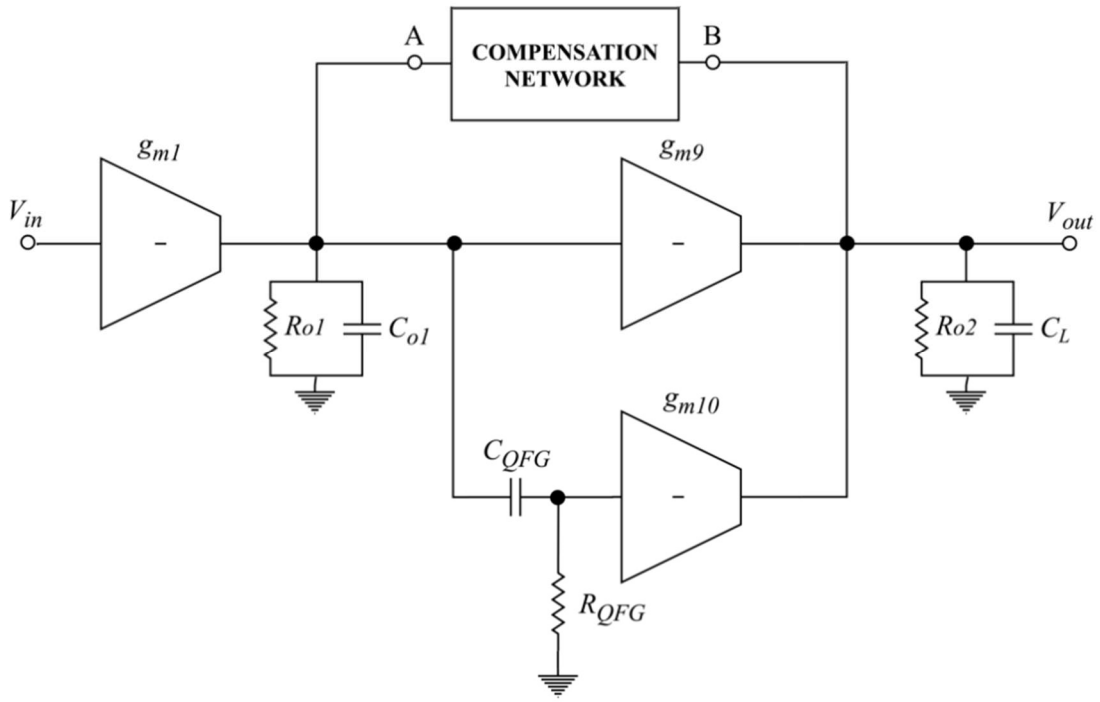


Fig. 14. (a) OTA Class-A amplifier. (b) OTA Class-AB amplifier.





(b)

Fig. 15. Small-signal equivalent models. (a) OTA Class-A amplifier. (b) OTA Class-AB amplifier based on QFG technique.

3.4.2. Design Procedure

Then, the designed procedure will be explained. The objective is to show some guidelines to follow in order to design the system. These guidelines will be explained in different organized points.

1) Sub-threshold inversion mode

The first system design constraint is the election of the inversion mode. In the current design, the sub-threshold mode has been elected, to obtain a low power system.

2) Current bias source I_B

Once the sub-threshold mode has been elected, the next step consists in the election of the current bias system value. Its value implies aspects like the total consume or the system gain-bandwidth. The greater the current value is, the greater the gain-bandwidth is, but the grater the total consumption is. In the current design, this value will be low, in the order of nano-amperes *nA*. This is due to the sub-threshold mode must be achieved. Due to the presence of the current mirror network, this current will be replicated in M_{b2}-M_{b3}, M_{b4}-M_{b5} and M_{b6} branches.

3) M_{b2}-M_{b3} current mirror branch

This pair of transistors form the first current mirror brunch. For doing the copy, the transistor M_{b2} is used. Depending on the aspect ratio elected, the copy can be the same, bigger or lower respect the current bias I_B. It is important to consider the expression (24), which shows that the bigger the transistor length is, the better the copy is.

The copied current by M_{b2} is introduced in M_{b3}. In M_{b3}, a $V_{GS\,Mb3}$ proportional to I_{Mb3} is generated. This voltage biases the M_5-M_6 cascode transistors. Then, the value of $V_{GS\,Mb3}$ is explained.

– For a given M_{b3} aspect ratio, the bigger the current I_{Mb3} is, the bigger $V_{GS\,Mb3}$ is. This increment of I_{Mb3} can be controlled by the aspect ratio of M_{b2}.

– For a given M_{b3} current, the lower the aspect ratio of M_{b3} is, the bigger $V_{GS\,Mb3}$ for achieving this given current value is.

This $V_{GS\,Mb3}$ value is important to consider because, as has been said, biases the M_5-M_6 cascode transistors. Later, the importance of this bias voltage value will be analyzed, because an adequate $V_{GS\,Mb3}$ value, which bias M_5-M_6, imply that M_3-M_4 be kept in the sub-threshold mode saturation region.

4) M_{b4}-M_{b5} current mirror branch

This case can be analyzed in the same way as the case 2), but for the transistors M_{b4} and M_{b5}. The difference with respect to the previously case is that the M_{b5} generates a voltage bias which polarizes the transistors M_3-M_4, which in turn, act like the current bias source for the folded-cascode section. Overall, M_{b5}, M_3 and M_4 form a current mirror.

Again, the importance of this bias voltage value will be analyzed because will imply that M_3-M_4 will be kept in the sub-threshold mode saturation region.

5) M_{b6} current mirror branch

This is the last transistor of the current mirror network to analyze. M_{b6} acts like a current source which biases the differential input stage pair. The copied current, which can be achieved electing an adequate M_{b6} aspect ratio, is divided in the differential pair. Again, it is important to consider the expression (24), which shows that the bigger the transistor length is, the better the copy is.

One good design practice consists in maintaining M_{b6} in the saturation region for achieving a good performance. One method consists in modify the transistor current. The lower the I_{Mb6} is, the more $V_{DS\text{-}Mb6}$ is. But this current could be a design constrain, so it could not be possible to modify it. Another method consists in modify the aspect ratio of the differential pair transistors. This aspect will be considered later.

6) M_1-M_2 differential pair transistors

These pair of transistors form the differential-input pair. They are an important element in the circuit because their produce the differential input signal and their transconductance values $g_{m1,2}$ are widely used in the design equations. These values are controlled by the current bias through transistors. It is important to appreciate that these current values are the half bias differential pair current, as can be seen in (27)

$$I_{M1,M2} = \frac{I_{Mb6}}{2} \tag{27}$$

where I_{Mb6} is the differential pair current bias generated by M_6. Due to the sub-threshold mode, as can be seen in (16a) of Section 2, the $g_{m1,2}$ transconductance value can be obtained in (28)

$$g_{m1,2} = \frac{I_{Mb6}/2}{nv_t} \tag{28}$$

As said before, an important design aspect is maintaining M_{b6} in the saturation region. One method consisted in modify the current I_{Mb6}, in which case the lower it was, the more $V_{DS\,Mb6}$ was achieved. But this current could be a design constrain, so it could not be possible to modify it. Another method consists in modify the aspect ratio of these differential pair transistors. The grater the aspect ratio is, the less $V_{GS\,M1\text{-}M2}$ is required. If $V_{GS\,M1\text{-}M2}$ is lower, for a constant $V_{G\,M1\text{-}M2}$, the bigger is the value of $V_{S\,M1\text{-}M2}$ and the bigger is $|V_{DS\,Mb6}|$, making that M_{b6} enter more deeply in the saturation region.

In Fig. 16(a) are shown these concepts, in which can be appreciated how must be the V_{DS6} signal below -100 mV for maintaining M_{b6} in the saturation region. Additionally, it is shown how can be improved this range making the aspect ratio bigger.

It must exist a compromise between the aspect ratio and the M_{b6} saturation region range. In the current project, M_1 and M_2 have been designed for maintaining M_{b6} in a wide temperature range.

7) M_3-M_4 current bias transistors

These two transistors form the current bias of the cascode stage. They are biased by the transistor M_{b5} already seen. As in case 6), is it important to keep these transistors in the saturation region for having a good circuit performance. For controlled this $V_{DS\ M3\text{-}M4}$ value, different approaches can be followed:

- Decreasing the current through M_3-M_4, which can be configured with the aspect ratio between M_{b5}, M_3 and M_4. The less currents $I_{M3\text{-}M4}$ are, the grater voltages $V_{DS\ M3\text{-}4}$ are, and therefore, M_3 and M_4 are in a deeper saturation state. But this $I_{M3\text{-}M4}$ currents could be a design constraint, so it could not be modified.
- Decreasing the $V_{G\ M5\text{-}M6}$, which is controlled by I_{Mb3}. The idea consists in achieve a $V_{G\ M5\text{-}M6}$ value which makes $V_{DS\ M3\text{-}M4}$ bigger than 100 mV. If I_{Mb3} is decreased, $V_{GS\ Mb3}$ is decreased. Due to the currents through M_5-M_6 are constants, the $V_{S\ M5\text{-}M6}$ is reduced and so, $V_{DS\ M3\text{-}M4}$ is increased.
- Decreasing the aspect ratio of M_5-M_6. Due to the currents through M_5-M_6 and the voltages bias $V_{G\ M5\text{-}M6}$ are constants, the smaller the aspect ratios of M_5-M_6 are, the less the voltages $V_{GS\ M5\text{-}M6}$ are and the greater the voltages $V_{D\ M5\text{-}M6}$ are. The conclusion is that $V_{DS\ M3\text{-}M4}$ is increased.

In Fig. 16(b) are shown these concepts, in which can be appreciated how must be the $V_{DS\ M3\text{-}M4}$ signal above 100 mV for maintaining M_3 and M_4 in the saturation region. Additionally, it is shown how can be improved this range making the aspect ratio bigger.

Another aspect to consider is the current configured through these transistors. In the current project, these values will be configured with the same value as I_{Mb6}. In case 8) will be justified.

Finally, M_3 and M_4 have been designed in a wide temperature range, which are controlled by $V_{GS\ M5\text{-}M6}$ and the aspect ratios of M_5-M_6.

8) M_5-M_6 cascode transistors

These two transistors act as cascode configuration. As can be seen, its presence implies the increment of the gain stage and to achieve a low voltage system. As has been explained in case 7), is important to select an adequate aspect ratio for maintaining M_3 and M_4 in the saturation region.

Another aspect to consider is the current elected through these transistors. In the current project, the current elected in M_5 and M_6 is the same as M_1 and M_2, that is, $I_{Mb6}/2$. The following general expression (29) defines the currents of the drains of M_3 and M_4 with the current of M_5 and M_6 properly. Considering that the current in M_3 and M_4 is the same as I_{Mb6}, and the current in M_1 and M_2 is $I_{Mb6}/2$, the equation (29) shows that the currents in M_5 and M_6 are the same as the currents in M_1 and M_2.

$$I_{M5,M6} = I_{M3,M4} - I_{M1,M2} = I_{Mb6} - \frac{I_{Mb6}}{2} = \frac{I_{Mb6}}{2} \tag{29}$$

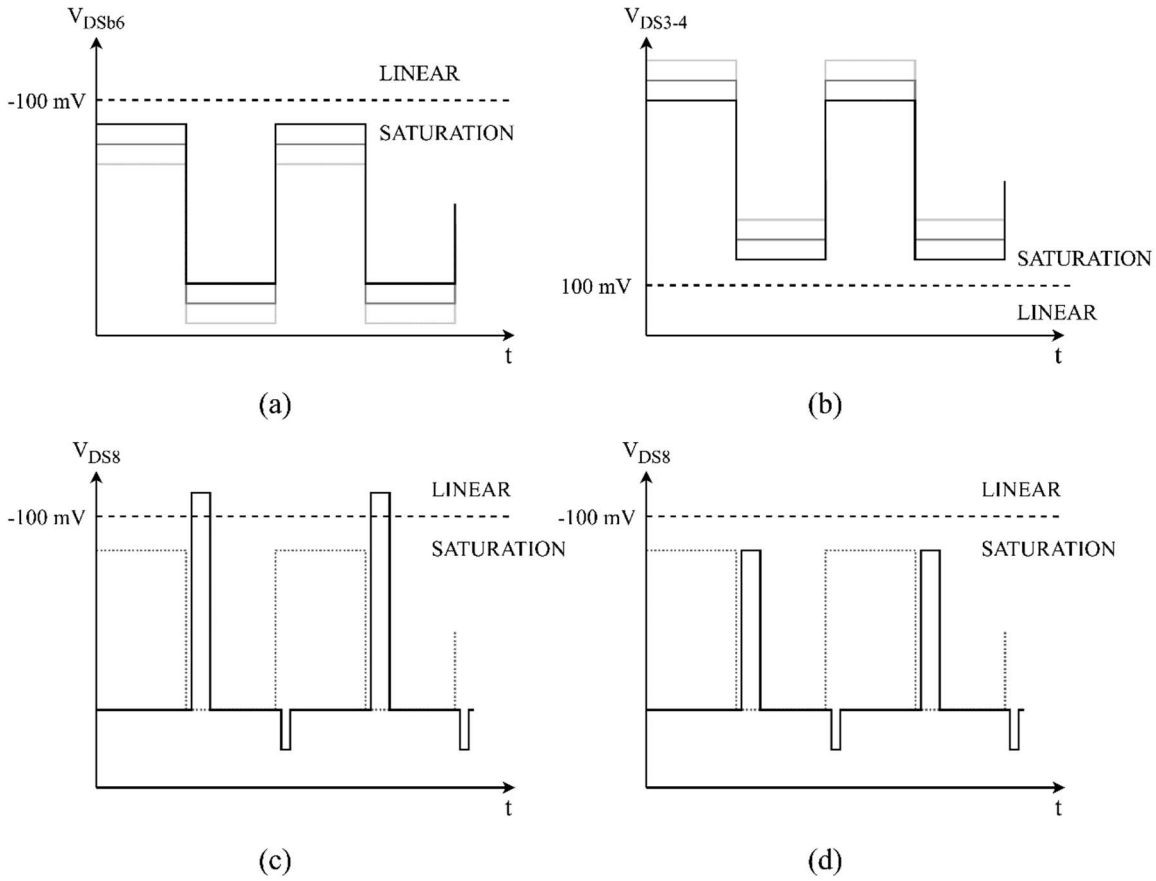


Fig. 16. Different drain-to-source voltages V_{DS} in some critical transistors which enter in the linear region. (a) V_{DS} in M_{b6}. (b) V_{DS} in M_3-M_4. (c) V_{DS} in M_8 entering in linear mode. (d) V_{DS} in M_8 maintaining in the transistor in saturation mode due to the QFG technique.

9) M_7-M_8 current mirror transistors

The principal characteristic of these transistors consists of converting the differential-input stage in a single-ended output design. For achieving this, the current in the drain of M_5 is copied by the current mirror M_7 and M_8. Then, the difference between the currents of I_{M5}, which is copied by the current mirror, and I_{M6} is generated. This difference generates a voltage that is amplified by the output stage, which is formed by M_9 and M_{10}.

It is important to maintain the transistor M_8 within the saturation region. Due to the sub-threshold mode is used, implies the presence of low currents and therefore, a slow system performance. This slow performance makes a slow high-to-low transition in the output first stage, which is not sufficient for discharging the output second stage. The maximum system output current used to discharge is given by M_{10}, which is low and as has been said, is not sufficient. This slow characteristic generates in M_8 a short glitch in time which makes M_8 entering in the linear region.

In Fig. 16(c) this problem is shown. In case 11), will be solved using the QFG transistor technique.

10) M_9-M_{10} output transistors

The system output is formed by these two transistors, which act as a common-source amplifier. Depending if the QFG technique is used, this output stage will be configured as a class-A or class-AB stage. The transistor which biases this stage is M_{10}. The greater its value, the lower the probability that M_8 will enter in the linear region is. This current bias can be configured with the aspect ratio of M_{10}, which form a current mirror with M_{b5}.

The transistor M_9 amplifies the first stage signal, generating a current proportional. The output system current can be analyzed in (30). It is important to consider the aspect ratio of this transistor, which affects to its parasitic capacitance. The greater the transistor is, the grater its parasitic capacitance is. This parasitic capacitance is used for calculating the compensation values, which will be analyzed in Section 3.

$$I_{out} = I_{M10} - I_{M9} \tag{30}$$

In the current project, the aspect ratio of M_9 has been elected for keeping the currents through M_7 and M_8 equal. This concept can be seen in Fig. 17.

11) QFG technique implications

As has been said, the QFG transistor technique pretends to improve the performance of the system. The main characteristic is to convert the class-A output stage in a class-AB stage. This change implies the improvement in the Slew-Rate parameters.

Another implication of this technique consists in maintaining M_8 in the saturation region. The presence of the QFG implies the increment of the $V_{GS\,M10}$ during the low-to-high transition in the output first stage, which introduces more current in the output stage and therefore, discharging faster the output load. In this case, the Negative-Slew-Rate will be improved. During the high-to-low transition, the $V_{GS\,M10}$ is decreased, so the Positive-Slew-Rate will have got worse. In Fig. 16(d), can be checked how has been solved this problem.

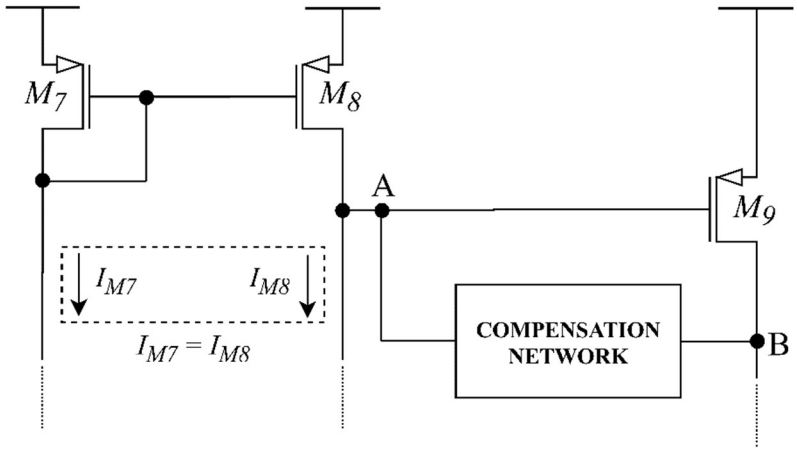


Fig. 17. Folded-cascode current mirror with the same drain currents for avoiding an offset voltage which are controlled by M_9 aspect ratio.

The QFG technique main performance is during the low-to-high transition in the output first stage. It must be considered that in the high-to-low input transition, due to the inverting characteristic of the folded-cascode amplifier, in the first output stage a low-to-high transition will be generated, which increases the $V_{GS\,M10}$ voltage. In conclusion, the Negative-Slew-Rate is improved during the high-to-low input transition, or what is the same, during the low-to-high transition in the output first stage. In the opposite case, the Positive-Slew-Rate is got worse during the low-to-high input transition, or what is the same, during the high-to-low transition in the output first stage. When the simulation will be done in Section 4 and 5, it could be checked how the Negative-Slew-Rate will be improved, and the Positive-Slew-Rate will have got worse, but not such a great quantity in comparison with Negative-Slew-Rate. In Fig. 18. could be analyzed all this process.

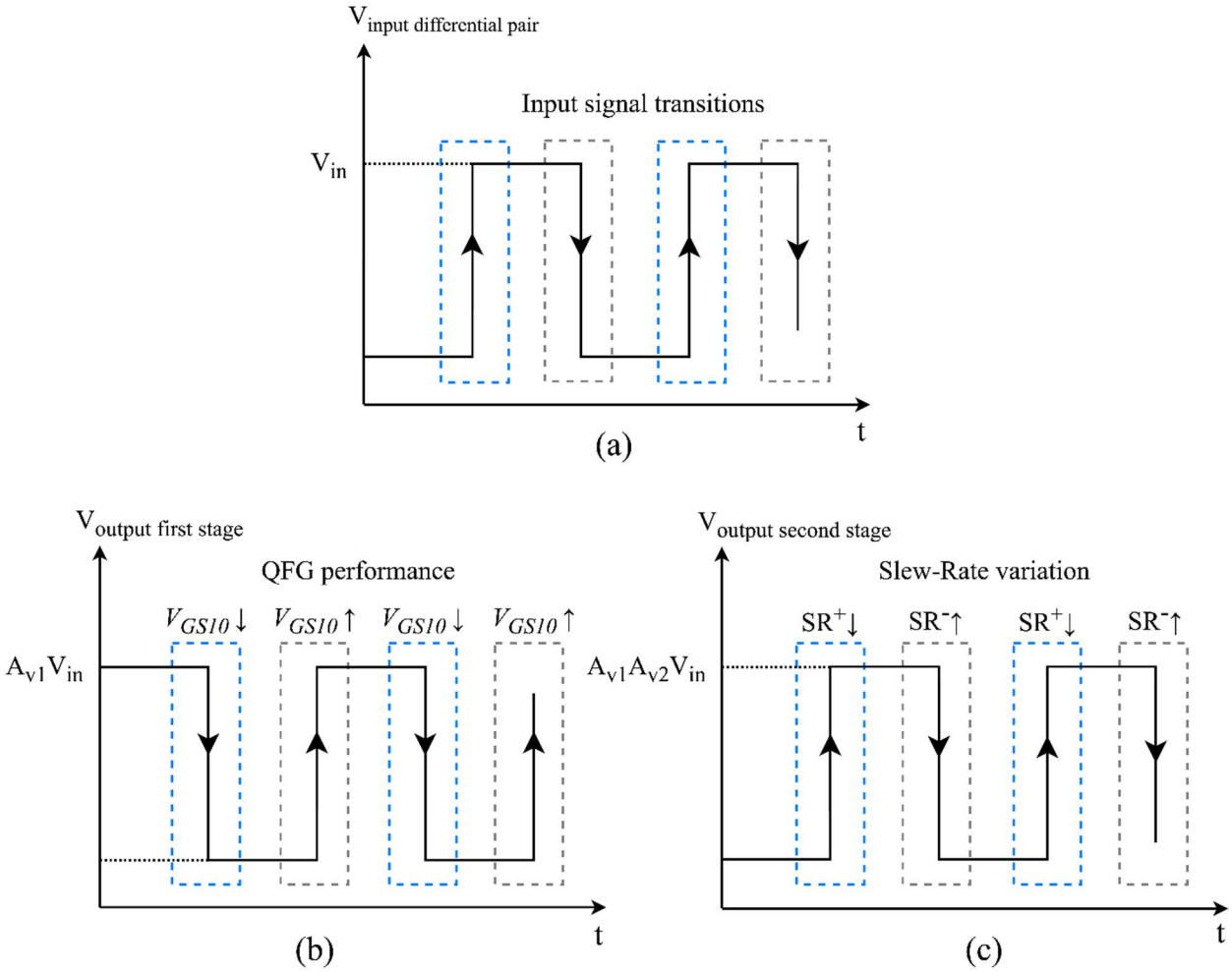


Fig. 18. QFG performance process which its implication in the Slew-Rate parameter. (a) Differential input signal. (b) First stage output signal. (c) Second stage output signal.

12) System compensation

For maintaining the stability of the system, some type of *compensation technique* between the nodes A-B must be used. This different compensation techniques, as has been said, will be analyzed in Section 4.

13) Temperature and process variations

With the aim of designing a robust system, the considerations in cases 5), 7) and 9) will be considered. For achieving this, the system must be simulated in different *temperature and different process variations cases*, as the corner analysis. These considerations are explained below:

- The temperatures to simulate are -10ºC, 27ºC and 85ºC.
- The corner analysis will include the Nominal, Fast, Slow, Fast N / Slow P and Slow N / Fast P process variations.

Then, the worst cases are analyzed, which will be used for making the system robust. The main idea is maintaining the transistor M_{b6}, M_3, M_4 and M_8 in the saturation region for the worst extreme temperature and process variation cases as much as possible.

- For the case 5), the -10ºC and Slow corner analysis will be considered.
- For the case 7), the -10ºC and Fast corner analysis will be considered.

– For the case 9), the 85ºC and Slow N / Fast P will be considered.

> ***Commentary**: These considerations will be carried out as much as possible in order to make the system as robust as possible. It is important to note that in some cases it is difficult to achieve the desired robustness for the extreme case without making variations of parameters such as aspect ratios or bias currents which are not viable.*

14) Interdigitation transistors

The last OTA aspect design is related with the pre-layout design plan. In order to achieve a compact design, the interdigitation transistor technique must be used. In the current design, the transistors which will be interdigitated are:

– The differential-input pair M_1-M_2 transistors.
– The current mirror network transistors and the differential pair current bias source M_{b1}-M_{b2}-M_{b4}-M_{b6}.
– The current mirror folded-cascode network and the output current bias source M_{b5}-M_3-M_4-M_{10}.
– The folded cascode current mirror M_7-M_8.

4. OTA FREQUENCY COMPENSATION

It is well known that when one or more stages are added in a simple OTA, some poles and zeros are introduced. In the case of the poles, it implies the presence of a relevant pole which can destabilize the system and produce, for example, oscillations at the output. This performance can be determined by the concept of phase margin. Low phase margins lead to poor stability.

The mechanism for compensate this relevant pole consist in moving it towards higher frequencies. For doing this, a *compensation frequency technique* is used. The presence of the compensation frequency technique is a simple but a very effective and necessary strategy because it produces the pole compensation. It can be said that is a simple idea which produces a great performance. This compensation network increases the phase margin towards a desired value.

In this section, the well-mentioned compensation frequency technique will be studied and explained, detailing the philosophy of the compensation process. Then, different compensation strategies will be introduced, which will be used and implemented in the OTA.

4.1. Concept of the Frequency Compensation

This section discusses the use of OTAs in closed-loop configurations and how to compensate them to ensure that the closed-loop configuration is stable.

Optimum compensation of OTAs is typically considered to be one of the most difficult parts of the OTA design procedure. However, if the systematic approach taken here is used, then a straightforward procedure can be followed that almost always results in a near-optimum compensation network.

> ***Commentary**: The following explanation corresponding to this "Section 1.1. Concept of the frequency compensation" has been taken from the pages (pp. 254-255) of the book reference [12]. Some variations have been done for adapt the explanations to this current project. The content of the book illustrates very well the concept of compensation and that is why it has been decided to take it. The author's rights are reserved and it is appreciated his work done.*

4.1.1. Dominant-Pole Compensation and Lead Compensation

The two most popular tools available to analog circuit designers for OTA compensation are *dominant-pole compensation* and *lead compensation*.

The dominant-pole compensation is performed by forcing a feedback system open-loop response to be closely approximated by a first-order response up to the loop unity gain frequency. First-order feedback systems are unconditionally stable with at least 90º phase margin. Unfortunately, OTA second and high-order circuits generally have multiple poles and zeros. Increasing the frequency of poles in a circuit is not generally practical since that would demand increased power consumption or some other undesirable trade-offs. Hence, the easiest way to make the system behave like a first-order system is to intentionally decrease the frequency of one dominant pole, making it much lower than the other poles and zeros of the system. The idea is shown in Fig. 19. which plots the open loop response, $L(\omega)$. Recall that $L(\omega)$ is the product of the amplifier response and the feedback network response (defined as the inverse of the desired closed-loop gain), $A(\omega)\beta$. During dominant-pole compensation, the pole frequency ω_{p1} has been decreased to a new much lower frequency. The result is a decrease in the unity-gain frequency of $L(\omega)$, ω_t, and an attendant increase in phase margin.

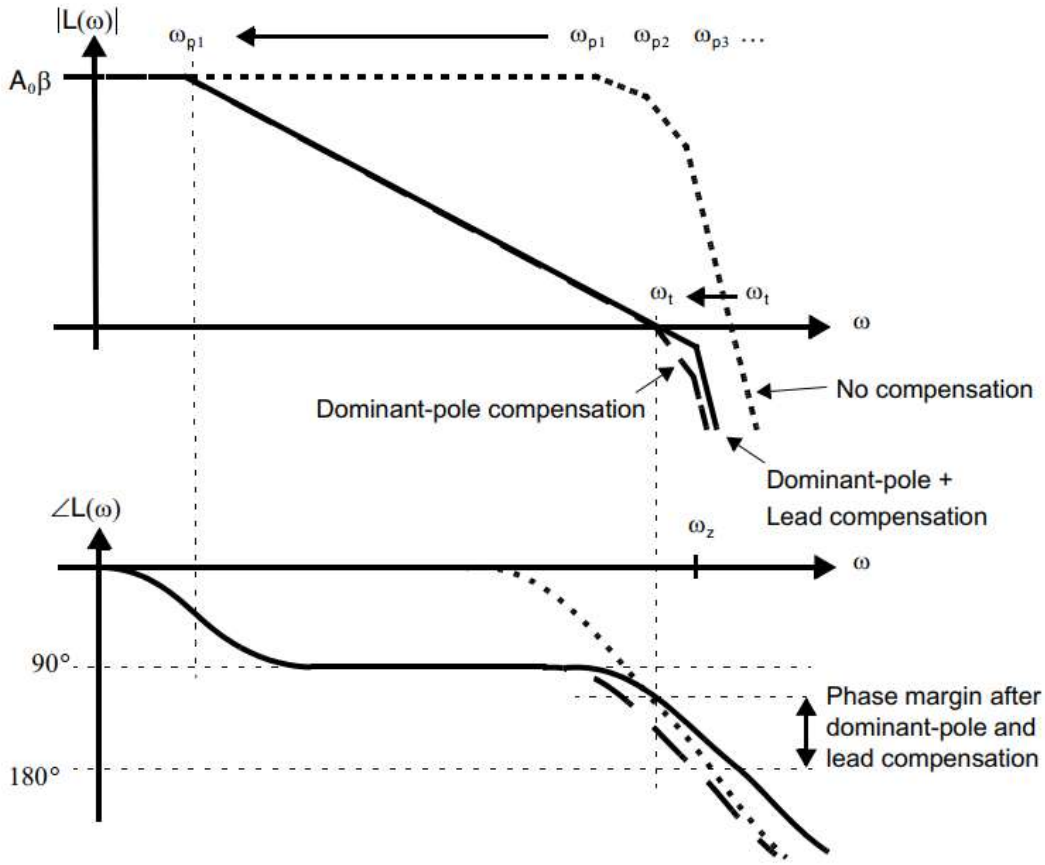


Fig. 19. A Bode plot of open-loop gain illustrating dominant-pole and lead compensation. Taking from [12].

A further increase in phase margin is obtained by lead compensation which introduces a left half-plane zero, ω_z, at a frequency slightly greater than ω_t. If done properly, this has minimal effect on the unity-gain frequency, but does introduce an additional approximately +20º phase shift around the unity-gain frequency. This results in a higher unity-gain frequency for a specified phase margin than would be attainable using dominant-pole compensation alone.

In Fig. 19., both dominant-pole and lead compensation are illustrated having minimal impact on the DC loop gain and the other pole and zero frequencies.

4.1.2. Compensating Process of a Two-Stage OTA

Stability and phase margin depend upon the loop gain of a feedback amplifier, *L(s)*, however, the next analysis has been focused on the response of the amplifier alone, *A(s)*. The feedback network must be accounted for in compensation. In Fig. 20. an undriven non-inverting circuit with a general feedback network is shown. Assuming the circuit has relatively high input impedance and an output impedance smaller than the load or feedback network, the loop gain may be approximated in (31)

$$L(s) = A(s)\beta \approx A(s)\frac{Z_1}{Z_1 + Z_2} \tag{31}$$

Although there are several different possible ways to factor *L(s)* into *A(s)* and β[3], the following straightforward approximation $\beta = Z_1 / (Z_1 + Z_2)$ may be adopted and it is assumed for analysis that β is constant up to the loop unity gain frequency. For example, in a unity gain configuration, $\beta = 1$, and $L(s) \simeq A(s)$. For an accurate determination of phase margin, simulation may be used to properly account for the impact of loading.

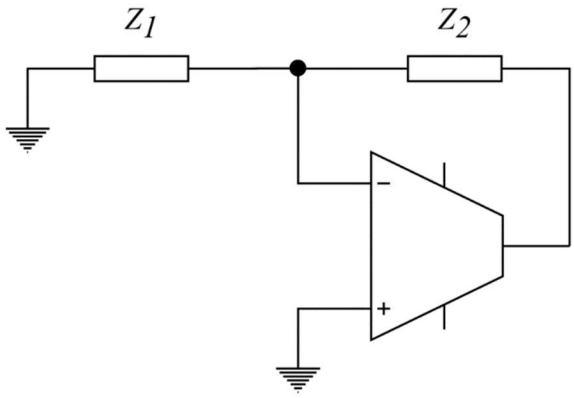


Fig. 20. An undriven non-inverting OTA circuit.

The simplest dominant-pole compensation technique consists in connect a capacitor between the output first stage and the output second stage. In Fig. 21(a) is shown this concept in a small-signal OTA circuit. The capacitor C_c controls the dominant first pole, (i.e., ω_{p1}), and so, the loop unity-gain frequency, ω_t as can be seen in (32)

$$\omega_t = \beta\frac{g_{m1}}{C_c} \underset{\beta=1}{\Longrightarrow} \frac{g_{m1}}{C_c}\ (unity\text{-}gain\ frecuency) \tag{32}$$

where β is the feedback network response, g_{m1} is the first stage transconductance and C_c is the compensation capacitor. Hence, by properly selecting the value of C_c, the dominant-pole compensation can be achieved.

Lead compensation is achieved using a resistor in series with the capacitor, names as R_c. If the small-signal model of Fig. 21(b) is analyzed with a nonzero R_c, then a third-order denominator results. The first two poles are still approximately at the frequencies given by (33) and (34). The third pole is

[3] Depending upon the configuration and application of the circuit, β may be taken as $-Z_1/Z_2$ (inverting configuration), $Z_1/(Z_1+Z_2)$ (non-inverting configuration) or $(-1)/Z_2$ (transimpedance feedback amplifier.)

at a high frequency and has almost no effect. However, the zero is now determined by the relationship (35)

$$\omega_{p1} \cong \frac{1}{g_{m2} R_1 R_2 C_c} \tag{33}$$

$$\omega_{p2} \cong \frac{g_{m2}}{C_1 + C_2} \tag{34}$$

$$\omega_z = \frac{-1}{C_c(1/g_{m2} - R_c)} \tag{35}$$

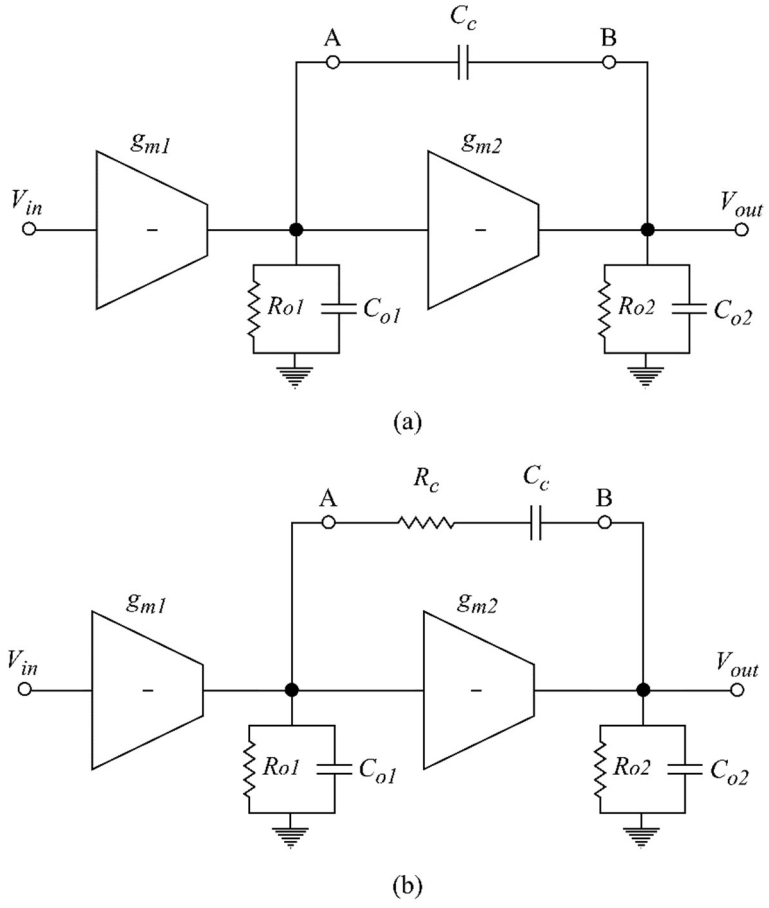


Fig. 21. OTA small-signal compensation process. (a) Dominant-pole compensation technique (b) Lead compensation.

where g_{m2} is the second stage transconductance, R_1 and R_2 are the output first and second stages resistances respectively, C_1 and C_2 are the output first and second stages capacitances respectively, C_c the compensation capacitor and R_c the compensation resistor.

This result allows the designer many possibilities of R_c depending of the assumptions taken and the followed method, which are shown in (36), (37) and (38)

$$R_c \cong \frac{1}{g_{m2}} \tag{36}$$

$$R_c \cong \frac{1}{g_{m2}}\left(1+\frac{C_1+C_2}{C_c}\right) \tag{37}$$

$$R_c = \frac{1}{1.7\beta g_{m1}} \tag{38}$$

where g_{m1} and g_{m2} is the first and second stage transconductances respectively, C_1 and C_2 are the output first and second stages capacitances respectively, C_c the compensation capacitor and R_c the compensation resistor and β is the feedback network response.

It should be noted that the last dominant-pole compensation corresponds with the classical Miller Compensation technique and the lead compensation with the Miller Compensation Pole-Zero Compensation technique. In the next Subsection 1.2., the Miller design equations will be given, as well as other compensation techniques.

4.2. Compensation Techniques for Two-Stage OTAs

Currently there are lots of compensation techniques. In [14], different compensation strategies for two-stage OTAs have been collected, studied, compared and simulated. They used passive or active components for achieve the compensation. These techniques are going to be simulated in the circuit described using the sub-threshold techniques. The different compensation techniques that will be implemented are:

- Miller Compensation with Nulling Resistor (MCNR).
- Miller Compensation with Nulling Resistor and Pole-Zero Cancellation (MCPZC).
- Voltage Buffer Compensation (VBC).
- Current Buffer Compensation (CBC).

In Fig. 22. the implementation of these four compensation techniques can be shown, which are connected between the nodes A and B. The node A corresponds to the output first stage and the node B to the output second stage.

The MCNR and MCPZC are passive strategies. It should be noted that both implementations are the same. But the pole-zero cancellation is more effective because produces the cancellation of a zero with a pole, as seen above. This cancellation is very useful because increases the bandwidth and the slew rate of the system. These two techniques are very simple because it only takes one capacitor and one resistor, which can be implemented by a linear region transistor.

The other two techniques VBC and CBC use active devices and seek to improve the isolation between the node A and B using a buffer strategy. This buffer can be implemented in voltage mode or in current mode. The voltage mode uses the finite output conductance of a voltage buffer to provide the pole-zero compensation. It should be noticed that this technique uses a common-drain circuit. In current mode, a current buffer is used for does the compensation. In this case, the circuit is based on a common-gate circuit.

> ***Commentary**: The detailed analysis of each compensation will not be detailed. Only, the implementation of each technique will be shown as well as the design equations. For MCNR and MCPZC consult [12] and [14]. For VBC consult [15]. Finally, for CBC consult [16]. In these references, the systematic design approach is developed.*

Once the compensation networks have been presented, it is useful to collect the equations that allow get the design value to perform the implementation. These equations are described in Table X. There are important variables in these equations, which are: g_{m1} and g_{m2} are the transconductance of

the first and the second stage respectively, C_L is the load capacitance, Φ is the phase margin, G_{nm} is the ratio between g_{m1} and g_{m2}, r_{01} is the output first stage resistance, C_A and C_{AC} are the parasitic capacitances of the output first stage. According to the circuits in Fig. 14., it should be noted that g_{m1} is the value of the transconductance of M_1 or M_2 and g_{m2} is the transconductance of M_9. If the QFG technique is used, $g_{m2}=g_{m9}+g_{m10}$, where g_{m9} and g_{m10} are the transconductances of M_9 and M_{10} respectively.

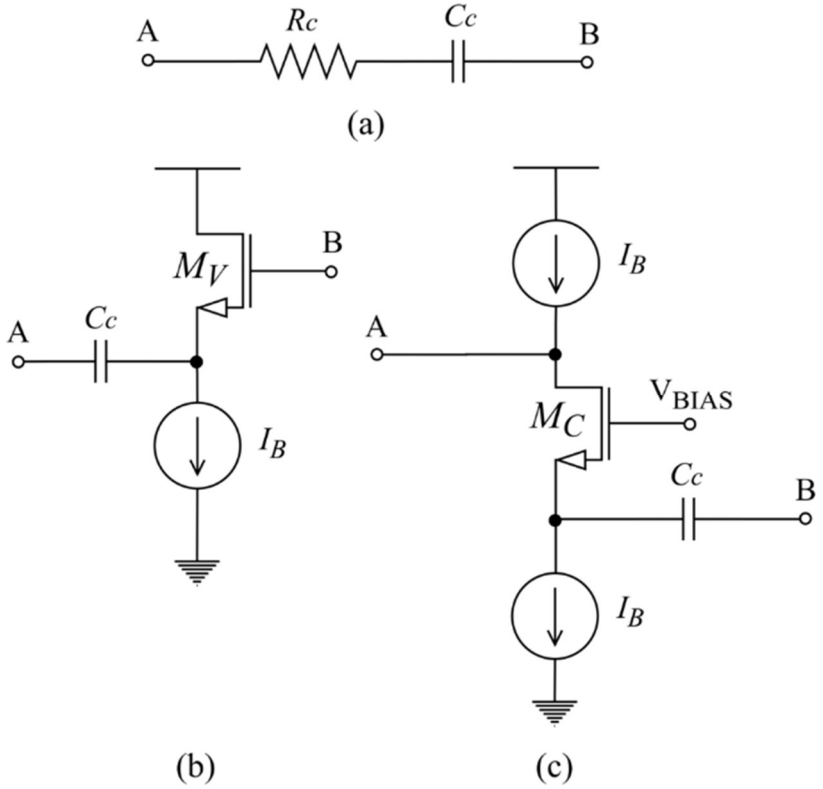


Fig. 22. Implementation of the compensation techniques. (a) MCNR and MCPZC. (b) VBC. (c) CBC.

TABLE X
TRANSCONDUCTANCE APROACH COMPENSATION TECHNIQUES EQUATIONS.

Miller Compensation Nulling Resistor (MCNR)	***Miller Compensation Nulling Resistor Pole-Zero Cancellation (MCPZC)***
$R_c = \frac{1}{g_{m2}}$ $C_c = \frac{g_{m1}}{g_{m2}} C_L \tan\Phi$ (39)	$R_c = \frac{C_L + C_c}{g_{m2} C_c}$ $C_c = \frac{g_{m1}}{g_{m2}} \frac{\tan\Phi}{2} \left(1 + \sqrt{1 + 4 \frac{C_L}{C_A G_{Nm} \tan\Phi}} \right) C_A$ (40) $G_{Nm} = \frac{g_{m1}}{g_{m2}}$

Voltage Buffer (VBC)	*Current Buffer (CBC)*
$C_c = \sqrt{\frac{g_{m1}}{g_{m2}} C_L C_A tan\Phi}$ (41) $g_{mVB} = g_{m2}\frac{C_c}{C_L}$	$C_c = \sqrt{\frac{g_{m1}}{g_{m2}}\frac{\omega_{GBWi}}{\omega_{GBW}} C_L C_{AC}} - \frac{C_L}{2g_{m2}r_{01}}$ (42) $g_{mVB} = tan\Phi\frac{\omega_{GBWi}}{\omega_{GBW}}\, g_{m1}$ $\frac{\omega_{GBW}}{\omega_{GBWi}} = \sqrt{1+\frac{4}{tan\Phi}} - 1$

It should be noted that the due to the sub-threshold mode is used, the g_m value can be expressed in terms of the transistor drain current. Considering that $g_m = I_D/nv_t$, this expression can be substituted in the equations (39), (40), (41) and (42). The results are shown in the Table XI. These equations are very interesting because allow to design the system in terms of the currents stages. This is one advantage of the sub-threshold mode, in which the transconductance is directly proportional to the drain current. For the case of the strong inversion mode, the relation between the transconductance and the drain current is quadratic, so the design equations are more complicated in current terms.

The variables of the Table XI are the same as in Table X. The new variables are I_1, which is the first stage current and which corresponds to the differential-input pair current transistors, I_2, which are the second stage current, n is the slope factor and $v_t = kT/q \sim 26$ mV is the thermal voltage ($T = 300$ °K is the temperature in degrees Kelvin at room temperature, $k = 1.38\text{x}10^{-23}$ JK^{-1} is Boltzmann's constant and $q = 1.602\text{x}10^{-19}$ C is the charge of the electron).

TABLE XI
CURRENT APROACH COMPENSATION TECHNIQUES EQUATIONS.

Miller Compensation Nulling Resistor (MCNR)	*Miller Compensation Nulling Resistor Pole-Zero Cancellation (MCPZC)*
$R_c = \frac{nv_t}{I_2}$ (43) $C_c = \frac{I_1}{I_2} C_L \tan\Phi$	$R_c = \frac{(C_L + C_c)nv_t}{I_2 C_c}$ (44) $C_c = \frac{I_1}{I_2}\frac{\tan\Phi}{2}\left(1 + \sqrt{1 + 4\frac{C_L}{C_A G_{Nm}\tan\Phi}}\right) C_A$ $G_{Nm} = \frac{I_1}{I_2}$

Voltage Buffer (VBC)	*Current Buffer (CBC)*
$C_c = \sqrt{\frac{I_1}{I_2} C_L C_A \tan\Phi}$ (45)	$C_c = \sqrt{\frac{I_1}{I_2}\frac{\omega_{GBWi}}{\omega_{GBW}} C_L C_{AC}} - \frac{C_L n v_t}{2 I_2 r_{01}}$
$g_{mVB} = \frac{I_2}{n v_t}\frac{C_c}{C_L}$	$g_{mVB} = \tan\Phi \frac{\omega_{GBWi}}{\omega_{GBW}}\frac{I_2}{n v_t}$ (46)
	$\frac{\omega_{GBW}}{\omega_{GBWi}} = \sqrt{1 + \frac{4}{tan\Phi}} - 1$

The last two aspects to consider in the Table X and Table XI equations is the output first stage resistance, namely as r_{01}, and the output first stage capacitance, namely as C_A in MCPZC and VBC, and C_{AC} in CBC. The value of this resistance and capacitor can be shown in (36) and (37). In Fig. 23. the first output stage interest parameters are shown, and in Fig. 24. the process for obtaining the output first stage capacitance.

$$r_{01} = \frac{1}{g_{ds8}} \tag{36}$$

$$C_A = C_{AC} = C_{db6} + C_{db8} + C_{gg9}$$
$$C_{gg9} = C_{gs9} + C_{gd9} + C_{gb9} \tag{47}$$

where g_{ds} is the drain-to-source transconductance, C_{db} is the drain-to-body capacitance, C_{gg} is the total gate capacitance, C_{gs} the gate-to-source capacitance, C_{gd} the gain-to-drain capacitance and C_{gb} the gate-to-body capacitance.

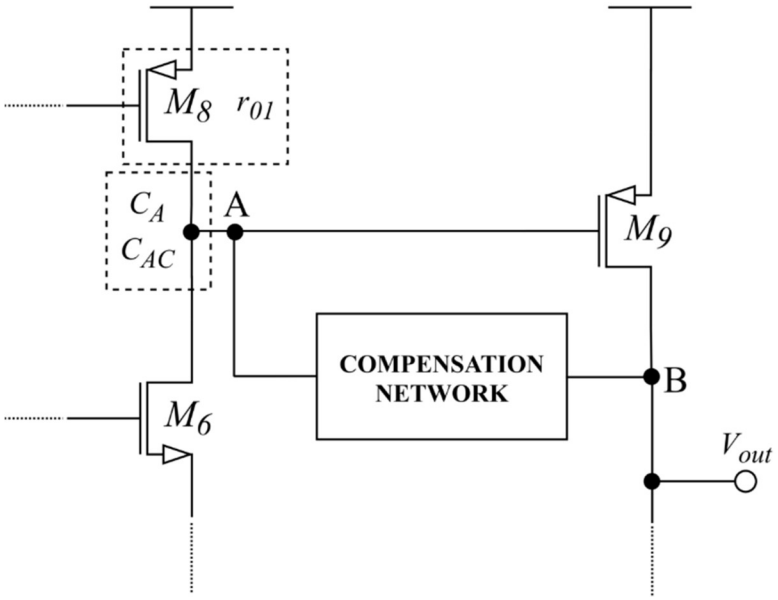


Fig. 23. First output stage resistance and capacitance.

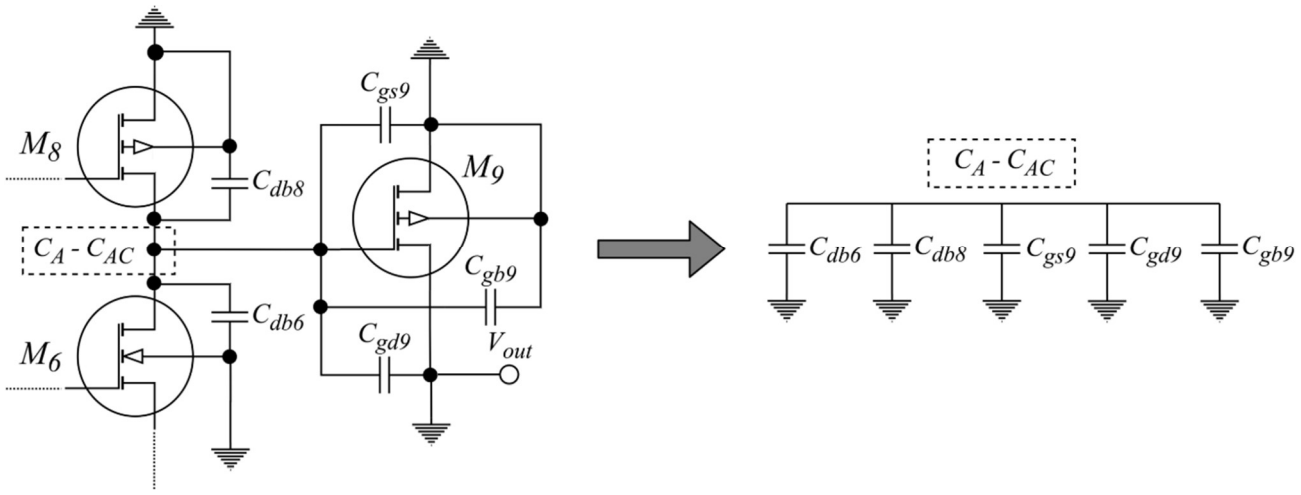


Fig. 24. Small-signal process for obtaining the output first stage capacitance.

4.2.1. Implementation in the OTA Circuit

Once the different compensation techniques have been presented, as well as their design equations, the final step consists in implement them in the circuits.

In Fig. 25. the MCNR and the MCPZC are implemented. As cited, the implementation for both techniques are the same, but the design equations for obtaining C_c and R_c are different. Then, in Fig. 26. the VBC is implemented. It should be appreciated how has been implemented the current source which biases M_V. For doing this, a simple current mirror is used. The advantage of using this current mirror is that the current value can be configured by M_{b7}, M_{b8} and M_{b9} aspect ratios. A simpler option could be the use of a single transistor connected to V_{bias3}. But due to a low current value should be used, the use of a single transistor is insufficiently. Finally, in Fig. 27. the CBC is shown. In this case, for implement the current sources, two simple transistors connected to V_{bias1} and V_{bias3} are used. The transistor M_C is biased using a pair of a minimum W/L transistors operating in the cut-off region. The voltage value of V_{bias4} is equal to $(V_{dd}+V_{ss})/2$.

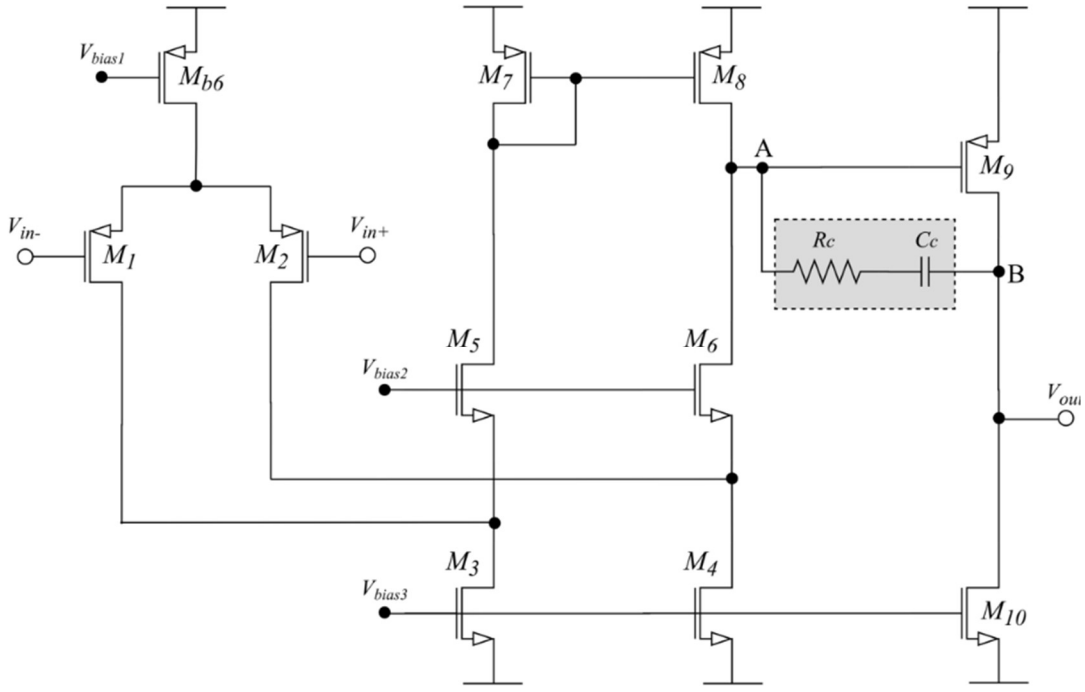


Fig. 25. Implementation of MCNR and MCPZC techniques in the OTA circuit.

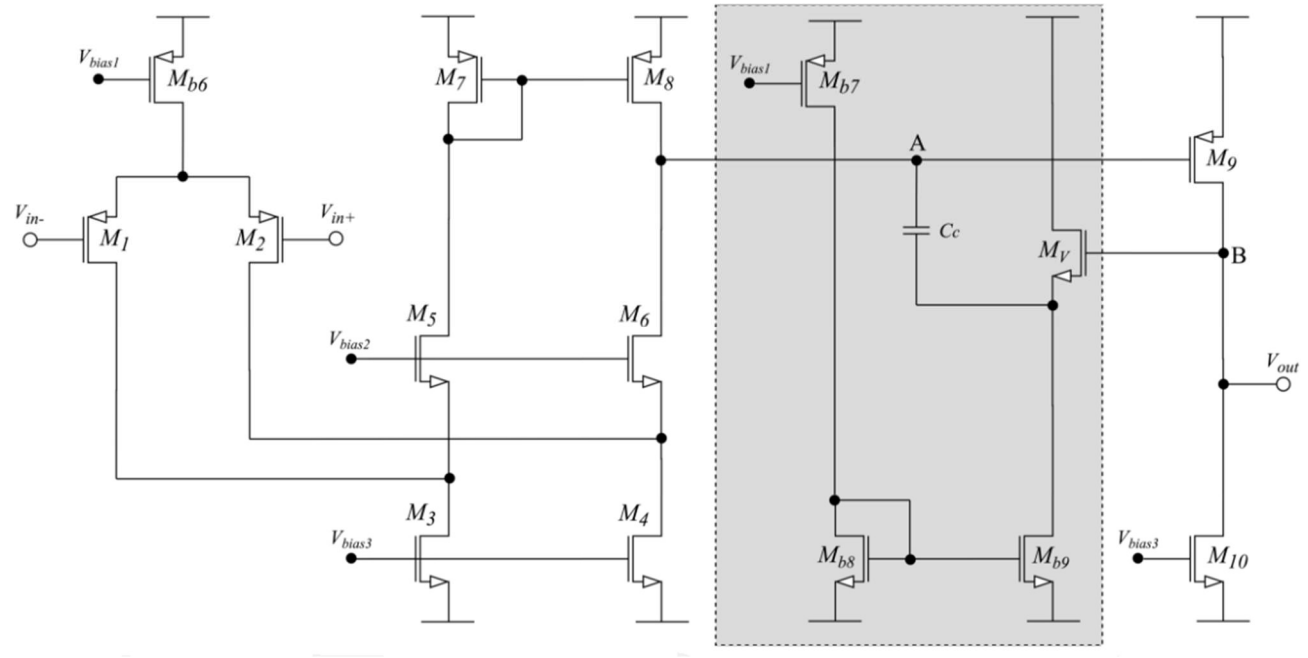


Fig. 26. Implementation of VBC technique in the OTA circuit.

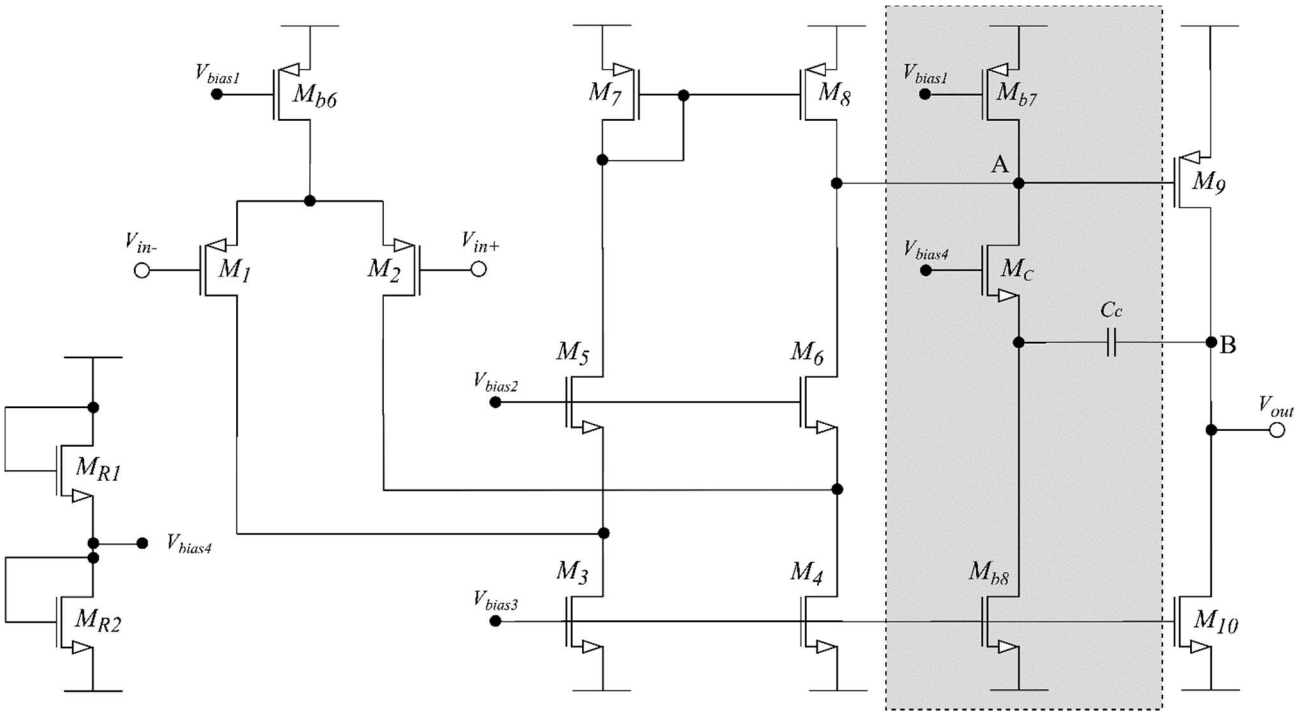


Fig. 27. Implementation of CBC technique in the OTA circuit.

5. CIRCUIT SIMULATION

Once the sub-threshold region, the OTA circuit and the compensation techniques have been presented, the next step consists in designing them and doing some simulations. It should be noted that this is the first phase of the design, which seeks to understand the circuit behavior and to check its performance. For doing this, the *Cadence Software* will be used with a technology of a minimum channel length of 0.5-µm and a threshold voltage of 0.83 V for NMOS and -0.97 V for PMOS. In concrete, the design kit SCN05, provided by AMIS, (an ON Semiconductor® company) will be used.

To begin with the design, different DC currents have been selected. In Fig. 28. the different DC currents of the circuit are shown. The current bias source is set to 150nA. Then, as it can be seen, the current mirrors replicate this current to the different branches. The current replicated in M_{b4} and M_{b5} branches are equal to M_{b1}, that is, 150nA. Then, due to the symmetric differential input stage, the replicated current on M_{b6}, set to 300nA, is divided in the two branches, having in M_1 and M_2 a current of $I_{Mb6}/2$ or which is the same, 150nA. In the case of M_{b2} and M_{b3} branch, the current changes to 350nA to bias M_5 and M_6. These currents have been selected according to the design procedure shown in "Section 1.4.2. Design Procedure".

Continuing with the description, the current drain in M_3 and M_4 is set to the same value of M_{b6} bias. This is because of the desired current in M_5 and M_6 is the same as M_1 and M_2, that is, $I_{Mb6}/2$, as said in (29) in the design procedure subsection. The current in the drain of M_5 is copied by the current mirror M_7 to M_8. Then, the difference between the currents of I_{M5} (that is copied by the current mirror) and I_{M6} is generated. This difference generates a voltage that is amplified by the class-A/class-AB output stage, which is formed by M_9 and M_{10} and which class-mode depends whether the QFG transistor technique is used or not. This output stage is bias with a 1000 nA current, generated by M_{10}.

It should be noted that the DC currents could be different in the two stages, may be the DC current of the first stage bigger or lower than the second. This aspect is important to remark because it will be considered in the design and optimization of the different compensation techniques. Remember that in the sub-threshold mode, the value of these currents is related to the transconductance of each stage. Finally, as can be seen, between the nodes A and B, the compensation technique is applied. The circuit will be simulated with the sub-threshold techniques described in Section 2.

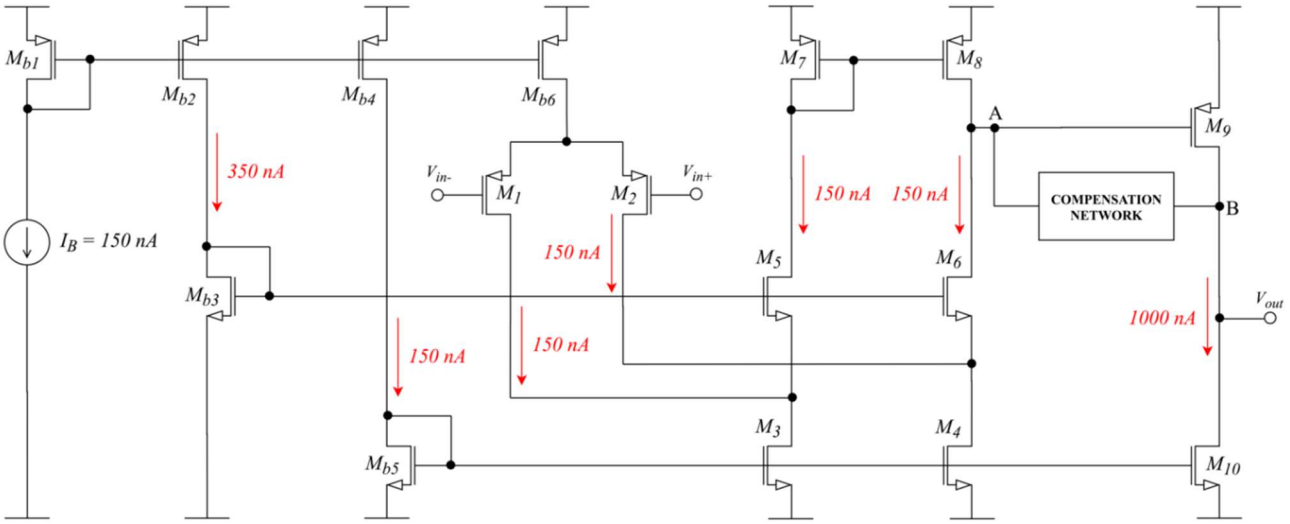


Fig. 28. General schematic for the proposed two-stage OTA with the different DC current stages.

In the successive subsections, different design aspects will be explained, related to the Class-A and Class-AB OTAs. The objective is to compare the performance of both circuits, and demonstrate how the performance of the system is affected using the QFG transistor technique.

5.1. DC Operation Point

Then, the DC operation point analysis is carried out. This analysis seeks to obtain the DC static currents explained before and to know some important parameters like the transconductance values of some transistors or the parasitic capacitances. For doing this analysis, the different currents are fixed through the aspect ratio of the different transistors.

In Table XII, the different DC static currents for doing the first simulations can be checked. In the table, the theoretical values and the simulated values are shown, where can be checked the similarity between them. The theoretical and simulated currents bias for the VBC and CBC techniques are also reported. Additionally, in Table XIII, the aspect ratio of each transistor can be checked to reach this DC current configuration. For the case of some current mirrors, the *L* parameter is incremented to improve the copy, according to (24).

> ***Commentary**: This DC operation point configuration will be taken for the four compensation techniques: MCNR, MCPZ, VBC and CBC and for both Class-A/Class-AB topologies.*

5.2. Design of the Compensation Techniques

Once the DC operation point of the circuits have been obtained, the next step consists in design the different compensation techniques. To perform such activity, the calculations can be made using the current or transconductance mode equations, which can be shown in Table X and Table XI. Remind that g_{m1} and g_{m2} are the transconductance values of the first and second stage, respectively. The same argument can be made for the current values I_1 and I_2 which represent the first and second stage current values.

For doing the calculations, some parameters are required such as the output first stage resistance or the parasitic capacitance. These parameters will be obtained by simulation, using the DC operation point analysis. Note that these parameters can be obtained by hand calculation, but the accuracy of the results are less, and the time employed for doing more. In Table XIV some important parameters related with the DC operation point configuration that have been described are shown, which will be used in the design of the compensation techniques.

TABLE XII
DC STATIC CURRENT BIAS FOR THE DIFFERENT TOPOLOGIES.

TRANSISTOR	***THEORETICAL CURRENT VALUE (nA)***	***SIMULATED CURRENT VALUE (nA)***		
		MCNR MCPZC	***VBC***	***CBC***
M_{b1} - M_{b4} - M_{b5}	150	150 - 153.2 - 153.2		
M_{b6}	300	298.1		
M_{b2} - M_{b3}	350	366		
M_1 - M_2 M_5 - M_6 M_7 - M_8	150	149.1 - 149.1 148.8 - 148.8 148.8 - 148.8	149.1 - 149.1 148.8 - 148.8 148.8 - 148.8	152.1 - 146.0 145.7 - 151.8 145.7 - 145.7
M_3 - M_4	300	297.8 - 297.8		
M_9 - M_{10}	1000	1069		
M_V [4]	45.16	-	45.64	-
M_C [4]	327.37	-	-	301.2

[4] The current that flows through these transistors has been calculated with the g_m parameter in Table XIV.

TABLE XIII
TRANSISTOR ASPECT RATIOS.

TRANSISTOR	***VALUE (W/L) (µm/µm)***		
	MCNR MCPZC	***VBC***	***CBC***
M_{b1} - M_{b4} - M_{b5}	30/1.95		
M_{b2}	70.05/1.95		
M_{b3}	4.95/1.05		
M_{b6}	60/1.05		
M_1 - M_2	139.95/0.60		
M_3 - M_4	60/1.95		
M_5 - M_6	180/1.05		
M_7 - M_8	30/1.95		
M_9	90/1.05		
M_{10}	199.95/1.95		
M_{b7}	-	19.95/1.95	60/1.95
M_{b8}	-	30/1.95	60/1.95
M_{b9}	-	15/1.95	-
M_V	-	19.95/1.05	-
M_C	-	-	19.95/1.05
M_{R1} - M_{R2}	-	-	1.5/1.05

Once the electrical parameters have been got by simulation, the compensation technique values can be calculated. These calculations should be done for both Class-A/Class-AB topologies. For doing this, some considerations will be taken.

- For the case of the *OTA Class-A*, the g_{m1} value will be related with M_1-M_2 transistor. For g_{m2}, will be related with M_9, that is it, $g_{m2} = g_{m9}$. If the current mode approach is used, I_1 is the current bias through M_1-M_2 and I_2 is the current through M_9-M_{10}.
- For the case of the *OTA Class-AB*, the g_{m1} value will be related with M_1-M_2 transistor, as the previous case. But for g_{m2}, will be related with M_9 and M_{10}, that is, $g_{m2} = g_{m9} + g_{m10}$. This is due to the QFG technique is used. If the current mode is used, I_1 is the current bias through M_1-M_2 and I_2 is the double current through M_9-M_{10}, that is it, $I_2 = 2 \cdot I_{M9\text{-}M10}$.

The rest of electrical parameters are the same for both topologies. The theoretical values for the different compensation values and for both Class-A/Class-AB topologies are shown in Table XV.

TABLE XIV
ELECTRICAL DC OPERATION PARAMETERS.

PARAMETER	*VALUE*
C_{load}	40 pF
Phase margin Φ (desired)	60º
$g_{m1,2}$ (First stage transconductance)	3.97 µA/V
g_{m9} (Second stage transconductance)	24.14 µA/V
g_{m10} (Transconductance included in QFG)	24.90 µA/V
$C_A = C_{AC} = C_{jd,8} + C_{jd,6} + C_{gg,9}$ (Parasitic capacitance at the output first stage)	323 fF
$r_{o1} = 1/g_{ds8}$ (Output resistance of the first stage)	146 MΩ
n (Slope factor)	1.5
v_t (Thermal voltage)	26 mV

TABLE XV
THEORETICAL VALUES FOR THE DIFFERENT COMPENSATION TECHNIQUES IN BOTH CLASS-A/CLASS-AB TOPOLOGIES.

COMPENSATION TECHNIQUE	*OTA CLASS-A AMPLIFIER*	*OTA CLASS-AB AMPLIFIER*
	VALUE	*VALUE*
MCNR	C_c = 11.39 pF	C_c = 5.61 pF
	R_c = 41.43 kΩ	R_c = 20.39 kΩ
MCPZC	C_c = 1.97 pF	C_c = 1.37 pF
	R_c = 885 kΩ	R_c = 616 kΩ
VBC	C_c = 1.92 pF	C_c = 1.35 pF
	g_{mVB} = 1.16 µA/V	g_{mVB} = 1.65 µA/V
CBC	C_c = 1.61 pF	C_c = 1.13 pF
	g_{mCB} = 8.39 µA/V	g_{mCB} = 8.39 µA/V

5.3. Gain-Bandwidth Product and Figures of Merit

One of the most important parameters that defines the performance of a system is the *gain-bandwidth product* (GBW), which is the product of the amplifier bandwidth and the gain at which the bandwidth is measured. For the case in which the gain is equal to unity, the GBW value is equal to the system bandwidth. So, the value of the GBW indicates how fast a system is. For calculate this value theoretically, the equation (48) can be used, which was introduced in "1.1.2. Compensating Process of a Two-Stage OTA",

$$GBW\ (Hz) = \frac{g_{m1}}{2\pi C_c} \tag{48}$$

where g_{m1} is the first stage transconductance and C_c is the compensation capacitor. Remark that (48) is defined in the frequency domain, and (32) in *rad/s*.

Another perspective that allows to know the performance of the circuit is the use of a *Figure of Merit* (FOM). To perform a comparison in terms of speed among the many compensation approaches independently of the amplifier topology, design choices and technology, the reference FOM relates the load capacitance, the gain-bandwidth and the total current consumption of the amplifier [14]. This figure of merit will be named as FOMS. In (49) the FOMS is defined as,

$$FOM_S = \frac{GBW}{g_{mT}} C_L \tag{49}$$

where GBW is the gain-bandwidth product, g_{mT} is the sum of each stage transconductances and C_L is the load capacitance.

If (48) is substituted in (49), a FOMS based on the transconductance approach can be got, which relates g_{m1} and g_{mT}, and which is shown in (50). Alternative, and considering that $g_m = I_D/nv_t$ in the sub-threshold mode, a FOMS based on the current approach which relates I_1 and I_T is shown in the same (50) expression. In (51), the FOMS expression which relates the GBW and the I_T can be shown,

$$FOM_S = \frac{1}{2\pi}\frac{g_{m1}}{g_{mT}}\frac{C_L}{C_c} \quad \xRightarrow{g_m = I_D/nv_t} \quad FOM_S = \frac{1}{2\pi}\frac{I_1}{I_T}\frac{C_L}{C_c} \tag{50}$$

$$FOM_S = \frac{GBW}{I_T} C_L \tag{51}$$

where g_{m1} and I_1 are the transconductance and current bias of the first stage, g_{mT} and I_T are the sum of each stage transconductances and currents, C_L is the load capacitance and C_c is the compensation capacitor. Should be noted that (49) and (51) are different FOM, in which (49) quantifies the GBW with respect the g_{mT}, and (50) the GBW with respect I_T. To make them equivalent, in (49), the $g_m = I_D/nv_t$ relationship must be substituted. In (52), is demonstrated this argument.

$$FOM_S = \frac{GBW}{g_{mT}} C_L = \frac{GBW}{I_T/nv_t} C_L \quad \neq \quad FOM_S = \frac{GBW}{I_T} C_L \tag{52}$$

With this FOMS, a better knowledge about the circuit can be achieved.

In a well-designed two-stage amplifier, the Slew-Rate is proportional to the quiescent current of the input stage I_1. The second stage, though subject to a larger capacitive load (given by C_L plus the compensation capacitor C_c) than the input stage, has usually a larger standby current, and hence, it does not limit the SR. As a result, SR is I_1/C_c. Consider now a single-stage amplifier (a differential pair with cascode mirror load) with the same load capacitance and total quiescent current I_T as the two-stage counterpart. After evaluating its Slew-Rate SR_1, and under the approximation that the saturation voltage V_{DS} is equal for all relevant transistors in both amplifiers, the ratio is SR/SR_1 can be checked in (53) [14]

$$\frac{SR}{SR_1} = \frac{I_1}{I_T}\frac{C_L}{C_c} \approx \frac{1}{2\pi}\frac{g_{m1}}{g_{mT}}\frac{C_L}{C_c} = FOM_S \tag{53}$$

This expression relates the load capacitance, the Slew-Rate and the total current consumption, which will be named as FOM_L and which can be seen in (53)

$$FOM_L = \frac{SR}{I_T} C_L \tag{54}$$

Dividing the numerator and denominator of (50) for the second stage transconductance g_{m2} given, the second stage (the output in this case) significantly affects the performance of the whole amplifier in terms of power dissipation, linearity, and bandwidth [14], obtaining the expression (55), which can be expressed also using the current mode approach, as is shown in (56)

$$FOM_S = \frac{1}{2\pi} \frac{g_{m1}/g_{m2}}{(g_{m1}/g_{m2}) + 1 + (g_{mCOMP}/g_{m2})} \frac{C_L}{C_c} \tag{55}$$

$$FOM_S = \frac{1}{2\pi} \frac{I_1/I_2}{(I_1/I_2) + 1 + (I_{COMP}/I_2)} \frac{C_L}{C_c} \tag{56}$$

where g_{m1} and I_1 are the transconductance and current bias of the first stage, g_{m2} and I_2 are the transconductance and current bias of the second stage, g_{mCOMP} and I_{COMP} are the sum of the compensation network transconductances and currents, C_L is the load capacitance and C_c is the compensation capacitor. It should be noted that g_{m1} and I_1 are related with the differential pair, that is to say, the transconductance or currents in M_1 or M_2. For the case of g_{m2} and I_2, these values are related with M_9 for both OTA Class-A and Class-AB.

If the different compensation capacitances C_c functions are substituted in the equation (55) and (56), after doing some algebraic manipulations, the different FOMs for each compensation technique are obtained, which could be checked in Table XVI. These FOM are written in both transconductance and current mode approach. Should be noted that these FOM are developed for both Class-A/Class-AB topologies. The difference procedure for getting is that in the Class-AB case, when the C_c functions is substituted, in its g_{m2} variable, must be considered $2 \cdot g_{m2}$. It is important to consider that the g_{m2} and I_2 variables not are substituted by $2 \cdot g_{m2}$ or $2 \cdot I_2$ in (55) or (56) because it would imply double power consumption. In conclusion, this change of variable is only substituted in the C_c function.

TABLE XVI
FOM EXPRESSIONS.

TRANSCONDUCTANCE APPROACH	*CURRENT APPROACH*
Miller Compensation Nulling Resistor (MCNR)	
$\frac{1}{2\pi} \frac{\alpha}{(g_{m1}/g_{m2} + 1) tan\Phi}$ (57a)	$\frac{1}{2\pi} \frac{\alpha}{(I_1/I_2 + 1) tan\Phi}$ (57b)
Miller Compensation Pole Zero Cancellation (MCPZC)	
$\frac{1}{2\pi} \frac{2\alpha}{\left(\frac{g_{m1}}{g_{m2}} + 1\right) tan\Phi \left(1 + \sqrt{1 + 4\alpha \frac{g_{m2} C_L}{C_A g_{m1} tan\Phi}}\right)} \frac{C_L}{C_A}$ (58a)	$\frac{1}{2\pi} \frac{2\alpha}{\left(\frac{I_1}{I_2} + 1\right) tan\Phi \left(1 + \sqrt{1 + 4\alpha \frac{I_2 C_L}{C_A I_1 tan\Phi}}\right)} \frac{C_L}{C_A}$ (58b)

Voltage Buffer Compensation (VBC)	
$\frac{1}{2\pi}\frac{\sqrt{\frac{g_{m1}}{g_{m2}}\alpha\frac{1}{tan\Phi}\frac{C_L}{C_A}}}{\frac{g_{m1}}{g_{m2}}+1+\sqrt{\frac{g_{m1}}{g_{m2}}\alpha\frac{C_A}{C_L}tan\Phi}}$ (59a)	$\frac{1}{2\pi}\frac{\sqrt{\frac{I_1}{I_2}\alpha\frac{1}{tan\Phi}\frac{C_L}{C_A}}}{\frac{I_1}{I_2}+1+\sqrt{\frac{I_1}{I_2}\alpha\frac{C_A}{C_L}tan\Phi}}$ (59b)
Current Buffer Compensation (CBC) [5]	
$\frac{1}{2\pi}\frac{\sqrt{\frac{g_{m1}}{g_{m2}}\alpha\frac{\omega_{GBW}}{\omega_{GBWi}}\frac{C_L}{C_{AC}}}}{\frac{g_{m1}}{g_{m2}}\left(1+tan\Phi\frac{\omega_{GBWi}}{\omega_{GBW}}\right)+1}$ (60a) $\frac{\omega_{GBW}}{\omega_{GBWi}}=\sqrt{1+\frac{4}{tan\Phi}}-1$	$\frac{1}{2\pi}\frac{\sqrt{\frac{I_1}{I_2}\alpha\frac{\omega_{GBW}}{\omega_{GBWi}}\frac{C_L}{C_{AC}}}}{\frac{I_1}{I_2}\left(1+tan\Phi\frac{\omega_{GBWi}}{\omega_{GBW}}\right)+1}$ (60b) $\frac{\omega_{GBW}}{\omega_{GBWi}}=\sqrt{1+\frac{4}{tan\Phi}}-1$
***NOTE**: Consider $\alpha = 1$ for the OTA Class-A and $\alpha = 2$ for the OTA Class-AB.*	

where g_{m1} and g_{m2} are the transconductance of the first and the second stage respectively, I_1 and I_2 are the current of the first and the second stage respectively, C_L is the load capacitance, Φ is the phase margin, C_A and C_{AC} are the parasitic capacitances of the output first stage and α is a coefficient which implies the use of the QFG or not. It should be noted that g_{m1} is the value of the transconductance of M_1 or M_2 and g_{m2} is the transconductance of M_9.

In Table XVII, the theoretical GBW values for the different compensation techniques and for both Class-A/Class-AB topologies are shown. It should be noted how the QFG technique improves the GBW. Additionally, the FOM_S values is shown in the same table. These values have been calculated using (49) - (50), the equations of Table XVI and (51).

TABLE XVII
THEORETICAL GBW AND FOM VALUES FOR THE DIFFERENT COMPENSATION TECHNIQUES IN BOTH CLASS-A/CLASS-AB TOPOLOGIES.

PARAMETER	***OTA CLASS-A AMPLIFIER***				***OTA CLASS-AB AMPLIFIER***			
	MCNR	***MCPZC***	***VBC***	***CBC***	***MCNR***	***MCPZC***	***VBC***	***CBC***
GBW (kHz)	58.90	326.55	334.11	399.36	117.81	464.91	472.50	564.21
Using (49) - (50) FOM_S (MHz·pF/(mA/V)) [6]	80	443	436	425	160	631	623	600
Using Table XVI. FOM_S (MHz·pF/(mA/V)) [7]	80	443	436	423	160	631	607	598
Using (51) FOM_S (MHz·pF/mA) [8]	2049	11358	11182	10813	4098	16171	15814	15276

[5] This FOM expression has been modified with respect the FOM expression of [14]. Different probes have been made to demonstrate it.
[6] The stage transconductances have been calculated using this equation, $g_{mT} = g_{m1}\text{-}g_{m2} + g_{m9}\text{-}g_{m10} + g_{mCOMP}$, where g_{mi} is the transconductance for the i-th transistor and g_{mCOMP} for the transconductance technique.
[7] The g_{m1}-I_1 is related with M_1-M_2, and g_{m2}-I_2 with M_9-M_{10}.
[8] The stage currents can be calculated using this equation, $I_T = I_{M1}\text{-}I_{M2} + I_{M9}\text{-}I_{M10} + I_C$, where I_{Mi} is the current for i-th transistor and I_C is the current of the compensation technique. The theoretical current values can be read in Table XII.

Another approach can be developed if a change of variable is done. The idea is to obtain a current FOMS approach as a function of I_2 and I_T, and as an alternative of the I_1-I_2 already seen. For doing this, consider that the total current consume in an OTA is shown in (61)

$$I_T = I_1 + I_2 \tag{61}$$

where I_1 and I_2 are the current of the first and the second stage respectively. If I_1 is isolated, the expression (62) is got

$$I_1 = I_T - I_2 \tag{62}$$

where can be checked how I_1 depends on the variables I_2 and I_T. Continuing with the development, dividing (62) by I_2, the expression (63) can be got

$$\frac{I_1}{I_2} = \frac{I_T}{I_2} - 1 \tag{63}$$

Note that if a compensation technique is used, the current consume of this technique I_{COMP} should be included in (63). If the same process is developed, the general expression is got, which can be checked in (64)

$$\frac{I_1}{I_2} = \frac{I_T}{I_2} - 1 - \frac{I_{COMP}}{I_2} \tag{64}$$

Finally, if the expression (64) is substituted in (56), the current FOMS approach as a function of I_2 and I_T is obtained, as can be seen in (65)

$$FOM_S = \frac{1}{2\pi}\frac{(I_T/I_2) - 1 - (I_{COMP}/I_2)}{(I_T/I_2)}\frac{C_L}{C_c} \tag{65}$$

As Table XVI, a new family of FOMS can be developed, but as a perspective of I_2 and I_T. This is an interesting approach, because the total current system consume, I_T, could be a design variable. In Table XVIII, this FOMS are developed. For the case of the VBC, a compact expression cannot be obtained because it is analytically irresoluble and this depends not only of I_2 and I_T, it also depends on I_{COMP}. The expression is shown as a future study case.

5.4. OTA Class-A Amplifier Simulation Results

Then, some simulations for the *OTA class-A amplifier* have been carried out to check the performance of the system. These simulations have been made with the DC current configuration of the Table XII and the compensation technique values of Table XV.

These results can be checked in the Table XIX, in which different parameters as well as the simulated FOM values can be checked. Additionally, the M_{b6}, M_3-M_4 and M_8 linear state are reported. The objective is that these transistors do not enter in that state.

In relation with the systems performance, the MCNR is the slowest compensation strategy with 48.03 kHz, but on the contrary, is the most robust in relation with the transistors linear state and the Phase Margin is practically the 60º desired value. The MCPZC improves notably the performance with

TABLE XVIII
FOM EXPRESSIONS AS A FUNCTION OF I_2 AND I_T.

CURRENT APPROACH	
Miller Compensation Nulling Resistor (MCNR)	
$$\frac{1}{2\pi}\frac{\alpha}{(I_T/I_2)tan\Phi}$$	(66a)
Miller Compensation Pole Zero Cancellation (MCPZC)	
$$\frac{1}{2\pi}\frac{2\alpha}{\left(\frac{I_T}{I_2}\right)tan\Phi\left(1+\sqrt{1+4\alpha\frac{C_L}{C_A\left(\frac{I_T}{I_2}-1\right)tan\Phi}}\right)}\frac{C_L}{C_A}$$	(66b)
Voltage Buffer Compensation (VBC)	
$$\frac{1}{2\pi}\frac{\sqrt{\left(\frac{I_T}{I_2}-1-\frac{I_{COMP}}{I_2}\right)\frac{C_L}{C_A tan\Phi}\alpha}}{I_T/I_2}$$	(66c)
Current Buffer Compensation (CBC)	
$$\frac{1}{2\pi}\frac{\sqrt{\left(\frac{I_T}{I_2}-1-\left(\frac{I_T}{I_2}-1\right)\left(\frac{tan\Phi\frac{\omega_{GBWi}}{\omega_{GBW}}}{tan\Phi\frac{\omega_{GBWi}}{\omega_{GBW}}+1}\right)\right)\alpha\frac{C_L}{C_A}\frac{1}{\frac{\omega_{GBWi}}{\omega_{GBW}}}}}{I_T/I_2}$$ $$\frac{\omega_{GBW}}{\omega_{GBWi}}=\sqrt{1+\frac{4}{tan\Phi}}-1$$	(66d)
NOTE: *Consider α = 1 for the OTA Class-A and α = 2 for the OTA Class-AB.*	

respect to the MCNR strategy, principally in the GBW parameter with a value of 263.04 kHz and the Slew-Rate parameter, which is the highest. It should be noted the *M8* linear state, which decreases the quality of the output response. The Phase Margin is decreased to a value of 46.83º. Should be remarked that both MCNR and MCPZC techniques have the minimum first and second stages current bias, as well as the total amplifier power consumption with values of 1218 nA and 4668 nW respectively. This is due to a passive strategy is used and no additional currents are used. With respect to the VBC, it shows a good GBW performance, which value is 227.59 kHz but having the lowest Slew-Rate values with respect to the previous technique. The *M8* transistor is in the linear state, which degrades the output signal quality. Its Phase Margin is similar to the MCPZC technique, with 44.62º. The current and power consume is a little bit higher respect the MCPZC, increasing them to 1264 nA and 4958 nW. This is due to an active strategy is used. Finally, the CBC has the highest GBW, 268.97 kHz and Slew-Rate values between the MCPZC and VBC techniques. Conversely, the 29.82º of Phase Margin value is very poor. Additionally, this compensation technique has the highest consume as well as the lowest DC gain. Other aspects to consider in relation with this technique is the Common Mode gain

TABLE XIX
INITIAL SIMULATIONS FOR THE OTA CLASS-A.

PARAMETER	***INITIAL SIMULATIONS***			
	MCNR	***MCPZC***	***VBC***	***CBC***
Initial values	C_c = 11.39 pF R_c = 41.43 kΩ	C_c = 1.97 pF R_c = 885 kΩ	C_c = 1.92 pF g_{mVB} = 1.16 µA/V	C_c = 1.61 pF g_{mCB} = 8.39 µA/V
Supply (V)	±1			
Positive Slew Rate (mV/µs)	23.55	304.05	138.38	215.44
Negative Slew Rate (mV/µs)	-20.26	-30.76	-26.28	-25.09
GBW (kHz)	48.03	263.04	227.59	268.97
Phase margin (º)	59.98	46.83	44.62	29.82
Equivalent Input Noise (µV/√Hz)	1.62/√20			
DC gain (dB)	95.34	94.78	94.58	84.81
CM gain (dB)	-1.89	-2.48	-2.68	4.58
CMRR (dB)	97.23	97.26	97.26	80.23
PSRR+ (dB)	93.99	101.83	101.87	44.16
PSRR- (dB)	112.07	112.07	111.72	44.36
First and Second Stage Current Bias I_T (nA) [9]	1218	1218	1264	1519
Total Amplifier Power Consumption P_{POWER} (nW)	4668	4668	4958	5270
FOM_S (MHz·pF/mA) [9]	1577	8638	7204	7081
FOM_L (V·pF/µs·mA) [9]	719	5497	2606	3166
M_{b6} Linear Region	NO	NO	NO	NO
M_3-M_4 Linear Region	NO	NO	NO	NO
M_8 Linear Region	NO	YES	YES	YES

(CM) value. This high value is due to the prescience of an offset, related with the difference between the currents in the M_8 and M_6 transistors. The current sources values which polarize the current buffer are not the same, so the well-mentioned offset is generated and the CM gain is increased. For increasing this CM value, a high precision current sources could be used. In Fig. 29. this aspect is explained in detailed to have a good knowledge about it.

The parameters which relates different aspects of the circuit performance are the FOM values. The highest FOM values has the MCPZC technique, due to it has a great GBW, the highest Slew-Rates and the lowest consume. The FOM values of VBC and CBC techniques are lower respect to the MCPZC technique. It is due to the current and power consume are increased, especially in the CBC technique. In relation with these two techniques, the CBC has a better performance in relation with the two FOM values. In conclusion, with these FOM values, the MCPZC shows the best performance. Then, the CBC and VBC respectively, and finally the MCNR technique. Should be note that this FOM_S values

[9] The total stage is calculated as $I_T = I_{M1}$-$I_{M2} + I_{M9}$-$I_{M10} + I_C$, where I_{Mi} is the current for i-th transistor and I_C is the current of the compensation technique.

are lower with respect the theoretical cases shown in Table XVII. This is due to the theoretical GBW is higher with respect the simulated cases.

Taking up the Table XIX and analyzing the Phase Margin values, can be checked how the MCPZC, VBC and CBC Phase Margin values are lower (46.83º, 44.63º and 29.82º respectively) with respect the MCNR technique, which has 59.98º. So, it is necessary to do a simulation for compensate the Phase Margin values to the 60º desired. This compensation is achieved increasing principally the C_c values, which decreases the GBW and increases the Phase Margin. In the MCPZC and VBC cases, this C_c change implies modify the R_c and g_{mVB} values respectively. For the case of CBC, the g_{mCB} is not modified because it does not depend on C_c.

This Phase Margin compensation activity can be checked in Table XX with the optimized resistor, capacitor and transconductance values. In the case of the MCNR, no optimization has been made because it does not require it. These Phase Margin values are practically the 60º desired. Due to the GBW and the Slew-Rate have been decreased, and the current and power consume values are the same, the FOM have been decreased. The rest of parameters are practically the same. Additionally, the relative error of the compensation techniques values is calculated.

Finally, the aspect ratios for the compensated activity and for the different topologies are shown in Table XXI. Remark that all of them are the same as Table XIII except the current bias VBC aspect ratio.

In Fig. 30, 31, 32, 33 and 34 the measured open-loop AC frequency response and phase margin, the CM gain as well as the measured unity-gain transient response are shown, for the four compensation techniques.

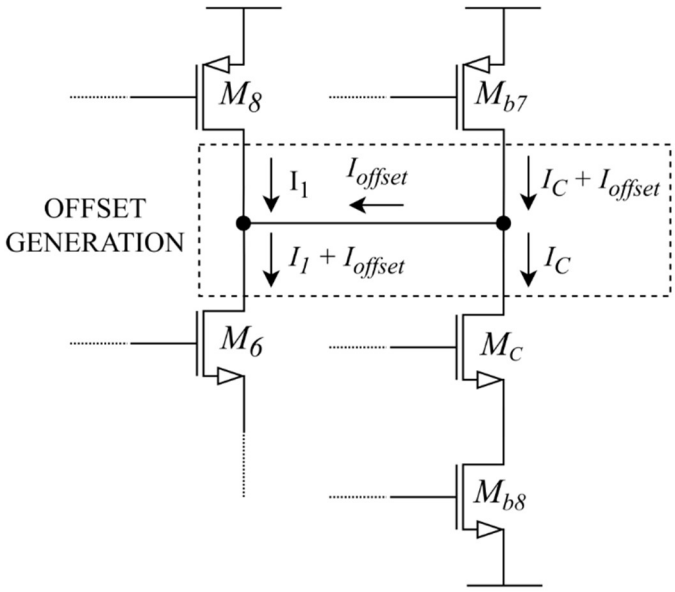


Fig. 29. Offset generation in the output first stage CBC OTA Class-A amplifier.

TABLE XX
INITIAL SIMULATIONS WITH COMPENSATED Φ FOR THE OTA CLASS-A.

PARAMETER	***INITIAL SIMULATIONS WITH COMPENSATED Φ***			
	MCNR	***MCPZC***	***VBC***	***CBC***
Compensated value	C_c = 11.39 pF R_c = 41.43 kΩ	C_c = 2.7 pF R_c = 655 kΩ	C_c = 3.6 pF g_{mVB} = 2.17 µA/V [10]	C_c = 3 pF g_{mCB} = 8.39 µA/V
Relative Error (%) [11]	$\delta C_c = 0$ $\delta R_c = 0$	$\delta C_c = 37$ $\delta R_c = 26$	$\delta C_c = 87.5$ $\delta g_{mVB} = 87$	$\delta C_c = 86$ $\delta g_{mCB} = 0$
Supply (V)	±1			
Positive Slew Rate (mV/µs)	23.55	211.47	82.18	196.01
Negative Slew Rate (mV/µs)	-20.26	-30.38	-26.88	-24.70
GBW (kHz)	48.03	208.35	156.64	214.79
Phase margin (º)	59.98	59.99	59.83	61.51
Equivalent Input Noise (µV/√Hz)	1.62/√20			
DC gain (dB)	95.34	95.05	95.06	85.00
CM gain (dB)	-1.89	-2.21	-2.19	5.18
CMRR (dB)	97.23	97.26	97.25	80.82
PSRR+ (dB)	93.99	101.27	100.48	44.16
PSRR- (dB)	112.07	112.07	110.94	44.36
First and Second Stages Current Bias I_T (nA) [12]	1218	1218	1295	1519
Total Amplifier Power Consumption P_{POWER} (nW)	4668	4668	4958	5270
FOM_S (MHz·pF/mA) [12]	1577	6842	4839	5655
FOM_L (V·pF/µs·mA) [12]	719	2905	1685	2905
M_{b6} Linear Region	NO	NO	NO	NO
M_3-M_4 Linear Region	NO	NO	NO	NO
M_8 Linear Region	NO	NO	YES	YES

[10] The theoretical current M_V value is 84.73 nA and the simulated value is 76.80 nA. This simulated value is used in the calculation of the First and Second Stages Current Bias, I_T.

[11] This relative error is calculated between the initial compensated values and the compensation values. For calculate, (58) can be used,

$$\delta x = \frac{x_0 - x}{x} \quad (58)$$

where x is the initial value and x_0 is the compensate value.

[12] The total stage is calculated as $I_T = I_{M1}$-I_{M2} + I_{M9}-I_{M10} + I_C, where I_{Mi} is the current for i-th transistor and I_C is the current of the compensation technique.

TABLE XXI
VBC CURRENT BIAS ASPECT RATIOS FOR THE OTA CLASS-A COMPENSATED *Φ*.

TRANSISTOR	***VALUE (W/L) (µm/µm)***
	VBC
M_{b7}	10.05/1.95
M_{b8}	30/1.95
M_{b9}	49.95/1.95
The remaining transistors for the MCNR, MCPZC, and CBC are the same as Table XIII.	

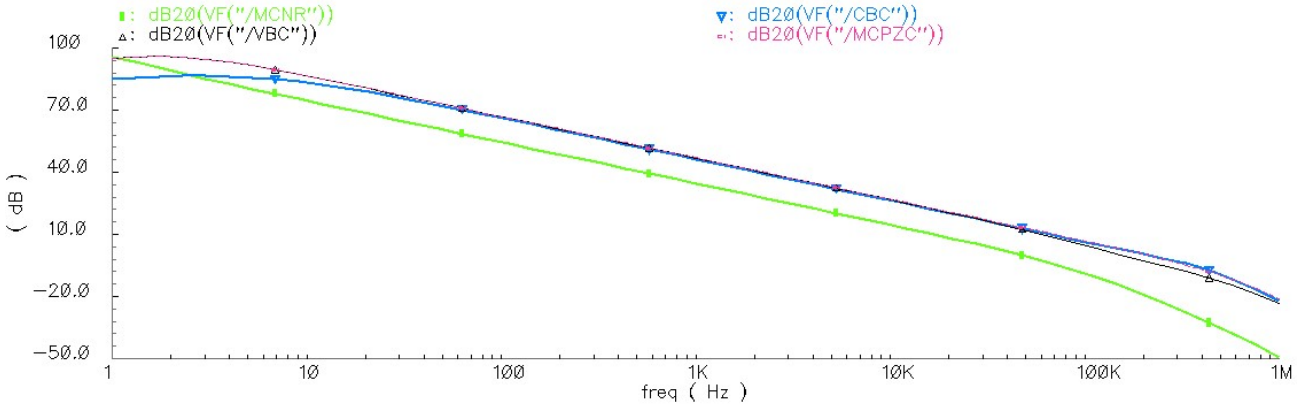


Fig. 30. Class-A measured open-loop AC frequency response for MCNR, MCPZC, VBC and CBC.

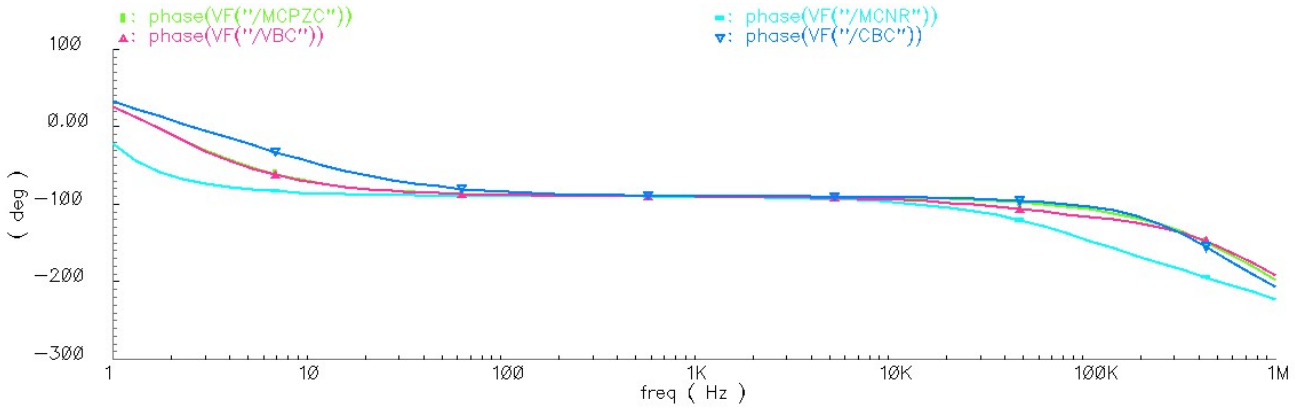


Fig. 31. Class-A measured open-loop AC phase margin response for MCNR, MCPZC, VBC and CBC.

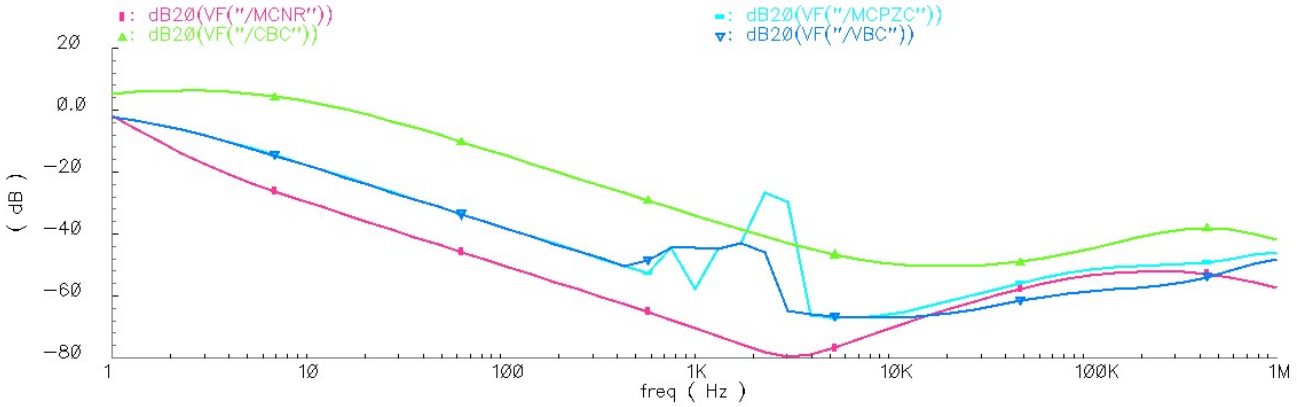


Fig. 32. Class-A measured CM for MCNR, MCPZC, VBC and CBC.

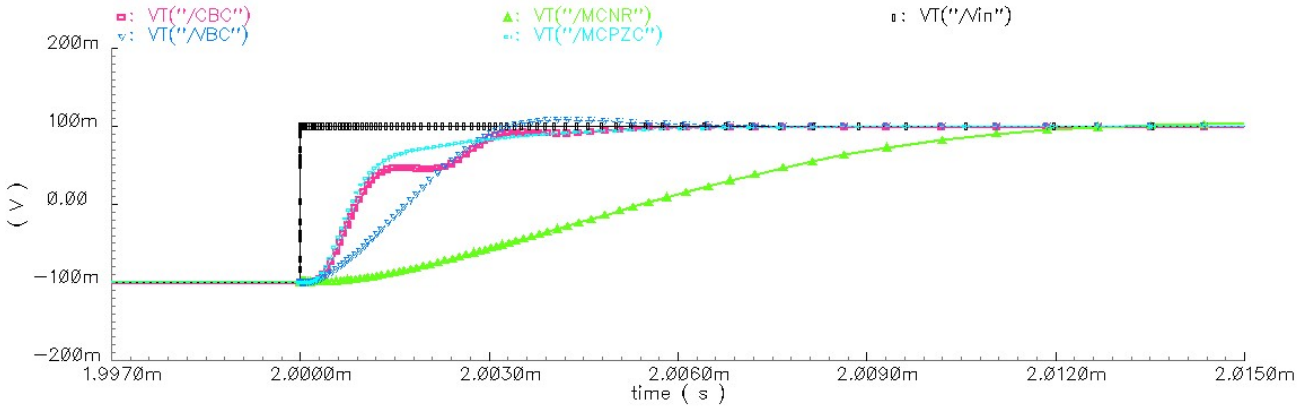


Fig. 33. Class-A measured unity-gain transient response for MCNR, MCPZC, VBC and CBC.

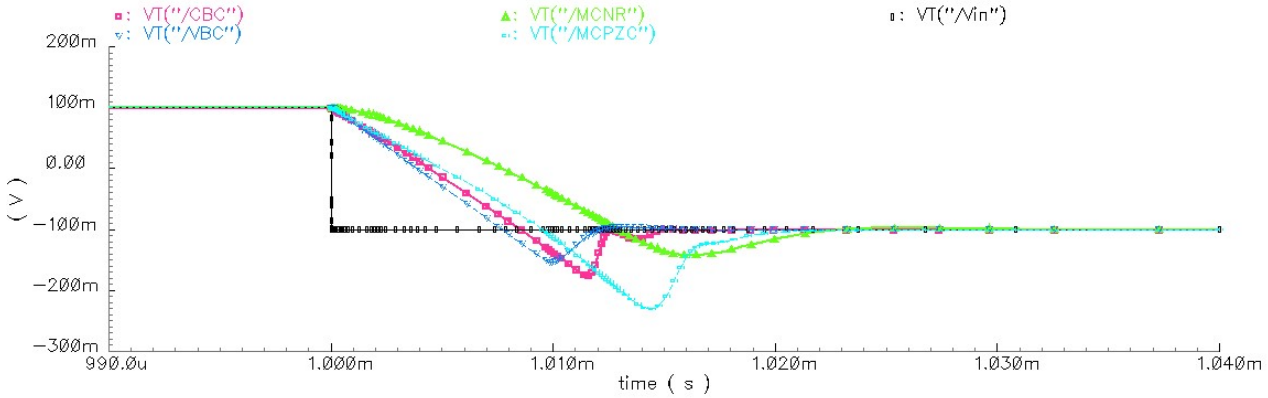


Fig. 34. Class-A measured unity-gain transient response for MCNR, MCPZC, VBC and CBC.

5.5. OTA Class-AB Amplifier Simulation Results

Then, the simulations for the *OTA Class-AB amplifier*, which implements the QFG transistor technique, have been carried out. These simulations have been made with the DC current configuration of Table XII and the compensation technique values of Table XV. Due to the new calculations, the compensation values are different with respect the OTA class-A amplifier. For the VBC technique, the current bias has changed, so the aspect ratio of the current mirror transistors must be readjusted. In Table XXII, these aspect ratios can be checked. Again, to mention that the aspect ratios for the compensate techniques and for the different topologies are the same as Table XIII except the current bias VBC aspect ratios already mention.

TABLE XXII
VBC CURRENT BIAS ASPECT RATIOS FOR THE INITIAL OTA CLASS-AB SIMULATIONS.

TRANSISTOR	***VALUE (W/L) (µm/µm)***
	VBC
M_{b7}	10.05/1.95
M_{b8}	30/1.95
M_{b9}	40.05/1.95
The remaining transistors for the MCNR, MCPZC, and CBC are the same as Table XIII.	

Analyzing the results of Table XXIII, can be appreciated how has influenced the QFG technique, balancing the values of the Positive and Negative Slew-Rates. The positive Slew-Rate has been decreased, but the Negative Slew-Rate has been increased. This is due to the QFG performance, which detailed analysis can be read in "Subsection 1.4.2. Design Procedure". Other important aspect of the QFG is the non-linear M_8 region, which improves the quality of the output signal. Comparing the four different compensation techniques, can be appreciated that the highest GBW is 229.62 kHz, which corresponds with the MCPZC technique. The other GBW values are 225.82 kHz for the VBC and 201.90 kHz for the CBC. The MCNR is the slowest OTA, with 75.94 kHz. If these GBW are compared with the OTA Class-A amplifier (without compensate its Phase Margin), the MCNR has been improved. The MCPZC and CBC have decreased their GBW values, and the VBC has practically the same GBW value. The Phase Margins are varied, with 54.87º for the MCNR, 47.43º for the MCPZC, 40.47º for the VBC and 54.52º for CBC, which value has been improved notably with respect the OTA Class-A initial simulations. Again, the CM value for the CBC is low due the well-mentioned current offset generation. Finally, comment that the current and power consume are practically the same as the OTA Class-A amplifier. In relation with the FOM performance, the MCPZC has the highest value FOM_L value, but now, the VBC has the highest FOM_S value. This is due to his Slew-Rate has been increased notably.

With the objective of equalizing the Phase Margin, the already made compensation activity has been made. This activity can be checked in Table XXIV with the optimized resistor, capacitor and transconductance values for the four compensation techniques. Due to the GBW and the Slew-Rate have been decreased, and the current and power consume values are the same, the FOM have been decreased. The rest of parameters are practically the same. Additionally, the relative error of the compensation techniques values is calculated. Finally, the aspect ratios for the compensated activity and for the different topologies are shown in Table XXV. Remark that all of them are the same as Table XIII except the current bias VBC aspect ratio.

In Fig. 35, 36, 37, 38 and 39 the measured open-loop AC frequency response and phase margin, the CM gain as well as the measured unity-gain transient response are shown, for the four compensation techniques.

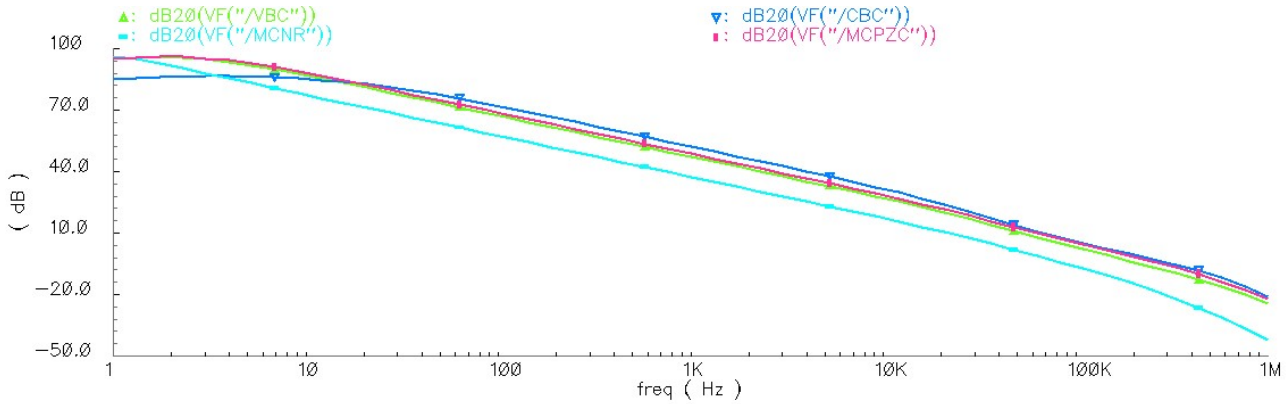


Fig. 35. Class-AB measured open-loop AC frequency response for MCNR, MCPZC, VBC and CBC.

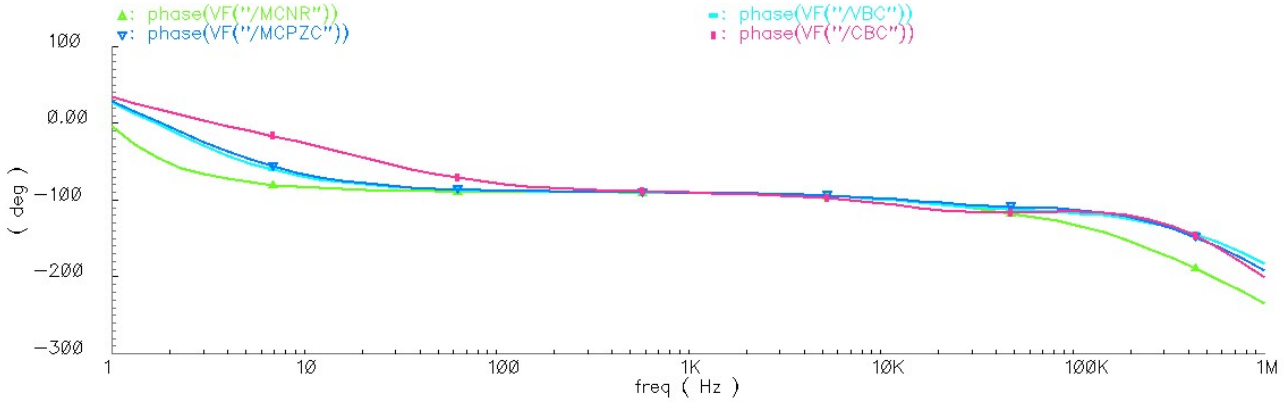


Fig. 36. Class-AB measured open-loop AC phase margin response for MCNR, MCPZC, VBC and CBC.

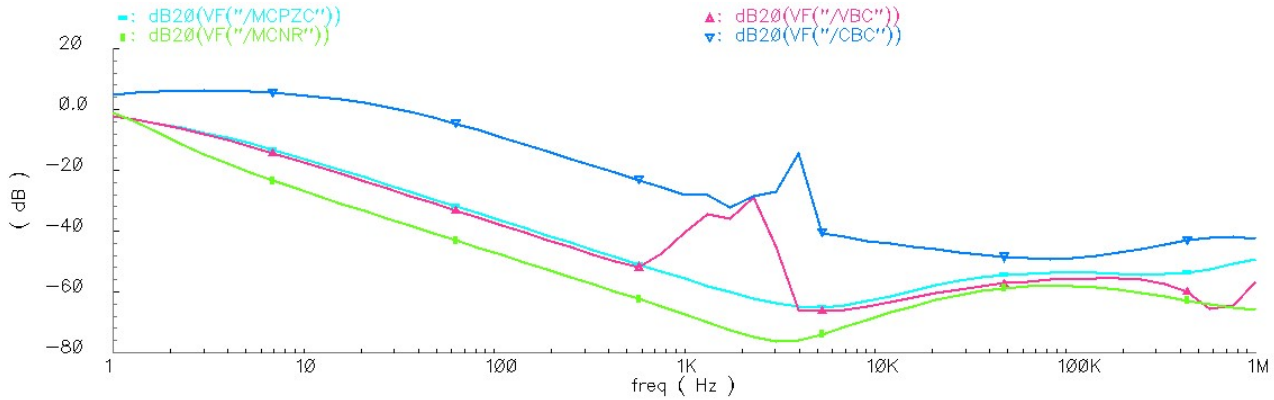


Fig. 37. Class-AB measured CM for MCNR, MCPZC, VBC and CBC.

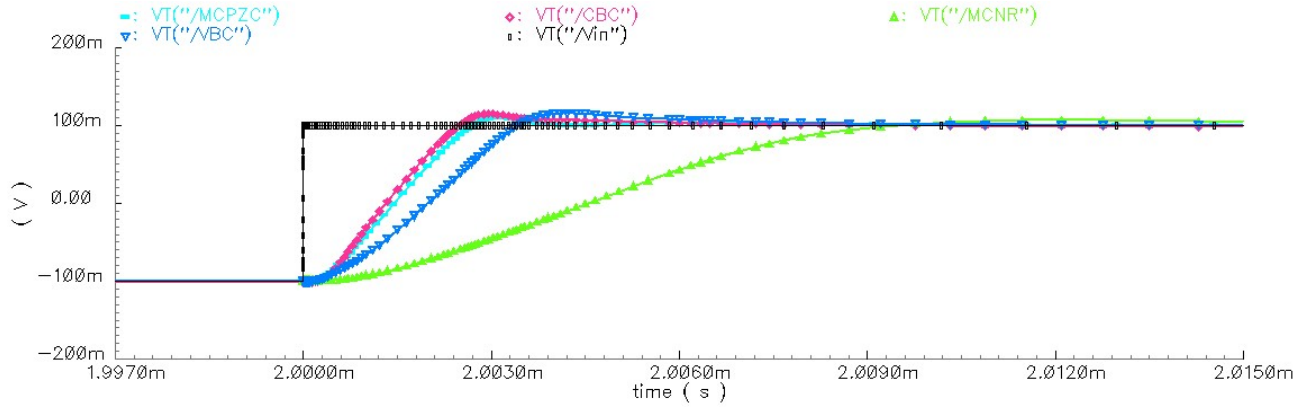


Fig. 38. Class-AB measured unity-gain transient response for MCNR, MCPZC, VBC and CBC.

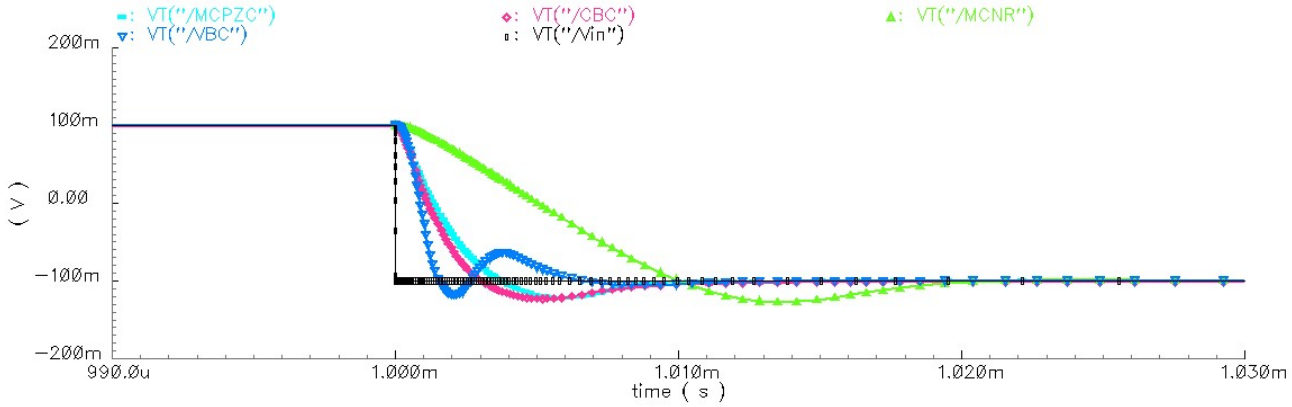


Fig. 39. Class-AB measured unity-gain transient response for MCNR, MCPZC, VBC and CBC.

TABLE XXIII
INITIAL SIMULATIONS FOR THE OTA CLASS-AB.

PARAMETER	***INITIAL SIMULATIONS***			
	MCNR	***MCPZC***	***VBC***	***CBC***
Initial Values	C_{QFG} = 1 pF R_{QFG} = 1 MΩ C_c = 5.61 pF R_c = 20.39 kΩ	C_{QFG} = 1 pF R_{QFG} = 1 MΩ C_c = 1.37 pF R_c = 616 kΩ	C_{QFG} = 1 pF R_{QFG} = 1 MΩ C_c = 1.35 pF g_{mVB} = 1.65 µA/V [13]	C_{QFG} = 1 pF R_{QFG} = 1 MΩ C_c = 1.13 pF g_{mCB} = 8.39 µA/V
Supply (V)	±1			
Positive Slew Rate (mV/µs)	41.66	135.98	140.27	120.04
Negative Slew Rate (mV/µs)	-31.05	-155.90	-342.10	-126.60
GBW (kHz)	75.94	229.62	225.82	201.90
Phase margin (º)	54.87	47.43	40.47	54.42
Equivalent Input Noise (µV/√Hz)	1.62/√20			
DC gain (dB)	95.83	94.55	94.41	84.74
CM gain (dB)	-1.42	-2.71	-2.85	4.92
CMRR (dB)	97.25	97.26	97.26	79.82
PSRR+ (dB)	97.67	104.26	101.56	44.16
PSRR- (dB)	110.64	113.31	109.74	44.36
First and Second Stages Current Bias I_T (nA) [14]	1218	1218	1280	1519
Total Amplifier Power Consumption P_{POWER} (nW)	4668	4668	4882	5270
FOM_S (MHz·pF/mA) [14]	2494	7540	7060	5316
FOM_L (V·pF/µs·mA) [14]	1194	4792	7540	3250
M_{b6} Linear Region	NO	NO	NO	NO
M_3-M_4 Linear Region	NO	NO	NO	NO
M_8 Linear Region	NO	NO	NO	NO

[13] The theoretical current M_V value is 64.37 nA and the simulated value is 61.38 nA. This simulated value is used in the calculation of the First and Second Stages Current Bias, I_T.
[14] The total stage is calculated as $I_T = I_{M1}$-I_{M2} + I_{M9}-I_{M10} + I_C, where I_{Mi} is the current for *i*-th transistor and I_C is the current of the compensation technique. In this case, the folded-cascode currents are included.

TABLE XXIV
INITIAL SIMULATIONS WITH COMPENSATED Φ FOR THE OTA CLASS-AB.

PARAMETER	***INITIAL SIMULATIONS WITH COMPENSATED Φ***			
	MCNR	***MCPZC***	***VBC***	***CBC***
Values	C_{QFG} = 1 pF R_{QFG} = 1 MΩ C_c = 8.2 pF R_c = 20.39 kΩ	C_{QFG} = 1 pF R_{QFG} = 1 MΩ C_c = 2.2 pF R_c = 391 kΩ	C_{QFG} = 1 pF R_{QFG} = 1 MΩ C_c = 3.4 pF g_{mVB} = 3.67 µA/V [15]	C_{QFG} = 1 pF R_{QFG} = 1 MΩ C_c = 1.5 pF g_{mCB} = 8.39 µA/V
Relative error (%)	$\delta C_{QFG} = 0$ $\delta R_{QFG} = 0$ $\delta C_c = 46$ $\delta R_c = 0$	$\delta C_{QFG} = 0$ $\delta R_{QFG} = 0$ $\delta C_c = 60.5$ $\delta R_c = 36.5$	$\delta C_{QFG} = 0$ $\delta R_{QFG} = 0$ $\delta C_c = 152$ $\delta g_{mVB} = 122$	$\delta C_{QFG} = 0$ $\delta R_{QFG} = 0$ $\delta C_c = 50$ $\delta g_{mCB} = 0$
Supply (V)	±1			
Positive Slew Rate (mV/µs)	30.01	92.52	75.05	110.64
Negative Slew Rate (mV/µs)	-23.09	-100.40	-200.95	-113.96
GBW (kHz)	56.62	174.93	135.99	187.43
Phase margin (º)	60.09	61.07	60.85	60.32
Equivalent Input Noise (µV/√Hz)	1.62/√20			
DC gain (dB)	95.96	94.87	95.01	84.79
CM gain (dB)	-1.28	-2.39	-2.25	4.97
CMRR (dB)	97.24	97.26	97.26	79.82
PSRR+ (dB)	95.54	100.84	99.74	44.16
PSRR- (dB)	110.67	110.60	108.39	44.36
First and Second Stages Current Bias I_T [16]	1218	1218	1367	1519
Total Amplifier Power Consumption P_{POWER} (nW)	4668	4668	5270	5270
FOM_S (MHz·pF/mA) [16]	1859	5744	3980	4935
FOM_L (V·pF/µs·mA) [16]	872	3168	4039	2957
M_{b6} Linear Region	NO	NO	NO	NO
M_3-M_4 Linear Region	NO	NO	NO	NO
M_8 Linear Region	NO	NO	NO	NO

[15] The theoretical current M_V value is 143.44 nA and the simulated value is 148.60 nA. This simulated value is used in the calculation of the First and Second Stages Current Bias, I_T.
[16] The total stage is calculated as $I_T = I_{M1}$-I_{M2} + I_{M9}-I_{M10} + I_C, where I_{Mi} is the current for *i*-th transistor and I_C is the current of the compensation technique.

TABLE XXV
VBC CURRENT BIAS ASPECT RATIOS FOR THE OTA CLASS-AB COMPENSATED Φ.

TRANSISTOR	*VALUE (W/L) (µm/µm)*
	VBC
M_{b7}	30/1.95
M_{b8}	30/1.95
M_{b9}	30/1.95
The remaining transistors for the MCNR, MCPZC, and CBC are the same as Table XIII.	

6. CIRCUIT OPTIMIZATION

In Section 5, the first simulations of the circuit have been made, which objective was to understand the performance of the circuit and to check the four different compensation strategies. Additionally, the concept of the FOM was introduced. It could be verified that the results were satisfactory and the system worked correctly. The next design phase consists in optimizing this performance using the figures of merit. Through these FOM, an optimization activity will be carried out with the aim of get the optimal DC static current relationship between the two stages.

To quantitatively compare the efficiency of the two-stage OTA compensation networks, the current approach relationships in Table XVI versus current ratio I_1/I_2 will be plotted. In this comparison, Φ value is 60º, C_L value is 40 pF and C_A and C_{AC} will be considered as constants with a value of 323 fF (the same value of the Table XIV). The objective consists in seek an optimal I_1/I_2 relationship which maximizes the performance of the system, in terms of the well-mention FOM. Should be noted that two current relationships will be sought. One corresponds to the OTA Class-A amplifier, and the another to the OTA Class-AB amplifier.

In Fig. 40 and Fig.40, these two comparisons can be checked, where I_1/I_2 ranges from 0.001 to 10. Analyzing the different graphics, can be checked that they have some maximum values of I_1/I_2 which maximizes the FOM. These are the optimal current relationships which maximizes the performance of the circuit in terms of gain-bandwidth product and current consumption, for a given load capacitance C_L. It should be noted that in both Fig. 40. and Fig. 41., the MCPZC, VBC and CBC techniques have a maximum value but the MCNR maximum value tends to 0. The MCNR case implies that the greater the current of the second stage with respect to the first is, the greater the gain-bandwidth product and the current consumption is. Is the same case as in a classic OTA, in which the more output current has, the more gain-bandwidth product has.

In the Table XXVI, the optimal values of I_1/I_2 as well as the mathematical expression that relate them can be checked. The interesting thing is that the optimal current relationships are the same for both topologies. This is due to the α coefficient introduced in the FOM, which only increases the FOM value but maintaining the current relationship. For the case of MCPZC, there are two current values depending on a Class-A or a Class-AB, but they are practically similar.

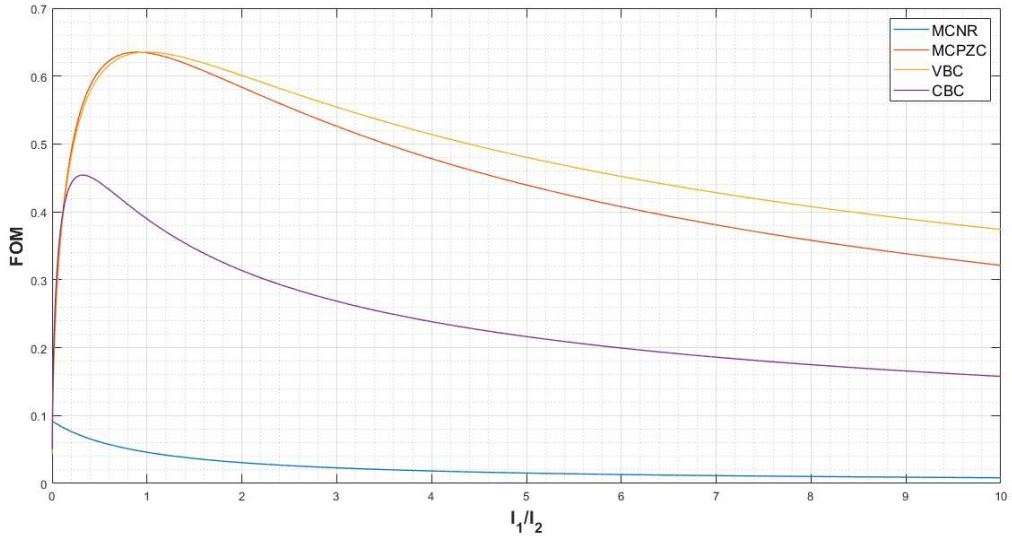


Fig. 40. I_1/I_2 current FOM relationship in OTA Class-A amplifier.

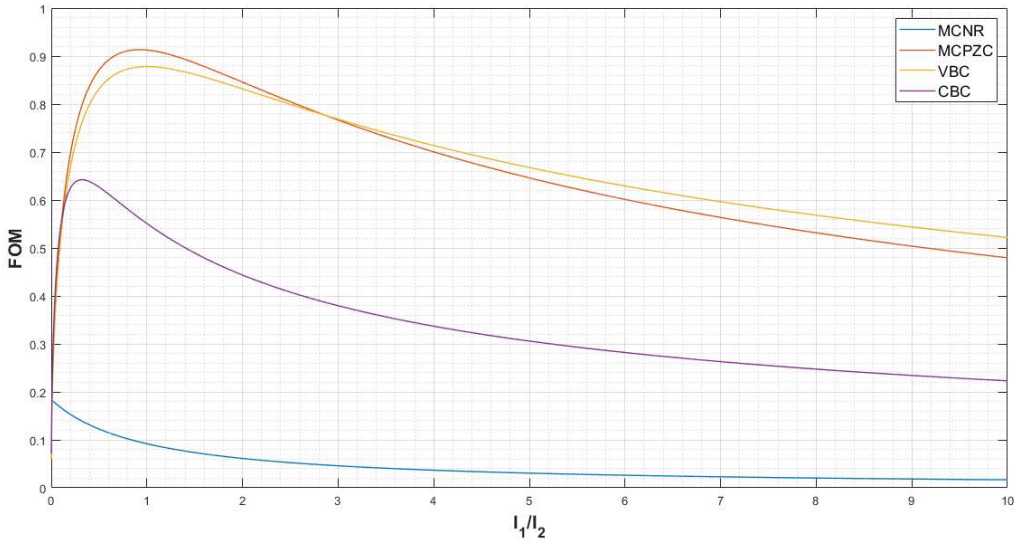


Fig. 41. I_1/I_2 current FOM relationship in OTA Class-AB amplifier.

TABLE XXVI
OTA CLASS-A/CLASS-AB CURRENT RELATIONSHIPS.

COMPENSATION TECHNIQUE	*I_1/I_2 OPTIMAL RELATION*	*MATHEMATICAL EXPRESSION*
MCNR (Class-A/Class-AB)	$0.001 \rightarrow 0$	$I_2 = 1000 \cdot I_1 \underset{I_1/I_2 \rightarrow 0}{\Longrightarrow} I_2 = \infty \cdot I_1$
MCPZC (Class-A) MCPZC (Class-AB)	0.8940 0.9230	$I_2 = 1.1186 \cdot I_1$ $I_2 = 1.0834 \cdot I_1$
VBC (Class-A/Class-AB)	1	$I_2 = I_1$
CBC (Class-A/Class-AB)	0.3210	$I_2 = 3.1153 \cdot I_1$

6.1. DC Optimum Point

Once the optimal I_1/I_2 current relationship has been searched, then, the DC operation point analysis is carried out. This analysis seeks to obtain the DC static currents explained before and to know some

important parameters like the transconductance values of some transistors or the parasitic capacitances. For doing this analysis, the different currents are fixed through the aspect ratio of the different transistors.

In Table XXVII, the different optimal DC static currents for both Class-A/Class-AB amplifiers can be checked which are based in Table XXVI relationships. For the case of MCNR, a I_1/I_2 relationship equal to 0.1 has been elected, or that is the same, $I_2 = 10 \cdot I_1$. In the table, the theoretical values and the simulated values are shown, where can be checked the similarity between them. For the MCPZC, the two theoretical current relationships are shown, but due to their similarity, only one simulated configuration has been elected. The theoretical and simulated currents bias for the VBC and CBC techniques are also reported. Additionally, in Table XXVIII, the aspect ratio of each transistor can be checked to reach this DC current configuration. For the case of some current mirrors, the *L* parameter is incremented to improve the copy, according to (24).

TABLE XXVII
OPTIMAL DC STATIC CURRENT BIAS FOR THE CLASS-A/CLASS-AB TOPOLOGIES.

TRANSISTOR	*CURRENT VALUE (nA) THEORETICAL*		*CURRENT VALUE (nA) SIMULATED*			
			MCNR	*MCPZC*	*VBC*	*CBC*
M_{b1} - M_{b4} - M_{b5}	150		150 - 153.2 - 153.2			
M_{b6}	300		298.1			
M_{b2} - M_{b3}	350		366			
M_1 - M_2 M_5 - M_6 M_7 - M_8	150		149.1 - 149.1 148.8 - 148.8 148.8 - 148.8	149.1 - 149.1 148.8 - 148.8 148.8 - 148.8	149.1 - 149.1 148.8 - 148.8 148.8 - 148.8	152.1 - 146.0 145.7 - 151.8 145.7 - 145.7
M_3 - M_4	300		297.8 - 297.8	297.8 - 297.8	297.8 - 297.8	297.8 - 297.8
M_9 - M_{10}	MCNR MCPZC VBC CBC	1500 (A/AB) 167.79 (A) - 162.51 (AB) 150 (A/AB) 467.30 (A/AB)	1497	157.1	157.1	480.1
M_V [17]	14.53		-	-	13.09	-
M_C [17]	327.37		-	-	-	301.2

6.2. Design of the Compensation Techniques

Once the different optimal I_1/I_2 values for each compensation technique have been obtained, the next phase consists in implement and simulate these relations in both Class-A/Class-AB amplifiers. For doing it, the current relation must be configured with the different aspect ratios of the transistors. To perform such activity, the calculations can be made using the current or transconductance mode equations, which can be shown in Table X and Table XI.

For doing the calculations, some parameters are required such as the output first stage resistance or the parasitic capacitance. These parameters will be obtained by simulation, using the DC operation point analysis. In Table XXIX some important parameters related with the DC operation point configuration that have been described are shown, which will be used in the design of the compensation techniques.

[17] The current that flows through these transistors has been calculated with the g_m parameter in Table XXIX.

TABLE XXVIII
TRANSISTOR ASPECT RATIOS.

TRANSISTOR	***VALUE (W/L) (µm/µm)***			
	MCNR (Class-A/AB)	***MCPZC (Class-A/AB)***	***VBC (Class-A/AB)***	***CBC (Class-A/AB)***
M_{b1} - M_{b4} - M_{b5}	30/1.95			
M_{b2}	70.05/1.95			
M_{b3}	4.95/1.05			
M_{b6}	60/1.05			
M_1 - M_2	139.95/0.60			
M_3 - M_4	60/1.95			
M_5 - M_6	180/1.05			
M_7 - M_8	30/1.95			
M_9	130.05/1.05	15/1.05	15/1.05	45/1.05
M_{10}	280.05/1.95	30/1.95	30/1.95	90/1.95
M_{b7}	-	-	10.05/1.95	60/1.95
M_{b8}	-	-	30/1.95	60/1.95
M_{b9}	-	-	10.05/1.95	-
M_V	-	-	19.95/1.05	-
M_C	-	-	-	19.95/1.05
M_{R1} - M_{R2}	-	-	-	1.5/1.05

TABLE XXIX
ELECTRICAL OPTIMAL DC OPERATION PARAMETERS.

PARAMETER	***MCNR (Class-A/AB)***	***MCPZC (Class-A/AB)***	***VBC (Class-A/AB)***	***CBC (Class-A/AB)***
C_{load}	40 pF			
Phase margin Φ (desired)	60º			
$g_{m1,2}$	3.97 µA/V			
g_{m9}	33.88 µA/V	3.57 µA/V	3.57 µA/V	10.91 µA/V
g_{m10}	34.89 µA/V	3.66 µA/V	3.66 µA/V	11.18 µA/V
$C_A = C_{AC} = C_{jd,8} + C_{jd,6} + C_{gg,9}$ (Parasitic capacitance at the output first stage)	374 fF	226 fF	226 fF	264 fF
$r_{o1} = r_{oM8} = 1/g_{ds8}$ (Output resistance of the first stage)	146 MΩ	146 MΩ	146 MΩ	149 MΩ

Once the electrical parameters have been got by simulation, the compensation technique values can be calculated. These calculations should be done for both Class-A/Class-AB topologies. For doing this, some considerations will be taken, which are the same as "Section 4.2. Design of the Compensation Techniques".

- For the case of the *OTA Class-A*, the g_{m1} value will be related with M_1-M_2 transistor. For g_{m2}, will be related with M_9, that is it, $g_{m2} = g_{m9}$. If the current mode approach is used, I_1 is the current bias through M_1-M_2 and I_2 is the current through M_9-M_{10}.
- For the case of the *OTA Class-AB*, the g_{m1} value will be related with M_1-M_2 transistor, as the previous case. But for g_{m2}, will be related with M_9 and M_{10}, that is, $g_{m2} = g_{m9} + g_{m10}$. This is due to

the QFG technique is used. If the current mode is used, I_1 is the current bias through M_1-M_2 and I_2 is the double current through M_9-M_{10}, that is it, $I_2 = 2 \cdot I_{M9\text{-}M10}$.

The rest of electrical parameters are the same for both topologies. The theoretical values for the different compensation values and for both Class-A/Class-AB topologies are shown in Table XXX.

TABLE XXX
THEORETICAL VALUES FOR THE DIFFERENT OPTIMUM COMPENSATION TECHNIQUES IN BOTH CLASS-A/CLASS-AB TOPOLOGIES.

COMPENSATION TECHNIQUE	*OTA CLASS-A AMPLIFIER*	*OTA CLASS-AB AMPLIFIER*
	VALUE	*VALUE*
MCNR	C_c = 8.11 pF	C_c = 4 pF
	R_c = 29.52 kΩ	R_c = 14.54 kΩ
MCPZC	C_c = 4.40 pF	C_c = 3.04 pF
	R_c = 2.82 MΩ	R_c = 1.96 MΩ
VBC	C_c = 4.17 pF	C_c = 2.93 pF
	g_{mVB} = 0.37 µA/V	g_{mVB} = 0.53 µA/V
CBC	C_c = 2.16 pF	C_c = 1.52 pF
	g_{mCB} = 8.39 µA/V	g_{mCB} = 8.39 µA/V

6.3. Gain-Bandwidth Product and Figure of Merit

Considering the same procedure followed in "Section 4.3. Gain-Bandwidth and Figure of Merit", the equations obtained in this section will be used. In Table XXXI, the theoretical GBW values for the different optimal compensation techniques and for both Class-A/Class-AB topologies are shown. Additionally, the FOMS values is shown in the same table. These values have been calculated using (49) - (50), the equations of Table XVI and (51).

Should be noted the relation between the results and Fig. 30. - Fig. 31. According to the figures, for both OTA Class-A/Class-AB amplifiers, the MCPZ and VBC have the best performance because they have the highest FOM values. In addition, can be appreciated their similarity in relation to the GBW and the well-mention FOM values. For the CBC case, it has a lower performance in comparison with the other techniques, which is reflected in its lower values. For the OTA Class-AB, the results are higher because the GBW is higher and the current bias stages are the same as the OTA Class-A.

6.4. OTA Class-A Optimized Amplifier Simulation Results

Then, some simulations for the *OTA Class-A amplifier* have been carried out to check the performance of the system. These simulations have been made with the DC current configuration of the Table X and the compensation technique values of Table X. These results can be checked in the Table X, in which different parameters as well as the simulated FOM values can be checked. As in the case of the simulations in Section 4, the M_{b6}, M_3-M_4 and M_8 linear states are reported. The objective is that these transistors do not enter in that state.

As seen throughout the project, the MCNR has the worst performance, principally in terms of GBW, with 66.94 kHz, and Slew-Rate. The Phase Margin is practically the 60º desired, with 58.43º. Its first and second stages current bias as well as the power consume are the highest, with 1646 nA and

5524 nW respectively. The main conclusion is that this compensation technique is not very efficient because with high current values with respect the other techniques, the performance is worse. One

TABLE XXXI
THEORETICAL GBW AND FOM VALUES FOR THE DIFFERENT OPTIMUM COMPENSATION TECHNIQUES IN BOTH CLASS-A/CLASS-AB TOPOLOGIES.

PARAMETER	*OTA CLASS-A AMPLIFIER*				*OTA CLASS-AB AMPLIFIER*			
	MCNR	*MCPZC*	*VBC*	*CBC*	*MCNR*	*MCPZC*	*VBC*	*CBC*
GBW (kHz)	88.35	156.14	154.70	302.59	176.71	220.20	218.77	427.23
Using (49) - (50) FOM_S (MHz·pF/(mA/V)) [18]	84	766	767	505	167	1099	1099	713
Using Table XVI. FOM_S (MHz·pF/(mA/V)) [19]	84	766	767	502	167	1099	1063	710
Using (52) FOM_S (MHz·pF/mA) [20]	2142	19653	19674	12813	4284	27716	27822	18090

important thing of this technique is that all transistors are in the linear region so the output signal quality is high. In comparison, the MCPZC present the best performance. It has the highest Positive Slew-Rate value, but it is true that this value is a little bit distorted due to the M_8 linear region so it cannot be considered an objective value. With respect the GBW, with 118.43 kHz, it is not the highest but should be noted that the first and second stages current bias are the lowest, with 306 nA, so in general, shows the best FOM_S performance. Additionally, the power consume is the lowest with 2844 nW. As a final comment, say that the Phase Margin is practically the 60º desired value, with 53.30º. The VBC compensation shows a similar performance with respect to MCPZC, with 107.34 kHz of GBW, 319 nA of first and second stages current bias and a power consume of 2964 nW. Its 55.23º of Phase Margin is practically the desired value. With respect to the Slew-Rate values, the Positive Slew-Rate is the lowest and the Negative Slew-Rate is similar to MCPZC. Note the M_8 linear state. The last compensation technique to analyze is the CBC. Its performance is lower with respect to MCPZC and VBC because it has a GBW of 182.15 kHz, which is the highest but on the contrary, the first and second stages current bias has increased notably with respect to MCPZC and VBC, which can be seen in its FOM_S value. Additionally, the 32.79º of Phase Margin shows a poor value, as well as the CM gain with 2.72 dB, which is due to the well-mention offset. Other aspects to compare between the three techniques is the DC gain and the CM gain. The highest DC and CM gain has the MCNR with 95.68 dB and -3.62 dB respectively. On the contrary, the other three techniques have a similar DC gain. Finally, the CBC has the worst CM gain, as has been said.

In Fig. 42, 43, 44, 45 and 46 the measured open-loop AC frequency response and phase margin, the CM gain as well as the measured unity-gain transient response are shown, for the four compensation techniques.

[18] The stage transconductances have been calculated using this equation, $g_{mT} = g_{m1}\text{-}g_{m2} + g_{m9}\text{-}g_{m10} + g_{mCOMP}$, where g_{mi} is the transconductance for the *i*-th transistor and g_{mCOMP} for the transconductance technique.
[19] The $g_{m1}\text{-}I_1$ is related with $M_1\text{-}M_2$, and $g_{m2}\text{-}I_2$ with $M_9\text{-}M_{10}$.
[20] The stage currents can be calculated using this equation, $I_T = I_{M1}\text{-}I_{M2} + I_{M9}\text{-}I_{M10} + I_C$, where I_{Mi} is the current for *i*-th transistor and I_C is the current of the compensation technique. The theoretical current values can be read in Table XXVII.

TABLE XXXII
SIMULATIONS FOR THE OPTIMUM OTA CLASS-A.

PARAMETER	***OPTIMAL SIMULATIONS***			
	MCNR	***MCPZC***	***VBC***	***CBC***
Initial values	C_c = 8.11 pF R_c = 29.52 kΩ	C_c = 4.40 pF R_c = 2.82 MΩ	C_c = 4.17 pF g_{mVB} = 0.37 µA/V	C_c = 2.16 pF g_{mCB} = 8.39 µA/V
Supply (V)	±1			
Positive Slew Rate (mV/µs)	32.59	463.45	64.35	206.26
Negative Slew Rate (mV/µs)	-27.63	-3.85	-3.94	-11.55
GBW (kHz)	66.94	118.43	107.34	182.15
Phase margin (º)	58.43	53.30	55.23	32.79
Equivalent Input Noise (µV/√Hz)	1.62/√20			
DC gain (dB)	95.68	82.15	81.93	80.92
CM gain (dB)	-3.62	0.64	0.42	2.72
CMRR (dB)	99.30	81.51	82.35	78.20
PSRR+ (dB)	96.45	89.89	100.13	44.16
PSRR- (dB)	112.71	112.92	111.22	44.36
First and Second Stages Current Bias I_T (nA) [21]	1646	306	319	930
Total Amplifier Power Consumption P_{POWER} (nW)	5524	2844	2964	4092
FOM_S (MHz·pF/mA) [21]	1627	15471	13447	7831
FOM_L (V·pF/µs·mA) [21]	732	30523	4278	4682
M_8 Linear Region	NO	YES	YES	YES
M_3-M_4 Linear Region	NO	NO	NO	NO
M_{b6} Linear Region	NO	NO	NO	NO

[21] The total stage is calculated as $I_T = I_{M1}$-I_{M2} + I_{M9}-I_{M10} + I_C, where I_{Mi} is the current for *i*-th transistor and I_C is the current of the compensation technique.

TABLE XXXIII
SIMULATIONS WITH COMPENSATED Φ FOR THE OPTIMUM OTA CLASS-A.

PARAMETER	***OPTIMAL SIMULATIONS WITH COMPENSATED Φ***			
	MCNR	***MCPZC***	***VBC***	***CBC***
Compensated value	C_c = 8.7 pF R_c = 29.52 kΩ	C_c = 5.2 pF R_c = 2.43 MΩ	C_c = 7 pF g_{mVB} = 0.37 µA/V	C_c = 4 pF g_{mCB} = 8.39 µA/V
Relative error (%)	$\delta C_c = 7.3$ $\delta R_c = 0$	$\delta C_c = 15.4$ $\delta R_c = 13.8$	$\delta C_c = 68$ $\delta g_{mVB} = 0$	$\delta C_c = 85.2$ $\delta g_{mCB} = 0$
Supply (V)	±1			
Positive Slew Rate (mV/µs)	30.53	406.76	41.76	168.90
Negative Slew Rate (mV/µs)	-26.40	-3.62	-3.94	-10.85
GBW (kHz)	63.11	105.88	108.21	142.76
Phase margin (º)	59.97	59.72	58.17	59.64
Equivalent Input Noise (µV/√Hz)	1.62/√20			
DC gain (dB)	95.52	82.29	82.31	81.17
CM gain (dB)	3.77	0.78	0.80	2.96
CMRR (dB)	99.29	81.51	81.51	78.21
PSRR+ (dB)	95.96	99.10	97.45	44.17
PSRR- (dB)	112.70	112.91	109.21	44.37
First and Second Stages Current Bias I_T (nA) [22]	1646	306	319	930
Total Amplifier Power Consumption P_{POWER} (nW)	5524	2844	2964	4092
FOM_S (MHz·pF/mA) [22]	1534	13831	13556	6138
FOM_L (V·pF/µs·mA) [22]	692	26805	2863	3864
M_{b6} Linear Region	NO	YES	YES	YES
M_3-M_4 Linear Region	NO	NO	NO	NO
M_8 Linear Region	NO	NO	NO	NO

[22] The total stage is calculated as $I_T = I_{M1}$-I_{M2} + I_{M9}-I_{M10} + I_C, where I_{Mi} is the current for *i*-th transistor and I_C is the current of the compensation technique.

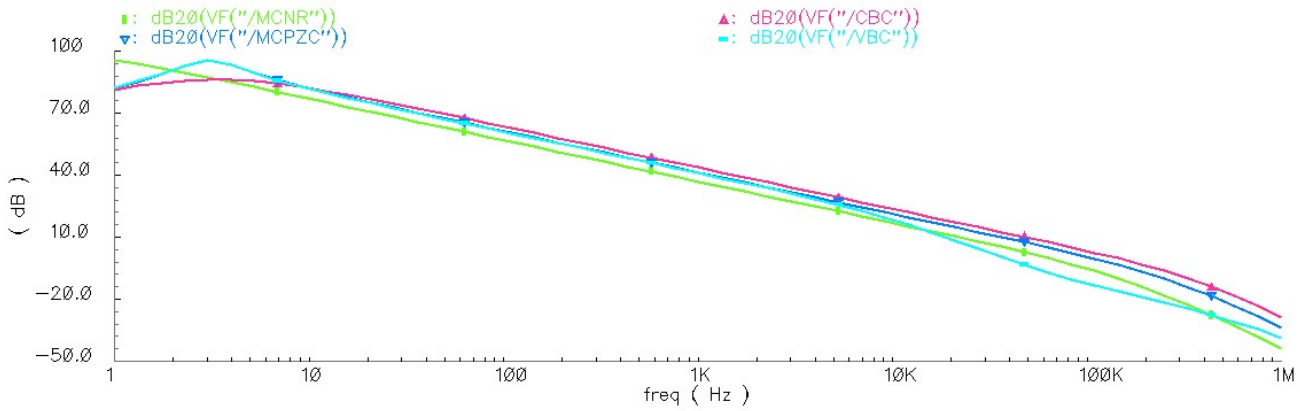


Fig. 42. Class-A measured open-loop AC frequency response for MCNR, MCPZC, VBC and CBC.

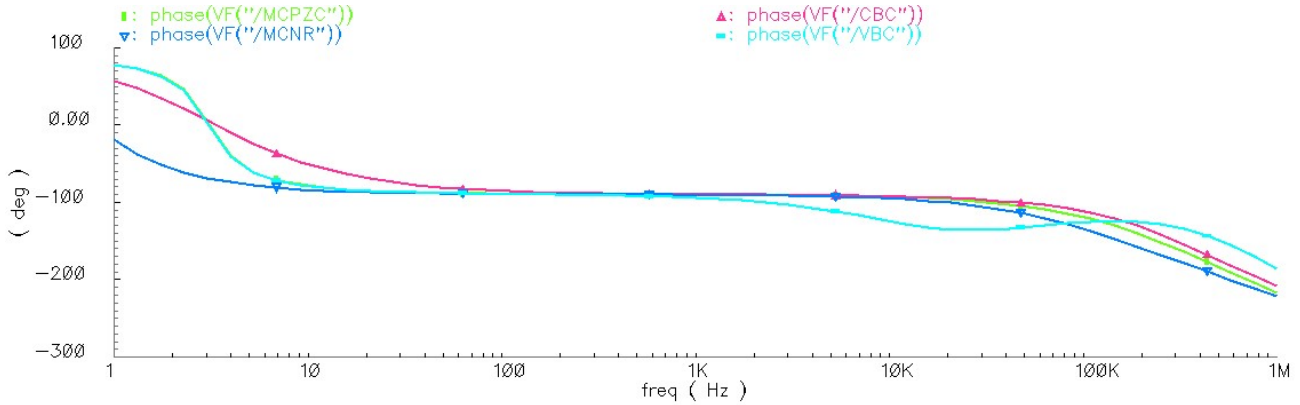


Fig. 43. Class-A measured open-loop AC phase margin response for MCNR, MCPZC, VBC and CBC.

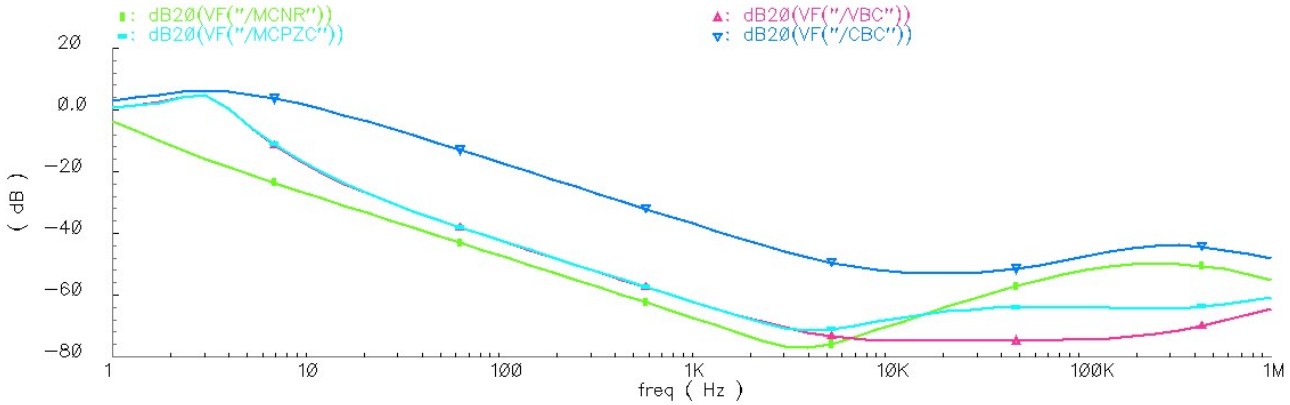


Fig. 44. Class-A measured CM for MCNR, MCPZC, VBC and CBC.

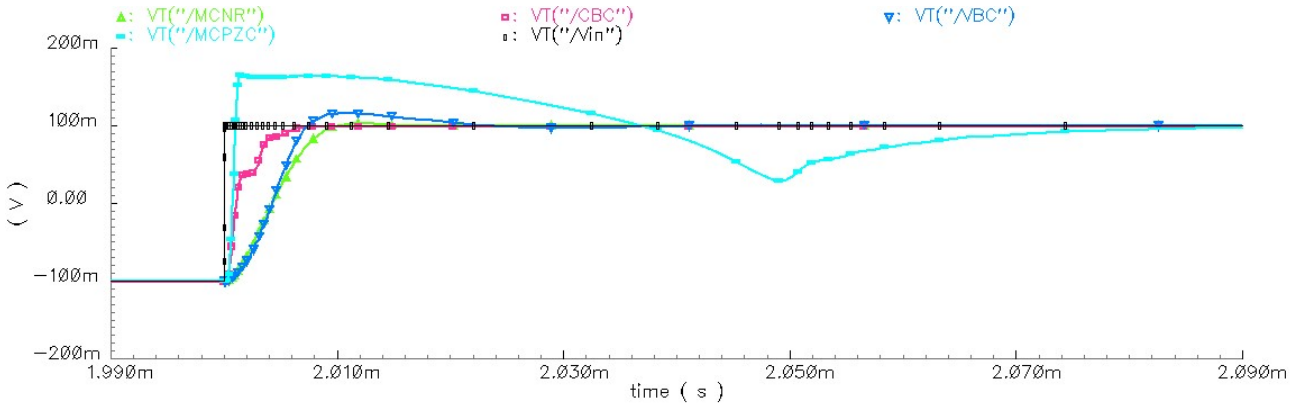


Fig. 45. Class-A measured unity-gain transient response for MCNR, MCPZC, VBC and CBC.

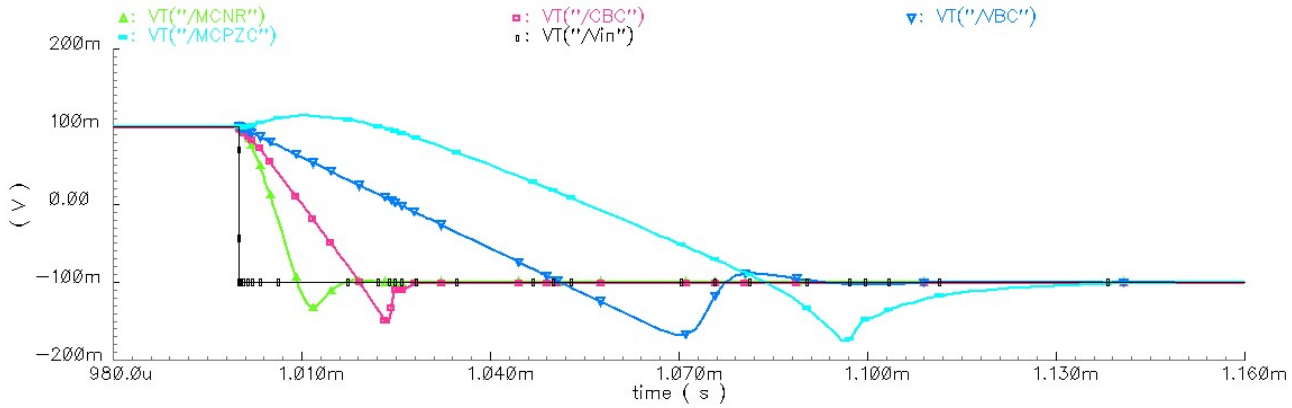


Fig. 46. Class-A measured unity-gain transient response for MCNR, MCPZC, VBC and CBC.

6.5. OTA Class-AB Optimized Amplifier Simulation Results

Then, the simulations for the *OTA class-AB amplifier*, which implements the QFG transistor technique, have been carried out. These simulations have been made with the DC current configuration of Table XXVII and the compensation technique values of Table XXX. For the VBC technique, the current bias has changed, so the aspect ratio of the current mirror transistors must be readjusted. In Table XXXIV, these aspect ratios can be checked. Mention that the aspect ratios for the compensate techniques and for the different topologies are the same as Table XIII except the current bias VBC aspect ratios already mention.

TABLE XXXIV
VBC CURRENT BIAS ASPECT RATIOS FOR THE OTA CLASS-AB COMPENSATED *Φ*.

TRANSISTOR	***VALUE (W/L) (μm/μm)***
	VBC
M_{b7}	15/1.95
M_{b8}	30/1.95
M_{b9}	10.05/1.95
The remaining transistors for the MCNR, MCPZC, and CBC are the same as Table XIII.	

Analyzing the results of Table XXXV, can be appreciated how has influenced the QFG technique, balancing the values of the Positive and Negative Slew-Rates. The Positive Slew-Rate has been decreased, but the Negative Slew-Rate has been increased. This is due to the QFG performance, which detailed analysis can be read in "Subsection 1.4.2. Design Procedure". Other important aspect of the QFG is the non-linear M_8 region, which improves the quality of the output signal. With respect to the Class-A amplifier, the GBW values of the MCPZC, VBC and CBC, with 73.91 kHz, 70.49 kHz and 100.14 kHz respectively, have been decreased but in MCNR has improved to 107.39 kHz. Comparing the four compensation techniques, should be appreciated the values of their Phase Margin, which practically are the desired 60º. In fact, in some techniques as MCPZC or VBC this value is higher, with 65.76º and 62.32º respectively. For the CBC, this value is higher with respect to the initial simulation, wit 58.91º. Finally, for the MCNR this value is lower with respect the previous initial simulations, with 52.68º. Comparing the DC and CM gain, the same analysis can be done with respect the Class-A amplifier. The highest DC gain value has the MCNR with 95.94 dB, then the MCPZC and VBC with practically the same values, that is, 81.91 dB and 81.77 dB. Finally, the CBC has the lowest with 80.84 dB. With respect to the CM gain, the best is the -3.36 dB MCNR technique. Then, the MCPZC and VBC with 0.40 dB and 0.26 dB respectively. Finally, the CBC has the worst value with 2.63 dB due to the current sources offset. With respect the FOM_L, the best performances have the MCPZC and the VBC respectively. The CBC is lower with respect the two previous techniques and the lowest is the MCNR. The FOM_L value can be analyzed in a similar way. The best performance has the VBC. Then, the MCPZC and CBC respectively, and finally the MCNR.

With the objective of achieve the 60º of Phase Margin, the compensation activity has been done again. The same comments can be said as the previous paragraph. The final values can be checked in Table XXXVI.

In Fig. 47, 48, 49, 50 and 51 the measured open-loop AC frequency response and phase margin, the CM gain as well as the measured unity-gain transient response are shown, for the four compensation techniques.

TABLE XXXV
SIMULATIONS FOR THE OPTIMUM OTA CLASS-AB.

PARAMETER	***OPTIMAL SIMULATIONS***			
	MCNR	***MCPZC***	***VBC***	***CBC***
Initial values	C_{QFG} = 1 pF R_{QFG} = 1 MΩ C_c = 4 pF R_c = 14.54 kΩ	C_{QFG} = 1 pF R_{QFG} = 1 MΩ C_c = 3.04 pF R_c = 1.96 MΩ	C_{QFG} = 1 pF R_{QFG} = 1 MΩ C_c = 2.93 pF g_{mVB} = 0.53 µA/V [23]	C_{QFG} = 1 pF R_{QFG} = 1 MΩ C_c = 1.52 pF g_{mCB} = 8.39 µA/V
Supply (V)	±1			
Positive Slew Rate (mV/µs)	56.23	90.56	66.17	82.55
Negative Slew Rate (mV/µs)	-46.94	-209.46	-343.05	-91.16
GBW (kHz)	107.39	73.91	70.49	110.14
Phase margin (º)	52.68	65.76	62.32	58.91
Equivalent Input Noise (µV/√Hz)	1.62/√20			
DC gain (dB)	95.94	81.91	81.77	80.84
CM gain (dB)	-3.36	0.40	0.26	2.63
CMRR (dB)	99.30	81.51	81.51	78.21
PSRR+ (dB)	99.26	99.61	100.37	44.17
PSRR- (dB)	111.08	110.56	109.07	44.37
First and Second Stages Current Bias I_T (nA) [24]	1646	306	327	930
Total Amplifier Power Consumption P_{POWER} (nW)	5524	2844	3030	4092
FOM_S (MHz·pF/mA) [24]	2601	9655	8632	4735
FOM_L (V·pF/µs·mA) [24]	1254	19596	25056	3734
M_8 Linear Region	NO	NO	NO	NO
M_3-M_4 Linear Region	NO	NO	NO	NO
M_{b6} Linear Region	NO	NO	NO	NO

[23] The theoretical current M_V value is 20.67 nA and the simulated value is 21.49 nA. This simulated value is used in the calculation of the First and Second Stages Current Bias, I_T.
[24] The total stage is calculated as $I_T = I_{M1}$-I_{M2} + I_{M9}-I_{M10} + I_C, where I_{Mi} is the current for *i*-th transistor and I_C is the current of the compensation technique.

TABLE XXXVI
SIMULATIONS WITH COMPENSATED Φ FOR THE OPTIMUM OTA CLASS-AB.

PARAMETER	***OPTIMAL SIMULATIONS WITH COMPENSATED Φ***			
	MCNR	***MCPZC***	***VBC***	***CBC***
Compensated value	C_{QFG} = 1 pF R_{QFG} = 1 MΩ C_c = 6 pF R_c = 14.54 kΩ	C_{QFG} = 1 pF R_{QFG} = 1 MΩ C_c = 2.3 pF R_c = 2.54 MΩ	C_{QFG} = 1 pF R_{QFG} = 1 MΩ C_c = 2.7 pF g_{mVB} = 0.53 µA/V	C_{QFG} = 1 pF R_{QFG} = 1 MΩ C_c = 1.7 pF g_{mCB} = 8.39 µA/V
Relative error (%)	$\delta C_{QFG} = 0$ $\delta R_{QFG} = 0$ $\delta C_c = 50$ $\delta R_c = 0$	$\delta C_{QFG} = 0$ $\delta R_{QFG} = 0$ $\delta C_c = 24.3$ $\delta R_c = 29.6$	$\delta C_{QFG} = 0$ $\delta R_{QFG} = 0$ $\delta C_c = 7.9$ $\delta g_{mVB} = 0$	$\delta C_{QFG} = 0$ $\delta R_{QFG} = 0$ $\delta C_c = 11.8$ $\delta g_{mCB} = 0$
Supply (V)	±1			
Positive Slew Rate (mV/µs)	39.91	103.85	69.42	78.42
Negative Slew Rate (mV/µs)	-34.11	-249.10	-342.78	-87.80
GBW (kHz)	78.64	83.71	70.75	107.63
Phase margin (º)	60.21	60.68	60.91	60.03
Equivalent Input Noise (µV/√Hz)	1.62/√20			
DC gain (dB)	96.00	81.78	81.74	80.86
CM gain (dB)	-3.30	0.27	0.23	2.65
CMRR (dB)	99.30	81.51	81.51	78.21
PSRR+ (dB)	97.40	100.97	100.60	44.16
PSRR- (dB)	111.10	111.18	109.23	44.36
First and Second Stages Current Bias I_T (nA) [25]	1646	306	327	930
Total Amplifier Power Consumption P_{POWER} (nW)	5524	2844	3030	4092
FOM_S (MHz·pF/mA) [25]	1911	10935	8664	4627
FOM_L (V·pF/µs·mA) [25]	899	23054	25238	3573
M_8 Linear Region	NO	NO	NO	NO
M_3-M_4 Linear Region	NO	NO	NO	NO
M_{b6} Linear Region	NO	NO	NO	NO

[25] The total stage is calculated as $I_T = I_{M1}$-I_{M2} + I_{M9}-I_{M10} + I_C, where I_{Mi} is the current for *i*-th transistor and I_C is the current of the compensation technique.

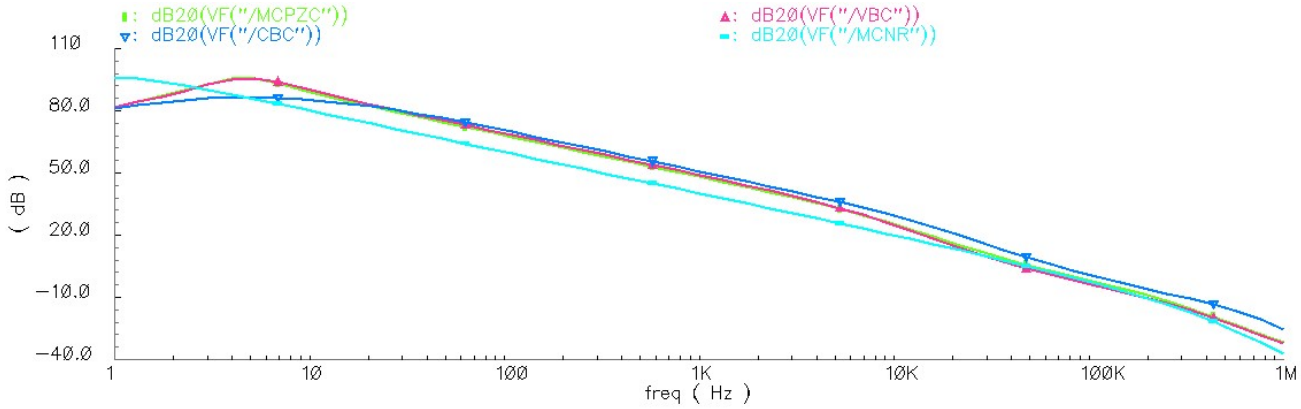


Fig. 47. Class-AB measured open-loop AC frequency response for MCNR, MCPZC, VBC and CBC.

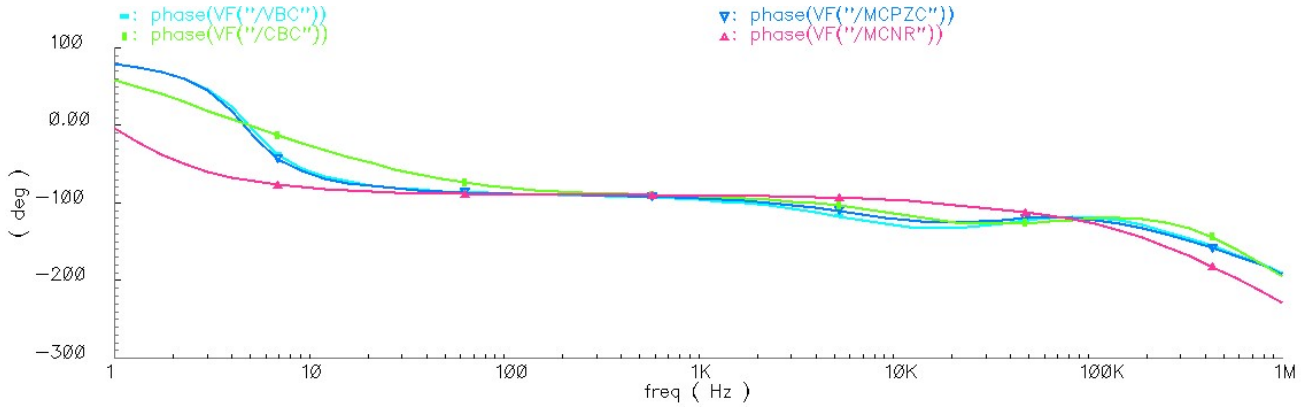


Fig. 48. Class-AB measured open-loop AC phase margin response for MCNR, MCPZC, VBC and CBC.

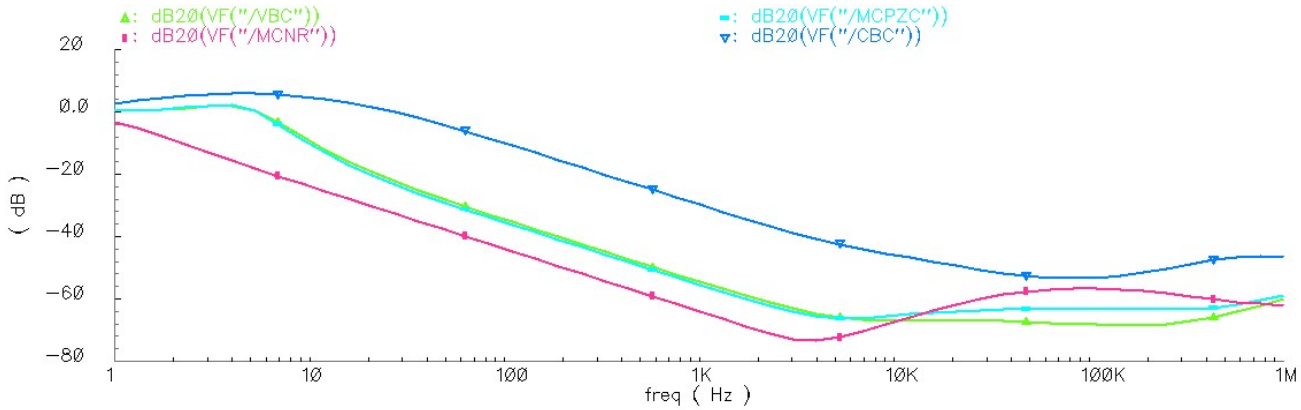


Fig. 49. Class-AB measured CM for MCNR, MCPZC, VBC and CBC.

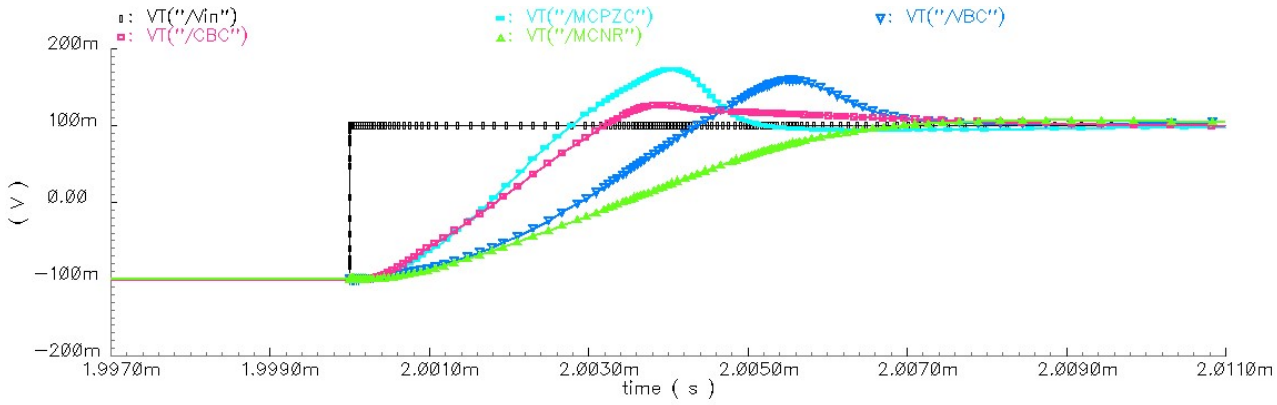


Fig. 50. Class-AB measured unity-gain transient response for MCNR, MCPZC, VBC and CBC.

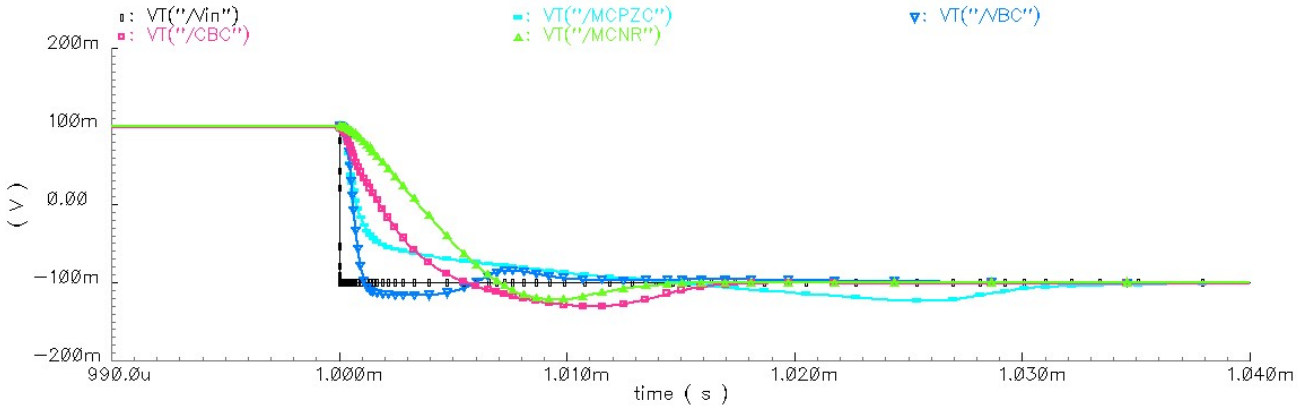


Fig. 51. Class-AB measured unity-gain transient response for MCNR, MCPZC, VBC and CBC.

6.6. Corner Analysis

In order to show the circuit robustness against process and temperature variation, results of corner analysis are summarized in Table XXXVII, XXXVIII and XXXIX. This corner analysis has been done for the MCPZC, VBC and CBC techniques with compensated Φ, with through temperatures (-10º, 27º and 85º) and the process variations Nominal (TT), Fast (FF), Slow (SS), Fast N/Slow P (FS) and Slow N/Fast P (SF).

TABLE XXXVII
MCPZC CORNER ANALYSIS.

PARAMETER	***MCPZC***														
	T = -10ºC					***T = 27ºC***					***T = 85ºC***				
	TT	***FF***	***SS***	***FS***	***SF***	***TT***	***FF***	***SS***	***FS***	***SF***	***TT***	***FF***	***SS***	***FS***	***SF***
S. R. + (V/µs)	113.4	117.2	109.9	112.5	113.6	103.9	107.5	100.5	102.9	104.1	91.5	94.3	88.8	90.7	85.9
S. R. – (V/µs)	-348.8	-375.4	-314.3	-347.0	-345.7	-249.1	-270.3	-226.7	-251.0	-246.2	-151.0	-165.4	-136.8	-153.5	-148.8
GBW (kHz)	100.06	107.50	92.96	98.04	100.51	83.71	90.57	77.99	81.91	84.01	65.78	70.11	61.50	64.32	65.74
P.M. (º)	61.10	62.52	59.91	61.62	60.84	60.68	62.10	59.29	61.12	60.48	58.86	60.62	57.30	59.12	58.72
DC gain (dB)	82.51	82.07	81.80	81.82	80.35	81.78	81.18	81.46	81.44	81.45	80.52	79.73	80.64	80.55	80.00
CM gain (dB)	0.25	0.12	0.36	0.32	0.20	0.27	0.16	0.31	0.29	0.24	0.31	0.24	0.35	0.33	0.27
I_T (nA)	303	304	302	303	304	306	307	306	306	307	309	310	309	309	310
P_{POWER} (nW)	2820	2810	2836	2826	2818	2844	2836	2858	2848	2842	2870	2866	2882	2872	2872
M_8 Linear	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO
M_3-M_4 Linear	NO	YES	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO
M_{b6} Linear	NO	NO	YES	YES	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO

TABLE XXXVIII
VBC CORNER ANALYSIS.

PARAMETER	***VBC***														
	T = -10ºC					***T = 27ºC***					***T = 85ºC***				
	TT	***FF***	***SS***	***FS***	***SF***	***TT***	***FF***	***SS***	***FS***	***SF***	***TT***	***FF***	***SS***	***FS***	***SF***
S. R. + (V/µs)	72.4	72.1	72.7	72.0	72.7	69.4	69.3	69.3	68.8	69.8	65.2	65.2	65.0	64.5	65.5
S. R. – (V/µs)	-466.4	-495.0	-422.0	-457.1	-468.9	-331.4	-366.3	-313.8	-342.0	-341.4	-216.0	-233.6	-197.7	-216.8	-213.1
GBW (kHz)	79.26	80.03	78.81	77.24	80.49	69.31	71.45	70.23	68.92	71.34	58.06	58.98	57.50	56.77	58.63
P.M. (º)	63.15	64.18	61.71	63.24	62.88	60.41	61.98	59.57	61.06	60.73	58.67	59.68	57.43	58.72	58.50
DC gain (dB)	82.47	82.04	81.75	81.79	82.31	81.74	81.41	81.41	81.40	81.42	80.48	79.70	80.58	80.51	79.96
CM gain (dB)	0.21	0.09	0.31	0.28	0.16	0.23	0.13	0.34	0.25	0.19	0.27	0.18	0.30	0.29	0.23
I_T (nA)	323	326	319	323	323	328	330	324	327	327	331	334	328	331	331
P_{POWER} (nW)	3004	3002	3012	3010	3002	3030	3030	3038	3034	3030	3060	3062	3066	3062	3062
M_8 Linear	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO
M_3-M_4 Linear	NO	YES	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO
M_{b6} Linear	NO	NO	YES	YES	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO

TABLE XXXIX
CBC CORNER ANALYSIS.

PARAMETER	*CBC*														
	T = -10ºC					*T = 27ºC*					*T = 85ºC*				
	TT	*FF*	*SS*	*FS*	*SF*	*TT*	*FF*	*SS*	*FS*	*SF*	*TT*	*FF*	*SS*	*FS*	*SF*
S. R. + (V/µs)	80.6	81.3	80.0	80.7	80.3	78.4	79.5	77.7	78.4	78.2	73.7	74.8	72.9	73.6	73.7
S. R. – (V/µs)	-98.7	-100.2	-96.6	-98.2	-99.2	-87.8	-90.0	-85.9	-87.6	-88.2	-73.7	-75.8	-71.2	-73.8	-73.5
GBW (kHz)	125.10	130.70	119.64	121.72	126.54	107.63	111.94	104.35	105.62	108.40	89.46	92.95	86.32	87.57	90.07
P.M. (º)	61.03	62.54	59.77	61.16	60.94	60.03	60.61	58.55	59.97	60.03	57.77	59.33	56.41	57.71	57.79
DC gain (dB)	81.27	80.23	81.00	80.72	80.97	80.86	79.73	80.93	80.62	80.42	79.95	78.73	80.39	80.05	79.36
CM gain (dB)	9.95	6.28	14.99	11.18	9.22	2.65	0.43	4.72	1.86	2.92	-0.61	-0.78	-0.44	-0.32	-0.74
I_T (nA)	928	912	933	924	920	930	922	941	932	929	939	933	949	941	940
P_{POWER} (nW)	4056	4024	4098	4068	4050	4092	4064	4130	4100	4088	4132	4110	4162	4136	4132
M_8 Linear	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO
M_3-M_4 Linear	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO
M_{b6} Linear	NO	NO	YES	YES	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO

7. DISCUSSION

Once the simulations have been done, the results obtained must be compared. First of all, it is important to appreciate that the simulations have been successful. The optimization effectively has improved the circuit performance in terms of FOM. To make a critical comparison, a review of the main results can be checked in Table XL. Remark that the results have been taken from the compensated Φ simulations.

Comparing the Class-A initial and optimal simulations, can be checked how the current stage optimization improves the performance for the MCPZC, VBC and CBC cases. For MCNR, the optimization has not taken affect. It is important to appreciate how the optimization reduces the GBW, but also reduces the I_T, so it implies a compensation between the performance values and an increment of the FOM_S and FOM_L. In this Class-A amplifier, due to M_8 linear state, the output quality signal is not very good, so the Slew-Rate is altered. Although the phase margin is the 60º desired value, the output signal is affected. The conclusion is that the lower the current output is, the lower the output quality signal is, as can be compared in Fig. 33-34. and Fig. 45-46. This is due to the decrement of the output current bias in the optimization, which implies a slower system.

This output quality signal can be improved using the QFG technique, which converts the Class-A amplifier in a Class-AB amplifier. The inclusion of this technique makes faster the system because more current is generated at the output and faster is the charge-discharge of the output transistors. This improvement can be seen comparing the Fig. 33-34-45-46 with Fig.38-39-50-51. Again, can be checked how improves the optimization the Class-AB amplifier with respect to the initial simulations. All compensation techniques have been improved, except the CBC FOM_S value.

Another discussion is based on the comparison among Class-A/Class-AB optimal amplifiers. Effectively, the QFG technique improves the Slew-Rate parameter. Only the MCPZC case cannot be compared because the optimal Class-A output signal is altered by the M_8 linear state. In conclusion, the Class-AB FOM_L performance is better with respect the Class-A amplifier. With respect to the FOM_S, the results are different. The MCNR of the Class-AB is better than the Class-A. For the case

of the Class-AB MCPZC, VBC and CBC cases, these values are worse with respect the Class-A amplifier. This result paradoxical because the Class-AB amplifier, theoretically, improves the GBW with respect the Class-A amplifier. This must be studied in detailed to discover why occurs.

Finally, the theoretically FOM performance is verified. According to the theoretical values, the MCPZC has the best performance, then the VBC and CBC respectively, and finally the MCNR. This same argument can be done in simulations, show the FOM concept effectively works.

TABLE XL
COMPARISION RESULTS

PARAMETER	***MCNR***	***MCPZC***	***VBC***	***CBC***	***MCNR***	***MCPZC***	***VBC***	***CBC***
	OTA CLASS-A INITIAL SIMULATIONS				***OTA CLASS-AB INITIAL SIMULATIONS***			
Positive Slew Rate (mV/µs)	23.55	211.47	82.18	196.01	30.01	92.52	75.05	110.64
Negative Slew Rate (mV/µs)	-20.26	-30.38	-26.88	-24.70	-23.09	-100.40	-200.95	-113.96
GBW (kHz)	48.03	208.35	156.64	214.79	56.62	174.93	135.99	187.43
I_T (nA)	1218	1218	1295	1519	1218	1218	1367	1519
P_{POWER} (nW)	4668	4668	4958	5270	4668	4668	5270	5270
FOM_S (MHz·pF/mA)	1577	6842	4839	5655	1859	5744	3980	4935
FOM_L (V·pF/µs·mA)	719	2905	1685	2905	872	3168	4039	2957
PARAMETER	***MCNR***	***MCPZC***	***VBC***	***CBC***	***MCNR***	***MCPZC***	***VBC***	***CBC***
	OTA CLASS-A OPTIMAL SIMULATIONS				***OTA CLASS-AB OPTIMAL SIMULATIONS***			
Positive Slew Rate (mV/µs)	30.53	406.76	41.76	168.90	39.91	103.85	69.42	78.42
Negative Slew Rate (mV/µs)	-26.40	-3.62	-3.94	-10.85	-34.11	-249.10	-342.78	-87.80
GBW (kHz)	63.11	105.88	108.21	142.76	78.64	83.71	70.75	107.63
I_T (nA)	1646	306	319	930	1646	306	327	930
P_{POWER} (nW)	5524	2844	2964	4092	5524	2844	3030	4092
FOM_S (MHz·pF/mA)	1534	13831	13556	6138	1911	10935	8664	4627
FOM_L (V·pF/µs·mA)	692	26805	2863	3864	899	23054	25238	3573

8. CONCLUSIONS AND FUTURE RESEARCH

8.1. Conclusions

A family of sub-threshold two-stage CMOS OTAs have been designed in a 0.5-µm technology, which are based in the Class-A and Class-AB amplifiers. This last uses the QFG technique to achieve this performance.

As cited, the sub-threshold inversion mode has been used. It has been checked the potential of this mode to obtain low power systems, with the counterpart of having low bandwidths. This inversion mode is suitable in systems in which the bandwidth is not a design requirement, but a very low power consume is desired. The advantage of this mode is based on the facility of using the design equations in the transconductance or current mode due to the direct relation between them.

For maintaining the stability of the systems, different compensation strategies have been used. It has been checked experimentally that the MCNR has the lowest performance. Conversely, the MCPZC

technique, which is implemented in the same way as the MCNR, has shown the best performance. Then, the VBC is similar to the MCPZC but with a higher consume and a worse performance. Finally, the CBC has a lower performance in comparison with MCPZC and VBC. Comment that in this technique, an offset is generated in the output first stage because the current bias sources have not got the same current values.

This compensation techniques have been compared by analytical figures of merit, which express a tradeoff between gain-bandwidth product, Slew-Rate, load capacitance, and the total current-transconductance for a given value of phase margin. Through these figures of merit, optimal current stage relationships have been searched, which optimize the performance of the system. It has been checked how has improved the performance of the systems. Remark that the optimal configuration in the OTA Class-A with MCNR and the OTA Class-AB with CBC technique has not improved with respect to the initial simulation.

In relation with the sub-threshold mode, is important to appreciate that due to the system is taken to an extreme condition, the small-signal models and the compensation techniques could change so new system models could be researched.

8.2. Future Research

With the aim of continuing to research with the project, some future researches are described. The immediately activity consist in design the final layouts, fabricate the chip and test it to check if the experimental results coincide with the simulated ones.

One interesting line could consist in the detailed study of the compensation techniques and the sub-threshold mode. Through this study, the equations which describe the compensation technique values could be readjusted. Additionally, different compensation techniques could be studied using the sub-threshold mode.

In relation with the QFG technique, an accurate small-signal amplifier model could be developed. Although it has not been contemplated in the project, it has been proven by simulations that modifying the QFG components, the gain-bandwidth product has increased. If a small-signal model is developed, and the same procedure for obtaining the figures of merit is followed, a general expression could be developed which not only optimizes the current stages bias, but also optimizes the QFG values to increase the FOM values obtained.

Another work could be the use of a more modern technology, which decreases the power consume and the voltage bias.

REFERENCES

[1] Wikipedia contributors. "MOSFET." Internet: https://en.wikipedia.org/w/index.php?title=MOSFET&oldid=835605896, 9 Apr. 2018. [11 Apr. 2018].

[2] G. Schrom. “Ultra-Low-Power CMOS Technology”. Ph. D. thesis, Universität Wien, Germany, 1998.

[3] D. J. Comer and D. T. Comer, "Using the weak inversion region to optimize input stage design of CMOS op amps," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 51, no. 1, pp. 8-14, Jan 2004.

[4] D. J. Comer and D. T. Comer, "Operation of analog MOS circuits in the weak or moderate inversion region," in *IEEE Transactions on Education*, vol. 47, no. 4, pp. 430-435, Nov. 2004.

[5] E. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operations," in *IEEE Journal of Solid-State Circuits*, vol. 12, no. 3, pp. 224-231, Jun 1977.

[6] M. Alioto, "Understanding DC Behavior of Subthreshold CMOS Logic Through Closed-Form Analysis," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 7, pp. 1597-1607, July 2010.

[7] Magnelli L., Amoroso F. A., Crupi F., Cappuccino G. and Iannaccone G. (2014), Design of a 75-nW, 0.5-V subthreshold complementary metal–oxide–semiconductor operational amplifier, *International Journal of Circuit Theory and Applications*, 42, pages 967–977, doi: 10.1002/cta.1898.

[8] A. D. Grasso, D. Marano, G. Palumbo and S. Pennisi, "Design Methodology of Subthreshold Three-Stage CMOS OTAs Suitable for Ultra-Low-Power Low-Area and High Driving Capability," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 6, pp. 1453-1462, June 2015.

[9] Z. Yan, W. Wang, P. I. Mak, M. K. Law and R. P. Martins, "A 0.0045-mm^2 32.4-μW Two-Stage Amplifier for pF-to-nF Load Using CM Frequency Compensation," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 62, no. 3, pp. 246-250, March 2015.

[10] C. García Alberdi, "Filtros CMOS integrados de muy bajo consumo para selección de canal en receptores Bluetooth y Zigbee," M.S. thesis, Electrical and Electronical Eng. Dept., Universidad Pública de Navarra, Pamplona, 2009.

[11] J. Ramirez-Angulo, A. J. Lopez-Martin, R. G. Carvajal and F. M. Chavero, "Very low-voltage analog signal processing based on quasi-floating gate transistors," in *IEEE Journal of Solid-State Circuits*, vol. 39, no. 3, pp. 434-442, March 2004.

[12] T.C. Carusone, D.A. Johns, K.W. Martin, *Analog Integrated Circuit Design*, 2nd Edition. Willey, 2012.

[13] S. Mallya and J. H. Nevin, "Design procedures for a fully differential folded-cascode CMOS operational amplifier," in *IEEE Journal of Solid-State Circuits*, vol. 24, no. 6, pp. 1737-1740, Dec 1989.

[14] A. D. Grasso, G. Palumbo and S. Pennisi, "Comparison of the Frequency Compensation Techniques for CMOS Two-Stage Miller OTAs," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 11, pp. 1099-1103, Nov. 2008.

[15] G. Palmisano and G. Palumbo, "An optimized compensation strategy for two-stage CMOS op amps," in IEEE *Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 42, no. 3, pp. 178-182, Mar 1995.

[16] G. Palmisano and G. Palumbo, "A compensation strategy for two-stage CMOS opamps based on current buffer," in *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 44, no. 3, pp. 257-262, Mar 1997.

[17] A. Luchetta, S. Manetti and A. Reatti, "SAPWIN-a symbolic simulator as a support in electrical engineering education," in *IEEE Transactions on Education*, vol. 44, no. 2, pp. 9 pp.-, May 2001.

[18] A. D. Grasso, G. Palumbo, and S. Pennisi, "Analytical comparison of frequency compensation techniques in three-stage amplifiers," *J. Circuit Theory. Appl.*, vol. 36, no. 1, pp. 53–80, Jan. 2008.

[19] Grasso, Alfio & Marano, Davide & Pennisi, Salvatore & Vazzana, G. (2015). Symbolic factorization methodology for multistage amplifier transfer functions. *International Journal of Circuit Theory and Applications*. 44. 10.1002/cta.2061.

[20] A. J. Lopez-Martin, S. Baswa, Jaime Ramirez-Angulo and R. G. Carvajal, "Low-Voltage Super class AB CMOS OTA cells with very high slew rate and power efficiency," in *IEEE Journal of Solid-State Circuits*, vol. 40, no. 5, pp. 1068-1077, May 2005.

[21] J. A. Galan, A. López-Martín, R. G. Carvajal, J. Ramírez-Angulo "Super Class-AB OTAs With Adaptive Biasing and Dynamic Output Current Scaling", in *IEEE Transactions on Circuits and Systems-I: Regular Papers*, VOL. 54, NO. 3, MARCH 2007 pp. 449–457.

[22] P. Monsurró, S. Pennisi, G. Scotti and A. Trifiletti, "Exploiting the Body of MOS Devices for High Performance Analog Design," in *IEEE Circuits and Systems Magazine*, vol. 11, no. 4, pp. 8-23, Fourthquarter 2011.

APPENDIX A: COMPENSATION TECHNIQUES CALCULATIONS SCRIPT

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%% COMPENSATION TECHNIQUES CALCULATIONS %%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%{
    # Description of the Script:

In this script, the calculations for the different compensation
techniques is carried out. It can be obtained the different
capacitor, resistor or transconductance-current compensation values.
%}

%%%%%%%%%%%%%%%%%%%%
%%%% VARIABLES %%%%
%%%%%%%%%%%%%%%%%%%%
phi = 60;                   % Phase margin
n = 1.5;                    % Slope factor
Vt = 26e-3;                 % Thermal voltage
gm1 = 3.84e-6;              % Transconductance of the first stage
gm9 = 38.85e-6;             % Transconductance of the second stage (M9)
%gm10 = 34.89e-6;           % Transconductance of M10
%gm9 = gm9+gm10;            % Transconductance for QFG
Gmn = gm1/gm9;              % Transconductance relationship
ro1 = 146.00e6;             % Output resistance of the first stage
Cload = 40e-12;             % Load capacitance
Cjd6 = 1.67e-13;            % Parasitic capacitance junction drain of M6
Cjd8 = 4.03e-14;            % Parasitic capacitance junction drain of M8
Cgg9 = 1.24e-14;            % Total gate parasitic capacitance of M9
CA = Cjd6 + Cjd8 + Cgg9;    % Total output first stage capacitance

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%% COMPENSATION VALUES CALCULATION %%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%% NULLING RESISTOR: NR %%
RcNR = 1/gm9;
CcNR = (gm1/gm9)*Cload*tand(phi);

%% NULLING RESISTOR POLE-ZERO CANCELATION: NRPZC %%
CcNRPZ = (gm1/gm9)*(tand(phi)/2)*(1+sqrt(1+4*(Cload/(CA*Gmn*tand(phi)))))*CA;
RcNRPZ = (Cload+CcNRPZ)/(gm9*CcNRPZ);

% Cc and Rc equalization for readjust the values in the phi compensation
% process
CcNRPZ_equalized = 2.3e-12;
RcNRPZ_equalized = (Cload+CcNRPZ_equalized)/(gm9*CcNRPZ_equalized);

%% VOLTAGE BUFFER: VB %%
CcVB = sqrt((gm1/gm9)*Cload*CA*tand(phi));
gmVB = (gm9*CcVB)/Cload;
```

```
IVB = gmVB*n*Vt;

% Cc and gm equalization for readjust the values in the phi compensation
% process
CcVB_equalized = 3e-12;
gmVB_equalized = (gm9*CcVB_equalized)/Cload;
IVB_equalized = gmVB_equalized*n*Vt;

%% CURRENT BUFFER: CB %%
Wgbw_Wgbwi = sqrt(1+(4/tand(phi)))-1;
Wgbwi_Wgbw = 1/Wgbw_Wgbwi;
CcCB = sqrt((gm1/gm9)*(Wgbwi_Wgbw)*CA*Cload)-Cload/(2*gm9*ro1);
gmCB = tand(phi)*Wgbwi_Wgbw*gm1;
ICB = gmCB*n*Vt;
```

APPENDIX B: FIGURE OF MERIT I1/I2 REPRESENTATION SCRIPT

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%% FIGURE OF MERIT REPRESENTATION V1: I1/I2 %%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%{
    # Description of the Script:

The aim of this script is to calculate the different FOMs of the
circuit. Once this FOMs have been calculated, the optimum value of them
will be searched. A figure with the FOM calculation will be shown.

    # Commentary Related With I1 and I2 Values:

For doing some calculations, two different currents will be used,
which are I1 and I2.
- I1: Is the current of each transistor in the differential pair.
- I2: Is the current of the output stage.
The I1/I2 relates the two currents described.
%}

%%%%%%%%%%%%%%%%%%%%
%%%% VARIABLES %%%%
%%%%%%%%%%%%%%%%%%%%
phi = 60;                       % Phase margin
Cload = 40e-12;                 % Load capacitance
CA =  3.23e-13;                 % Total output first stage capacitance
CAC = CA;                       % Total output first stage capacitance
relation_upper_limit = 10;      % Maximum I1/I2 relationship
relation_down_limit = 0.001;    % Minimum I1/I2 relationship
QFG_Flag = 2;                   % QFG flag
                                  %%% QFG_flag = 1 --> Without QFG
                                  %%% QFG_flag = 2 --> With QFG

%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%% FOMs CALCULATION %%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%
%% NULLING RESISTOR: NR %%
% I1/I2 relation array %
var_NR_I1_I2 = relation_down_limit:0.001:relation_upper_limit;

% FOM calculation %
FOM_NR = (1/(2*pi)).*(1./((var_NR_I1_I2+1)*tand(phi))).*QFG_Flag;
```

```
% Search the optimum value %
max_FOM_NR = max(FOM_NR);                % Maximum value of the FOM
pos_max_NR = find(FOM_NR == max_FOM_NR); % Position of the maximum FOM value
ratio_NR = var_NR_I1_I2(pos_max_NR);     % I1/I2 optimum relation

%% NULLING RESISTOR POLE-ZERO CANCELATION: NRPZC %%
% I1/I2 and I2/I1 relation arrays %
var_NRPZC_I1_I2 = relation_down_limit:0.001:relation_upper_limit;
var_NRPZC_I2_I1 = 1./var_NRPZC_I1_I2;

% FOM calculation %
FOM_NRPZC =
(1/(2*pi)).*(2*QFG_Flag./((var_NRPZC_I1_I2+1).*tand(phi).*(1+sqrt(1+4*QFG_Flag.*C
load./(CA*tand(phi).*var_NRPZC_I1_I2)))))*(Cload/CA);

% Search the optimum value %
max_FOM_NRPZC = max(FOM_NRPZC);                    % Maximum value of the FOM
pos_max_NRPZC = find(FOM_NRPZC == max_FOM_NRPZC); % Position of the maximum FOM
value
ratio_NRPZC = var_NRPZC_I1_I2(pos_max_NRPZC);     % I1/I2 optimum relation

%% VOLTAGE BUFFER: VB %%
% I1/I2 relation array %
var_VB_I1_I2 = relation_down_limit:0.001:relation_upper_limit;

% FOM calculation %
FOM_VB =
(1/(2*pi)).*((sqrt(var_VB_I1_I2.*QFG_Flag*(1/tand(phi))*(Cload/CA))./(var_VB_I1_
I2+1+sqrt(var_VB_I1_I2.*QFG_Flag*tand(phi)*(CA/Cload))));

% Search the optimum value %
max_FOM_VB = max(FOM_VB);                % Maximum value of the FOM
pos_max_VB = find(FOM_VB == max_FOM_VB); % Position of the maximum FOM value
ratio_VB = var_VB_I1_I2(pos_max_VB);     % I1/I2 optimum relation

%% CURRENT BUFFER: CB %%
% I1/I2 relation array %
var_CB_I1_I2 = relation_down_limit:0.001:relation_upper_limit;

% FOM calculation %
Wgbw_Wgbwi = sqrt(1+(4/tand(phi)))-1;
Wgbwi_Wgbw = 1/Wgbw_Wgbwi;

    % Original Version %
FOM_CB_v1 =
(1/(2*pi)).*(sqrt((var_CB_I1_I2.*(QFG_Flag).*Wgbw_Wgbwi*Cload)/CAC)./(var_CB_I1_I
2.*(1+(2/(Wgbwi_Wgbw-1)))+1));
    % New Version %
FOM_CB_v2 =
(1/(2*pi)).*(sqrt((var_CB_I1_I2.*(QFG_Flag).*Wgbw_Wgbwi*Cload)/CAC)./(var_CB_I1_I
2.*(1+(tand(phi)*Wgbwi_Wgbw))+1));

% Search the optimum value (Original Version) %
max_FOM_CB_v1 = max(FOM_CB_v1);                    % Maximum value of the FOM
pos_max_CB_v1 = find(FOM_CB_v1 == max_FOM_CB_v1); % Position of the maximum FOM
value
ratio_CB_v1 = var_CB_I1_I2(pos_max_CB_v1);        % I1/I2 optimum relation

% Search the optimum value (New Version)%
```

```
max_FOM_CB_v2 = max(FOM_CB_v2);                     % Maximum value of the FOM
pos_max_CB_v2 = find(FOM_CB_v2 == max_FOM_CB_v2); % Position of the maximum FOM
value
ratio_CB_v2 = var_CB_I1_I2(pos_max_CB_v2);          % I1/I2 optimum relation

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%% GRAPHIC OF THE FOMs %%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% FOMs graphics %
plot(var_NR_I1_I2,FOM_NR,'linewidth',1);
hold on
plot(var_NRPZC_I1_I2,FOM_NRPZC,'linewidth',1);
hold on
plot(var_VB_I1_I2,FOM_VB,'linewidth',1);
hold on
%plot(var_CB_I1_I2,FOM_CB_v1,'linewidth',1);
%hold on
plot(var_CB_I1_I2,FOM_CB_v2,'linewidth',1);
%title('Figures of Merit','fontsize',18)
xlabel('I_1/I_2','fontsize',15,'fontweight','bold')
ylabel('FOM','fontsize',15,'fontweight','bold')
%legend({'MCNR','MCPZC','VBC','CBC orig','CBC new'},'FontSize',13)
legend({'MCNR','MCPZC','VBC','CBC'},'FontSize',13)
grid on
grid minor
hold off
```

APPENDIX C: FIGURE OF MERIT IT/I2 REPRESENTATION SCRIPT

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%% FIGURE OF MERIT CALCULATION V2: IT/I2 %%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%{
    # Description of the Script:

The aim of this script is to calculate the different FOMs of the
circuit. Once this FOMs have been calculated, the optimum value of them
will be searched. A figure with the FOM calculation will be shown.

    # Commentary Related With I1, I2 and IT Values:

For doing some calculations, two different currents will be used,
which are IT and I2.
- IT: Is the total current of the system.
- I2: Is the current of the output stage.
The IT/I2 relates the two currents described. Once this current
relationship is got, the I1/I2 are calculated.

    # Comments related to the calculations:
The calculations are done for NR, NRPZC and CB compensation techniques.
In the case of VB, the calculation are not be able. This is due to some
complex number are got. However, the VB calculation is included.
%}

%%%%%%%%%%%%%%%%%%%
%%%% VARIABLES %%%%
%%%%%%%%%%%%%%%%%%%
phi = 60;                  % Phase margin
Cload = 40e-12;            % Load capacitance
```

```
CA =  2.52e-13;             % Total output first stage capacitance
CAC = CA;                   % Total output first stage capacitance
relation_upper_limit = 10;  % Maximum I1/I2 relationship
relation_down_limit = 1;    % Minimum I1/I2 relationship
QFG_flag = 1;               % QFG flag
                              %%% QFG_flag = 1 --> Without QFG
                              %%% QFG_flag = 2 --> With QFG

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%% FOMs CALCULATION: NR - NRPZC - CB %%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%% NULLING RESISTOR: NR %%
% IT/I2 relation array %
var_NR_IT_I2 = relation_down_limit:0.001:relation_upper_limit;

% FOM calculation %
FOM_NR = (1/(2*pi)).*(1./(var_NR_IT_I2*tand(phi))).*QFG_flag;

% Search the optimum value %
max_FOM_NR = max(FOM_NR);                % Maximum value of the FOM
pos_max_NR = find(FOM_NR == max_FOM_NR); % Position of the maximum FOM value
ratio_NR_IT_I2 = var_NR_IT_I2(pos_max_NR);     % IT/I2 optimum relation

% I1/I2 relation
ratio_NR_I1_I2 = ratio_NR_IT_I2 - 1;

%% NULLING RESISTOR POLE-ZERO CANCELATION: NRPZC %%
% IT/I2 relation array %
var_NRPZC_IT_I2 = relation_down_limit:0.001:relation_upper_limit;

% FOM calculation %
FOM_NRPZC =
(1/(2*pi)).*((2*QFG_flag)./(var_NRPZC_IT_I2.*tand(phi).*(1+sqrt(1+4*QFG_flag*Cloa
d./(CA*tand(phi).*(var_NRPZC_IT_I2-1))))))*(Cload/CA);

% Search the optimum value %
max_FOM_NRPZC = max(FOM_NRPZC);                   % Maximum value of the FOM
pos_max_NRPZC = find(FOM_NRPZC == max_FOM_NRPZC); % Position of the maximum FOM
value
ratio_NRZPC_IT_I2 = var_NRPZC_IT_I2(pos_max_NRPZC);     % IT/I2 optimum relation

% I1/I2 relation
ratio_NRPZC_I1_I2 = (ratio_NRZPC_IT_I2 - 1);

%% CURRENT BUFFER: CB %%
% IT/I2 relation array %
var_CB_IT_I2 = relation_down_limit:0.001:relation_upper_limit;

% FOM calculation %
Wgbw_Wgbwi = sqrt(1+(4/tand(phi)))-1;
Wgbwi_Wgbw = 1/Wgbw_Wgbwi;

FOM_CB = sqrt((var_CB_IT_I2-1-(var_CB_IT_I2-
1).*((tand(phi)*Wgbwi_Wgbw)/(tand(phi)*Wgbwi_Wgbw+1))).*((Cload*QFG_flag)/(Wgbwi_
Wgbw*CAC))./var_CB_IT_I2;

% Search the optimum value %
max_FOM_CB = max(FOM_CB);                  % Maximum value of the FOM
pos_max_CB = find(FOM_CB == max_FOM_CB);   % Position of the maximum FOM value
```

```
ratio_CB_IT_I2 = var_CB_IT_I2(pos_max_CB); % IT/I2 optimum relation

% I1/I2 relation
ratio_CB_I1_I2 = ratio_CB_IT_I2-1-(ratio_CB_IT_I2-
1).*((tand(phi)*Wgbwi_Wgbw)/(tand(phi)*Wgbwi_Wgbw+1));

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%% GRAPHIC OF THE FOMs: NR - NRPZC - CB %%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% FOMs graphics %
plot(var_NR_IT_I2,FOM_NR,'linewidth',1);
hold on
plot(var_NRPZC_IT_I2,FOM_NRPZC,'linewidth',1);
hold on
plot(var_CB_IT_I2,FOM_CB,'linewidth',1);
title('Figures of Merit')
xlabel('I_T/I_2')
ylabel('FOM')
legend('MCNR','MCPZC','CBC');
grid on
grid minor
hold off

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%% FOMs CALCULATION: VB (PARTICULAR CASE) %%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%% VOLTAGE BUFER: VB %%
var_VB_IT_I2 = linspace(2.7,2.8,1000);
var_VB_IC_I2 = linspace(0.01,0.1,1000);

[VB_IT_I2,VB_IC_I2] = meshgrid(var_VB_IT_I2, var_VB_IC_I2);
FOM_VB = sqrt((VB_IT_I2-1-VB_IC_I2).*(Cload/(CA*tand(phi)))))./VB_IT_I2;

% Search the max value and the position x,y
[Zmax_VB,Idx_VB] = max(FOM_VB(:));
[ZmaxRow_VB,ZmaxCol_VB] = ind2sub(size(FOM_VB), Idx_VB);

% Search the optimum values %
ratio_VBC_IT_I2 = var_VB_IT_I2(ZmaxRow_VB); % IT/I2 optimum relation
ratio_VBC_IC_I2 = var_VB_IC_I2(ZmaxCol_VB); % IC/I2 optimum relation

% I1/I2 relation
ratio_VBC_I1_I2 = ratio_VBC_IT_I2 - 1 - ratio_VBC_IC_I2;

% Represent the graphic
surf(VB_IT_I2,VB_IC_I2,FOM_VB);
title('Figure of Voltage Buffer')
xlabel('I_T/I_2','FontSize',11)
ylabel('I_C/I_2','FontSize',11)
zlabel('FOM','FontSize',11)
axis on
grid minor
box on
```

APPENDIX D: FIGURE OF MERIT CALCULATOR V1 SCRIPT

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%% FIGURE OF MERIT CALCULATOR V1 %%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%{
    # Description of the Script:

In this script, the FOMs and FOML are calculated using the S.R.+,
S.R.-, the GBW, the IT and the Cload.
%}

%% VARIABLES %%
SR_pos = 66.17;     % Positive Slew Rate
SR_neg = -343.05;   % Negative Slew Rate
GBW = 70.49;        % Gain Band-Width product
IT = 149.1+1497;    % Total first and second stage current consumption
Cload_pF = 40;      % Load capacitance

%% FOMs (MHz·pF/mA) %%
FOM_S = ((GBW/1.0e3)*Cload_pF)/(IT/1.0e6);

%% FOML (V·pF/µs·mA) %%
FOM_L = ((((SR_pos/1e3)+(-1)*(SR_neg/1e3))/2)*Cload_pF)/(IT/1e6);


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%% FIGURE OF MERIT CALCULATOR V2: I1/I2 %%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%{
    # Description of the Script:

In this script, the FOMs will be calculated using the relation between the
I1 and I2, or that is the same, the current mode approach.

The FOM results will be de-normalized respecto I2.
%}

%%%%%%%%%%%%%%%%%%%%
%%%% VARIABLES %%%%
%%%%%%%%%%%%%%%%%%%%
n = 1.5;           % Slope factor
Vt = 26e-3;        % Thermal voltage
phi = 60;         % Phase margin
Cload = 40e-12;   % Load capacitance
CA =  264e-15;   % Total output first stage capacitance
CAC = CA;         % Total output first stage capacitance
I1 = 150e-9;      % First Stage Current Bias
I2 = 467.3e-9;     % Second Stage Current Bias
gm1 = I1/(n*Vt);   % Filrst Stage Transconductance
gm2 = I2/(n*Vt);   % Second Stage Transconductance
QFG_Flag = 2;

%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%% FOMs CALCULATION %%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%
%% NULLING RESISTOR: NR %%
FOM_NR = (1/(2*pi))*(1/(((gm1/gm2)+1)*tand(phi)))*1e3*QFG_Flag;
```

```
%% NULLING RESISTOR POLE-ZERO CANCELATION: NRPZC %%
FOM_NRPZC =
(1/(2*pi))*((2*QFG_Flag)/(((gm1/gm2)+1)*tand(phi)*(1+sqrt(1+4*((gm2*QFG_Flag)/gm1
)*Cload/(CA*tand(phi))))))*(Cload/CA)*1e3;

%% VOLTAGE BUFFER: VB %%
FOM_VB =
(1/(2*pi))*((sqrt(((gm1*QFG_Flag)/gm2)*(1/tand(phi))*(Cload/CA)))/((gm1/gm2)+1+sq
rt(((gm1*QFG_Flag)/gm2)*tand(phi)*(CA/Cload))))*1e3;

%% CURRENT BUFFER: CB %%
Wgbw_Wgbwi = sqrt(1+(4/tand(phi)))-1;
Wgbwi_Wgbw = 1/Wgbw_Wgbwi;

FOM_CB =
(1/(2*pi))*(sqrt((((gm1*QFG_Flag)/gm2)*Wgbw_Wgbwi*Cload)/CAC)/((gm1/gm2)*(1+(tand
(phi)*Wgbwi_Wgbw))+1))*1e3;
```

APPENDIX E: GAIN-BANDWITH AND FOM CALCULATOR SCRIPT

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%% GAIN-BANDWITH AND FOM CALCULATION %%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%{
    # Description of the Script:

In this script, the GBW product will be calculated, as well as the two FOMs
descibed in the memory.
- FOMs = (MHz·pF/(mA/V)
- FOMs = (MHz·pF/(mA)
%}

%%%%%%%%%%%%%%%%%%%%
%%%% VARIABLES %%%%
%%%%%%%%%%%%%%%%%%%%
phi = 60;          % Phase margin
n = 1.5;           % Slope factor
Vt = 26e-3;        % Thermal voltage
ro1 = 149.00e6;    % Output resistance of the first stage
Cload = 40e-12;    % Load capacitance
CA = 226e-15;      % Total output first stage capacitance
CAC = CA;          % Total output first stage capacitance
I1 = 150e-9;       % First Stage Current Bias
I2 = 150e-9;      % Second Stage Current Bias
gm1 = I1/(n*Vt);   % Filrst Stage Transconductance
gm2 = I2/(n*Vt);   % Second Stage Transconductance
Gmn = gm1/gm2;     % Transconductance relationship
QFG_Flag = 2;      %2

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%% GBW VALUE CALCULATION  %%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%% NULLING RESISTOR: NR %%
Cc_NR = (gm1/(gm2*QFG_Flag))*Cload*tand(phi);
GBW_NR = gm1/(2*pi*Cc_NR);

FOM_NR_1 = ((GBW_NR/1e6)/((gm1+gm2)*(1e6/1e3)))*Cload*1e12;
FOM_NR_2 = ((GBW_NR/1e6)/(((I1+I2)*1e9)/1e6))*Cload*1e12;
```

```
%% NULLING RESISTOR POLE-ZERO CANCELATION: NRPZC %%
Cc_NRPZ =
(gm1/(gm2*QFG_Flag))*(tand(phi)/2)*(1+sqrt(1+4*(Cload/(CA*(gm1/(gm2*QFG_Flag))*ta
nd(phi)))))*CA;
GBW_NRPZ = gm1/(2*pi*Cc_NRPZ);

FOM_NRPZ_1 = ((GBW_NRPZ/1e6)/((gm1+gm2)*(1e6/1e3)))*Cload*1e12;
FOM_NRPZ_2 = ((GBW_NRPZ/1e6)/(((I1+I2)*1e9)/1e6))*Cload*1e12;

%% VOLTAGE BUFFER: VB %%
Cc_VB = sqrt((gm1/(gm2*QFG_Flag))*Cload*CA*tand(phi));
gmVB = (gm2*Cc_VB)/Cload;
IVB = gmVB*n*Vt;
GBW_VB = gm1/(2*pi*Cc_VB);

FOM_VB_1 = ((GBW_VB/1e6)/((gm1+gm2+gmVB)*(1e6/1e3)))*Cload*1e12;
FOM_VB_2 = ((GBW_VB/1e6)/(((I1+I2+IVB)*1e9)/1e6))*Cload*1e12;

%% CURRENT BUFFER: CB %%
Wgbw_Wgbwi = sqrt(1+(4/tand(phi)))-1;
Wgbwi_Wgbw = 1/Wgbw_Wgbwi;

Cc_CB = sqrt((gm1/(gm2*QFG_Flag))*Wgbwi_Wgbw*CAC*Cload)-
(Cload/(2*(gm2*QFG_Flag)*ro1));
gmCB = tand(phi)*Wgbwi_Wgbw*gm1;
ICB = gmCB*n*Vt;
GBW_CB = gm1/(2*pi*Cc_CB);

FOM_CB_1 = ((GBW_CB/1e6)/((gm1+gm2+gmCB)*(1e6/1e3)))*Cload*1e12;
FOM_CB_2 = ((GBW_CB/1e6)/(((I1+I2+ICB)*1e9)/1e6))*Cload*1e12;
```