Silicon Integrated Subharmonic Mixer on a Photonic-Crystal Platform

Alicia E. Torres-García, José M. Pérez-Escudero, Jorge Teniente, Ramón Gonzalo, *Member*, IEEE, Iñigo Ederra, *Member*, IEEE

Abstract—**This paper presents a planar silicon integrated subharmonic mixer on top of a photonic-crystal platform. The local oscillator (LO) power is injected through a 2D photonic-crystal (PC) slab to a resonant cavity that effectively couples the signal to a planar bow-tie antenna. The same antenna, which is printed on the top of the PC cavity, contains an antiparallel Schottky diode pair which performs the down-conversion. The proposed design is a simple, easy to integrate, low cost, low profile device. Moreover, the described fabrication process is compatible with active components integration. The performance of the design has been experimentally demonstrated showing good agreement with the simulation and is comparable with the state-of-the-art of planar mixers. The work presented here is based on concepts and technologies from electronics and photonics domains and may be a good starting point for the creation of new devices, allowing the integration and upgrading of existing techniques from both worlds.**

Index Terms—**Photonic Crystal, Silicon Integration, Subharmonic Mixer, Planar, Terahertz Silicon Platform.**

I. INTRODUCTION

THe terahertz band has remained underdeveloped for many years, in between the well-established highest frequency microwave technologies and the well-developed optical engineering of infrared detectors. However, recent breakthroughs in fabrication processes and progress in electronic and photonic technologies have boosted the terahertz field. For high resolution applications, where high sensitivity to resolve spectral lines is required, sub-mm heterodyne receivers have proved to be the best solution. This is the case of many planetary remote sensing applications, chemistry and biological spectral marker detectors and new medical imaging applications [1]–[8]. However, most of the implemented devices consist of either a single pixel or arrays based on stacked machined metallic waveguide housing modules. The development of large multi-pixel heterodyne arrays is still a challenge, limiting the mapping ability and scanning velocity of these systems. Recent research works have shown some promising results [9]–[11]. Nevertheless, they are based on either bulky structures or multilayer silicon structures, where

Alicia E. Torres-García, Jose M. Perez-Escudero, Jorge Teniente, Ramón Gonzalo and Iñigo Ederra are with the Department of Electric, Electrical and Communications Engineering, Public University of Navarra, Pamplona, Navarra, 31006 Spain. Jorge Teniente, Ramón Gonzalo and Iñigo Ederra are also with the Institute of Smart Cities, Universidad Pública de Navarra, Pamplona, Navarra, 31006 Spain. e-mail: (aliciaelena.torres@unavarra.es; jose-manuel.perez@unavarra.es; jorge.teniente@unavarra.es; ramon@unavarra.es; inigo.ederra@unavarra.es).

the fabrication and alignment requirements increase exponentially with the frequency up scaling (dimensions down scaling). Thus, high level component integration with efficient LO power distribution and coupling are key factors in the development of new heterodyne detectors.

Recently, several studies dealing with electronic devices on silicon-based platforms have been reported as an alternative for highly integrated devices. The basic concept behind these studies comes from the photonics domain, where optical waveguides based on Silicon-on-Insulator (SOI) technology, including optical Photonic-Crystal (PC) waveguides, have been widely investigated [12]. In this context, high-resistivity silicon (HR–Si) has been successfully used as an efficient platform for passive PC-based devices at terahertz frequencies, namely, dielectric PC waveguides [13]–[15], diplexers for integrated communication circuits [16] and high Q-factor resonators for sensing [17]. One step further has been done for PC integration with active components. In [18], a Resonant-Tunneling Diode (RTD) chip was mounted directly onto a PC waveguide where evanescent coupling takes place, resulting in coupling efficiency lower than 0.1 %. The same research group presented a RTD detector attached to a PC waveguide connected to a THz fiber demonstrating a 10 Gbit/s error-free data rate communication at 300 GHz [19]. In order to improve mode and impedance matching between the RTD and the PC waveguide, a tapered-slot mode converter printed on an external InP substrate connected to the RTD was used. This showed coupling efficiency higher than 90 % with 50 GHz 3-dB bandwidth and achieved real-time error-free data transmission at 32 Gbit/s [20]. In all these approaches, the coupling element and the output lines (read-out lines) were fabricated as separated components and then, welded or attached to the PC slab.

The presented study addresses the design and implementation of a silicon integrated subharmonic mixer on a PC platform. A PC waveguide terminated in a high Q-factor resonant cavity is created in the silicon to inject the LO signal. A bow-tie antenna (which contains the mixer Schottky diode flip-chip) is printed on the top of the PC cavity and optimized for high coupling. In previous works several mixer configurations using PC substrates were proposed [21], [22]. However, in both cases the PC was used to improve the radiating performance of the radiating element, a dipole antenna. The LO injection was based on a conventional waveguide [21] or quasi-optically fed through the PC [22], with low efficiency.

A recent research proposed a metallic waveguide-input three terminal RTD fundamental mixer based on a PC waveguide

platform operating at 0.3 THz [23]. The device demonstrated 20 dB conversion loss and >10 Gbit/s error-free transmission operating as coherent THz receiver. However, it exhibited low RF-LO isolation (6 dB) and required external bias. In our proposed design, the LO distribution uses the PC guiding possibilities and leads to several improvements. Firstly, although a single-pixel approach is presented, the design can be easily extended into a 2D multi-pixel array. PC waveguides have shown very high transmission even in very sharp bends [24]. Therefore, a low-loss LO distribution network is fully feasible with PC waveguides. Additionally, high RF-LO and RF-IF isolation can be achieved. Lastly, this technology dispenses the use of high precision milling metal housing-blocks which increase the cost and weight of the system.

The contents of this work are organized as follows. First, the general configuration of the proposed subharmonic mixer is presented in Section II. The study and design of a PC silicon platform consisting of a PC waveguide and a PC cavity can be found in Section III. Afterwards, in Section IV, the mixer topology is analysed in terms of the optimum embedding impedances required to obtain the minimum achievable CL. In Section V, the planar antenna is simultaneously optimized for coupling with the LO signal and the RF radiation, while being impedance matched to the anti-parallel diodes. Finally, the fabrication, assembly and measurement of the prototype in terms of noise temperature and conversion loss are detailed in Section VI.

II. GENERAL CONFIGURATION

The 3D view of the proposed approach can be seen in Fig. 1. It consists of an antiparallel Schottky diode (APD) pair connected to a double bow-tie antenna and a coplanar stripline (CPS) filter, which provides the Intermediate Frequency (IF) output. The subharmonic mixer circuit is printed on a silicon dioxide (SiO_2) membrane on top of a PC silicon slab. The Local Oscillator (LO) signal is guided within the PC waveguide and coupled to the diodes through the bowtie antenna that is located on top of a PC cavity. The same printed antenna collects the RF signal coming from the air or from an external quasi-optical element (e.g. silicon lens). The LO port corresponds to a WR-08 rectangular waveguide that is connected to the PC waveguide by a linear transition. The proposed prototype is optimized to operate at LO frequency (f_{LO}) around 100-105 GHz and RF frequency (f_{RF}) bandwidth from 200-220 GHz; which lead to IF output frequencies (f_{IF}) around 0-15 GHz (*i.e.* $f_{IF} = |(f_{RF} - 2f_{LO})|$).

III. SILICON PHOTONIC-CRYSTAL PLATFORM

The first step in the silicon integrated mixer design is the Photonic-Crystal study. Photonic-Crystals are artificial periodic structures where the periodicity can be defined in one, two, or three orthogonal directions. If the wavelength of the incident wave is in the same order of magnitude of the periodicity, and the difference between dielectric constants is high enough, a frequency range where the propagation is impossible (i.e. a photonic band gap) can happen in certain directions for certain polarizations [12].
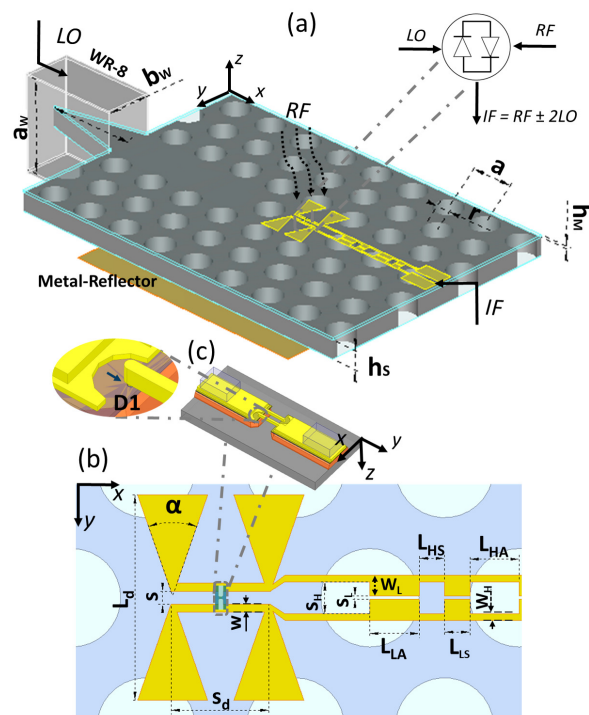

Fig. 1: (a) 3D perspective view of the silicon integrated subharmonic mixer and (b) its top view with (c) detail of the APD ports and epitaxial layers.

2D PC waveguides can be constructed by creating defects in a row (e.g. removing cylinders, changing their radius . . .) of a 2D PC slab [25]. The waveguide behaviour is obtained by the combination of guiding in the crystal periodicity plane with index confinement in the vertical direction, provided by total internal reflection. These 2D PC waveguides have gained large attention in the last years and have enabled the development of complex Photonic Integrated Circuits (PICs). [13], [26], [27].

The design of the line defect Photonic-Crystal waveguide, which will serve to guide the LO signal in the mixer, begins with the study of a PC structure with a band gap in the desired frequency range. Furthermore, the index contrast between the dielectric and the air must be large enough to guarantee confinement of the waves in vertical direction. In our work, high resistivity silicon is used as platform. It has been chosen because of its very low losses, easy etching, and maturity of silicon devices fabrication and integration in active devices.

From [28], the maximum thickness of an slab satisfying the single mode condition is:

$$h_m = \frac{\lambda_0}{2\pi} \frac{1}{\sqrt{n^2 - n_2^2}} \left[\pi + \arctan \frac{\sqrt{n_2^2 - n_1^2}}{\sqrt{n^2 - n_2^2}} \right] \quad (1)$$

where λ_0 is the free space wavelength, n is the refraction index (RI) of the guiding layer, n_1 and n_2 are the RI of the upper and lower cladding, respectively. The use of a cladding is almost imperative in photonics, where single mode slabs are very thin and, besides, supports for the structures are needed. On the contrary, scaling this technology to the sub-mm range allows using thicker slabs, which can be used as self-supported
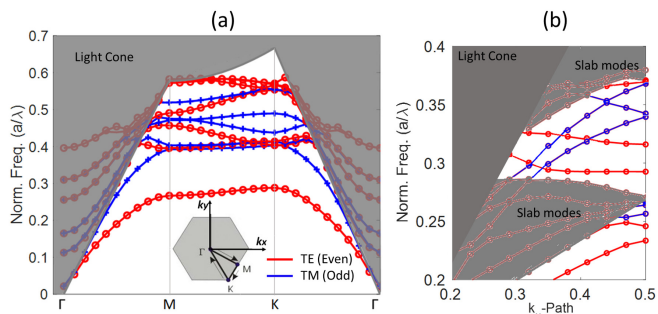
Fig. 2: (a) Band diagram for a hexagonal lattice of air cylinders in silicon ($\varepsilon_r = 11.67$, $r = 0.33a, h_s = 0.43a$) for TE-like (red lines) and TM-like (blue lines) polarizations. The inset shows the irreducible Brillouin zone. The light grey color highlights the region outside the light cone. (b) Dispersion diagrams of TE-like (red lines) and TM-like (blue lines) modes of a 7x1 supercell in the line defect PC slab. The clear grey regions correspond to the slab bands.
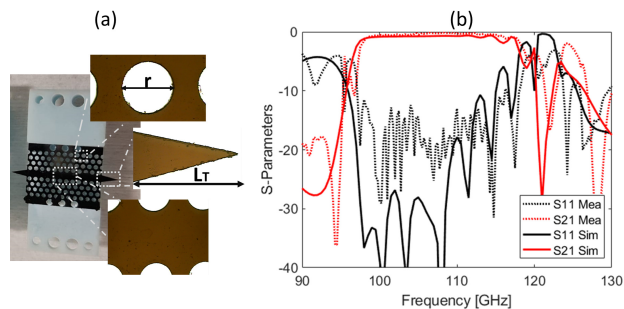

Fig. 3: (a) Photograph of the back-to-back WR-08 waveguide excited line defect PC waveguide, with detail of the linear taper, the holes and the waveguide channel. (b) Comparison between the predicted and measured response of the back-to-back transition.

structures. From (1), the maximum thickness, h_{max}, for single mode operation up to 105 GHz is 418 μm. Thinner slabs will provide weak wave confinement (i.e. the guided mode will be very close to the light cone) and thicker slabs generate higher order modes, which can eliminate the band-gap. Thus, a commercial 400 μm thick silicon slab was selected.

A. Photonic-Crystal Design

The selected periodic structure is formed by air holes etched in a silicon slab ($\varepsilon_r = 11.67$) and arranged in a 2D periodical hexagonal lattice, with lattice constant a. A silicon dioxide membrane ($h_m = 0.003a$) is placed on the top and bottom faces of the silicon slab (see Fig. 1). The band diagram for the PC slab was obtained with the Plane Wave Expansion (PWE) solver of the commercial solver OptiwaveFDTD15 (see Fig. 2(a)). For the analysis, the silicon slab was embedded in a $7a$ air box. The slab is in the xy-plane and the direction normal to the slab is z. With these coordinates, TE-like modes are those in which E_x, E_y and H_z are the dominant field components, whereas TM-like modes are those in which H_x, H_y, and E_z are the dominant field components. The dispersion diagram shows a band-gap for TE-like modes (even modes) from 0.28 to 0.4 normalized frequency. The selected radius of the air cylinders (r) and the slab thickness (h_s) are $0.33a$ and $0.43a$ respectively.

B. Photonic-Crystal Waveguide

Once we have a structure with a band gap, a row of air cylinders is completely removed from the 2D lattice plane to create a channel, which will act as a waveguide [29]. Due to the introduced perturbation, defect states are created. If these states fall within the band gap, the periodic structure around the guiding channel will provide field confinement in the waveguide in the 'xy'- plane in this frequency range [12]. The field confinement in the vertical direction is achieved by total internal reflection at the silicon-air interface.

For evaluation of the line defect, the PC waveguide dispersion diagram was computed using a 7×1 supercell, Fig. 2 (b). New guided modes appear within the frequency band gap of the original PC. The TE-like mode bandgap is sufficient to confine these guided modes in the waveguide. In our case, only TE modes of the line defect waveguide will be excited, and they will not couple to the TM_z modes of the Photonic-Crystal structure due to field mismatch.

A back-to-back structure (Fig. 3(a)) was designed to evaluate the performance of the PC waveguide. To this aim, a transition from rectangular metallic waveguide to PC waveguide will be used. By means of this transition, the fundamental mode of a rectangular waveguide (TE_{10}) excites the dominant field components of TE-like modes in the PC waveguide. The silicon slab must be aligned with the rectangular waveguide E-Plane and a linear taper was created in the silicon slab to improve the coupling and matching. In addition, it helps to align and fit the PC waveguide and the WR-08 waveguide aperture. The silicon taper length (L_T) was optimized and the resulting optimum length was found to be 2.5 mm and its width 930 μm. With these dimensions, the fundamental mode of the metallic waveguide is adiabatically coupled to the PC waveguide mode, entailing low insertion losses and return losses higher than 29 dB in the LO frequency range (see Fig. 3). The lattice constant a is chosen to be 930 μm, i.e. $0.33\lambda_0$ at 105 GHz. This will be the frequency for the LO signal. The air cylinder radius are $r = 306$ μm ($0.33a$), the total length of the analysed PC waveguide is 11.16 mm ($12a$) and the total width of the slab is 7.9 mm ($8.5a$). Finally, the HR-Si slab is 400 μm thick and its parameters are: $\varepsilon_r = 11.67$ and $\rho \simeq 10^4$ $\Omega - cm$.

The back-to-back transition from WR-08 waveguide to PC waveguide was fabricated and measured at the Public University of Navarra's facilities. The manufacturing procedure is described in Section V. An Agilent PNA-X N5242A Microwave Network Analyser with two OML F-Band VNA Extenders were used for the characterization. The measured transmission and reflection coefficients, presented in Fig. 3(b), show very good agreement with respect to the predictions, calculated with Ansys HFSS. There is a transmission band
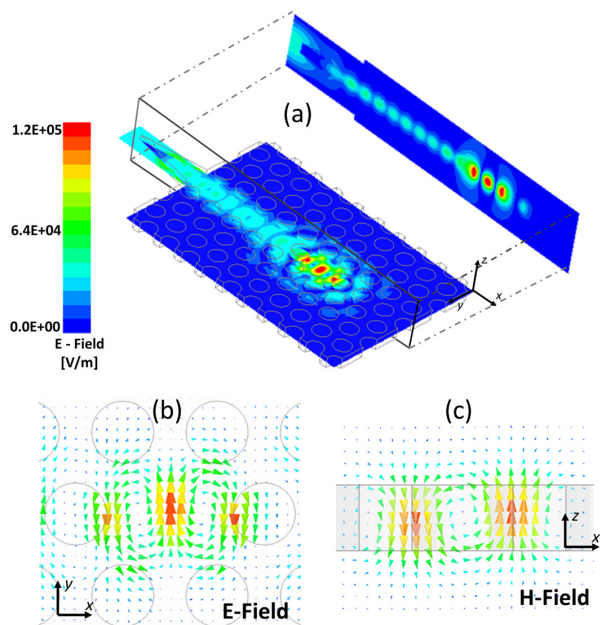
Fig. 4: (a) E-Field distribution in the PC waveguide coupled with the PC resonant cavity at 105 GHz. (b) Vector E-Field in the xy-equatorial plane (middle of the slab), (c) Vector H-Field in the xz-meridian plane of the cavity.
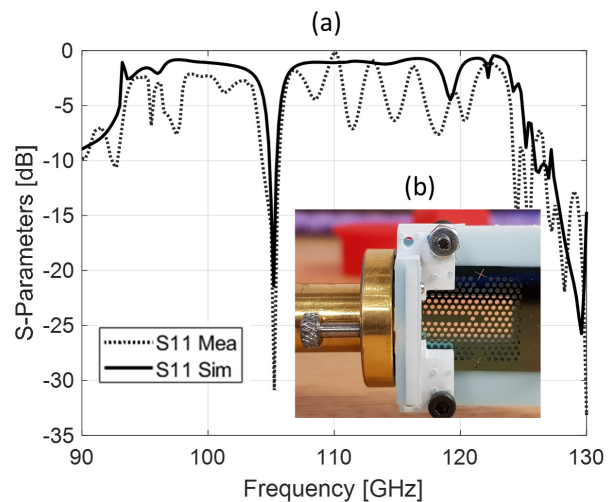

Fig. 5: (a) Comparison of the simulated and measured return loss of the PC cavity. (b) Inset with the photograph of the fabricated structure connected to the WR-08 metallic waveguide.

with about 18 % fractional bandwidth (from 98 to 117 GHz) which corresponds to the transmission in the 0.3 to 0.37 band of normalized frequencies (Fig. 2 (b). The losses associated with the PC waveguide were estimated as 0.64 dB/cm from simulation whilst the transition from WR-08 to PC waveguide contributes with 0.005 dB. The losses of the evanescent modes above the light line are not appreciated in the transmission response due to the relatively short length ($\sim 3\lambda_0$) of the PC waveguide. Similar behaviours has been reported in [14], [30]. Note also that since the PC waveguide is intended for LO injection, narrow band is required. Therefore, even if a longer waveguide were required it would be broadband enough to accommodate the LO signal.

C. Photonic-Crystal Cavity

Reported studies in the state-of-the-art of PC integration with active components highlight that the current challenge lies in mode and impedance matching between the active device and the photonic waveguide for maximum coupling efficiency [26]. Here, we propose a solution, which allows the whole receiver front-end integration in the same substrate with a high coupling efficiency, while preserving planarity and guaranteeing compatibility with active semiconductor device fabrication.

In order to effectively couple the LO signal, guided through the PC waveguide, to the mixer diodes, the found solution was based on the design of a PC resonant cavity, which will be fed by the PC waveguide. The PC cavity was obtained by removing one air cylinder as is shown in Fig. 4(a). This cavity is separated from the PC waveguide by one hole.

By doing this, we introduce a new defect state in the PC where the field will be highly resonant. The E-Field distri-

bution at the resonant frequency (105 GHz) of the proposed PC cavity can be seen in Fig. 4(a). The field distribution of the resonant response must be studied in detail to find the ideal planar antenna shape and orientation. The vector field distribution, for the E and $H-$planes can be seen in Fig. 4 (b and c).

The observed field corresponds to the $HEM12\delta$ mode in a resonant dielectric cylindrical cavity. From the theory of dielectric resonant cavities [31], the first index denotes the number of full-period field variations in azimuthal direction, and the second one the number of radial variations. In classical waveguide cavities, the third index is used to denote the number of half-wavelength variations in the axial direction of the waveguide. Here, the third index, δ, denotes the fact that the dielectric resonator is shorter than one-half wavelength. This resonance will be used to couple the LO signal to the mixer.

To verify the performance of the PC cavity, a prototype was manufactured and tested. A plastic housing jig that ensures alignment between the metal waveguide and the PC waveguide was 3D-printed. The inset in Fig. 5(b) shows the assembled device connected to the metallic flange of the WR-08 waveguide for the return loss measurement. The measured return losses, presented in Fig. 5 (a), exhibit very good agreement with the simulations. A resonant peak, with return loss higher than 20 dB at 105 GHz can be seen. This resonance frequency will be selected for the LO injection to the mixer.

IV. MIXER TOPOLOGY

The general overview of the proposed mixer was introduced in Section II. An antiparallel Schottky-diode pair (ADP) is the selected mixing element and will be placed in the centre of the PC resonant cavity, connected to a planar antenna. It is known that if integrated diodes are used, better performance can be achieved, especially when the operating frequency increases. However, for this proof of concept prototype VDI SC1T2-D20
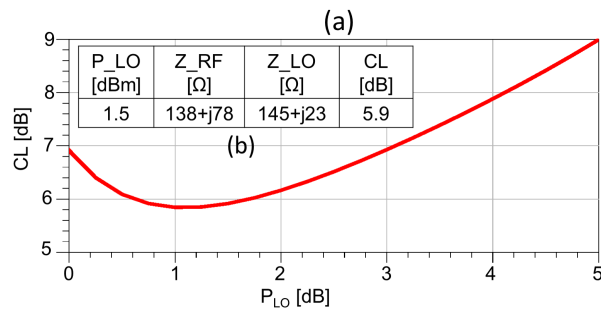
Fig. 6: (a) Conversion Loss vs LO input power for the impedance values listed in (b). These were obtained with $P_{LO} = 1.5$ dBm and $P_{RF} = -30$ dBm.

Fig. 7: (a) CPS line running on the PC platform. (b) CPS step impedance filter on the PC platform. (c)S-parameters of the CPS line (black) and step impedance filter (red) on the PC silicon substrate.

[32] discrete diodes have been used. Their main characteristics are: saturation current I_s= 0.2 fA, series resistance R_s= 13 Ω, ideality factor $\eta = 1.3$, zero voltage junction capacitance C_{jo}= 1.3 fF and forward voltage V_j= 0.73 V.

The mixer performance was optimized in terms of conversion loss by the load-pull technique and the optimum embedding impedances at LO and RF frequencies were obtained. The HB parameters used for the simulation are: $f_{LO} = 105\ GHz$, $f_{RF} = 215\ GHz$ and $f_{IF} = 5\ GHz$ ($f_{RF} - 2 * f_{LO}$). Likewise, the employed powers are: $P_{LO} = 1.5$ dBm and $P_{RF} = -30$ dBm. The optimum mixer conversion losses vs LO power can be seen in Fig. 6(a), where the best RF and LO impedance values from the Load-Pull simulations, which are listed as an inset in Fig. 6(b), were employed. Thus, these impedances will be our design goal for the whole assembled mixer.

This study only considers the internal parameters of the diodes. Therefore, in order to take into account the 3D full diode model in our design (which means including the parasitic impedance in the simulation), all the diode epitaxial layers and packaging structures are included in the HFSS full-wave simulation in a realistic environment, as can be seen in Fig. 1. The 3D-model for the VDI antiparallel Schottky diodes have been previously created by our group and can be found elsewhere [33]. Besides, a thin layer of silver epoxy (EPOTEK H20E) which will be used to weld the diodes is also included. Finally, it should be noted that the diode structure represents a small portion of the entire simulated structure. Accordingly, a mesh resolution of 0.01 μm was imposed for the air finger environment and 0.1 μm for the rest of the diode layers in HFSS to ensure an accurate simulation that takes into account the main parasitic impedances and coupling effects.

A. Filter Design

The low-pass filter is an essential component in the mixer. It must provide high rejection for the LO and RF frequency bands and allow adjusting the diode embedding impedance. In our design the filter runs on the PC substrate. However, when placing the CPS lines on the PC substrate, an abrupt impedance change is obtained due to the change in the dielectric permittivity between the dielectric and air regions. Therefore, the line by itself will act as a low-pass filter, due
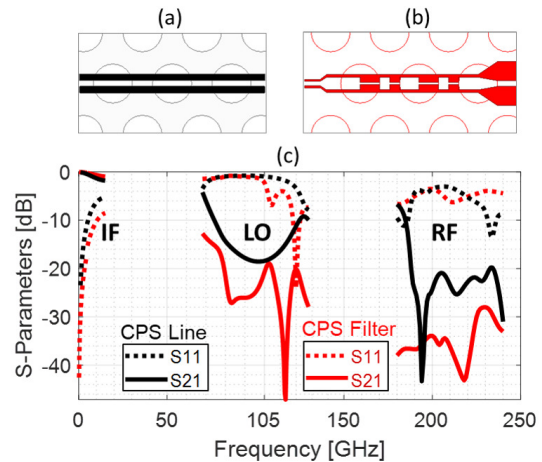
to the high/low impedance sections and its stop frequency band will depend on the PC periodicity and parameters. A CPS line as the one shown in Fig. 7(a), where the width of the metallic strips is 90 μm and the separation is also 90 μm, was simulated in HFSS and the obtained S-Parameters can be seen in Fig. 7 (c) (black lines). In such CPS line, alternate high/low impedance zones with lengths of 316 μm and 614 μm are formed with corresponding impedances of 105 Ω and 6Ω (derived at 100 GHz using ADS [34]). It can be seen that this structure inherently rejects frequencies around 100 GHz and 200 GHz, which are the LO and RF frequency bands. Finally, we designed a more complex low-pass filter by combining the intrinsic filtering property of the PC with a conventional CPS step impedance filter (see Fig. 7 (b)). The main dimensions of the new filter are listed in Table I (see Fig. 1(b) for clarification).

From the S-Parameters simulations shown in Fig. 7 (c) (red lines), the step impedance filter successfully rejects the LO and RF frequencies, presenting higher rejection than the simple CPS line for both bands although, above 105 GHz it presents higher losses. Furthermore, the IF frequencies are better transmitted in the improved CPS filter.

B. Antenna Design

The core of an integrated planar receiver is the planar antenna and the antenna-mixer matching. The coupling efficiency between the planar antenna and the incoming radiation is the first loss the signal encounters in the receiver, which contributes directly to the receiver noise figure (noise temperature in radiometry) [35]. This topic has been extensively studied and a very good solution has arisen thanks to the use of dielectric lenses. High dielectric lenses offer a solution for the undesired surface wave mode excitation and may increase the antenna gain by a n^2 factor, where n is the refractive index. Lens antennas with high gain (> 30 dB) over larger bandwidth (> 20 %) can be found in [36]–[38]. However,

this kind of antennas presents the disadvantage of having low aperture efficiency. A recent solution can be found in leaky-wave antennas (LWA) employed as lens illuminator. Thus, very high aperture efficiencies and gaussianity up to 1.9 THz have been reported [11], [39], [40]. Nevertheless, not much work has been found oriented to optimizing the antenna-mixer matching and the LO coupling in a planar configuration as is the one presented here. Therefore, the simultaneous RF and LO matching in the planar heterodyne mixer is the matter that will focus the major efforts in this research.

Most of the reported research about integrated planar mixer and detectors are based in Coplanar waveguide transmission lines (CPW). With this technology, slot antennas are the most natural solution. These antennas radiate mainly towards the substrate side where usually a high dielectric constant lens is integrated. The advantage of using CPW technology over microstrip or coplanar stripline (CPS) in those designs is out of discussion. Nevertheless, in our proposed approach, a ground plane cannot be used. Another look into the field distribution at the resonant frequency in the PC cavity (Fig. 4) indicates that the E-Field is parallel to the slab and is not zero at the silicon-air interface. Therefore, the proposed design will be based on CPS technology.

In this planar integrated antenna mixer design, several factors must be taken into account. The geometry and orientation of the antenna must serve a double function. The first one is to effectively couple the LO signal from the cavity to the non-linear mixing element, namely the Schottky diodes. The second one is to couple the incoming RF signal to the same mixing element. The Load-Pull analysis in Section IV shows that the selected antenna should present an inductive performance for both LO and RF frequencies to compensate the diode intrinsic capacitive behavior. Therefore, the simultaneous RF and LO matching in the planar heterodyne mixer will be discussed.

Different printed dipole based antennas were studied keeping in mind all the condition previously explained. The resonant length of a half-wave printed dipole on a $0.14\lambda_0$ thick substrate (ϵ_r=10) is around $0.19\lambda_0$, while the full-wave resonance happens around $0.31\lambda_0$ [41]. The input impedances are about 25 and 150 Ω for a half-wave and full-wave dipole, respectively. Therefore, by choosing these dipole lengths, matching for LO and RF frequencies cannot be simultaneously obtained, since the load-pull analysis determines that the embedding impedance must be higher than 100 Ω and present an inductive component. Nevertheless, for a full-wave resonant length at LO frequency, the RF resonance (around twice the LO) also exhibits high impedance values.

The bow-tie printed antenna is a natural modification of dipole antennas and is commonly used when some specific or wider bandwidth input impedance is required. Moreover, double element antennas are usually preferred over single element antenna designs because they provide higher radiating resistance and more symmetric beam patterns, leading to higher Gaussian beam efficiency [42]. In our case, the double-bow-tie antenna was the structure that showed the impedance closest to our needs. The best results were obtained for the dimensions listed in Table I.

TABLE I: Double Bow-tie Antenna and CPS Filter Dimensions

| Parameter	Description	Design	Measured
L_d	Bow-tie length	1330 μm	1320 μm
S_d	Bow-tie separation	550 μm	545 μm
s	Feed separation	80 μm	82 μm
w	Feed width	50 μm	49 μm
α	Bow-tie angle	40 °	40 °
h_m	Membrane thickness	3 μm	3.3 μm
h_s	Substrate thickness	400 μm	401 μm
W_H	CPS High-Z sections width	40 μm	42 μm
W_L	CPS Low-Z sections width	130 μm	130 μm
s_H	CPS High-Z sections sep.	200 μm	199 μm
s_L	CPS Low-Z sections sep.	20 μm	21 μm
$L_{LA} = L_{HA}$	CPS Length of Low/High Z sections on SiO_2/Si	307 μm	306 μm
$L_{LS} = L_{HS}$	CPS Length of Low/High sections on Si/SiO_2	158 μm	159 μm
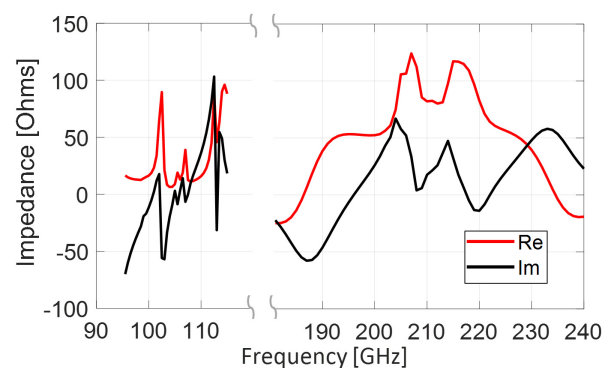
Fig. 8: Double bow-tie antenna (see Fig. 1) input impedance for the dimensions listed in Table I.

1) Input impedance: The input impedance for the final double bow-tie design can be seen in Fig. 8. For the desired RF frequencies (200-220 GHz), similar values to those obtained in the Load-Pull analysis are achieved.

2) Radiation Pattern: The radiation performance of the double bow-tie on the PC cavity was evaluated. The power radiated by the structure is divided into two parts. One part propagates into the air, whilst the other part is radiated through the substrate as can be seen in Fig. 9 (black lines) where the directivity vs frequency is shown. A back-metal reflector could be included at approximately $3/4\lambda_0@RF$ to improve the front to back radiation (it could not be placed closer not to affect the performance of the PC). With the back-metal plane, constant directivity values about 8 dB can be obtained for the RF frequency band as it is presented in Fig. 9 (red lines). Nevertheless, it must be pointed out that the insertion of the metal reflector implies an extra layer in the design and could compromise the simplicity and planarity of the prototype.

Additionally, the simulated radiation efficiency of only the double bow-tie antenna on the PC platform was also included in Fig. 9 and exhibits mean values of 85 %. The deduction of the substrate modes that do not contribute to the main radiation was included in its calculation. Furthermore, an extra simulation, taking into account the full structure of the diode, the silver epoxy material and the CPS filter was performed presenting a mean value of radiation efficiency of 43 %
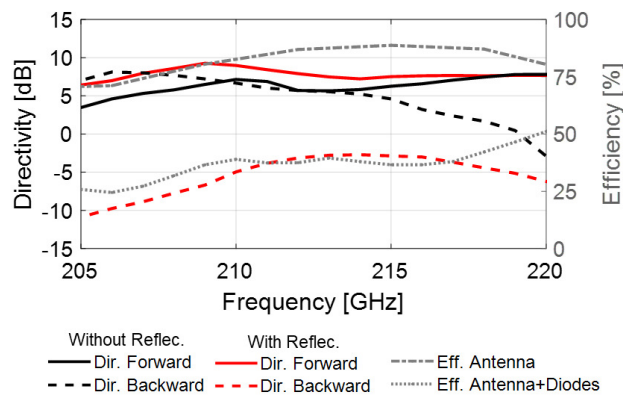
Fig. 9: Simulated directivity vs RF frequency of the double-bow-tie on top of the silicon PC cavity without and with a back metal reflector (left axis). Radiation efficiency of the double-bow-tie on top of the silicon PC cavity without and with the diode (right axis).
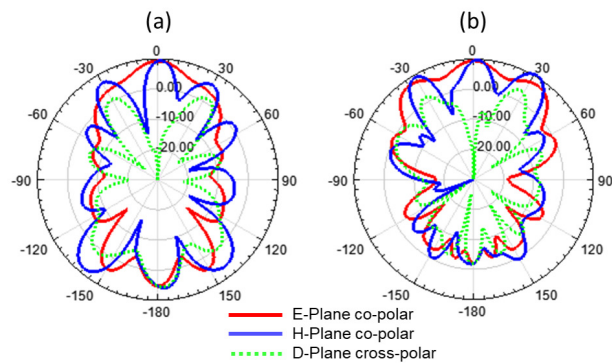

Fig. 10: Simulations of the co-polar radiation patterns in the E-plane (yz-plane) and H-Plane(xz-plane) and cross-polar in D-plane (45°-plane) according to Ludwig 3 definitions of the double-bow-tie on top of the silicon PC cavity at 215 GHz. (a) Without and (b) with a back-metal reflector.

within the RF band. The new layout contains lossy materials around the port which introduce extra losses in the design. Nevertheless, this is a more realistic simulation of the mixer radiation performance.

The co-polar radiation patterns in the E-plane (yz-plane) and H-Plane (xz-plane) and the cross-polar radiation patterns in D-plane (45°-plane) are shown Fig. 10 for $f_{RF} = 215\,GHz$. According to the employed Ludwig third definition, the diagonal plane is the one that shows the worst cross-polar level with a critical point at $\phi = 45°$ and $\theta = 45°$. Ripples due to the existence of some substrate modes can be seen, emphasized in the H-Plane where the PC is not periodical, since it corresponds the plane of the defected PC line. However, even though the PC that surrounds the antenna is not designed to work in the RF band, it decreases the effective dielectric constant and reduces the excitation of substrate modes.

3) Coupling: With this configuration, the antenna is also used to couple the LO power to the diodes. Therefore, coupling between the LO signal and diode-ports on the antenna
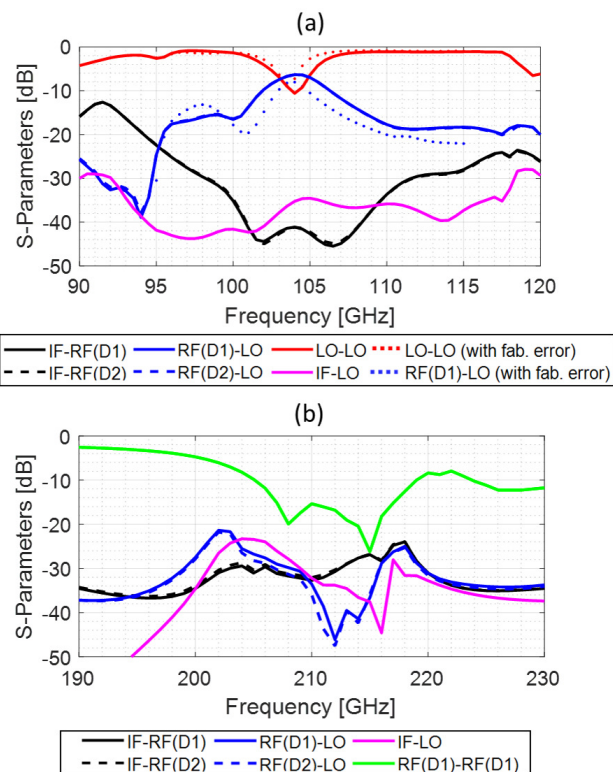

Fig. 11: Coupling and isolation between the mixer ports at the (a) LO and (b) RF frequencies.

has been studied, Fig. 11. The LO-Diode coupling obtained from the S-parameters simulation is -6.3 dB, which means that approximately 23 % of the LO power is coupled to each diode. However, it must be pointed out that the simulations include the two diode ports. Thus, the LO power is divided between both diodes. The coupling efficiency between the bow-tie and the PC waveguide (considering the coupling of both diodes) is higher than 45 %.

Furthermore, in any mixer it is necessary to have good isolation between ports. In Fig. 11 we can see both coupling and ports isolation. There is a high rejection ($\geq$ 24 dB) from the diodes to the IF output at both RF(210 GHz-230 GHz) and LO (105 GHz) frequencies. Besides, good isolation between the LO and the diodes ports (RF port) at RF frequency is achieved ($\geq$ 25 dB). Finally, the return losses of the antenna connected to the diode were obtained considering the diode impedance resulting from the non-linear analysis and are shown in Fig. 11(b) (green line). Good matching bandwidth (S11< -10 dB) is achieved from 205 to 220 GHz, with a minimum, below -20 dB, obtained around 215 GHz.

V. SILICON INTEGRATED SUBHARMONIC MIXER PERFORMANCE

The S-Parameters from the 3D full-wave simulated mixer (Fig. 1) are imported to Keysight ADS software for the Harmonic Balance (HB) analysis. The Conversion Losses (CL) and the Equivalent Noise Temperature (ENT) of the whole sub-harmonic mixer are shown in Fig. 12. The LO input power at 103.5 GHz (red lines) and 105 GHz (blue lines) has been
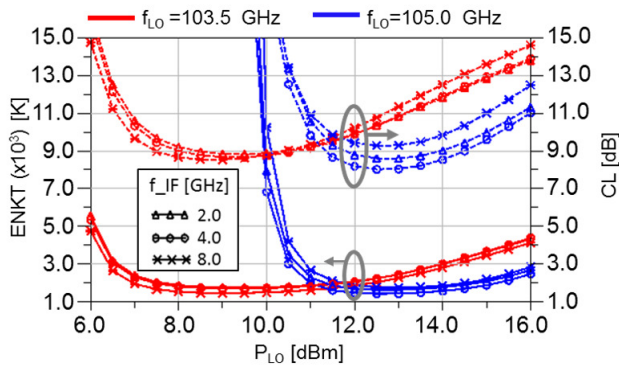
Fig. 12: Simulated Conversion Loss (CL) and Equivalent Noise Temperature (ENT) vs P_{LO} with f_{LO} = 103.5 GHz (red lines) and f_{LO} = 105 GHz (blue lines) for three IF frequencies: 2 GHz (triangular marker), 4 GHz (circle marker) and 8 GHz (cross marker). The RF power input signal was fixed to -30 dBm in all simulations.

swept from 6 dBm to 16 dBm, for different IF frequency values (namely, 2 GHz, 4 GHz and 8 GHz).

Although the PC cavity was designed to maximize coupling at 105 GHz, when the bow-tie antenna is introduced the resonance is slightly shifted to lower frequencies. That is why the best coupling is obtained for f_{LO} = 103.5 GHz which implies that lower LO power is needed to pump the diodes as can be seen in Fig. 12. We can observe that the best absolute conversion loss value, 8 dB, is achieved for $f_{LO} = 105$ GHz when the LO power is 13 dBm and $f_{IF} = 4$ GHz. Likewise, the best absolute equivalent noise temperature is 1438 K and is obtained for the same LO power and frequency values. Furthermore, for $f_{LO} = 103.5 \ GHz$, better mean CL and ENT are achieved in a wider bandwidth. Additionally, from the non-linear analysis in ADS, the best coupling efficiency between the LO signal and the diodes is 54 % and was obtained with $P_{LO} = 12$ dBm and $f_{LO} = 103$ GHz.

The mixer RF bandwidth performance can be seen in Fig. 13, where the CL and ENT are simulated for $f_{LO} = 103.5 \ GHz$, sweeping the f_{RF} with a P_{LO} variation from 7 to 12 dBm. For 9 dBm LO power, the obtained 3 dB bandwidth is 5.6 % (between 207.5 GHz and 219.5 GHz); whilst, the mean CL is 9.6 dB and the mean ENT is 1816 K for the whole RF band. CL values lower than 11 dB and ENT lower than 2000 K are obtained for P_{LO} between 8 and 12 dBm.

VI. FABRICATION AND MEASUREMENTS

The mixer fabrication and assembly was carried out at the UPNA's facilities. For the PC fabrication, the first step is to deposit 3 μm of Silicon Dioxide (SiO_2) on the 400 μm-thick high-resistivity silicon wafer by means of evaporation using an Angstrom e-Beam evaporator. The second step is etching the alignment marks. These are required to align the metallic circuits (antenna and CPS filter) with the PC structure. The alignment marks were etched using a 3 step-Bosch Deep Reactive Ion Etching (DRIE) procedure. Afterwards, the antenna and CPS filter were fabricated by conventional
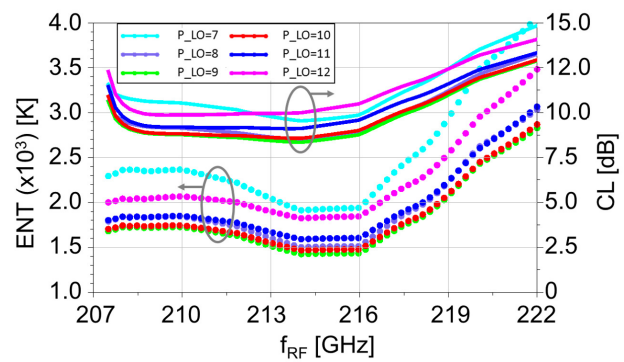

Fig. 13: Simulated Conversion Loss (CL) and Equivalent Noise Temperature (ENT) for $f_{LO} = 103.5 \ GHz$ and P_{LO} in the range between 7 dBm and 12 dBm.

photolithography with 20 nm of Cr, followed by 2 μm of Cu and 30 nm of Au, in order to avoid oxidation. The last step is etching of the air cylinders backside, employing the same DRIE process used for the alignment marks. The SiO_2 membrane acts as a stopping layer in the Bosch silicon etching, protecting the metal circuits.

The antiparallel VDI flip-chip Schottky diode was welded to the antenna pads using EPO-TEK-H20E silver loaded epoxy adhesive. The epoxy and the diode were placed using a wire bonding and die placing machine (TPT HB16D). Fig. 14 shows the details of the fabricated prototype. Finally, the silicon structure was assembled in a 3D printed housing box, and the final result can be seen in Fig. 15. The IF output consists of a SMA end launch connector attached to the silicon slab using two through holes.

The diode manual welding is the part of the manufacturing process where the largest errors can be introduced. Nevertheless, it is still the most cost-effective solution in small facilities to design and proof-concept first prototypes, as is the case of this work. Still, the above fabrication procedure is fully compatible with semiconductor active manufacturing process. Thus, the diode and the silicon PC structure could be fabricated altogether. Another approach, to avoid the manual diode welding, could be to use GaAs membrane beamlead Schottky diode technology [43], [44].

A picture of the setup for the measurement of the subharmonic mixer, is shown in Fig. 16. The Y-Factor gain method [45]–[47] was employed, using liquid nitrogen and a room temperature absorber as cold and hot loads.

The IF chain consists of two LNA amplifiers (GAMP0100.0600SM10 [48]) with 35 dB gain and 1.8 dB Noise Figure (NF). The LO signal is generated with a millimetre wave generator (ELVA G4-143f) and the silicon integrated subharmonic mixer is directly connected to its WR-08 output waveguide. Finally, the IF output power was measured for a fixed LO frequency from 1 to 6 GHz in 1 GHz steps. The measured mixer results, i.e. Equivalent Noise Temperature and Conversion Loss at 103.5 and 105 GHz with $P_{LO} = 13$ dBm, are shown in Fig. 17.

New simulations including a misalignment between the antenna and the PC slab during the fabrication process were done
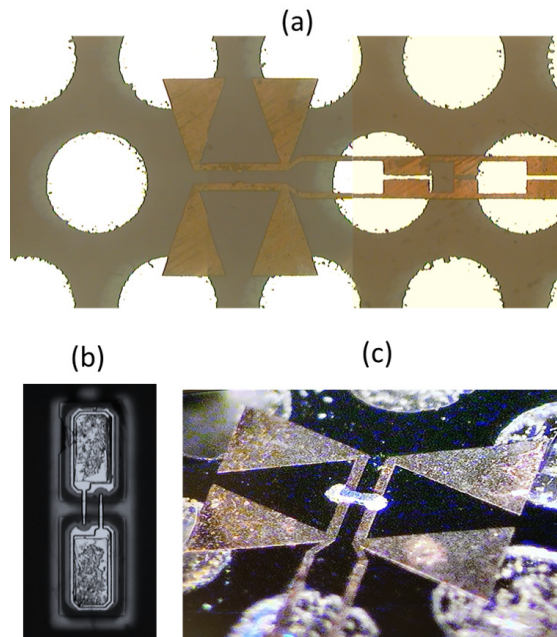
Fig. 14: (a) Picture collage of the antenna at the microscope with back illumination. The silicon dioxide membrane is transparent and the suspended parts of the antenna and the filter can be seen. (b) 50X back-view of the VDI diode at the microscope before welding. (c) Picture of the welded diode.

Fig. 15: Picture of the mixer before the IF end-launcher connector assembly on the left and final assembled device on the right.
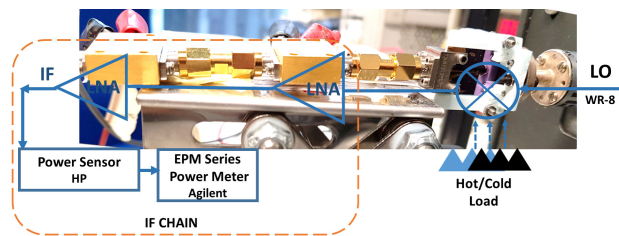

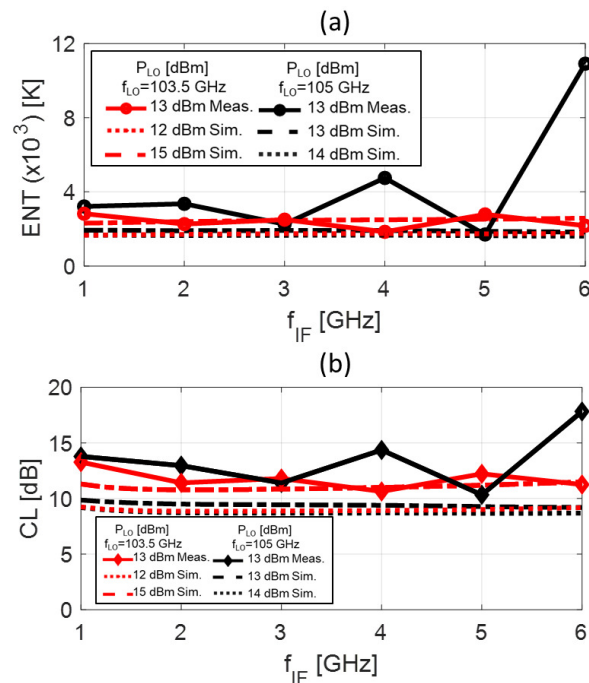Fig. 16: Mixer setup for Y-factor characterization.

Fig. 17: Comparison of measured and simulated (a) Equivalent Noise Temperature and (b) Conversion Losses including fabrication misalignments for $f_{LO} = 103.5$ GHz (red lines) and $f_{LO} = 105$ GHz (black lines).

(i.e. the antenna is not exactly at the center of the resonant cavity). This misalignment was measured to be 10 and 12 μm in the x and y directions, respectively. Other dimensions, as can be those related directly with conventional photolitography and DRIE process, were measured and found to be in good agreement with their nominal values (see Table I). The S-parameters related with the LO-Diode coupling taking into account the fabrication errors are included in Fig. 11 (a) (dotted lines). They show certain decrease in the coupling efficiency which causes that higher LO power will be required. The ENT and CL obtained from new simulation in HFSS and ADS including the fabrication misalignment can be also seen in the same Fig. 17 for comparison.

For $f_{LO} = 103.5$ GHz the best measured ENT value is 1668 K obtained at 4 GHz and the mean value for the whole measured IF band is 2400 K. Moreover, for $f_{LO} = 105$ GHz, the best measured ENT value was 1527 K at 5 GHz. For the same LO frequency, the mean value for the whole measured IF band is 4370 K. As can be seen, the power needed to obtain the best ENT values is higher than the ideal one due to the LO-antenna coupling decrease caused by the misalignment. In particular, the best simulated results including the fabrication deviation are obtained with $P_{LO} = 12$ dBm and $P_{LO} = 14$ dBm for $f_{LO} = 103.5$ GHz and $f_{LO} = 105$ dBm respectively (see Fig. 17), whereas it was achieved for $P_{LO} = 9$ dBm and $P_{LO} = 13$ dBm in the ideal simulations (see Fig. 12). The respective simulated and measured CL can be seen in Fig. 17(b). The measured mean CL is 11.8 dB for $f_{LO} = 103.5$ GHz (red line) and 13.5 dB for $f_{LO} = 105$ GHz (black line).

Summarizing, by introducing the fabrication misalignment errors in the simulation, good agreement between simulated and measured results is obtained.

VII. CONCLUSIONS

The theory and demonstration of an integrated subharmonic mixer on a silicon PC platform have been presented in this work. Table II shows a comparison between this work and the state-of-the-art for room-temperature subharmonic mixers with

different technologies. First references [49]–[53] correspond to conventional metallic block housings and metallic waveguides for LO and RF signals. The previously mention superiority of membrane Schottky integrated fabrication can be seen in [51]. Until now, this technology has been the best proven solution to compensate the ohmic losses from metal-based transmission lines and passive components at high frequencies. However, such implementations increase the complexity and cost and restrict the compactness and reliability of terahertz integrated circuits.

Afterwards, the reported state-of-the-art for receivers based on planar antenna placed on silicon lenses [54], [55] and on a 3D EBG structures [21], [22] is presented. The LO and RF are external signals for these last ones. In those approaches, the requirement of an external high power LO source is an additional limitation. From the previous comparison can be seen that, the results of this work are not far from the state-of-the-art. Nevertheless, additional advantages may be obtained with the presented approach from the point of view of weight, cost and full circuit integration. A monolithic heterodyne receiver, as the one presented here, is a very attractive solution, which may allow the realization of compact two-dimensional multi-pixel array.

TABLE II: State of the art of room-temperature subharmonic mixers working at similar frequencies to this work.

Ref. Ref.	RF (GHz)	ENT (K)	CL (dB)	P_{LO} (mW)	$IF(BW)$ (GHz)
[49]^a	170-260	600-1200	8(mean)	3-6	<36
[50]^b	198-238	1384-1848*	<7	3.1	-
[51]^c	183	450-720	-	1	13.4
[52]^a	170-210	550	5.5	5	20
[53]^b	210-220	> 1500	>8.4	10	-
[21]^d	250	3000(m)	11.5	5-6	-
[22]^d	90	3300-4000(m)	-	+60	-
		<3500(s)	-	<7.1	-
[54]	182	1820	6.3	-	-
[55]	335	1750	-	-	-
This Work	200-220	2400(m)	11.8	20	1-6
		1453-2200(s)	9.6	<10	0.1-15

^{a} Schottky diode, unspecified technology. $T_{DSB} = 2 * T_{SSB}$.
^{b} Flip-Chip Schottky diode on suspended microstrip.
^{c} GaAs membrane beam lead Schottky on suspended stripline.
^{d} Flip-Chip Schottky diode on 3D EBG wood-pile based substrate.
* Converted from SSB where CL is usually 3dB more than DSB CL.
(s) Simulated result.
(m) Measured result.

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Alicia E. Torres-García was born in Cuba in 1990. She received the Degree in Telecommunication Engineering from the Instituto Superior Politécnico José Antonio Echeverría (ISPJAE), Havana, Cuba, in 2013. She is currently working as a Predoctoral Research Fellow in the Antenna Group in the Electrical, Electronic and Communication Engineering Department of the Public University of Navarre (UPNA), Spain. Her interests include millimeter wave and THz components and antennas, metamaterials, planar antennas and different research fields in the microwave range.

Jose M. Pérez-Escudero was born in Murcia, Spain, in 1988. He received the Degree in Telecommunication Engineering from the Universidad Politécnica de Cartagena, Murcia, Spain in 2014 and Ph.D. degree from Public University of Navarra, Pamplona, Spain in 2019. From September of 2013 to March of 2014 he was with Fraunhofer Institute for High Frequency Physics and Radar Techniques FHR, Bonn, Germany, where he was working on waveguide and planar technology filters and their applications in Radar systems. Since April 2015 he is with the Antenna Group at the Electrical, Electronic and Communication Department of the Public University of Navarra. His interests include Terahertz components, antennas and their applications in the millimeter and sub-millimeter wave ranges.

Jorge Teniente was born in Lodosa, Navarra, Spain, in 1973. He received the M.Sc. and Ph.D. degrees in telecommunication engineering from the Public University of Navarra (UPNA), Pamplona, Spain. Since 1997, he has been with the Antenna Group, Public University of Navarra. From 1999 to 2000, he was fifteen months with the European Space Research and Technology Centre (ESTEC), ESA, Noordwijk, The Netherlands and in 2002, he joined as a Research Scientist for 4 months at the ESA Project StarTiger 1, Rutherford Appleton Laboratory, Oxfordshire, England. He is a member of the Institute of Smart Cities, UPNA.

Ramón Gonzalo (M'94) received the M.Sc. and Ph.D. degrees (Hons.) in Ingeniero de Telecomunicación from the Public University of Navarra (UPNA), Pamplona, Spain.

Since 1995, he has been with the Antenna Group, Electrical and Electronic Engineering Department, UPNA, where he is currently a Full Professor. From 1997 to 1998, he was a Research Fellow of the Antenna Section, ESA-ESTEC, Noordwijk, The Netherlands. From 2008 to 2010, he was the Head of the Electrical and Electronic Engineering Department. He is a member of the Institute of Smart Cities, UPNA, Pamplona. He has authored over 60 journal publications in peer-reviewed magazines and 100 conference papers related to his research lines.

Dr. Gonzalo was a co-recipient of the LAPC 2006, LAPC 2007, and IWAT 2007 Best Paper Award.

Iñigo Ederra (M'2015) received the Ingeniero de Telecomunicación and Ph.D. degrees from the Universidad Pública de Navarra, Pamplona, Spain, in 1996 and 2004, respectively.

In 1997, he joined the Microwave and Millimetre Wave Group, Universidad Puública de Navarra. From 1999 to 2000 he was with the European Space Research and Technology Centre (ESTEC), ESA, Noordwijk, The Netherlands, where he was working on Electromagnetic Bandgap materials and their applications in the field of antennas. Since 2001 he is with the Antenna Group, Universidad Pública de Navarra. From June to October 2002 he was visitor scientist at the Rutherford Appleton Laboratory, Chilton, Didcot, UK, participating in ESA's Startiger I project. Currently, he holds an Associate Professor position at the Universidad Pública de Navarra and is a member of its Institute of Smart Cities.

His research interests are in the field of Metamaterials and Metasurfaces and their applications in microwave, millimetre wave and THz components and antennas.