Zero-Loss Switching in DC-DC Series Resonant Converters under Discontinuous Conduction Mode

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***Abstract*—Many thriving applications where isolation is required, such as traction and EV fast charging, implement solid-state transformers (SST). Half-cycle discontinuous-conduction-mode series resonant converters (HC-DCM-SRC) are suitable for these applications. The focus of this paper is to perform a comprehensive approach to HC-DCM-SRC and provide straight-forward requirements in order to ensure zero-loss switching (ZLS) of semiconductors. In addition, these requirements can be expressed as design boundaries for the transformer. Finally, the paper shows that, due to ZLS, silicon devices may have larger power capability than silicon-carbide switches. Therefore, IGBTs can be used instead of SiC MOSFETs, resulting in a significant cost reduction of the converter.**

Keywords—DC-DC power conversion, resonant power conversion, soft-switching, discontinuous conduction mode, power transformers.

I. Introduction

Power applications where isolation is required, such as traction [1]–[3], smart grids [4] and EV fast charging [5], [6], tend to avoid the implementation of transformers operating in line frequency (50-60 Hz). The main reason is that low-frequency power transformers are bulky and heavy [7]. The preferred alternative is to use power transformers within DC-DC power conversion structures, that is, solid-state transformers (SST), also called power-electronic transformers (PET). Operating at high switching frequencies, the size and weight of the transformer can be significantly reduced [8].

One of the most used DC-DC topologies is the series-resonant DC-DC converter (SRC). This type of converter comprises a series LC resonant tank, such as the one depicted in Fig. 1 for a unidirectional, full-bridge SRC. In SST applications, where voltage regulation is not compulsory [9], half-cycle discontinuous-conduction-mode SRC (HC-DCM-SRC) is an interesting option [7], [9], [10], since it accomplishes ZCS for both primary and secondary converters. Nevertheless, as discussed in several papers [7], [11], ZCS in primary switches is not free of switching losses. Hence, a minimum current during the switching process is necessary. It can be ensured through the magnetizing current of the transformer, achieving turn-on ZVS. However, turn-off losses may still take place. As a consequence, SiC devices have to be used instead of Si semiconductors in order to reach high switching frequencies.

This paper performs a comprehensive approach to HC-DCM-SRC in Section II and provides boundaries which must be fulfilled in order to ensure DCM. Then, in Section III, a requirement for the magnetizing current is obtained in order to accomplish turn-on ZVS. Moreover, the turn-off process is discussed, and an additional requirement is obtained so zero-loss switching or ZLS is achieved. As it is mentioned, an ideal lossless switching is not possible, but really low losses are reached. More importantly, these switching losses are dependent on the output parasitic capacitance of the switches, but independent of the delivered power. As a consequence, ZLS can be ensured for any load condition. In Section IV, the obtained requirements are transformed into requirements for the design of the transformer. These expressions can be easily introduced into the design algorithm of the transformer. Finally, in Section V, a key advantage of the HC-DCM-SRC operating under ZLS is presented. Due to quasi-lossless switching, it is possible to use silicon devices at high switching frequencies. Actually, it is concluded that Si IGBTs, thanks to their lower output parasitic capacitance, may be able of larger power capability than SiC MOSFETs. As a result, the cost reduction in the converter due to implementing a high-frequency transformer is further extended by using Si devices instead of SiC.

II. Discontinuous Conduction Mode

Discontinuous conduction mode (DCM) in series resonant converters has been deeply analysed in various publications, e.g. [12], [13]. As stated in [13], $k < 1$ in order to allow the converter to work under DCM, where

$$k = f_{sw}/f_r, \tag{1}$$

being f_{sw} the switching frequency and f_r the series resonant frequency. Then, it is desirable to maximize the time when power is delivered to the load. That is, to minimize the current intensity RMS value for a given active power. For this, $k > 0.5$ is chosen, so only one resonant half cycle takes place in each half-switching period (HC-DCM). Thus, reverse energy flow is avoided. Hence, the converter is operated under odd discontinuous mode with

$$0.5 < k < 1. \tag{2}$$

Another requirement to be fulfilled in order to work under HC-DCM is that the voltage in the series resonant capacitor is [12]

$$v_{C_r}(T_r/2) < V_{DD,1} + V'_{DD,2} = V_{DD,1} + n \cdot V_{DD,2}. \tag{3}$$

This way, when the current in the secondary, i_2, reaches zero, all the diodes in the secondary converter become reversed biased and, thus, $v_{KA,5}, v_{KA,6}, v_{KA,7}, v_{KA,8} > 0$.

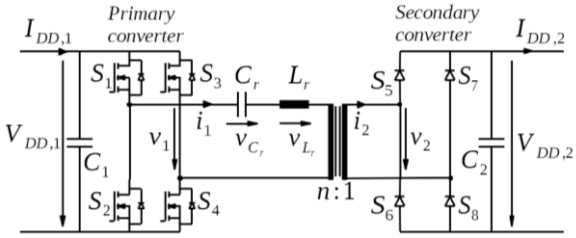

Fig. 1. Circuit diagram of unidirectional, full-bridge SRC.

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Regarding that in DCM with $0.5 < k < 1$ the resonant tank voltage gain is one [12], [13], (3) becomes

$$v_{C_r}(T_r/2) < 2 \cdot V_{DD,1}. \tag{4}$$

Despite the simplicity of this limit, it may not be a straightforward expression to be used during design. Thus, it is convenient to transform it into a more useful expression, linking it to the load condition. First, the capacitor peak voltage, V_{C_r}, is related to its charge, Q_{C_r}. During the resonant half cycle, the voltage in the resonant capacitor changes from its negative peak value at $t = 0$ to its positive peak value at $t = T_r/2$, as depicted in Fig. 2. Hence, the charge introduced in the capacitor during this time is

$$Q_{C_r} = \int_{-V_{C_r}}^{+V_{C_r}} C_r \cdot dv_{C_r} = C_r \cdot 2 \cdot V_{C_r}. \tag{5}$$

The introduced charge is also linked to the primary current. While the positive half-switching period is taking place, the resonant current is positive, as shown in Fig. 2. Thus, it charges the series resonant capacitor. Capacitor charge and current are related through

$$Q_{C_r} = \int_0^{T_r/2} i_1 \cdot dt = \int_0^{T_r/2} \frac{i_2}{n} \cdot dt, \tag{6}$$

regarding that the primary-to-secondary current ratio of the resonant tank is one, but the transformer turns ratio n has to be considered. As can be seen in (6) and in Fig. 2, $t = 0$ is set at the instant when the positive half-switching period begins.

Once at the load side, the output DC current intensity can be obtained from i_2 as

$$I_{DD,2} = \frac{1}{T_{sw}/2} \cdot \int_0^{T_{sw}/2} |i_2| \cdot dt = \frac{1}{T_{sw}/2} \cdot \int_0^{T_r/2} i_2 \cdot dt, \tag{7}$$

since the load side converter is a synchronous rectifier. Then, (6) and (7) can be combined, resulting in

$$Q_{C_r} = T_{sw} \cdot \frac{I_{DD,2}}{2 \cdot n} = \frac{I_{DD,2}}{2 \cdot n \cdot f_{sw}}. \tag{8}$$

The resonant capacitor peak voltage can be related to $I_{DD,2}$ by introducing (8) into (5), resulting in

$$V_{C_r} = \frac{I_{DD,2}}{4 \cdot n \cdot C_r \cdot f_{sw}}. \tag{9}$$

Introducing that $I_{DD,1} = I_{DD,2}/n$ and $P = V_{DD,1} \cdot I_{DD,1}$, for the DC currents and the delivered power, respectively, V_{C_r} becomes

$$V_{C_r} = \frac{P}{4 \cdot V_{DD,1} \cdot C_r \cdot f_{sw}}. \tag{10}$$

Finally, substituting (10) into (4) and rearranging the expression, the DCM requirement is

$$P < 8 \cdot C_r \cdot f_{sw} \cdot V_{DD,1}^2, \tag{11}$$

which can also be expressed by means of the characteristic impedance of the resonant tank, $Z_C = \sqrt{L_r/C_r}$, as

$$P < \frac{4 \cdot k \cdot V_{DD,1}^2}{\pi \cdot Z_C}. \tag{12}$$

HC-DCM is ensured as long as f_{sw} is such that (2) is accomplished and P fulfils (12).

It must be highlighted that this analysis and the resulting requirement for the active power is also valid for bidirectional, CLLC series resonant converters. In that case, C_r and L_r are the equivalent series capacitance and inductance, respectively, referred to the primary side.

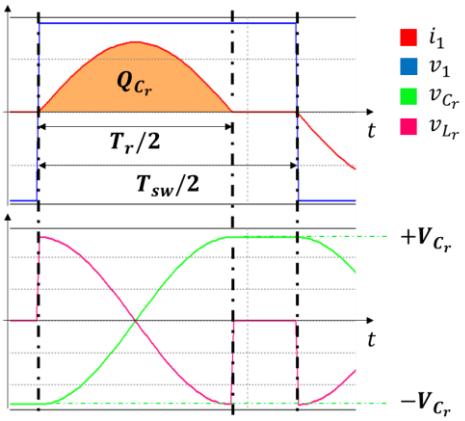

Fig. 2. Main waveforms in the primary side of the HC-DCM-SRC.

III. ZCS AND ZVS

In the HC-DCM-SRC, the resonant current becomes zero before the half-switching period ends. Therefore, ZCS is accomplished for the transistors in the primary and the diodes in the secondary [12]–[14]. However, under zero-current condition, ZVS in the primary is not achieved [1], [11], [15]. Thus, lossless turn-on of the transistors is not reached unless a ZVS requirement is fulfilled. Moreover, lossless turn-off may also be possible for the switches in the primary if certain requirements are met.

A. Zero-current switching

The ZCS process can be explained starting from the MOSFET equivalent circuit of Fig. 3 (a), where its parasitic capacitances have been included. When the MOSFET of S_i is conducting, $v_{DS,i} \cong 0$. Thus, the complementary MOSFET of the cell, S_j, is blocking with $v_{DS,j} \cong V_{DD}$, where V_{DD} is the bus voltage.

At the end of the resonant half cycle (see Fig. 4 (a)), the resonant current becomes zero. As a consequence, S_i turns off with zero current (see Fig. 4 (b)). Due to ZCS, there is no current available to charge the output capacitance of S_i and discharge the output capacitance of S_j. As a result, the voltage is not switched between them, so $v_{DS,i} = v(C_{oss,i}) \cong 0$ and $v_{DS,j} = v(C_{oss,j}) \cong V_{DD}$. When the following half-switching period starts and S_j is turned on (Fig. 4 (c)), $C_{oss,i}$ and $C_{oss,j}$ are espontaneously charged/discharged through the channel resistance of S_j (Fig. 4 (d)). Hence, ZCS is not lossless. The energy stored in $C_{oss,j}$, which is $E_{oss}(V_{DD})$, is dissipated in the channel of S_j. Moreover, the same amount of energy introduced in $C_{oss,i}$ when it is charged is dissipated in the channel of S_j as well [16]. Therefore, the switching mechanism is so $2 \cdot E_{oss}(V_{DD})$ is lost in the switch that is turned on. Regarding that the primary converter is a full bridge, the switching energy loss in a half-switching period is $4 \cdot E_{oss}(V_{DD})$. Then, the switching power loss in the primary converter under ZCS is obtained as

$$P_{sw} = 8 \cdot E_{oss}(V_{DD}) \cdot f_{sw}. \tag{13}$$

The stored energy E_{oss} can be calculated as [15]

$$E_{oss}(V_{DD}) = \int_0^{V_{DD}} v_{DS} \cdot C_{oss}(v_{DS}) \cdot dv_{DS}. \tag{14}$$

It becomes clear from (14) that the larger C_{oss} and the higher V_{DD}, the greater the switching power loss.

B. *Turn-on zero-voltage switching*

In order to avoid the mentioned switching losses, turn-on ZVS is desirable. For this, it is necessary that some current remains in the primary of the resonant tank, so the output parasitic capacitances can be completely charged/discharged. This way, the diode of S_j is forward biased before its MOSFET is turned on. Then, the MOSFET is turned on with zero losses.

Under CCM, the current during the switching process depends on the load condition. Therefore, it may be large, ensuring turn-on ZVS, but leading to large turn-off losses. On the other extreme, it may not be large enough to charge/discharge both C_{oss} in each cell before the MOSFET of S_j turns on. Hence, not achieving ZVS. However, under DCM, ZVS can be ensured for any load condition. During the discontinuous time, which takes place between $t = T_r/2$ and $t = T_{sw}/2$, the resonant current is zero, $i_r = 0$. Nevertheless, the primary current is

$$i_1 = i_r + i_m, \tag{15}$$

that is, the sum of the resonant current in the primary and the magnetizing current. Thus, $i_1 = i_m$ for $t \in (T_r/2\,, T_{sw}/2)$ and, as a result, the magnetizing current is in charge of achieving complete ZVS.

Taking Fig. 5 as reference, the switching process at the end of the positive half-switching period is considered. Switches S_1 and S_4, which were conducting, are turned off once i_r has become zero. As can be deduced from Fig. 5, the magnetizing current simultaneously charges C_{oss} of S_1 and S_4 and discharges C_{oss} of S_2 and S_3. Due to the full-bridge topology, the charge moved during the voltage switching is $2 \cdot Q_{oss}(V_{DD})$. As a result, the necessary magnetizing current is obtained as

$$I_m > i_m(ZVS) = \frac{2 \cdot Q_{oss}(V_{DD})}{t_{vr}}, \tag{16}$$

to ensure that the diodes of S_2 and S_3 start conducting before their MOSFETs and, thus, turn-on ZVS is accomplished. The requirement in (16) defines the minimum magnetizing current during the switching process in order to completely switch the voltage in a time t_{vr}. As can be seen, the obtained expression is time-based. Furthermore, during t_{vr} , the magnetizing current, and thus the energy stored in L_m, may change. Hence, it must be ensured as well that the energy in L_m is enough for the soft-switching process to happen. This leads to an energy-based requirement. Applying an energy balance between the beginning and the end of the switching process in the full bridge, the following expression is obtained [15]

$$E_i + E_{trans} = E_f + E_{dis}. \tag{17}$$

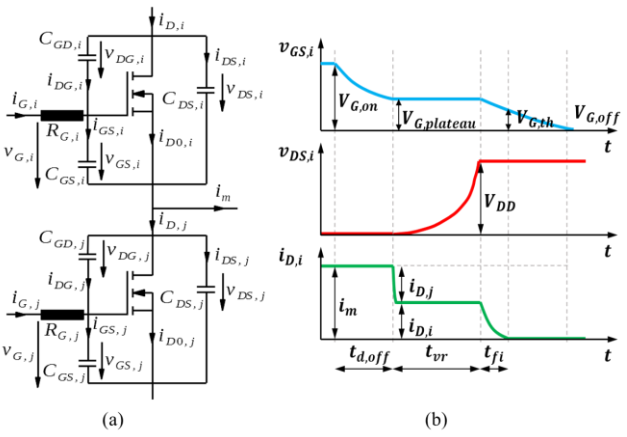

Fig. 3. (a) Single switching cell with MOSFET model; (b) main waveforms during S_i turn-off process.

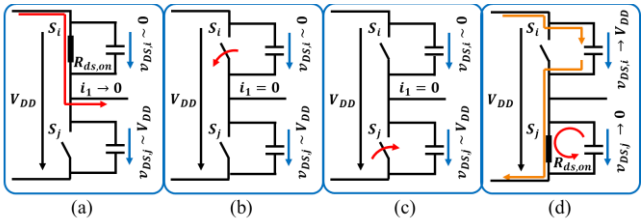

Fig. 4. Step-by-step ZCS process in a switching cell.

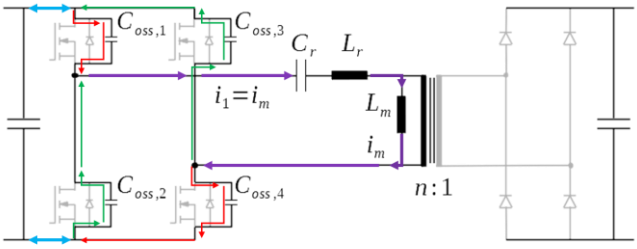

Fig. 5. Current flow during the voltage switching process in the primary full-bridge converter.

The initial energy of the system is

$$E_i = \frac{1}{2} \cdot L_m \cdot I_{m,i}^2 + 2 \cdot E_{oss}(V_{DD}), \tag{18}$$

which is the sum of the initial energy in L_m and the energy stored in C_{oss} of the two switches that are initially off, blocking a bus voltage V_{DD}. The net energy transferred by the source to the system during the process, E_{trans}, is zero. This is due to the full-bridge topology, where the charge recirculates as in Fig. 5. Note that during the process there is actually a charge flow from/to the source (in blue), since C_{oss} varies with voltage during t_{vr}. However, the total charge extracted from $C_{oss,2}$ and $C_{oss,3}$ (in green) is reintroduced in $C_{oss,1}$ and $C_{oss,4}$ (in red), resulting in a null net charge from the source. Then, the final energy is

$$E_f = \frac{1}{2} \cdot L_m \cdot I_{m,f}^2 + 2 \cdot E_{oss}(V_{DD}), \tag{19}$$

again with $2 \cdot E_{oss}(V_{DD})$, since the other two switches finish the process blocking voltage and with their output capacitances charged. As a result, the energy balance shows that

$$\frac{1}{2} \cdot L_m \cdot I_{m,i}^2 = \frac{1}{2} \cdot L_m \cdot I_{m,f}^2 + E_{dis}, \tag{20}$$

hence, $I_{m,f} \leq I_{m,i}$. In order to ensure enough magnetizing current during t_{vr} when switching losses take place, requirement (16) must be applied to $I_{m,f}$ and, then, the necessary initial current, $I_{m,i}$, is to be calculated by means of (20), leading to

$$I_{m,i} > \sqrt{\frac{4 \cdot Q_{oss}^2(V_{DD})}{t_{vr}^2} + \frac{2 \cdot E_{dis}}{L_m}}, \tag{21}$$

which is a more demanding requirement for the magnetizing current than (16). A particular scenario takes place if $E_{dis} = 0$ is accomplished. In that case, the magnetizing current would be constant during t_{vr}. As a consequence, there would be no energy requirement for the magnetizing inductance. Note that this happens for full-bridge converters (regardless the switches are MOSFETs or IGBTs) where L_m is in charge of the ZVS. The energy requirement is different for half or full bridges where L_m is clamped to the secondary-side bus voltage, so there is energy transferred to the secondary source during t_{vr} [17], [18], even if $E_{dis} = 0$ is assumed [15]. In these last cases, the series inductance is the one that participates in the ZVS. The requirement for achieving $E_{dis} = 0$ in the HC-DCM-SRC is obtained below.

C. Zero-loss switching (ZLS)

While MOSFET lossless turn-on is achieved if i_m fulfils (21), the complementary MOSFET turn-off may take place with losses, because part of i_m may flow through its channel. This can be seen attending to Fig. 3 (a) and considering a conventional, hard-switching turn-off, such as the one presented in Fig. 3 (b). During t_{vr}, when the voltage is switched between S_i and S_j, the current through the MOSFET which is turned off (S_i) is divided. One part of this current, i_{D0}, flows through the channel of the MOSFET and causes power losses, since $v_{DS} > 0$. The other part charges the output capacitance, $C_{oss} = C_{GD} + C_{DS}$. The aim is not only to accomplish lossless turn-on, but also lossless turn-off. Due to this switching mechanism, $E_{dis} \cong 0$ and (21) becomes (16). Therefore, a zero-loss switching (ZLS) is obtained in the primary converter.

Considering the circuit for one switching cell in Fig. 3 (a), the analysis is performed assuming that S_i turns off and S_j turns on afterwards. Regarding S_i, its total drain current is $i_{D,i}$. If the channel is put out before S_i begins to block voltage, i.e., before $v_{DS,i} > 0$, it results in $i_{D0,i} \cong 0$. Thus, the energy loss in the turn-off is $E_{off,i} \cong 0$ [19]. Then, as can be deduced from Fig. 3 (a),

$$i_m = i_{D,i} - i_{D,j}, \tag{22}$$

where

$$i_{D,i} = i_{D0,i} + i_{DS,i} + i_{DG,i}, \tag{23}$$

$$i_{D,j} = i_{DS,j} + i_{DG,j}. \tag{24}$$

In addition, the drain-to-source voltages of S_i and S_j fulfils that

$$v_{DS,i} + v_{DS,j} = V_{DD} \Rightarrow \frac{dv_{DS,i}}{dt} + \frac{dv_{DS,j}}{dt} = 0. \tag{25}$$

The goal is to achieve $i_{D0} = 0$ thanks to reducing the gate-to-source voltage of the MOSFET so $v_{GS} < V_{G,th}$ before the voltage switching begins. In order to achieve this, the gate resistance

$$R_G = \frac{V_{G,off} - v_{GS}}{i_G} \tag{26}$$

must be below a certain boundary, $R_{G,lim}$, so the switching process is quick enough. During t_{vr},

$$\frac{dv_{GS}}{dt} \cong 0 \Rightarrow \frac{dv_{DS}}{dt} \cong \frac{dv_{DG}}{dt} \Rightarrow \frac{i_{DS}}{C_{DS}} \cong \frac{i_{DG}}{C_{GD}}, \tag{27}$$

$$i_m = i_{DS,i} + i_{DG,i} - i_{DS,j} - i_{DG,j}, \tag{28}$$

$$i_{DG,i} \cong -i_{G,i}. \tag{29}$$

Introducing (25) and (27) into (28), the expression for the magnetizing current becomes

$$i_m = \frac{dv_{DS,i}}{dt} \cdot \left(C_{oss,i} + C_{oss,j}\right). \tag{30}$$

Finally, (26) is particularized to the conditions imposed by (29) and (30), leading to

$$R_G < R_{G,lim} = \frac{\left(V_{G,th} - V_{G,off}\right)\left(C_{ossQeq,i}(V_{DD}) + C_{ossQeq,j}(V_{DD})\right)}{i_m(ZVS) \cdot C_{GDQeq,i}(V_{DD})}, \tag{31}$$

which is the requirement for the gate resistance in order to accomplish lossless turn-off of S_i at the same time that $i_m \geq i_m(ZVS)$ to ensure lossless turn-on of S_j as well. Since the parasitic capacitances C_{oss} are not constant during the switching process, the charge-equivalent capacitances C_{ossQeq} have to be considered [15].

As can be deduced from the obtained boundary for R_G, the larger the current during the switching process, the lower the limit of gate resistance that allows to achieve lossless turn-off. In fact, it may happen that the boundary in (31) for R_G is less than the internal gate resistance of the MOSFET, $R_{G,int}$. In that case, this turn-off method is not possible. Nevertheless, in this case, thanks to only switching part of the magnetizing current, which is expected to have a low value, the lossless turn-off is easily achieved by selecting $R_{G,ext} < R_{G,lim} - R_{G,int}$.

D. Comments on ZLS

a) Converter operating conditions: Several requirements have been presented in order to ensure that the full-bridge SRC works under HC-DCM with null switching losses. Particularly, equations (2) and (12) establish the conditions for HC-DCM, equation (21) defines the boundary to obtain turn-on ZVS and (31) shows the condition to ensure lossless turn-off.

b) Parasitic capacitances estimation: The lossless switching requirements rely on knowing the value of C_{GD} and C_{DS} and, thus, C_{oss}. However, C_{oss} may exhibit significant hysteresis [20]. Therefore, during design, a safety margin from the obtained boundaries is recommended.

c) Lossless switching: Despite the lossless switching mechanism described, the charging and discharging of C_{oss} is not completely free of losses. This is due to the charge moved during the process [20]. Hence, $E_{dis} > 0$ and (21) has to be used. Moreover, the switching losses have to be considered in the design stage to avoid semiconductor overheating during operation. Nevertheless, the switching power loss due to the charging/discharging process is less than (13) for ZCS, where all the stored energy is dissipated.

d) ZLS with IGBTs: The analysis of the lossless switching mechanism has been performed considering MOSFETs. The same requirements are valid for IGBTs as well. Regarding the turn-on process, many papers such as [1], [7], [11], have treated the ZVS on IGBTs, agreeing on: defining enough interlock time (or discontinuous time) and ensuring sufficient magnetizing current. The effect of both parameters has been considered in this paper. The discontinuous time can be defined by selecting an appropriate switching-to-resonant ratio k, while the magnetizing current is established through a suitable design of the magnetizing inductance of the transformer. Furthermore, the lossless turn-off can also be applied to IGBTs [19].

IV. Consequences on Transformer Design

The resulting requirements for achieving DCM and ZVS affect the design of the high-frequency transformer of the converter. On one hand, the boundary in (11) – which ensures DCM – leads to an upper boundary for the series resonant inductance, which is the leakage inductance of the transformer. On the other hand, the expression in (21) – requirement for accomplishing ZVS – establishes an upper boundary for the magnetizing inductance.

A. Leakage inductance boundary

In the converter, the leakage inductance of the transformer is used as the resonant inductance, so $L_r = L_{lk}$. Therefore, the series equivalent leakage inductance, L_{lk}, resonates with C_r at frequency

$$f_r = \frac{1}{2\pi \cdot \sqrt{L_{lk} \cdot C_r}}. \tag{32}$$

Then, C_r is obtained from (32) and introduced into (11), resulting in

$$P < \frac{8 \cdot f_{sw} \cdot V_{DD,1}^2}{(2\pi \cdot f_r)^2 \cdot L_{lk}}. \quad (33)$$

Introducing (1) for the ratio k into (33) and rearranging, the boundary for the leakage inductance of the transformer is obtained as

$$L_{lk} < L_{lk,lim1} = \frac{2 \cdot k^2 \cdot V_{DD,1}^2}{\pi^2 \cdot f_{sw} \cdot P}. \quad (34)$$

L_{lk} must be designed considering the most demanding scenario, which is for rated power. Note that (34) is a maximum limit and not a minimum.

B. *Magnetizing inductance boundary*

The general expression to be considered in the design of the magnetizing inductance of the transformer, L_m, has been obtained in (21). Nevertheless, under ZLS, it must be noted that the second term in (21) is usually negligible in comparison with the first term. Thus, for the boundary of L_m, (16) can be used in this case. If ZLS is lost and there is a larger E_{dis}, the requirement for L_m can be obtained the same way as indicated below but using exactly (21).

During the resonant half-cycle, the combined voltage drop in the series inductance and capacitance is zero. Therefore, the magnetizing inductance is clamped to the bus voltage. As a result, the magnetizing current has a constant slope from $t = 0$ to $t = T_r/2$ and responds to

$$\frac{di_m}{dt} = \frac{V_{DD,1}}{L_m}. \quad (35)$$

Then, from $t = T_r/2$ to $t = T_{sw}/2$, the applied voltage is no longer $V_{DD,1}$, but $V_{DD,1} - V_{C_r}$ (assuming that the voltage drop in L_{lk} is negligible). Thus, the slope of i_m is no longer as in (35), but

$$\frac{di_m}{dt} = \frac{V_{DD,1} - V_{C_r}}{L_m}, \quad (36)$$

until the switching process begins. As a result, from (35), the magnetizing current at $t = T_r/2$ is obtained as

$$i_m(T_r/2) = i_m(0) + \frac{V_{DD,1}}{L_m} \cdot \frac{T_r}{2}, \quad (37)$$

where $i_m(0)$, as depicted in Fig. 6, is the magnetizing current intensity at $t = 0$, that is, at the beginning of the positive half-switching period. Then, for $t \in (T_r/2, T_{sw}/2)$, the magnetizing current is

$$i_m(t) = i_m(T_r/2) + \frac{V_{DD,1} - V_{C_r}}{L_m} \cdot \left(t - \frac{T_r}{2}\right). \quad (38)$$

Knowing that $i_m(T_{sw}/2) = -i_m(0)$, the initial value $i_m(0)$ can be obtained from (37) and (38), resulting in

$$i_m(0) = -i_m(T_{sw}/2) = \frac{V_{C_r} \cdot (1-k) - V_{DD,1}}{4 \cdot f_{sw} \cdot L_m}. \quad (39)$$

It can be seen that, depending on the value of V_{C_r}, the slope of i_m during the discontinuous time may be (a) negative or (b) positive. Hence, the lowest possible current for the switching process is $i_m(T_{sw}/2)$ in scenario (a) and $i_m(T_r/2)$ in scenario (b). Determining which scenario takes place is key in order to ensure enough magnetizing current for complete ZVS. In the boundary between scenarios (a) and (b), $i_m(T_{sw}/2) = i_m(T_r/2)$. Thus, from (37) – (39), it is obtained that $V_{C_r} = V_{DD,1}$. Then, starting with the expression for V_{C_r} in (10) and applying the transformations in (34), the boundary can be expressed by means of the leakage inductance,

$$L_{lk,lim2} = \frac{k^2 \cdot V_{DD,1}^2}{\pi^2 \cdot f_{sw} \cdot P} = L_{lk,lim1}/2\,. \quad (40)$$

As it is obtained hereunder, the value of L_{lk} affects the design of L_m. If $L_{lk,lim2} < L_{lk} < L_{lk,lim1}$, the converter works under DCM and scenario (a), as shown in Fig. 6 (a). Therefore, $i_m(T_{sw}/2) > i_m(ZVS)$ to ensure ZVS, regardless the precise instant in which the switching process begins during the discontinuous time. From (10), (16) and (38), it is obtained that the magnetizing inductance must fulfil

$$L_m < L_{m,lim_a} = \frac{\left(V_{DD,1}^2 \cdot k^2 - P \cdot \pi^2 \cdot f_{sw} \cdot L_{lk} \cdot (1-k)\right) \cdot t_{vr}}{8 \cdot f_{sw} \cdot V_{DD,1} \cdot k^2 \cdot Q_{oss}(V_{DD,1})}, \quad (41)$$

to reach complete ZVS in scenario (a). On the other hand, if $L_{lk} < L_{lk,lim2}$, the converter works under DCM as well, but in scenario (b), corresponding to Fig. 6 (a). Hence, the design requirement is $i_m(T_r/2) > i_m(ZVS)$ in this case. From (10), (16) and (37), it is obtained that the magnetizing inductance must fulfil

$$L_m < L_{m,lim_b} = \frac{\left(P \cdot \pi^2 \cdot f_{sw} \cdot L_{lk} \cdot (1-k) - V_{DD,1}^2 \cdot k^2 \cdot (1-2k)\right) \cdot t_{vr}}{8 \cdot f_{sw} \cdot V_{DD,1} \cdot k^2 \cdot Q_{oss}(V_{DD,1})}, \quad (42)$$

to reach complete ZVS in scenario (b).

To sum up, the leakage inductance must accomplish (34) and the magnetizing inductance has to fulfil (41) in scenario (a) or (42) in scenario (b). These limits can be easily implemented in an optimal design algorithm for the high-frequency transformer.

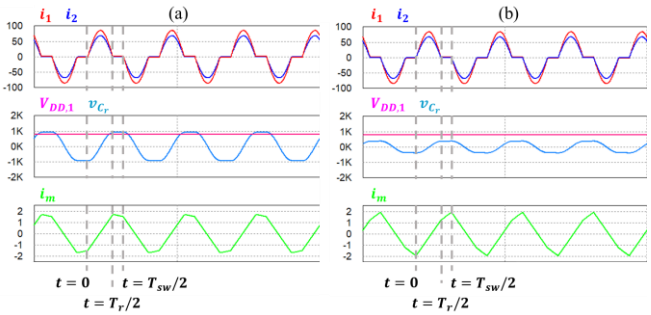

Fig. 6. Waveforms of HC-DCM-SRC: (a) $L_{lk} > L_{lk,lim2}$; (b) $L_{lk} < L_{lk,lim2}$.

V. Consequences of ZLS on Semiconductor Selection

Even when conventional ZVS or ZCS is achieved in high-frequency DC-DC power converters, the remaining switching losses in the primary switches make it not possible to use IGBTs at such high frequency, penalizing the resonant tank design. Thus, in these applications, SiC superior features and ability to switch at high frequencies overcome their higher cost. However, in HC-DCM-SRC under ZLS, the switching losses in the primary converter are theoretically null. Even with the charging/discharging mechanism not being lossless [15], the switching losses in the primary converter can only be as large as (13). Hence, the use of IGBT switches is feasible, even at frequencies above 100 kHz, as shown in Fig. 7., where the power capability of the primary converter is depicted as a function of the switching frequency. Assuming an analysis during the design stage, the maximum possible switching losses should be considered as a safety design criterion. The performance of four devices is represented: in solid lines, 50 and 100 A IGBT modules and, in dashed lines, 50 and 100 A SiC MOSFET modules. Further data of the semiconductors are presented in Table I.

Due to the larger C_{oss} of the analyzed SiC devices, the maximum switching losses are higher than those of IGBTs with same rated current. It must be noted that, according to (13), switching losses are not dependent on RMS current intensity. Therefore, the power capability,

$$P = \frac{2 \cdot \sqrt{2 \cdot k}}{\pi} \cdot V_{DD,1} \cdot I_1, \quad (43)$$

can be directly calculated with I_1 (RMS current in the primary of the tank), obtained from the maximum allowable conduction losses, $P_{con,max}$. The criterion to use is not

surpassing the maximum temperature rise allowed in the semiconductor ($T_{j,des} - T_{hs,des} = 40\ ºC$), leading to

$$P_{con,max}(I_1) = \frac{T_{j,des} - T_{hs,des}}{R_{th,j-hs}} - 2 \cdot E_{oss}(V_{DD,1}) \cdot f_{sw}, \qquad (44)$$

where $T_{j,des}$ is the junction temperature of design, $T_{hs,des}$ the heatsink temperature, and $R_{th,j-hs}$ is the equivalent junction-to-heatsink thermal resistance for one transistor. The maximum switching losses possible are defined for a single switch from (13), resulting in $2 \cdot E_{oss}(V_{DD,1}) \cdot f_{sw}$ in (44).

As can be seen in Fig. 7, the negative slope of the power capability is steeper in the studied SiC devices than in the Si devices. This behavior results in higher power capability of IGBTs. Thus, the IGBT module would be selected rather than the SiC MOSFET module of the same rated current, especially when considering the SiC-Si cost ratio, which is between 2 and 3 for the studied devices.

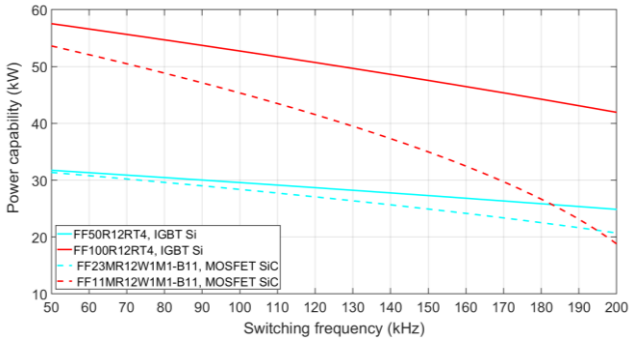

Fig. 7. Power capability of primary converter vs. switching frequency for different Si and SiC semiconductors at $V_{DD,1} = 800\ V$ and $k = 0.7$.

TABLE I. SI & SIC FEATURES

Code & Technology	Features		
	$V_{breakdown}$ (V)	I_{rated} (A)	E_{oss} @800 V (μJ)
FF50R12RT4 / Si IGBT	1200	50	56
FF100R12RT4 / Si IGBT	1200	100	112
FF23MR12W1M1_B11 / SiC MOSFET	1200	50	90
FF11MR12W1M1_B11 / SiC MOSFET	1200	100	179

VI. CONCLUSIONS

A detailed as well as comprehensive approach to the HC-DCM-SRC has been developed, resulting in a set of requirements to ensure the desired operating conditions of the converter. Then, the zero-loss switching or ZLS is studied. Despite the losses related to the movement of charges during the switching process, switching losses are really low and, moreover, dependent on the output parasitic capacitance of the switches, but not on the conducted current. As a consequence, ZLS can be ensured for any load condition through a proper design. For this, easy-to-use requirements for the leakage and the magnetizing inductances of the transformer are obtained. Finally, a key advantage of ZLS is presented: silicon devices, thanks to their lower parasitic output capacitance, may handle larger power than silicon-carbide ones. Therefore, IGBTs are eligible for HC-DCM-SRC, resulting in a significant cost reduction. Future research will focus on the effect of secondary-side parasitic capacitances on ZVS and on the experimental validation of the described ZLS mechanism.

REFERENCES

[1] H. Hoffmann and B. Piepenbreier, "High voltage IGBTs and medium frequency transformer in DC-DC converters for railway applications," SPEEDAM 2010, 2010, pp. 744-749, doi: 10.1109/SPEEDAM.2010.5542109.

[2] D. Dujic, F. Kieferndorf, F. Canales and U. Drofenik, "Power electronic traction transformer technology," Proceedings of The 7th International Power Electronics and Motion Control Conference, 2012, pp. 636-642, doi: 10.1109/IPEMC.2012.6258820.

[3] C. Zhao et al., "Power Electronic Traction Transformer—Medium Voltage Prototype," in IEEE Transactions on Industrial Electronics, vol. 61, no. 7, pp. 3257-3268, July 2014, doi: 10.1109/TIE.2013.2278960.

[4] J. E. Huber and J. W. Kolar, "Applicability of Solid-State Transformers in Today's and Future Distribution Grids," in IEEE Transactions on Smart Grid, vol. 10, no. 1, pp. 317-326, Jan. 2019, doi: 10.1109/TSG.2017.2738610.

[5] S. Srdic and S. Lukic, "Toward Extreme Fast Charging: Challenges and Opportunities in Directly Connecting to Medium-Voltage Line," in IEEE Electrification Magazine, vol. 7, no. 1, pp. 22-31, March 2019, doi: 10.1109/MELE.2018.2889547.

[6] E. I. Pool-Mazun, J. J. Sandoval, P. N. Enjeti and I. J. Pitel, "An Integrated Solid-State Transformer With High-Frequency Isolation for EV Fast-Charging Applications," in IEEE Journal of Emerging and Selected Topics in Industrial Electronics, vol. 1, no. 1, pp. 46-56, July 2020, doi: 10.1109/JESTIE.2020.3003355.

[7] G. Ortiz, H. Uemura, D. Bortis, J. W. Kolar and O. Apeldoorn, "Modeling of Soft-Switching Losses of IGBTs in High-Power High-Efficiency Dual-Active-Bridge DC/DC Converters," in IEEE Transactions on Electron Devices, vol. 60, no. 2, pp. 587-597, Feb. 2013, doi: 10.1109/TED.2012.2223215.

[8] J. E. Huber, "Conceptualization and Multi- Objective Analysis of Multi-Cell Solid-State Transformers," Ph.D. dissertation, ETH Zurich, 2016.

[9] J. Huber, G. Ortiz, F. Krismer, N. Widmer and J. W. Kolar, "η-ρ Pareto optimization of bidirectional half-cycle discontinuous-conduction-mode series-resonant DC/DC converter with fixed voltage transfer ratio," 2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2013, pp. 1413-1420, doi: 10.1109/APEC.2013.6520484.

[10] G. Ortiz, M. G. Leibl, J. E. Huber and J. W. Kolar, "Design and Experimental Testing of a Resonant DC–DC Converter for Solid-State Transformers," in IEEE Transactions on Power Electronics, vol. 32, no. 10, pp. 7534-7542, Oct. 2017, doi: 10.1109/TPEL.2016.2637827.

[11] L. Lindenmüller, R. Alvarez, P. Kleinichen and S. Bernet, "Characterization of a 6.5 kV / 500A IGBT module in a series resonant converter," 2011 IEEE Energy Conversion Congress and Exposition, 2011, pp. 4138-4143, doi: 10.1109/ECCE.2011.6064332.

[12] V. Vorperian and S. Cuk, "A complete DC analysis of the series resonant converter," 1982 IEEE Power Electronics Specialists conference, 1982, pp. 85-100, doi: 10.1109/PESC.1982.7072398.

[13] R. W. Erickson and D. Maksimovic, Fundamentals of Power Electronics. Springer US, 2001, pp. 705-759.

[14] W. C. Ho and M. H. Pong, "Design and analysis of discontinuous mode series resonant converter," Proceedings of 1994 IEEE International Conference on Industrial Technology - ICIT '94, 1994, pp. 486-489, doi: 10.1109/ICIT.1994.467080.

[15] M. Kasper, R. M. Burkart, G. Deboy and J. W. Kolar, "ZVS of Power MOSFETs Revisited," in IEEE Transactions on Power Electronics, vol. 31, no. 12, pp. 8063-8067, Dec. 2016, doi: 10.1109/TPEL.2016.2574998.

[16] C. Zucker, "Condenser Problem," Am. J. Phys., vol. 23, no. 7, p. 469, Oct. 1955, doi: 10.1119/1.1934050.

[17] M. Zareie, B. Poorali, S. Eren and M. Pahlevani, "New DC–DC Converter With Direct Power Transfer Capability," in IEEE Transactions on Power Electronics, vol. 36, no. 5, pp. 5647-5663, May 2021, doi: 10.1109/TPEL.2020.3028873.

[18] Y. Yan, H. Gui and H. Bai, "Complete ZVS Analysis in Dual Active Bridge," in IEEE Transactions on Power Electronics, vol. 36, no. 2, pp. 1247-1252, Feb. 2021, doi: 10.1109/TPEL.2020.3011470.

[19] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. De Doncker, Semiconductor Power Devices: Physics, Characteristics, Reliability. Springer Berlin Heidelberg, 2011.

[20] J. B. Fedison and M. J. Harrison, "COSS hysteresis in advanced superjunction MOSFETs," 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), 2016, pp. 247-252, doi: 10.1109/APEC.2016.7467880.