Low-Voltage CMOS Bulk-Driven Buffer With Bootstrapping Technique for Gain Enhancement and THD–Noise Reduction

De La Cruz-Blas, Carlos A.
Institute of Smart Cities, IEEC Department
Public University of Navarre
Pamplona, Spain
carlos.aristoteles@unavarra.es

Carrillo, Juan M.
Dept. of Electrical, Electronic and Automation Engineering
University of Extremadura
Badajoz, Spain
jmcarcal@unex.es

***Abstract*—In this paper, a bootstrapping technique is applied to a bulk-driven voltage buffer for canceling the gate-source transconductance in order to improve the cell gain, the linearity and reduce the input-referred noise. The bootstrapped circuitry is conveniently implemented by only using a capacitor and a pseudo resistor. The suitability of the technique is demonstrated by simulation results using a flipped voltage follower, even though it is general and can be applied to other structures. A 1-V buffer is designed in 0.18 μm CMOS technology, showing a 4.3 times improvement in the voltage gain (conventional 0.21 V/V, bootstrapped 0.90 V/V), increasing 5 times the input voltage range for a 1% THD (conventional 50 mV, bootstrapped 250 mV) and reducing the input equivalent noise around a 16% (conventional 180 nV/$\sqrt{}$Hz, bootstrapped 155 nV/$\sqrt{}$Hz at 10 kHz).**

***Index Terms*—Bootstrapping, bulk-driven, linearized transconductor, quasi-floating gates.**

I. Introduction

Analog CMOS buffers can find applications as basic building blocks in filters, output stages of OPAMs, input drivers of ADCs, etc. Nowadays, the bulk-driven technique results appropriate in low-voltage CMOS analog design, since it allows operation with very low supply voltages and overcomes the non-zero threshold voltage constraint. Following this approach different voltage buffers have been previously reported [1]. Nevertheless, one of the main drawbacks of such technique is the reduction of the effective transconductance [2], due to the lower value of the bulk-source transconductance, g_{mb}, as compared to the gate-source transconductance, g_m. Thus, several techniques have been proposed to electronically enhance the effective transconductance of a circuit section, consequently increasing area and power consumption [3], [4].

To overcome this detrimental feature, a bootstrapping technique is proposed to be applied in a bulk-driven buffer. The scheme is based on the classical implementation used to increase a resistance electronically, i.e., by connecting a voltage buffer between the terminals of the device to be bootstrapped [5], [6]. In this case, the connection of a capacitor between the source and the gate of the driver transistor allows shorting these terminals for AC signals, thus canceling the contribution of the gate-source transconductance. Besides, a pseudo-resistor is required to properly set the DC operating point of the driver transistor and, hence, of the overall voltage follower. As a result, the performance of the cell is improved. The approach is similar to the quasi-floating gate transistor technique [7] in the sense that it requires a large resistor and a capacitor but, to the best of the Authors knowledge, this technique has not been proposed to reduce (increase) a conductance (resistance) using bootstrapping. Also in [8] several similar structures are presented, but the main principle of operation proposed here is different and novel.

This paper is organized as follows: Section II describes the proposed circuit along with the main parameters and is compared to the conventional solution. In Section III, gain, linearity, noise and Monte Carlo simulations, as well as their corresponding analyses, are reported. Finally, in Section IV some conclusions are remarked.

II. Circuit description

Fig. 1(a) shows a conventional bulk-driven flipped voltage follower, where the input voltage is applied to the bulk of transistor M_2, a bias voltage V_{bias} is applied to its gate to turn on the device, and the output voltage is obtained at the source. Note that transistor M_B and bias current I_{b2} are forming a voltage level shifter that is used to provide enough room to transistor M_2 to prevent it to enter in the triode region at low levels of V_{bias}. A negative feedback loop is established around transistors M_1, M_2, and M_B, which forces the current I_{b1} to flow through the drain of device M_2 and ensures a very low output resistance. Fig. 1(c) shows the equivalent small signal circuit and the main parameters of this cell are summarized in the second column of Table I, where g_{mi}, g_{mbi}, and r_i are the gate-source transconductance, the bulk-source transconductance, and the output resistance of transistor i, respectively. R_{D2} and R_{S2} are the equivalent resistances seen from the drain and source terminals of M_2, also respectively.

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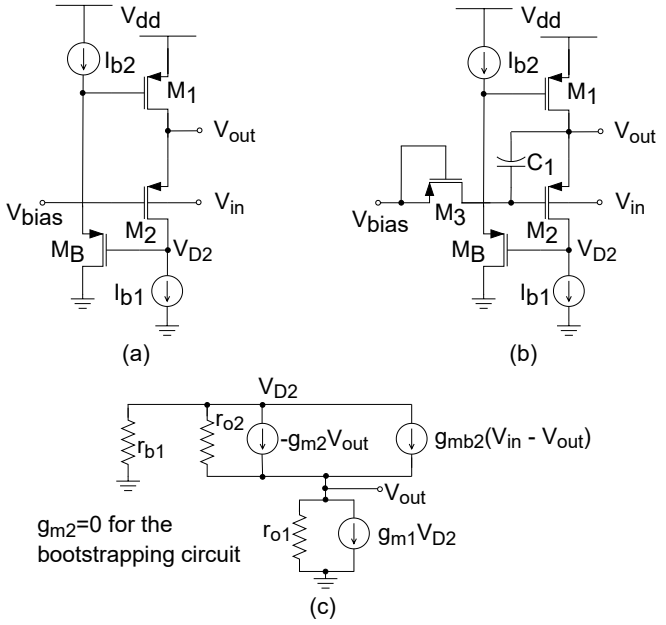


Fig. 1. (a) Conventional bulk-driven flipped voltage follower (b) Proposed bootstrapped version (c) Small–signal circuit of (a), for the case of (b) it is almost the same but $g_{m2} = 0$.

The proposed circuit is implemented by adding a capacitor C_1 between the gate and source terminals of M_2 and a cutoff transistor M_3 acting as a pseudo resistor between V_{bias} and the gate of M_2, as shown in Fig. 1(b). Note that these elements are the ones usually employed to design a bootstrapping circuit [6], but they are used here to cancel out the gate–source transconductance of transistor M_2, i.e., $g_{m2} = 0$ in Fig. 1(c), as compared to the circuit in Fig. 1(a). As a result, the corresponding small-signal expressions are modified accordingly for the proposed approach, as shown in the third column of Table I. Note that for the case of the voltage gain, the proposed circuit avoids the signal attenuation inherent in the bulk-driven technique. In return, the values of R_{out} and R_{S2} are incremented due to the cancellation of g_{m2}. On the other hand, the open loop gain is the same for both circuits, i.e., $g_{mb2}r_{o2}$, however, the loop gain is $(g_{m2} + g_{mb2})r_{o2}$ and $g_{mb2}r_{o2}$, for the conventional and bootstrapping version, respectively [9].

Next, the simulated performance of the proposed cell, accompanied by different analyses, is discussed in detail, illustrating the benefits and drawbacks of the bootstrapped buffer.

III. Simulation and analytical results

In order to provide more insight in the proposed cell, in this Section simulation results and analytical expressions are provided. They have been obtained using a standard 0.18 μm CMOS technology with the following aspect ratios for the common transistors $W_1/L_1 = 100$ μm/540 nm, $W_2/L_2 = 20$ μm/540 nm, $W_B/L_B = 1$ μm/540 nm, $I_{b1} = 10$ μA, and $I_{b2} = 1$ nA. For the bootstrapped implementation, transistor

TABLE I
Conventional and bootstrapping solution
small-signal parameter comparison

	Conventional	Bootstrapping
Gain	$\frac{g_{mb2}}{g_{m2}+g_{mb2}}$	≈ 1
R_{out}	$\frac{1}{g_{m1}(g_{m2}+g_{mb2})\cdot(r_{o2}\|\|r_{Ib1})}$	$\frac{1}{g_{m1}g_{mb2}\cdot(r_{o2}\|\|r_{Ib1})}$
R_{D2}	$\frac{1}{g_{m1}}$	$\frac{1}{g_{m1}}$
R_{S2}	$\frac{1}{g_{m2}+g_{mb2}}$	$\frac{1}{g_{mb2}}$
Open loop gain	$g_{mb2}r_{o2}$	$g_{mb2}r_{o2}$
Loop gain	$(g_{m2} + g_{mb2})r_{o2}$	$g_{mb2}r_{o2}$

M_3 ($W_3/L_3 = 240$ nm/340 nm) is connected as a pseudo resistor, implemented by a thick oxide device to obtain the technique benefits at low frequencies, and $C_1 = 0.2$ pF. The supply voltage was 1 V, both cells were loaded with a capacitor of 0.5 pF at its outputs, and V_{bias} was set equal to 0.1 V.

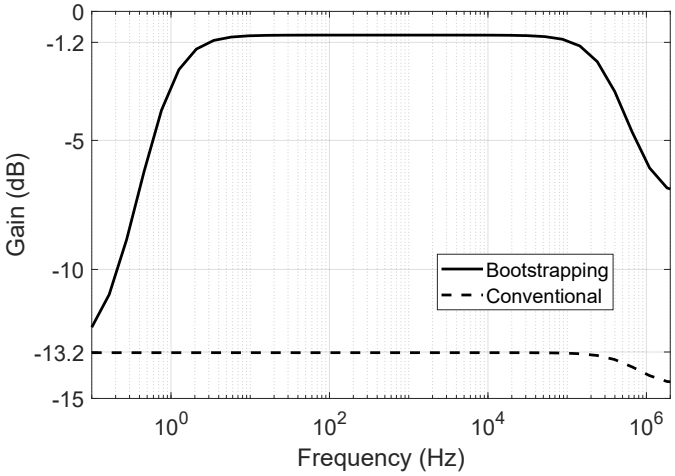


Fig. 2. Frequency response comparison of the conventional and bootstrapped buffers.

A. Gain, area, and power consumption

Fig. 2 shows a comparison of the AC small-signal response of the conventional and the bootstrapped buffers. It is worth to note that the technique operates properly for frequencies higher than 1 Hz, obtaining a gain of 0.21 V/V (-13.55 dB) and 0.90 V/V (-0.91 dB) for the conventional and the proposed cell, respectively. For obtaining operation at lower frequencies, capacitor C_1 should be made larger or the configuration of the pseudo resistor could be modified to increase its value. In the case of the high cutoff frequency, the proposed cell is lower than conventional one, since the output resistance of the proposed cell has been increased. The power consumption is the same in both designs, 10 μW (not including the bias circuits), whereas in terms of silicon area, the proposed buffer will require a 25% more due to the

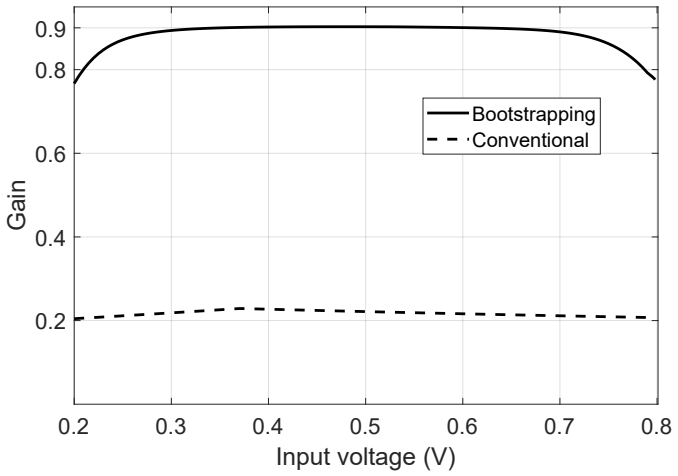


Fig. 3. Gain versus input voltage swept.

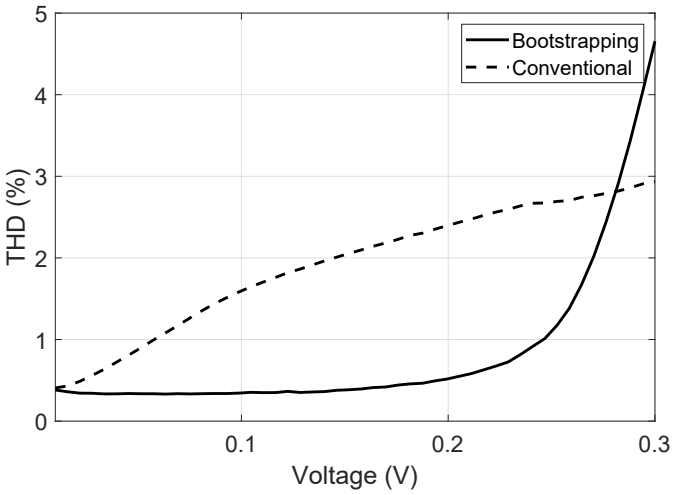


Fig. 4. THD comparison.

capacitor, even though this amount can be decremented if a larger value can be achieved for the pseudo resistor.

Fig. 3 shows the voltage gain of the conventional and bootstrapped buffers as a function of the input voltage in a range from 200 mV to 800 mV. Note that the gain of the proposed cell is more than four times higher than that of the conventional cell in the voltage range between 250 mV and 750 mV, and it is much closer to unity. In addition, the proposed cell has a more constant response than the conventional cell, leading to a more linear behavior, as it will be demonstrated in next Section.

B. THD analysis

Considering that the PMOS transistors in Fig. 1 operate saturated in the strong inversion region, and neglecting the channel length modulation effect, their drain current can be defined as $I_D = \frac{\beta}{2}(V_{SG} + V_{TH})^2$, with $V_{TH} = V_{TH0} - \gamma_P\left(\sqrt{2\phi + V_{BS}} - \sqrt{2\phi}\right)$, where β, V_{TH0}, ϕ, and γ_P are fabrication process constants with their usual meaning and V_{TH} and V_{TH0} are negative. Using this expression, it is possible to find a closed-form relationship between V_{out} and V_{in} for the circuits in Fig. 1. Indeed, the large-signal input/output voltage expression for the conventional cell is the solution of a quadratic function that can be written as follows:

$$V_{out} = \frac{-(2A + \gamma_P^2) \pm \sqrt{\gamma_P^4 + \gamma_P^2\,(4A + 8\phi) + 4\gamma_P^2 V_{in}}}{2} \tag{1}$$

with $A = -V_{bias} + V_{TH0} + \gamma_P\sqrt{2\phi} - \sqrt{\frac{2I_D}{\beta}}$. An evident non-linear behaviour can be observed in the input/output transfer characteristic of the conventional voltage follower. On the other hand, the $V_{out} - V_{in}$ transfer characteristic of the proposed buffer is inherently linear and given by:

$$V_{out} = 2\phi - \frac{A^2}{\gamma_P^2} + V_{in} \tag{2}$$

As inferred from (2), the linearity of the proposed cell is improved since the AC signal at the source terminal of M_2 is copied to its gate, allowing the input/output voltage relationship to become linear and, hence, the THD performance is better for the proposed bootstrapped buffer as compared to the conventional approach.

Fig. 4 shows the simulated THD comparison for a sinusoidal input signal of 1 kHz with an amplitude swept from 10 mV to 300 mV. The dominant distortion contribution in both cases is due to the second-order harmonic. Note that the proposed cell has a THD lower than 1 % for input signals up to 240 mV, with an output voltage of 216 mV, whereas for the conventional cell an input signal of only 50 mV, corresponding to an output voltage of 10 mV, is allowed to achieve the same distortion level. This represents an increase of almost 5 and 20 times of the maximum input and output signal levels, respectively, that can be processed.

C. Noise analysis

A straightforward analysis of the noise equivalent circuit of the conventional buffer reveals that the power spectral density of the input-referred noise is:

$$\begin{aligned}\frac{\overline{n_{iC}^2}}{\Delta f} = \frac{\overline{i_{n1}^2}}{\Delta f}\frac{1}{g_{m1}^2 g_{mb2}^2 (r_{o2} \parallel r_{Ib1})^2} + \frac{\overline{i_{n2}^2}}{\Delta f}\frac{1}{g_{mb2}^2} \\ + \frac{\overline{i_{nb1}^2}}{\Delta f}\frac{(g_{m2} + g_{mb2})^2}{g_{m1}^2 g_{mb2}^2}\end{aligned} \tag{3}$$

where the subscripts of the noise current sources correspond to the transistors in Fig. 1, and the noise contribution of device M_B has been neglected since the value of its current is much lower than the current flowing through transistors M_{1-2}. On the other hand, for the bootstrapped version we have:

$$\frac{\overline{n_{iB}^2}}{\Delta f} = \frac{\overline{i_{n1}^2}}{\Delta f}\frac{1}{g_{m1}^2 g_{mb2}^2 (r_{o2} \parallel r_{Ib1})^2} + \frac{\overline{i_{n2}^2}}{\Delta f}\frac{1}{g_{mb2}^2} + \frac{\overline{i_{nb1}^2}}{\Delta f}\frac{1}{g_{m1}^2} \tag{4}$$

As it can be seen in (3) and (4), the first two noise contributions are equal, because the ratio of R_{out} to gain and

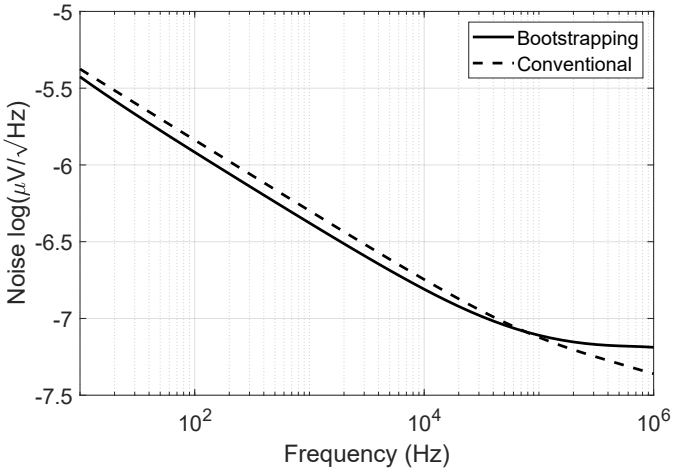


Fig. 5. Noise comparison. The Y axis is the logarithm of the input power spectrum density to illustrate more clearly the tendencies.

R_{S2} to gain are the same in both circuits. The difference relies on the last term, related to the ratio of R_{D2} to gain, which is different in both implementations. Subtracting both equations and defining $g_{mb2} = \eta g_{m2}$ and $g_{mb2} = \lambda g_{m1}$, the extra noise for the conventional buffer is:

$$\frac{\overline{n_{iC}^2}}{\Delta f} - \frac{\overline{n_{iB}^2}}{\Delta f} = \frac{\overline{i_{nb1}^2}}{\Delta f} \frac{\frac{2\lambda^2}{\eta} + \frac{\lambda^2}{\eta^2}}{g_{mb2}^2} \tag{5}$$

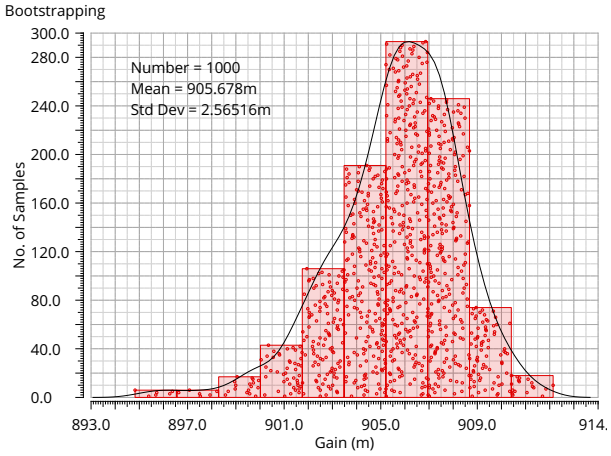
In Fig. 5 it is evidenced by simulations that the noise corresponding to the bootstrapped buffer is lower than in the conventional solution, according also to the prediction in (5).

D. Monte Carlo simulations of the gain

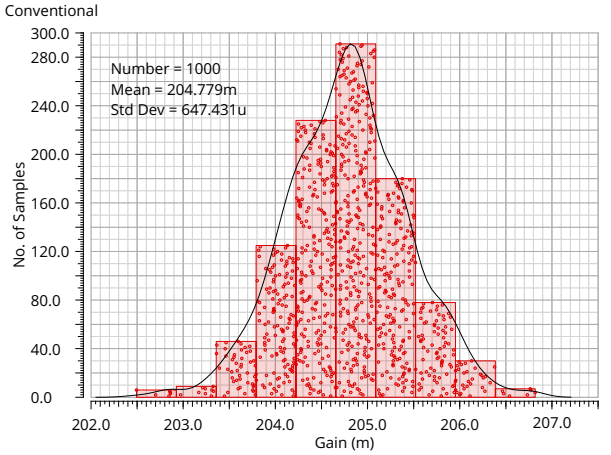
In order to know the gain robustness of the proposed and the conventional circuit against variations in the fabrication process, a 1000-run Monte Carlo simulation considering mismatches and process variations has been performed and the corresponding results are shown in Figs. 6(a) and 6(b), respectively. The variability of each implementation, defined as σ/μ, is equal to 2.8% and 3.2% for the bootstrapped and the conventional solution, respectively, which shows a similar behavior for both approaches despite the much larger value of the voltage gain for the proposed approach.

IV. Conclusions

In this paper, a novel bulk-driven buffer using a bootstrapping section is introduced. The technique is applied using a capacitor and a pseudo resistor implemented by a cutoff MOS transistor, which allows keeping the same power consumption as the conventional counterpart. The proposed circuit has been designed in 0.18-μm CMOS technology to operate with a 1-V supply and simulation results have been reported to demonstrate the benefits of the technique. The solution presented leads to increased voltage gain, higher linearity, and lower input-referred noise.



(a)



(b)

Fig. 6. Monte Carlo simulation results of (a) the proposed and (b) the conventional cell gain based on a 1000-run analysis.

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