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Class AB Amplifier with Enhanced Slew Rate and GBW

Abstract

The design of a micropower class AB operational transconductance amplifier with large dynamic current to quiescent current ratio is addressed. It is based on a compact and power-efficient adaptive biasing circuit and a class AB current follower using the Quasi-Floating Gate (QFG) technique. The amplifier has been designed and fabricated in a 0.5 μm CMOS process. Simulation and measurement results show a slew rate (SR) improvement factor versus the class A version larger than 4 for the same supply voltage and bias currents, as well as enhanced small-signal performance.

Keywords Current followers, Current amplifiers, Analog integrated circuits, CMOS integrated circuits, Class AB circuits.

1. INTRODUCTION

Power efficiency is critical in several current application scenarios of VLSI circuits requiring portable and/or wearable devices. A key building block in these systems in terms of power budget is the operational transconductance amplifier (OTA) [1]. Single-stage OTA topologies are best suited to get high power efficiency [2]. The single-stage telescopic cascode OTA [3] provides both high gain and high current efficiency [4], but it has limited output swing as the input transistors are at the output branch. To solve it preserving the single-stage configuration, a current follower (CF) or current amplifier (CA) can be used to convey to the output branch (and scale by factor K>1 with the CA) the signal current generated at the differential pair. This is shown in Fig. 1(a). The CF/CA has low input impedance (ideally a signal ground) to sense the input current without adding low-frequency poles or zeros, and high-impedance output to achieve large amplifier gain.

Two common implementations of this block, using current mirrors and common-gate amplifiers, are shown in Figs. 2(a) and 2(b), respectively [5]. The common-mode feedback (CMFB) circuit is not shown for simplicity. The circuit of Fig. 2(b) is simpler, but it cannot implement a CA since it cannot provide current gain (hence K=1). When the circuits of Figs. 2(a) and 2(b) are applied to the circuit of Fig. 1(a), the conventional cascode current mirror (CCM) OTA and folded cascode (FC) OTA result, respectively. The CCM and FC OTAs essentially keep the gain and bandwidth of the telescopic cascode amplifier and at the same time improve the output range. Note that in these arrangements the differential pair already provides an input bias current I_B to the CF/CA, so the input bias current sources I_B in Fig. 2(a) are not needed for the CCM OTA and the bottom current sources in Fig. 2(b) are $2I_B$ for the FC OTA.

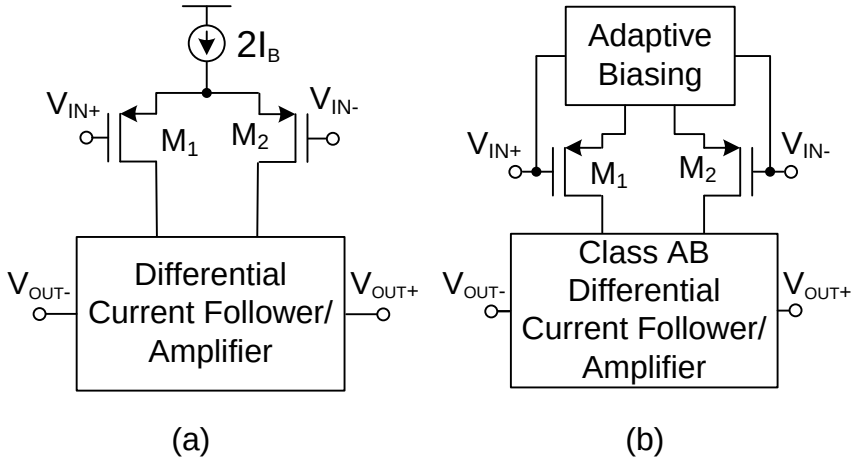


Figure 1. (a) Conventional single-stage class A amplifier (b) Proposed single-stage class AB amplifier.

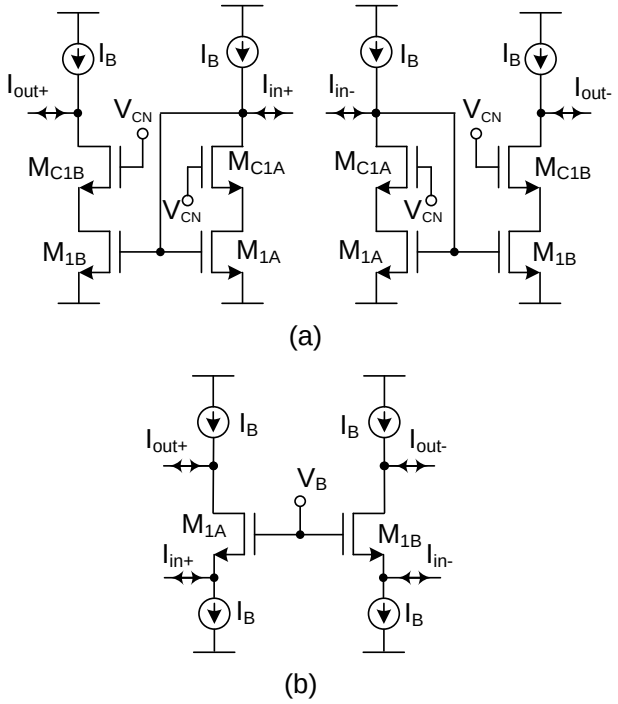


Figure 2. Differential current follower (a) with current mirrors (b) with common-gate transistors.

A limitation of the topology of Fig. 1(a) is that it operates in class A, yielding maximum output currents limited by the bias current. Thus the maximum output current of the FC OTA is $2I_B$ and for the CCM OTA it is $2KI_B$, with K the current mirror gain. This leads to a tradeoff between static power consumption and dynamic performance. To overcome this issue, adaptive biasing can be applied to the differential pair. Hence low quiescent currents can be used in the differential pair and at the same time large dynamic currents not bounded by the quiescent currents are generated for large input signals, yielding class AB operation. Several class AB amplifiers have been reported with different adaptive biasing techniques, e.g. [6]-[17]. However, the CF/CA is often unchanged [17], which may limit the power efficiency and dynamic performance of the

OTA. This paper addresses the design of such CF/CA required to achieve efficient class AB amplifiers. As an application example, a novel class AB OTA is presented.

2. CIRCUIT DESCRIPTION

The proposed single-stage class AB amplifier corresponds to the topology shown in Fig. 1(b), combining adaptive biasing of the differential pair and a class AB CF/CA. There are several choices for the adaptive biasing circuit. For instance, three alternatives are presented in [4]. In this paper, two floating DC batteries have been cross-coupled to the differential pair transistors, as shown in Fig. 3(a). These batteries are implemented by the Flipped Voltage Followers (FVFs) [18] M_3-M_5 and M_4-M_6, biased with a DC current I_B, as shown in Fig. 3(b). The resulting DC voltage is $V_B = V_{SG3} = V_{SG4}$. Under quiescent conditions $V_{SG1}^Q=V_{SG2}^Q=V_{SG3}^Q=V_{SG4}^Q=V_B$, hence M_1, M_2, M_3 and M_4 have equal quiescent current I_B despite process, supply voltage or temperature (PVT) variations. This quiescent current can be very low to save power. However, for a nonzero input signal $V_{id}= V_{in+}-V_{in-}$ voltage V_{SG1} is increased by V_{id} and voltage V_{SG2} is decreased by V_{id}. This leads to dynamic currents not limited by I_B. Also an increment in transconductance by a factor 2 is obtained compared to the constant biasing of Fig. 1(a), where only $V_{id}/2$ is added to V_{SG1} and subtracted from V_{SG2}.

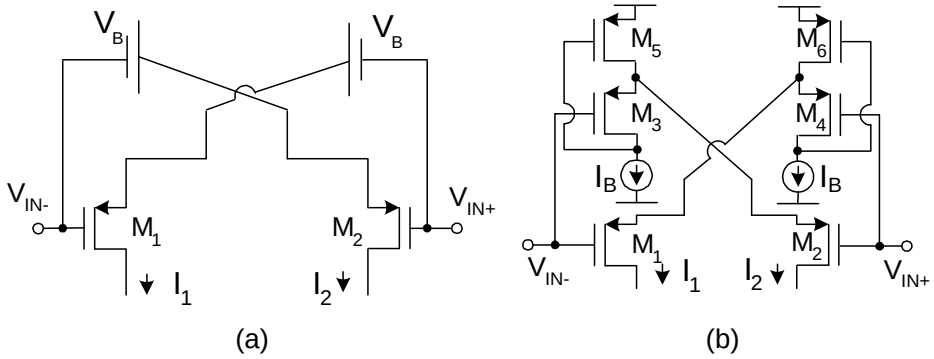


Figure 3. Adaptive biasing (a) Diagram (b) Implementation using FVFs.

The differential CF/CA employed is shown in Fig. 4. It is based on the differential high-swing current mirror implementation of Fig. 2(a). Current gain is given by $K=(W/L)_{MN2}/(W/L)_{MN1}=(W/L)_{MP2}/(W/L)_{MP1}$. Two modifications are included compared to the circuit of Fig. 2(a). First, the input current is sensed at the source of M_{CN1}-M_{CN2}, in order to benefit from the reduced input resistance at this node due to the FVF feedback loop. Second, the quasi-floating gate (QFG) technique [4, 16, 19, 20] is applied to achieve class AB operation. It is based on including two capacitors C_{bat} and two high-resistance pseudo-resistors M_{PR}. In quiescent operation these new devices have no effect since capacitors act as open circuits and there is no current flowing through transistors M_{PR}. However, when a positive differential input current $I_{ind}=I_{in+}-I_{in-}$ appears, voltage at

node A increases and voltage at node B decreases. Due to the large value of the equivalent leakage resistance R_{large} of the pseudo-resistors M_{PR}, capacitors C_{bat} cannot discharge rapidly so that they behave as floating batteries, transferring voltage variations from nodes A and B to nodes C and D, respectively. The increased voltage at node C reduces the current flowing through transistors M_{P1}-M_{P2} at the left-hand side, and the decreased voltage at node D boosts the current flowing through transistors M_{P1}-M_{P2} at the right-hand side above I_B, so currents I_{in-} and I_{out-} flowing out can be larger than I_B and KI_B, respectively. When a negative differential input current $I_{ind}=I_{in+}-I_{in-}$ appears, now voltage at node A decreases and voltage at node B increases, yielding a decrease at node C and an increase at node D. Hence currents I_{in+} and I_{out+} flowing out can be much larger than I_B and KI_B, respectively. The end result is that $I_{out+}=KI_{in+}$, $I_{out-}=KI_{in-}$ and therefore $I_{outd}=KI_{ind}$ for input currents not limited by I_B and output currents not limited by KI_B. Consequently, positive and negative input currents larger than I_B can be applied to either input terminal without compromising dynamic performance.

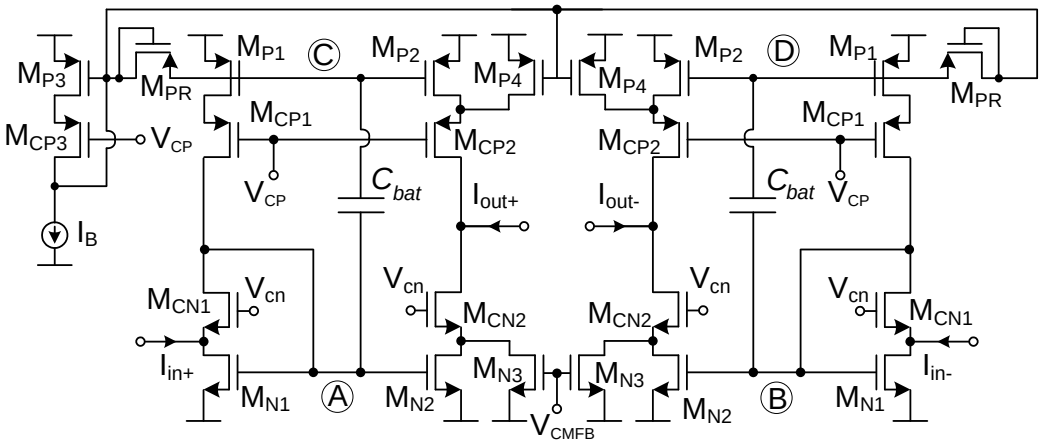
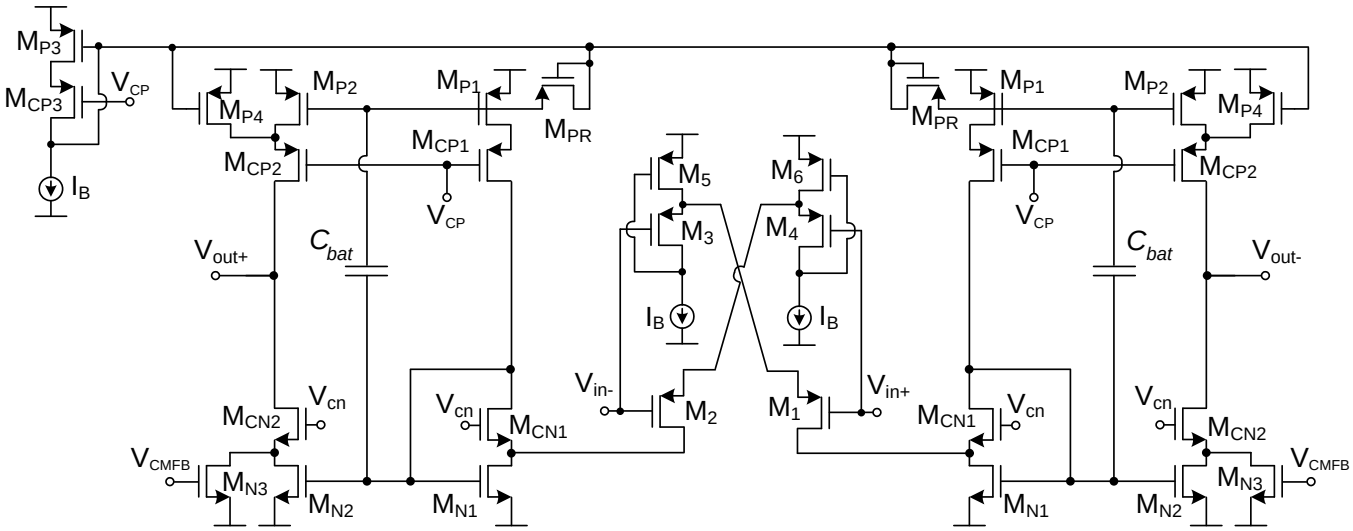


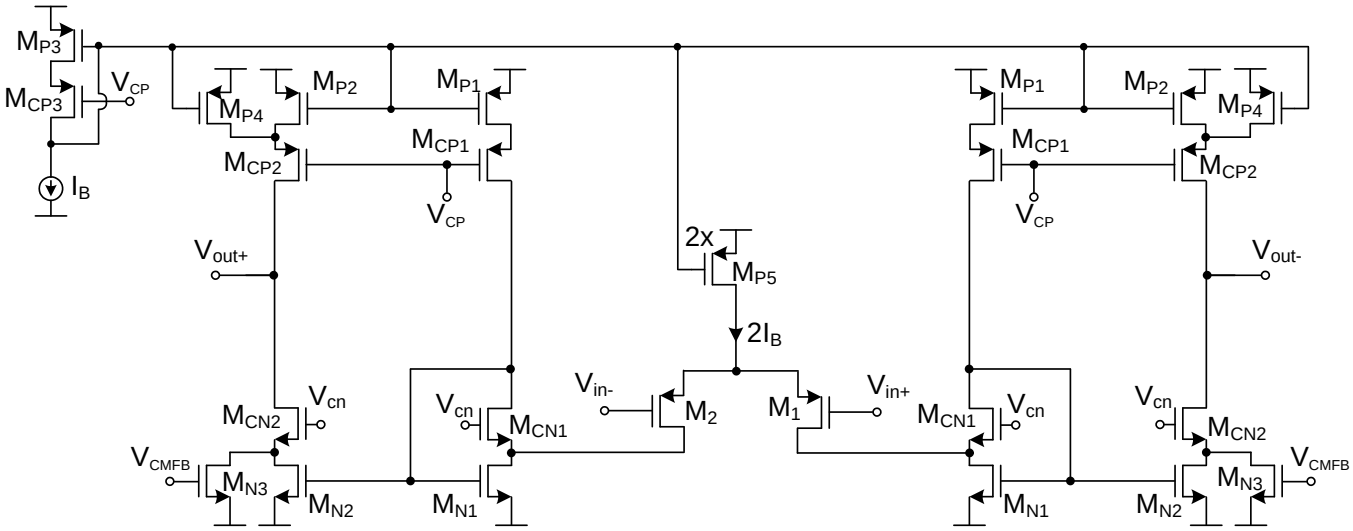
Figure 4. Class AB differential CF/CA using QFG techniques.

The capacitive divider formed by C_{bat} and the intrinsic capacitance C_P at the gate of M_{P1}-M_{P2} leads to attenuation in the voltage transfer from nodes A to C (and B to D) given by the expression $\alpha=C_{bat}/(C_{bat}+C_P)$. Moreover, the signal transferred to these nodes is also high-pass filtered by the first order RC filter formed by C_{bat} and M_{PR}, with cutoff frequency $f_{-3dB}=1/[2\pi R_{large}(C_{bat}+C_P)]$. Due to the extremely large value of R_{large} and the typically low value of C_P, a $f_{-3dB} < 1$ Hz and $\alpha > 0.75$ can be achieved with $C_{bat} \approx 1$ pF. Hence in practice all the AC components of voltage at nodes A and B can be transferred to nodes C and D with low attenuation for a modest increase in silicon area.

The detailed schematic of the proposed amplifier of Fig. 1(b) using the adaptive biasing of Fig. 3 and the CF/CA of Fig. 4 is shown in Fig. 5(a). A conventional CMFB circuit, based on a differential difference amplifier [21] was employed. It is shown in Fig. 6.



(a)



(b)

Figure 5. (a) Proposed class AB amplifier (b) Class A amplifier used for comparison

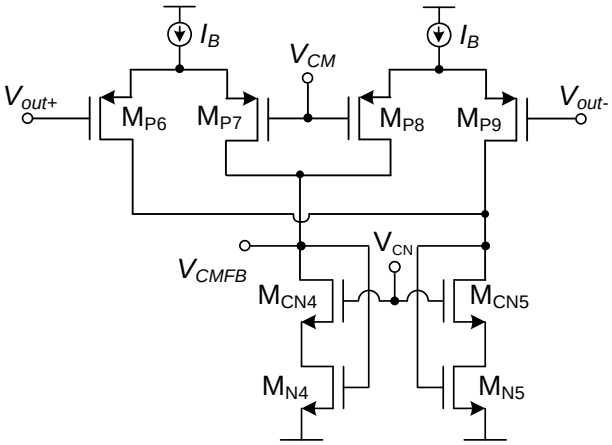


Figure 6. Common-mode feedback circuit.

Alternatively, the gate of M_{P1} can be connected directly to the gate of M_{P3} in Fig. 5(a). This way the CF/CA does not operate linearly and the maximum current leaving the CF/CA input is limited to I_B, but for the circuit of Fig. 5(a) this is not a limitation (currents always enter the CF/CA and CF/CA nonlinearity is not critical in closed-loop operation). This reconnection provides a slight extra slew rate increase.

2.1. Small-Signal Transconductance, Gain, GBW and PM

The small-signal transconductance of the proposed class AB OTA is

$$G_{mAB}=2Kg_{m1} \tag{1}$$

with g_{m1} the transconductance gain of differential pair transistors M_1 and M_2. Factor 2 is due to the adaptive biasing employed, as described above. The output resistance of the OTA is

$$R_{oAB} \approx g_{mCP2}r_{oCP2}\left(r_{oP2} \parallel r_{oP4}\right) \parallel g_{mCN2}r_{oCN2}\left(r_{oN2} \parallel r_{oN3}\right) \tag{2}$$

with r_i the drain-source resistance of transistor M_i. Hence the DC gain is $A_{DC}=G_{mAB}\cdot R_{oAB}$.

As a single-stage amplifier, it is load compensated and the dominant pole $\omega_{p1} = -1/(R_{oAB}\, C_L)$ is set by the output terminal, with C_L the load capacitance (also including any parasitic capacitance at the output node). Hence no extra compensation capacitance is required to enforce closed-loop stability. The GBW is

$$GBW_{AB} = \frac{Kg_{m1}}{\pi C_L} \tag{3}$$

The main non-dominant pole is set by the gate of M_{N1}-M_{N2} and is given by $\omega_{p2} \approx -g_{mN1}/C_{pN}$ with C_{pN} the parasitic capacitance at this node, which is approximately $C_{pN} \approx C_{GSN1}+C_{GSN2}+C_{bp}+\alpha(C_{GSP1}+C_{GSP2}+C_{tp})$, with C_{GSi} the gate-source capacitance of transistor M_i and C_{tp} and C_{bp} the top plate and bottom plate parasitic capacitance of C_{bat}, respectively. Since C_{bat} is implemented in this work as a poly-poly capacitor, $C_{tp} \approx 0.001C_{bat} \approx 1$ fF and $C_{bp} \approx 0.01C_{bat} \approx 10$ fF. As $C_{GSi}=(2/3)W_iL_iC_{ox}+W_iL_{ov}C_{ox}$ (with C_{ox} the gate oxide capacitance per unit area and L_{ov} the effective gate-source overlap distance), C_{GSi} is proportional to W_i and therefore $C_{GSN2}=K\cdot C_{GSN1}$ and $C_{GSP2}=K\cdot C_{GSP1}$ so $C_{pN} \approx (1+K)(C_{GSN1}+\alpha C_{GSP1})+0.01C_{bat}$. The phase margin (PM) becomes

$$PM \approx 90° - tan^{-1}\left(\frac{GBW}{f_{P2}}\right) \approx 90° - tan^{-1}\left(2K\frac{g_{m1}}{g_{mN1}}\frac{C_{pN}}{C_L}\right) \approx$$
$$90° - tan^{-1}\left(2K\frac{g_{m1}}{g_{mN1}}\frac{(1+K)(C_{GSN1}+\alpha C_{GSP1})+0.01C_{bat}}{C_L}\right) \tag{4}$$

Note the tradeoff between PM and GBW that represents the choice of K, and that larger K values can be used for larger C_L. For instance, from (4) to have a PM≈70º then f_{p2}=3GBW, which neglecting C_{bp} leads to

$$K = \sqrt{\frac{g_{mN1}}{6g_{m1}}\frac{C_L}{C_{GSN1}+\alpha C_{GSP1}}+\frac{1}{4}}-\frac{1}{2} \tag{5}$$

Hence, PM≈70º for K=1 is obtained with C_L=12(g_{m1}/g_{mN1})($C_{GSN1}+\alpha C_{GSP1}$). The analysis is only approximate as other parasitic terms in C_{pN} and other non-dominant poles have been neglected to make the expressions tractable, but it is useful to illustrate the main design tradeoffs affecting GBW, PM and K.

2.2. Slew Rate

Using the simple square law model for the MOS transistor in strong inversion and saturation, an approximate expression for slew rate (SR) can be obtained. For a large positive differential input voltage $V_{id}=V_{in+}-V_{in-}$, current in M_1 is [4]

$$I_1 = \frac{\beta_1}{2}\left(\sqrt{\frac{2I_B}{\beta_4}} + V_{id}\right)^2 \tag{6}$$

with $\beta_i=\mu_p C_{ox}(W/L)_i$, and current in M_2 becomes negligible. This large current is conveyed to the output by the circuit of Fig. 4. Hence for a differential input step of A Volts, the SR_+ is

$$SR_{AB+} \approx \frac{K\beta_1}{2C_L}\left(\sqrt{\frac{2I_B}{\beta_4}} + A\right)^2 \tag{7}$$

Likewise, for a large negative differential input step of amplitude -A the SR_- is

$$SR_{AB-} \approx \frac{K\beta_2}{2C_L}\left(\sqrt{\frac{2I_B}{\beta_3}} + A\right)^2 \tag{8}$$

In practice SR values are lower due to second-order effects not considered in the simple MOS square law model, and because some transistors can leave saturation for large transients. This latter effect is specially relevant for transistors M_{N1}, M_{N2}, M_{P1} and M_{P2} since cascode transistors M_{CN1}, M_{CN2}, M_{CP1} and M_{CP2} limit their V_{DS} voltage and can make them enter triode mode for large dynamic currents. To mitigate this issue dynamic biasing of the cascode transistors can be implemented using the QFG technique [19].

Note that the SR for the class A version of Fig. 1(a) using the same bias current is proportional to I_B:

$$SR_{A+} = SR_{A-} = \frac{2KI_B}{C_L} \tag{9}$$

2.3. Noise Analysis

Considering thermal noise and assuming that all transistors operate in strong inversion and saturation, the equivalent input noise of the amplifier is

$$\overline{v_{n,inAB}^2} = \frac{4k_B T\Delta f}{3g_{m1}^2} \times \left(\frac{g_{m1} + g_{m4} + g_{mN1} + g_{mP1} + g_{mP2} + g_{mP4} + g_{mN2} + g_{mN3} + g_{mN4}}{K^2} \right) \quad (10)$$

with k_B the Boltzmann's constant and T the absolute temperature. Note that as expected the influence of the output branch transistors decreases for larger K when referred to the input. The CMFB circuit does not influence noise as its noise is cancelled by the differential output arrangement.

3. DESIGN METHODOLOGY

It is complicated to provide a generic design methodology for the amplifier proposed, since the design tradeoffs to be made depend on the specific application. However, usually what is required is to optimize GBW, PM and SR. Therefore the starting point for the design are expressions (3), (4), (7) and (8), valid for preliminary hand-calculation design. Finer adjustment can be made during simulation. Conventional design practices can be used for selecting the aspect ratios of the transistors [1]. This way, input transistors M_1, M_2, M_3 and M_4 usually have large aspect ratio to have them biased in moderate or even weak inversion, hence enhancing GBW and reducing input offset and noise.

The value of C_{bat} is chosen as low as possible to reduce silicon area and parasitic capacitance at the gates of M_{N1}-M_{N2} and M_{P1}-M_{P2}. As described in Section 2, this minimum value is set by the maximum tolerable attenuation in the voltage transfer from nodes A to C (and B to D) in Fig. 4 and is around $C_{bat} \approx 1$ pF in the CMOS technology employed. Process, supply voltage and temperature (PVT) variations or nonlinearity of the pseudo-resistor employed is not relevant as long as its resistance R_{large} remains large enough to get a cutoff frequency $f_{\text{-3dB}}=1/[2\pi R_{large}(C_{bat}+C_P)]$ higher that the lowest signal component. Therefore, the simplest pseudo-resistor is employed, implemented by a single minimum-size PMOS transistor as shown in Fig. 4.

A critical design choice in our proposal is the value of K, as it represents a tradeoff between GBW and SR enhancement, reduction of input noise and PM, and increase of power and silicon area. In order to evaluate the effect of K, two common figures of merit are used: $\text{FoM}_L=\text{SR}\cdot C_L/I_{supply}$ where I_{supply} is the total quiescent current consumption, which evaluates large-signal performance versus quiescent power, and $\text{FoM}_S=100\cdot\text{GBW}\ C_L/I_{supply}$ (MHz·pF/μA) which reflects small-signal performance versus quiescent power. From (3) and (7) and noting that $I_{supply}=4(K+2)I_B$ (including the CMFB current consumption), both FoM_L and FoM_S become proportional to $K/(K+2)$. Hence $K>1$ values are beneficial if PM and power constraints allow it, although the improvement is soon becoming lower as K increases. This is because the K factor scales both quiescent and signal currents. A suggested approach is as follows: once a power constraint (hence

maximum I_B), load capacitance C_L and minimum required PM is set, the maximum K that can be employed can be estimated from (4)-(5). Then GBW and SR can be estimated (to a first order approach) using (3) and (7)-(8). Finally, simulations can be carried out to refine the K value.

4. SIMULATION AND MEASUREMENT RESULTS

The class A and class AB amplifiers of Figs. 1(a) and 1(b), with detailed schematic shown in Figs. 5(b) and 5(a), respectively, were simulated with Cadence DFWII. A 0.5 μm CMOS n-well process with nominal nMOS and pMOS threshold voltages of 0.64 V and –0.92 V was used. The CF/CA used in the circuit of Fig. 5(b) is the same as in Fig. 4, but without capacitors C_{bat} and pseudo-resistors M_{PR}. The transistor aspect ratios, quiescent currents I_Q and simulated small-signal transconductances g_m are shown in Table I. Capacitors C_{bat} have a value of 850 fF. Supply voltages were ±1 V, and bias current I_B was 10 μA. Cascode bias voltages V_{CP} and V_{CN} were set to -0.3 V and 0.2 V, respectively. Load capacitance was C_L=25 pF.

Table I. Transistor parameters

Transistor	**W/L** (μm/μm)	I_Q (μA)	g_m (μA/V)
M_1, M_2, M_3, M_4	100/1	I_B	190
M_5, M_6	30/0.6	$2I_B$	260
M_{N1}, M_{N2}	60/1	$2I_B$	380
M_{CN1}	60/0.6	I_B	230
M_{CN2}	60/0.6	$3I_B$	620
M_{P1}, M_{P2}, M_{P3}	100/0.6	I_B	200
M_{P4}, M_{P5}	200/0.6	$2I_B$	400
M_{P6}, M_{P7}, M_{P8}, M_{P9}	30/1	$I_B/2$	80
M_{CP1}, M_{CP3}	200/0.6	I_B	220
M_{CP2}	200/0.6	$3I_B$	580
M_{N3}, M_{N4}, M_{N5}	15/1	I_B	130
M_{CN4}, M_{CN5}	60/0.6	I_B	220
M_{PR}	1.5/1	0	0

Figure 7 shows the simulated open loop AC small signal response of both amplifiers. The DC gain of the class A and class AB amplifiers is 54.9 dB and 61.5 dB respectively. This improvement is mainly due to the extra 6 dB provided by the adaptive biasing topology of Fig. 3. The GBW of the class A and class AB amplifiers is 1.07 MHz and 2.31 MHz, respectively. Note the increase in GBW by a factor >2.

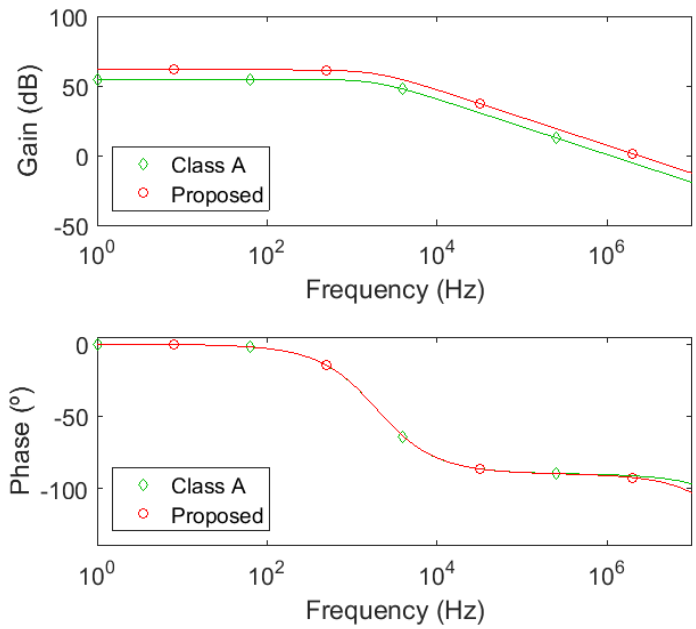


Figure 7. Simulated open-loop frequency response.

The phase margin of the class A and class AB amplifiers is 89.3º and 87º, respectively. At 2.31 MHz the phase margin of the class A amplifier is 88º, hence a degradation of just 1º is observed for the class AB version.

The transient response of the amplifiers was simulated connecting them in unity gain configuration using passive feedback resistors of R=100 kΩ, as shown in Fig. 8, and the same C_L=25 pF. A 100 kHz 0.4 V differential input square was applied to the input. Figure 9 shows the simulated output of the amplifiers. Note the stable and faster settling of the proposed class AB amplifier. The SR of the class A amplifier is 0.62 V/µs, while the SR of the proposed class AB amplifier is 2.7 V/µs, i.e., >4 times higher for the same quiescent current and load.

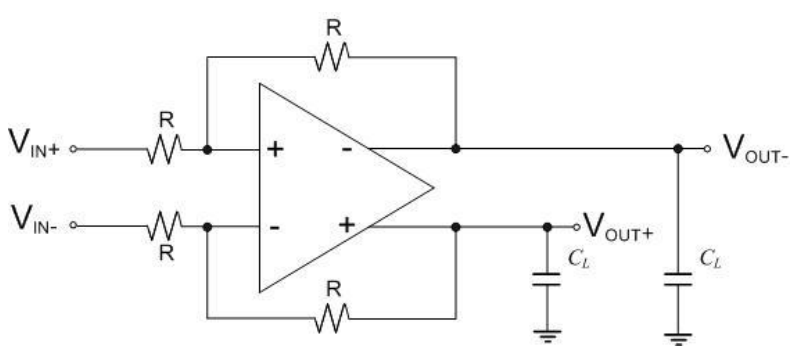


Figure 8. Unity gain configuration scheme.

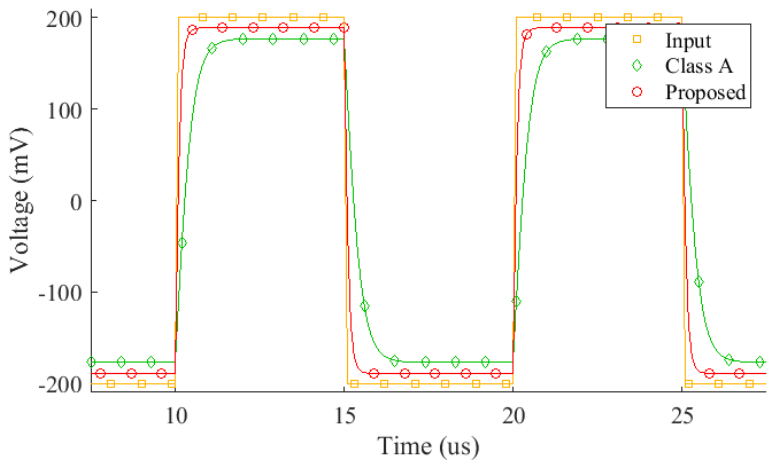


Figure 9. Simulated transient response.

Figure 10 shows the simulated Total Harmonic Distortion (THD) using a 100 kHz differential input tone of different amplitude. Note the improved linearity of the proposed amplifier, due to the enhanced dynamic performance.

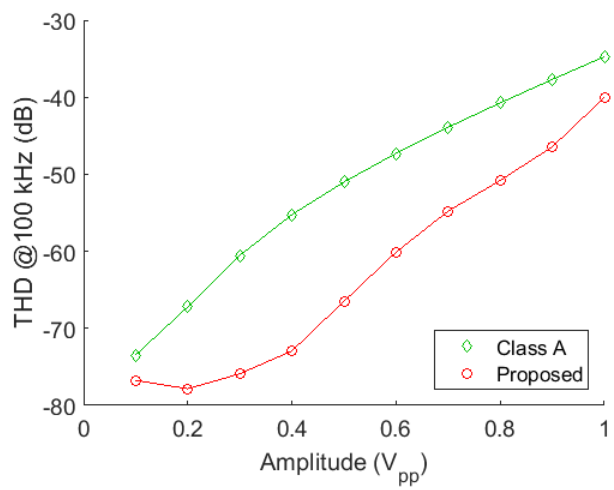


Figure 10. Simulated THD vs input amplitude at 100 kHz.

Table II**.** Simulated SR, GBW and PM for different *K* and C_L values

	C_L=5 pF			**C_L=25 pF**		
K	**SR (V/µs)**	**GBW (MHz)**	**PM (º)**	**SR (V/µs)**	**GBW (MHz)**	**PM (º)**
1	9.2	11.3	75	2.7	2.3	89
2	15.8	22.4	57	5	4.6	83
3	21.3	32.2	35	6.5	6.9	80

Table II shows the simulated SR, GBW and PM for different K values and two load capacitances. Note the improved SR and GBW values for larger K as expected, but that depending on the load capacitor the PM degradation can be significant. Hence, as discussed in section 2, larger C_L allows using larger K. Note however that static power consumtion also increases with K, limiting the FoM_L and FoM_S improvement.

The class AB amplifier in the arrangement shown in Fig. 8 was fabricated in the same 0.5 μm double-poly n-well CMOS technology used for the simulations. In our target application the amplifier is used with C_L=2pF, so a K=1 was required despite the subobtimal FoM_L and FoM_S achieved. On-chip resistors R were made by a high resistance polysilicon layer available in the technology. The outputs were directly connected to bonding pads. As no load capacitors were used off-chip, load capacitance in the measurements corresponds to the pad, board and test probe capacitance. Its approximate value is 25 pF, which is estimated using a PM6303 RCL meter. Figure 11 shows a microphotograph of the class AB amplifier, enclosed by the white rectangle. The silicon area required is 500 μm x 150 μm. Supply voltage as well as bias currents/voltages employed for the measurements were the same as for the simulations.

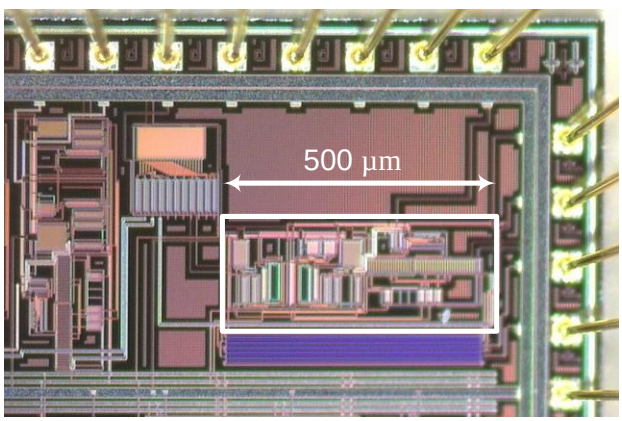


Figure 11. Test chip microphotograph.

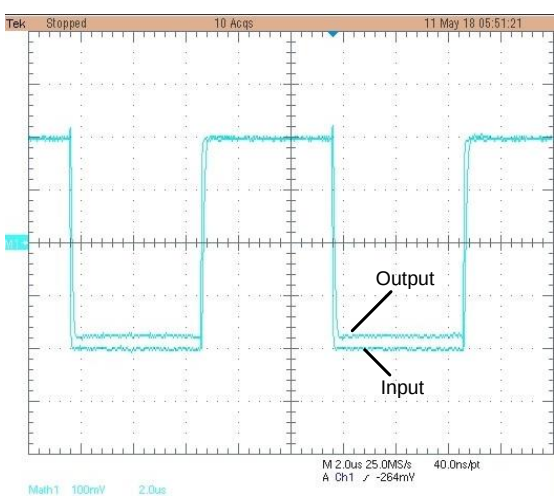


Figure 12. Measured transient response.

Measurements were carried out by generating a differential input signal using the Keysight 33522A function generator, and capturing the differential output signal by the Tektronix TDS5104 oscilloscope. Figure 12 shows the measured response to a 0.4 V 100 kHz periodic input square waveform. The measured SR is 3.4 V/µs, in close agreement with the simulation results.

Table III summarizes the main measurement results of the amplifier and other reported class AB amplifiers. The DC gain and PM were only simulated as it is very difficult to measure them for high-gain open-loop amplifiers. Note the competitive performance of the proposed amplifier versus state-of-the-art alternatives. The main drawback is a small area increase due to the capacitors C_{bat} and the adaptive biasing. Proposals in [7]-[9],[11] achieve higher FoM_S but they are multi-stage topologies featuring more complex settling behavior [22] and requiring compensation capacitors, which demand extra area and current to drive them [2].

Table III**.** Summary of measurement results and performance comparison

Parameter	**This work**	**[6]**	**[7]**	**[8]**	**[9]**	**[10]**	**[11]**	**[12]**	**[13]**	**[14]**
Simulated/Measured	Meas	Meas	Meas	Meas	Meas	Sim	Sim	Sim	Meas	Meas
CMOS process (nm)	500	350	500	350	500	90	50	40	180	180
Nº of gain stages	1	1	2	2	3	3	2	1	1	1
Supply voltage (V)	±1	0.9	3.3	1	±1.25	1.2	0.4	1.2	1.8	0.8
Capacitive load (pF)	25	10	30	15	25	2	20	0.5	200	8
SR (V/µs)	3.4	0.25	24	2.53	2.7	488	0.86	538	74.1	0.14
THD @100kHz	-47 dB @0.5V_{pp}	--	-54dB @1V_{pp}	--	-47.1 dB @2V_{pp}	--	--	--	--	--
DC Gain[a] (dB)	61.5	65	68	88.3	63.4	72.4	60	51.5	72	51
PM[a] (º)	89	60	73	66.1	83	63.8	56	59	50	60
GBW (MHz)	2.31	1	21.8	11.67	4.9	121	2.2	347	86.5	0.057
CMRR @DC (dB)	90	45	75	40	80	--	80	253	--	--
PSRR+ @DC (dB)	51	--	78	40	61.2	--	--	--	--	--
PSRR-@DC (dB)	50	--	75	46.8	--	--	--	--	--	--
Eq. input noise @1MHz (nV/√Hz)	93	65	--	<60	--	--	89	--	--	--
Power (µW)	240	24.3	1380	197	437.5	2500	24	121	11900	1.2
Area (mm^2)	0.075	0.014	0.034	0.157	0.029	--	--	--	0.070	0.057
FoM_L	0.71	0.09	0.26	0.19	0.38	0.47	0.28	2.66	2.24	0.74
FoM_S	48	37	156	88	70	11	73	172	261	30

[a] Simulation

These drawbacks are not reflected in this FoM_S. It is true than in this work also two extra capacitors are required, but its total capacitance is only $2C_{bat}$=1.7 pF versus the compensation capacitances of 10 pF [7], 4.7 pF [8], and 12 pF [9],[11]. Moreover, capacitors C_{bat} do not require dynamic current to drive them as they act as floating batteries with approximately constant charge. There are also some reported single-stage class AB topologies that provide higher FoM_L and/or FoM_S, but they achieve it at the expense of PM degradation

even using large capacitive loads. This is typically because they require increasing the impedance level at internal nodes (e.g. using Local Common-Mode Feedback in [4],[19], adaptive loads in [13] or extra signal paths in [16],[22]) which lead to non-dominant poles at lower frequencies. This issue may preclude the use of these topologies for small load capacitors without using techniques such as output lead compensation [22]. A remarkable work is [12], where higher FoM values are achieved for a PM of 59º and a low C_L=0.5 pF. However, a much more advanced technology is used (40 nm) and only simulation results are provided.

5. CONCLUSION

The combination of a power efficient adaptive biasing circuit and a class AB current follower able to handle the large dynamic currents generated is the main idea of the proposed OTA. Simulation and measurement results confirm the advantages of this approach.

REFERENCES

[1] Assaad R, Silva-Martinez J. The recycling folded cascode: A general enhancement of the folded-cascode amplifier. *IEEE Journal of Solid-State Circuits* 2009;**44**:2535–2542.

[2] Yao L, Steyaert M, Sansen W. Low-power low-voltage sigma-delta modulators in nanometer CMOS. Springer. Dordrecht, The Netherlands, 2006.

[3] Gulati K, Lee HS. A high-swing CMOS telescopic operational amplifier. *IEEE Journal of Solid-State Circuits* 1998;**33**:2010-2019.

[4] Lopez-Martin A, Baswa S, Ramirez-Angulo J, Carvajal RG. Low-voltage super class AB CMOS OTA cells with very high slew rate and power efficiency. *IEEE Journal of Solid-State Circuits* 2005;**40**:1068-1077.

[5] Lopez-Martin AJ, Garde MP, Carvajal RG, Ramirez-Angulo J. On the optimal current followers for wide-swing current-efficient amplifiers. *Proc. IEEE International Symposium on Circuits and Systems*, Florence (Italy), 27-30 May 2018.

[6] Grasso AD, Pennisi S, Scotti G, Trifiletti A. 0.9-V class-AB Miller OTA in 0.35-µm CMOS with threshold-lowered non-tailed differential pair. *IEEE Transactions on Circuits and Systems I: Regular Papers* 2017;**64:**1740-1747.

[7] Aguado-Ruiz J, Lopez-Martin A, Ramirez-Angulo J. Power efficient class AB op-amps with high and symmetrical slew rate. *IEEE Transactions on VLSI Systems* 2014;**22**:943–947.

[8] Zuo L, Islam SK, Low-voltage bulk-driven operational amplifier with improved transconductance. *IEEE Transactions on Circuits and Systems I: Regular Papers* 2013;**60**:2084-2091.

[9] Surkanti PR, Furth PM. Converting a three-stage pseudoclass-AB amplifier to a true-class-AB amplifier. *IEEE Transactions on Circuits and Systems II: Express Briefs* 2012;**59**:229-233.

[10] Golabi S, Yavari M. A three-stage class AB operational amplifier with enhanced slew rate for switched-capacitor circuits. *Analog Integrated Circuits and Signal Processing* 2015;**83**:111-118.

[11] Kulej T. 0.4-V bulk-driven operational amplifier with improved input stage. *Circuits Systems and Signal Processing* 2015;**34**:1167–1185.

[12] Centurelli F, Monsurrò P, Parisi G, Tommasino P, Trifiletti A. A topology of fully differential class-AB symmetrical OTA with improved CMRR. *IEEE Transactions on Circuits and Systems II: Express Briefs* 2018;**65**:1504-1508.

[13] Sutula S, Dei M, Teres L, Serra-Graells F. Variable-mirror amplifier: A new family of process-independent class-AB single-stage OTAs for low-power SC circuits. *IEEE Transactions on Circuits and Systems I: Regular Papers* 2016;63:1101-1110.

[14] Valero Bernal MR, Celma S, Medrano N, Calvo B. An ultralow-power low-voltage class-AB fully differential OpAmp for long-life autonomous portable equipment. *IEEE Transactions on Circuits and Systems II: Express Briefs* 2012;**59**: 643-647.

[15] Chatterje S, Tsividis Y, Kinget P. A 0.5-V bulk-input fully differential operational transconductance amplifier. *Proc. ESSCIRC*, Leuven (Belgium), 21-23 Sept. 2004, pp. 147–150.

[16] Lopez-Martin A, Garde MP, Algueta JM, De la Cruz Blas CA, Carvajal RG, Ramirez-Angulo J. Enhanced single-stage folded cascode OTA suitable for large capacitive loads. *IEEE Transactions on Circuits and Systems II: Express Briefs* 2018;**65**: 441-445.

[17] M. Pennisi, G. Palumbo and R.G. Carvajal, Analysis and comparison of class AB current mirror OTAs. *Analog Integrated Circuits and Signal Processing* 2011;**67**:231–239.

[18] Carvajal RG et al. The flipped voltage follower: a useful cell for low-voltage low-power circuit design. *IEEE Transactions on Circuits and Systems I: Regular Papers* 2005;**52:**1276-1291.

[19] Pourashraf S, Ramirez-Angulo J, Lopez-Martin A, Carvajal RG. Super class-AB OTA without open loop gain degradation based on dynamic cascode biasing. *International Journal of Circuit Theory and Applications* 2017;**45**:2111-2118.

[20] Pourashraf S, Ramirez-Angulo J, Lopez-Martin A, Carvajal RG, Diaz-Sanchez A. ±0.18 V supply voltage gate driven PGA with 0.7 Hz to 2 kHz constant bandwidth and 0.15 µW power dissipation. *International Journal of Circuit Theory and Applications* 2018;**46**:272-279.

[21] Kwan T, Martin K. An adaptive analog continuous-time CMOS biquadratic filter. *IEEE Journal of Solid-State Circuits* 1991;**26**:859-867.

[22] Garde MP, Lopez-Martin A, Carvajal RG, Ramirez-Angulo J. Folded cascode OTA with 5540 MHz·pF/mA FoM. *Proc. IEEE International Symposium on Circuits and Systems*, Florence (Italy), 27-30 May 2018.