Dual-Stage Control Strategy for a Three-Level Neutral Point Clamped Converter with Selective Harmonic Mitigation PWM

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***Abstract*—Grid-connected converters must meet the requirements imposed by grid codes, such as harmonic emission limits and grid voltage support during voltage dips. Selective harmonic mitigation pulsewidth modulation (SHMPWM) is a very interesting technique for high power converters to meet the maximum harmonic emission levels, while keeping a low switching frequency. However, the combination of this modulation with a proportional integral (PI) controller requires slow dynamics, which makes it difficult to comply with the dynamic response requirements of grid codes. As an alternative, model predictive control (MPC) offers a very fast dynamic response, but a wide spread harmonic spectrum in steady state. Thus, the combination of MPC with a PI controller with SHMPWM is advantageous. In this work, a dual-stage control strategy is implemented. During transients, finite control set MPC (FCS-MPC) is activated to rapidly drive the current to the desired reference, while in steady state, the PI controller with SHMPWM is used. Therefore, the dual-stage control strategy allows to comply with the two requirements of grid codes, becoming a suitable strategy for grid-connected converters.**

***Index Terms*—Selective Harmonic Mitigation Pulsewidth Modulation, Model Predictive Control, Linear Control, Grid-connected Power Converter.**

I. Introduction

Medium voltage high power converters are widely used for grid-connected applications. In these cases, multilevel converters are commonly used, since they allow to increase the output voltage [1] using lower rated voltage power switches. These semiconductors must operate at low switching frequencies, given their high power losses. At the same time, grid-connected power converters must meet the requirements imposed by grid codes regarding the current and voltage harmonics at the point of common coupling (PCC) [2], thus, an output filter is needed to reduce the harmonics generated by the converter. In the case of using an *L* filter, a bulky and expensive inductor would be required, and in the case of an *LCL* filter, it will have a very low resonance frequency, which may cause additional stability issues. In order to reduce the size of the output filter, while avoiding resonant harmonic filters, the selective harmonic mitigation pulsewidth modulation is a very interesting technique [3], [4], since it allows to meet the limits for current and voltage harmonics of a specific grid code with a reduced number of switching angles, i. e., a reduced switching frequency.

To perform a closed-loop control of the converter current, a conventional approach is to combine this modulation technique with linear control strategies that employ PI regulators. However, the SHMPWM technique is designed considering that the control action is constant over one fundamental period, whereas the control output is calculated in each sampling period. For this reason, slow controllers are required when PI regulators are combined with SHMPWM, which limits the dynamic performance of the converter [5], [6] and makes it difficult to comply with other aspects of grid codes such as low voltage ride through (LVRT) [7].

In order to improve the dynamic response when the SHMPWM technique is used, model predictive control has emerged as a promising alternative [6]. Among the existing MPC control strategies, finite control set MPC (FCS-MPC) has gained significant attention [8] since it is simple to design, it can directly handle non-linearities and multiple control objectives, and it provides a fast dynamic response. However, it presents some drawbacks for grid-connected converters, such as a variable switching frequency, a wide spread spectrum and nonzero steady state error [9], [10].

With the objective of enhancing the dynamics of the converter during transients, while maintaining the benefits of linear control in steady state, i.e. a defined spectrum and zero steady state error, some authors [11] have combined FCS-MPC with linear controllers, but using carrier-based PWM modulators. In [11] a dual-stage control strategy is applied to a stand-alone flying capacitor converter. FCS-MPC is activated

This work is part of the projects PID2019-110956RB-I00 and TED2021-132604B-I00, funded by MCIN/AEI/10.13039/501100011033 and by the European Union NextGenerationEU/PRTR. It has also been partially supported by Ingeteam Power Technology and the Public University of Navarre. The authors also acknowledge the support of ANID through projects FB0008 Advanced Center for Electrical and Electronics Engineering, FONDECYT 1230250.

https://doi.org/10.1109/ACEMP-OPTIM57845.2023.10287062

during transients, achieving a fast dynamic response, and a PI controller with a PWM is used in steady state, obtaining a constant switching frequency with a concentrated spectrum and zero steady state error.

This combination of linear controllers and FCS-MPC can be of particular interest for grid-connected converters using SHMPWM since the PI regulators required by this modulation are particularly slow, an alternative that so far has not been explored in the literature. In this work, a dual-stage control strategy is applied to a three-level neutral point clamped (NPC) grid-connected converter. The desired harmonic content is obtained in steady state thanks to a slow PI controller with SHMPWM, fulfilling the grid code harmonic emission requirement. The FCS-MPC strategy guarantees a fast dynamic response during transients, which allows to comply with LVRT requirements imposed by grid codes, solving one of the main limitations of grid-connected converters with SHMPWM.

The paper is organized as follows. In Section II, the dual-stage control strategy is presented and each element of the control is explained in detail. Section IV shows the simulation results when this strategy is applied to a three-level grid-connected NPC converter and its performance is compared to the FCS-MPC and the linear control.

II. Dual-Stage Control Strategy

Fig. 1 shows a representation of the dual-stage control strategy for a three-level grid-connected NPC converter with an inductive harmonic filter. L_{conv} is the converter output inductance. A step-up transformer is used to connect the converter to the grid at the PCC, thus L_t is the transformer leakage inductance. L_g is the grid inductance, whose value depends on the short circuit ratio. In this work, it is assumed that the dc bus capacitor voltages are balanced, with the total dc bus voltage being V_{DC}. The system parameters are reported in Table I.

This section explains the fundamentals of the two control strategies that are used in the dual-stage controller, namely FCS-MPC and PI-based control, as well as the transition between the two of them. The FCS-MPC strategy, represented in blue in Fig. 1, is used to achieve a fast dynamic response during transients. The linear controller with SHMPWM represented in orange, is used to ensure tracking of the reference in steady state, and compliance with the maximum harmonic levels imposed by the grid code. The converter current measurements, i_{conv}^{abc}, are filtered using a low-pass analog filter, LPAF, with a cutoff frequency of 1000 Hz, and two notch filters at 250 and 350 Hz in order to filter the low order harmonics introduced by the SHMPWM. The voltage at the PCC, v_{pcc}^{abc}, is also filtered using a SOGI filter [12] to obtain the fundamental component.

TABLE I: System Parameters

Parameter	Magnitude
Grid	
Fundamental frequency	50 Hz
Grid voltage	3100 V
Power converter	
Rated power	5 MW
DC bus voltage	4700 V
Switching frequency	1100 Hz
Converter output inductance	0.149 p.u.
Converter output resistance	0.005 p.u.
Transformer inductance	0.108 p.u.
Transformer resistance	0.003 p.u.
Short circuit ratio	15
Control	
Sampling frequency	8000 Hz
PI proportional gain, K_p	0.3982 V/A
PI integral constant, T_n	0.0131 s
λ_{sw}	0.005
E_l	0.0001 p.u.
E_h	0.1 p.u.

A. Finite Control Set Model Predictive Control

This control strategy uses a model of the system to predict its future behavior as a function of the converter switching states. The predictions are evaluated through a cost function that includes the control objectives such as tracking of the reference current. Then, the converter voltage that minimizes the cost function is applied.

In this work, the control is performed in the stationary reference frame, $\alpha\beta$. The discrete-time model of the plant is given by

$$i_{conv}^{\alpha\beta}(k+1) = (1 - \frac{RT_s}{L})i_{conv}^{\alpha\beta}(k) + \frac{T_s}{L}(v_{conv}^{\alpha\beta}(k) - v_{pcc}^{\alpha\beta}(k)), \tag{1}$$

where $i_{conv}^{\alpha\beta}$ is the converter current, $v_{pcc}^{\alpha\beta}$ is the voltage at the PCC, and $v_{conv}^{\alpha\beta}$ is the voltage applied by the converter, which depends on the converter switching states. The superscript $\alpha\beta$ indicates that they are expressed in $\alpha\beta$ axis. The resistance R is the sum of the converter inductance series resistance, R_{conv}, and the transformer resistance, R_t. $L = L_{conv} + L_t$, and T_s is the sampling period.

There is a delay of one sampling period due to the calculations performed by the digital signal processor (DSP) that is compensated [13]. For the converter current this delay compensation is done using the model of the plant

$$i_{conv}^{\alpha\beta}(k) = (1 - \tfrac{RT_s}{L})i_{conv}^{\alpha\beta}(k-1) + \tfrac{T_s}{L}(v_{conv}^{\alpha\beta}(k-1) - v_{pcc}^{\alpha\beta}(k-1)). \tag{2}$$

The voltage at the PCC is assumed to be a sinusoidal waveform, thus the computational delay is compensated by adding $\omega_0 T_s$ to the PCC voltage angle. ω_0 is the grid fundamental angular speed.

In this work, a one-step prediction cost function, $J(k)$, is used that considers tracking of the current reference and penalization of the switching effort

$$J(k) = \frac{\|i_{conv}^{'\alpha\beta}(k+1) - i_{ref}^{\alpha\beta}(k+1)\|_2^2}{I_n^2} + \lambda_{sw}|u^{abc}(k) - u^{abc}(k-1)|. \tag{3}$$

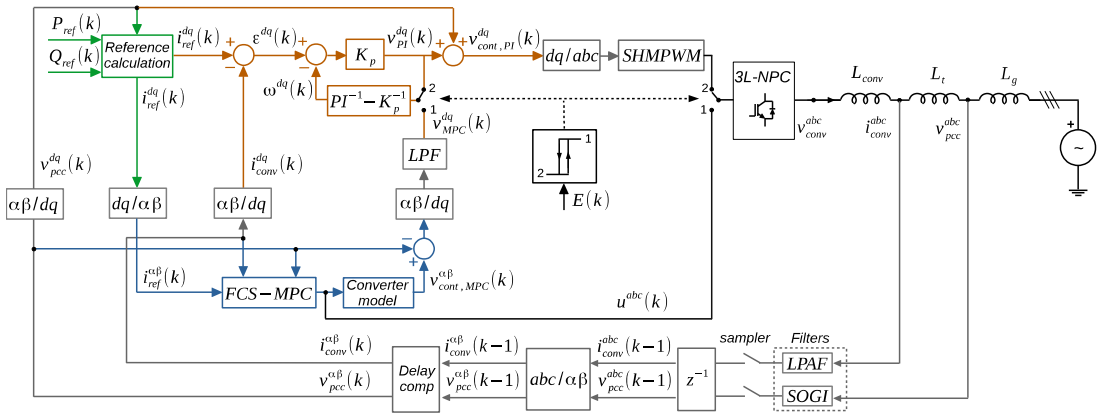


Fig. 1: Dual-stage control strategy for a three-level grid-connected NPC power converter.

$i'^{\alpha\beta}_{conv}(k+1)$ are the predicted currents for the 27 possible switching states of a NPC converter, $i^{\alpha\beta}_{ref}(k+1)$ is the reference current at the next sampling instant and I_n is the rated converter current. $u^{abc}(k)$ denotes the switching state of the three phases of the converter, which can take the values 1, 0 or -1 for each phase leg. Notice that switching between 1 and -1 is prohibited. The switching state that minimizes the cost function will be selected as the control action, and the corresponding gate signals are applied to the converter.

The weighting factor λ_{sw} is adjusted through simulations so that the number of commutations when the FCS-MPC strategy is applied is close to the expected value given by the SHMPWM pattern, to ensure that the converter works within its thermal limits. Its value appears in Table I.

B. Linear Controller with SHMPWM

In the linear control strategy with SHMPWM, used in steady state, the converter current is controlled in the synchronous reference frame, *dq*, by a PI regulator (one for each axis). The converter current, $i^{\alpha\beta}_{conv}(k)$, is transformed to the synchronous reference frame by means of the Park transformation, which uses the angle of the voltage at the PCC.

The discrete transfer function of the PI regulator of each axis is given by

$$PI(z) = K_p \frac{z-a}{z-1}, \tag{4}$$

where $a = 1 - \frac{T_s}{T_n}$.

In this work, the PI controller is implemented through its feedback form [14], thus the PI output voltage is given by

$$v^{dq}_{PI}(k) = K_p(\varepsilon^{dq}(k) - \omega^{dq}(k)), \tag{5}$$

where ε^{dq} is the current tracking error and ω^{dq} is the PI regulator inner state, which is given by

$$\omega^{dq}(z) = (PI^{-1}(z) - K_p^{-1})v^{dq}_{PI}(z) = \frac{a-1}{K_p(z-a)}v^{dq}_{PI}(z). \tag{6}$$

This implementation is very useful in the design of the dual-stage control strategy, specifically in the transition between the two controllers.

As represented in Fig. 1, the voltage at the PCC in the synchronous reference frame, v^{dq}_{pcc}, is added to the PI output voltage, v^{dq}_{PI}, to improve the rejection of grid disturbances. The final control action, $v^{dq}_{cont,PI}$, is transformed to the *abc* reference frame. From this voltage, a modulation index and an angle is obtained for each phase, and the SHMPWM modulator is accessed, which consists of a look-up table that stores the converter switching angles, α_i, that allow to maintain all the harmonics below the maximum levels given by a certain grid code for a given output filter [3], [4].

The following describes the optimization problem that needs to be solved for the calculation of the switching angles stored in the look-up table, which is done offline due to the large computational burden involved. In this work, we consider the grid code IEC 61000-3-6 [2], which defines a maximum level for each voltage harmonic and the voltage total harmonic distortion, THDv, at the PCC. The SHMPWM pattern has odd quarter-wave symmetry, therefore only the non triplen odd harmonics up to the 50th must be limited. The optimization problem given in (7) is solved for the desired range of modulation index.

$$\begin{aligned}
\min_{\alpha_i} \quad & c_{THDv}THDv + \sum_{n=5,7,\ldots,49} c_n H_n \\
\text{s.t.} \quad & H_1 = |\frac{4}{\pi}\sum_{i=1}^{N_\alpha}(-1)^{i-1}cos(\alpha_i)| = M \\
& H_n = |\frac{4}{n\pi}\frac{V_{DC}}{2}\sum_{i=1}^{N_\alpha}(-1)^{i-1}cos(n\alpha_i)| \leq L_n \\
& THDv = \sqrt{\sum_{n=5}^{49}\left(\frac{H_n}{H_1}\right)^2} \leq Lim_{THDv} \\
& \alpha_{i+1} - \alpha_i > \theta \quad \alpha_0 > \theta/2 \quad \pi/2 - \alpha_{N_\alpha} > \theta/2
\end{aligned} \tag{7}$$

The fundamental harmonic, H_1, equals the desired modulation

index, M, and the nth harmonic, H_n, is kept below the limit, L_n, imposed by the grid code, with $n = 5, 7, .., 49$. The problem constraints also include the limit for the TDHv (calculated considering the harmonics up to the 50th), and the minimum pulsewidth θ required due to the minimum turn-on time of the semiconductors and the dead time. Since medium-voltage semiconductors are used in this application, $\theta = 0.01\ rad$. N_α is the number of switching angles in a quarter of the fundamental period. In this work $N_\alpha = 11$, so the converter switching frequency is 1100 Hz. Finally, the costs of the objective function c_{THDv} and c_n are defined as explained in [3].

The SHMPWM technique is designed assuming a constant control action (or modulation index) in one fundamental period. For this reason, it is necessary to design a slow PI controller, to ensure that the control action does not vary too much between consecutive sampling periods and that the desired harmonic content is obtained, meeting the grid code requirements. The parameters of the PI controller are given in Table I.

C. Transition between linear control and FCS-MPC

In the dual-stage control strategy the PI controller and the FCS-MPC are combined to take advantage of the benefits of each of them. In steady state, the PI controller with SHMPWM is used to fulfill the grid code in terms of harmonic emissions. During transients, the FCS-MPC is applied to obtain a fast dynamic response and meet other aspects of grid codes related to the dynamic performance of the converter, specifically current injection during voltage dips.

The commutation between the two control strategies is controlled by an hysteresis comparator, whose input, $E(k)$, is the squared 2-norm of the current tracking error in *dq* axis

$$E(k) = \frac{\|\varepsilon^{dq}(k)\|_2^2}{I_n^2}. \tag{8}$$

The two hysteresis bands are denoted by E_l and E_h and the transitions are as follows:

1) When $E(k) > E_h$ the FCS-MPC strategy is activated to rapidly drive the current close to the desired reference, so the switch is at position 1.
2) When $E(k) < E_l$ the linear controller is applied (switch at position 2), since the system is close to the steady state.
3) If $E_l < E(k) < E_h$ the same controller is used as in $k-1$.

The transition from the FCS-MPC to the PI controller is not trivial. The PI regulator has an internal state that is updated to the new operation point to obtain a soft transition. For this purpose, the feedback implementation of the PI controller is very useful, since it allows to properly update the internal controller state, $\omega^{dq}(k)$, whenever the actual control action applied to the plant differs from the one calculated by the controller. In this case, the internal state is updated with the control action applied by the FCS-MPC. However, the output of the FCS-MPC is the switching state of each phase, $u^{abc}(k)$. Therefore, the converter model is used to obtain the voltage applied by the FCS-MPC in $\alpha\beta$ axis

$$v^{\alpha\beta}_{cont,MPC}(k) = [C]\frac{V_{DC}}{2}u^{abc}(k), \tag{9}$$

where $[C]$ is the Clarke transformation matrix. The voltage at the PCC, $v^{\alpha\beta}_{pcc}(k)$, is subtracted to account for the feedforward term of the linear controller, and the resulting action is transformed to *dq* axis. This signal is a switched waveform so it is filtered with a low-pass filter, *LPF*, to update the PI inner state smoothly. A second order Butterworth filter with a cutoff frequency of 2 kHz is used. The filtered voltage applied by the FCS-MPC in *dq* axis, $v^{dq}_{MPC}(k)$, is used to update the internal state of the PI controller

$$w^{dq}(z) = \frac{a-1}{K_p(z-a)}v^{dq}_{MPC}(z). \tag{10}$$

Therefore, when the dual-stage strategy commutes to the linear controller, the PI inner state will be compatible with the new operation point and a soft transition will be achieved.

The two hysteresis bands, E_l and E_h, are adjusted through simulations and their values are given in Table I.

III. Simulation Results

Simulations are performed in Matlab/Simulink, where a model of the system is created using the Simscape Electrical Library. The dual-stage control strategy is tested and compared to the PI controller and the FCS-MPC in terms of harmonic emissions and dynamic performance.

A. Harmonic Emissions

The harmonic content is measured in steady state when the rated active power is injected to the PCC with unity power factor. Fig. 2 shows the voltage harmonics at the PCC with the dual-stage control strategy, in blue, and the FCS-MPC strategy, in red, compared to the limits given in the IEC61000-3-6 grid

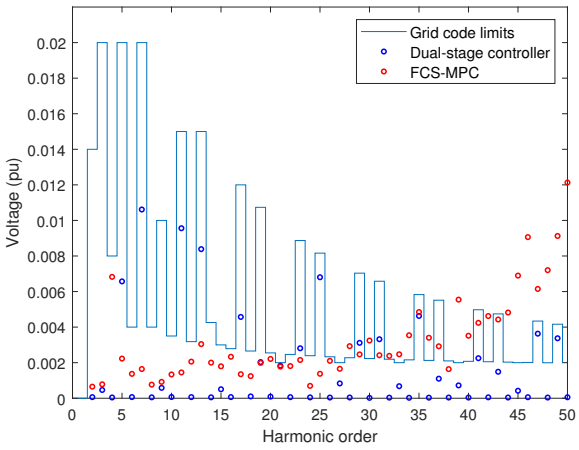


Fig. 2: Comparison of the harmonic content of the voltage at the PCC when injecting rated active power with unity power factor with the dual-stage controller and FCS-MPC.

code [2]. As it is observed, the grid code is fulfilled with the dual-stage controller thanks to the use of the SHMPWM technique and a slow PI controller. The voltage total harmonic distortion equals 2.2 %, which is below the maximum level of 3 % imposed by the grid code. On the other hand, the grid code limits are not met with the FCS-MPC strategy, since it has a wide spread spectrum, and the THDv is 2.8 %. Note that the result with the PI controller would be the same as with the dual-stage controller since the latter uses the PI regulator in steady state.

B. Step Response

In this subsection the step response of the three control strategies is analyzed. For this purpose, a step in the reference active power from 50% to 100% of the rated value, with unity power factor, is simulated. The *d* axis is aligned with the voltage at the PCC, thus, considering the power invariant Clarke transformation, the reference current in *dq* axis is given by

$$i^d_{ref}(k) = \frac{P_{ref}(k)}{v^d_{pcc}(k)} \tag{11}$$

$$i^q_{ref}(k) = -\frac{Q_{ref}(k)}{v^d_{pcc}(k)}, \tag{12}$$

where P_{ref} and Q_{ref} are the reference active and reactive power, respectively. This way, a step in the reference active power with unity power factor implies a change in the reference current in the *d* axis.

Fig. 3 (a) shows the step response of the converter current in *dq* axis with the PI controller, Fig. 3 (b) shows the response of the FCS-MPC strategy, and Fig. 3 (c) the one obtained with the dual-stage control strategy. In this case, the FCS-MPC is activated after the step during 20 ms, and a soft transition between the FCS-MPC and the PI control is achieved thanks to the update of the PI internal state. The PI controller reaches the reference in 130 ms, whereas the FCS-MPC and the dual-stage controller in 30 ms, with less overshoot and oscillations. The results are summarized in Table II.

It is worth noting the current ripple in steady state. Comparing Fig. 3 (a) and (b), it is observed that the ripple is higher with the FCS-MPC than the PI control with SHMPWM, which is in agreement with the results of Fig. 2.

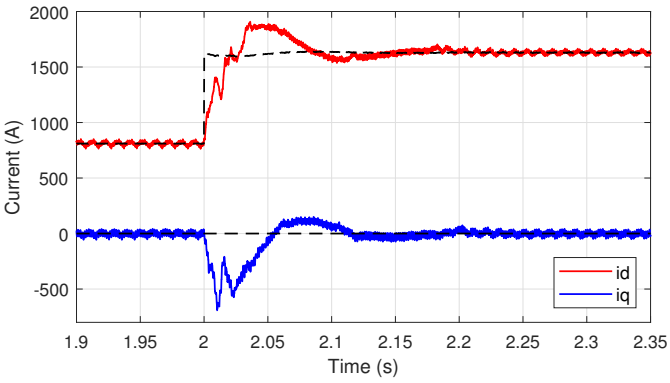
TABLE II: Step response results

	PI	FCS-MPC	Dual-stage controller
Rise time	20 ms	3.5 ms	3.5 ms
Settling time	130 ms	30 ms	30 ms

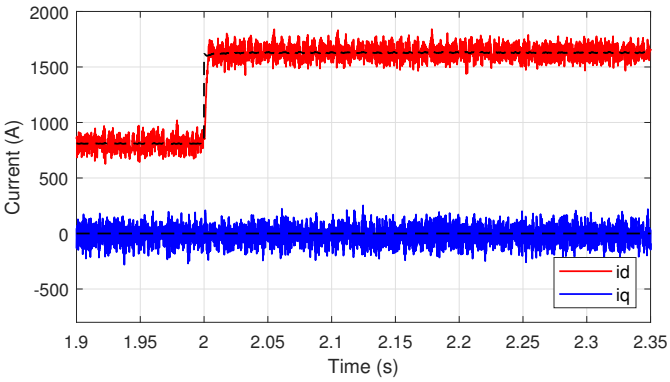
Fig. 4 shows the converter output voltage of phase *a* after the reference step when the converter uses the dual stage control strategy. Fig. 4 (a) shows the voltage during the first fundamental cycle, when the FCS-MPC is activated, while Fig. 4 (b) shows the voltage when the PI controller is used. It is observed that in steady state the converter applies the precomputed SHMPWM pattern, showing the quarter-wave symmetry previously mentioned with 11 angles per quarter of the fundamental period. However, when FCS-MPC is applied, switching is uneven and no symmetry is observed. For this reason it is also observed in Fig. 2 that the even harmonics are not equal to zero with the FCS-MPC strategy.

C. Low Voltage Ride Through

Grid codes require that power converters remain connected to the grid during grid transients such as voltage dips. Besides, voltage support is usually required during these faults, which



(a)



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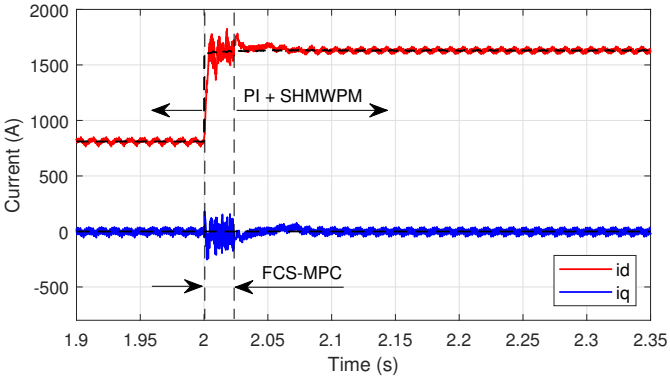


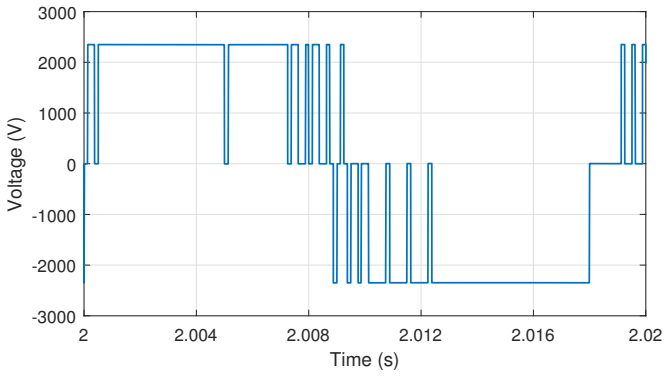
(c)

Fig. 3: Step response of the current in *dq* axis for the PI controller (a), the FCS-MPC (b), and the dual-stage controller (c).

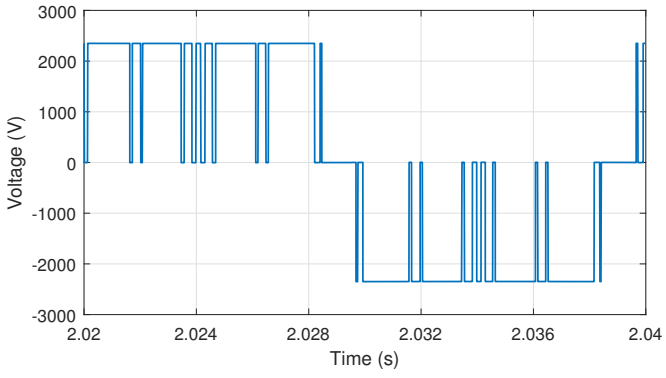
is done by supplying reactive current to the grid. Normally, a constant of proportionality of 2 is used between the voltage sag and the required reactive current, until the rated current is reached [7]. As specified in [7], the most demanding grid codes in Europe require a settling time of 60 ms. Fig. 5 shows the converter current in *dq* axis during a 90 % voltage dip. In this case, rated reactive current is injected to the PCC, thus the reference current on *q* axis equals the rated value. It is observed in Fig. 5 (a) that the PI controller is not able to meet the LVRT requirement since the converter trips due to overcurrent. Fig. 5 (b) and (c) show the response of the FCS-MPC strategy and the dual-stage control strategy, respectively. These strategies reach the new reference within 15 ms, fulfilling the grid code requirement. Moreover, the dual-stage controller achieves a soft transition to the PI control.

IV. Conclusion

In this work, a dual-stage control strategy based on PI controllers and FCS-MPC is applied to a three-level NPC converter connected to the grid. In high power applications, the converter switching frequency is limited, therefore a selective harmonic mitigation PWM is used to meet the grid code requirements regarding harmonic emissions, since it allows to reduce the size of the converter output filter with a low switching frequency. However, when this modulation technique is combined with traditional linear controllers, such as PI regulators, a slow dynamic is required, which causes that other aspects of grid codes such as low voltage ride trough capability are not fulfilled. For this reason, the combination of the PI controller with FCS-MPC is very beneficial. When the current tracking error increases, the FCS-MPC is applied, obtaining a fast dynamic response. In steady state, the PI controller with SHMPWM is used, obtaining the desired harmonic content.

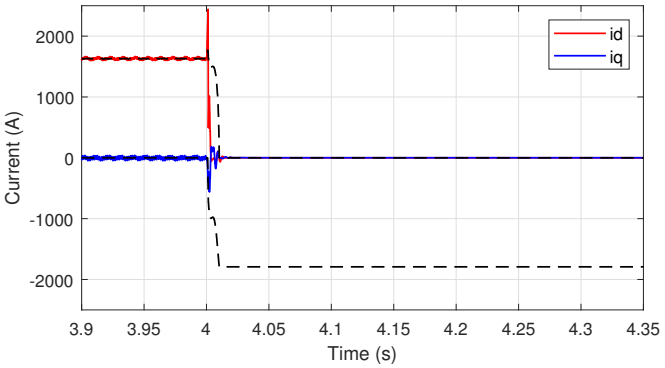


(a)

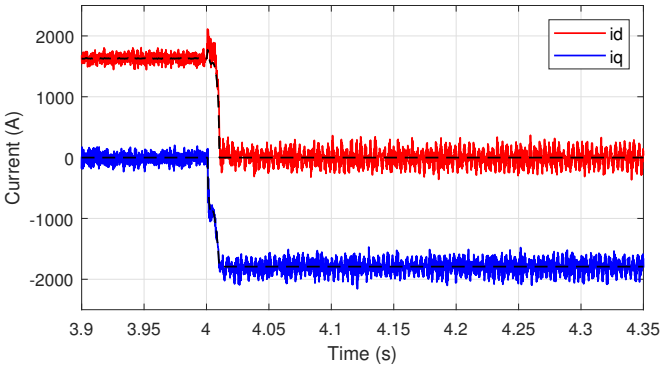


(b)

Fig. 4: Converter output voltage of phase *a* with the dual-stage strategy when the FCS-MPC is activated after the reference step (a), and when the PI controller with SHMPWM controls the converter in steady state (b).



(a)



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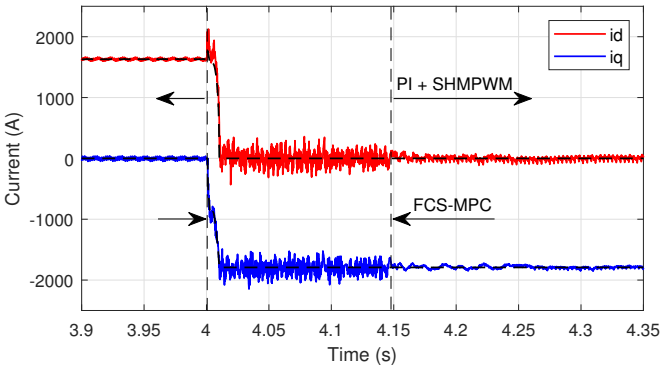

(c)

Fig. 5: Dynamic response of the current in *dq* axis for a voltage dip of 90 % for the PI controller (a), the FCS-MPC (b), and the dual-stage controller (c).

The implementation of the PI regulator through its feedback form allows to update the PI inner state whenever the FCS-MPC is used, so that a soft transition between both controllers is achieved. This way, the dual-stage control strategy allows to comply with both aspects of grid codes, namely harmonic emission limits and dynamic response during grid transients, which makes it a suitable solution for high power grid-connected converters and solves the main limitation of the SHMPWM in this application.

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