1-V 15-µW 130-nm CMOS Super Class AB OTA

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***Abstract*—A super class AB recycling folded cascode amplifier in 130 nm CMOS is presented. It combines for the first time adaptive biasing of the differential input pair, nonlinear current mirrors with current starving and dynamic biasing of the cascode transistors in the output branch. Measurements using a ±0.5V supply show slew rate and gain bandwidth product improvement factors of 26 and 112 versus the conventional topology for the same bias currents, yielding the highest combined FoM to date.**

Keywords—Amplifiers, Analog integrated circuits, CMOS integrated circuits, Class AB circuits.

I. Introduction

Energy efficiency is a critical aspect in applications where portable/wearable devices are supplied by small batteries or even by energy harvesting techniques. Particularly, emerging Internet of Things (IoT) scenarios are rapidly gaining momentum. In many of these scenarios edge nodes require extreme energy efficiency, and the availabitily of high-performance power-efficient amplifiers is critical [1].

An ideal OTA in terms of power efficiency should achieve the highest small-signal and large-signal performance for a given quiescent current. A common way to quantify these requirements is using two conventional figures of merit [2]. The first one is $FoM_L=SR\cdot C_L/I_{supply}=I_{maxL}/I_{supply}$, with SR the Slew Rate, C_L the load capacitance, $I_{maxL}= SR\cdot C_L$ the maximum load current and I_{supply} the total quiescent current consumption. FoM_L quantifies the large-signal performance for a given I_{supply}. The second one is $FoM_S=GBW\cdot C_L/I_{supply}$ with GBW the gain-bandwdith product, and quantifies the small-signal performance for a given I_{supply}. Besides maximizing FoM_L and FoM_S, a power-efficient OTA should maximize the portion of supply current delivered to the load. This parameter is the current efficiency or current utilization [3], and is optimal if the large dynamic currents are generated directly at the output branch without unnecesary internal replication of them.

In terms of power efficiency, single-stage OTAs are preferred [4] as they are load compensated. Among the proposed single-stage OTAs, an optimal choice in terms of power efficiency is the so-named super class AB OTA [3]. It combines adaptive biasing of the input differential pair and nonlinear current amplifiers to convey and additionally boost the differential pair current to the output. Super class AB OTAs can potentially achieve very large FoM_L due to this double current boosting process, and can also achieve very large FoM_S if the adaptive biasing and nonlinear current amplifiers employed provide enhanced OTA transconductance. Moreover, current utilization is very high as the large dynamic currents achieved are generated directly at the output transistors of the nolinear current amplifier, right at the output branch.

To date super class AB OTAs have been implemented using symmetrical (current mirror) [3], [5]-[7] and recycling folded cascode (RFC) [8]-[11] topologies. In this paper we present a new super class AB OTA outperforming the previous ones in terms of average $FoM_{AVG}=(FoM_S\cdot FoM_L)^{1/2}$ thanks to a new way of exploting the triode-saturation transition and cascode biasing to improve SR, and a different use of current steering.

II. Proposed OTA

Figure 1(a) depicts the conventional RFC OTA presented in [12]. It can be regarded as a hybrid cascode current mirror (CCM) and Folded Cascode (FC) OTA. Each differential pair transistor is split into two half-width devices creating two different paths: one path corresponds to a CCM OTA using NMOS current mirrors with gain *K* and the other path to a FC topology. Typically *K*=3 is chosen to have the same quiescent power as the conventional FC OTA.

The proposed super class AB RFC OTA is shown in Fig. 1(b). The four modifications made from Fig. 1(a) are 1) Adaptive biasing of the differential input pair, 2) Biasing of transistors M_{3B}-M_{4B} near ohmic region, 3) Current starving, and 4) Dynamic biasing of the cascode transistors in the output branch. These modifications are described in detail below.

A. Adaptive Biasing of Input Pair

The constant bias current in Fig. 1(a) is replaced by two cross-coupled floating batteries [3], which are implemented by two Flipped Voltage Followers (FVF) [13] M_{1C}-M_{1D} and M_{2C}-M_{2D}. In quiescent conditions M_{1C}-M_{2C} have the same V_{GS} as M_{1A}, M_{1B}, M_{2A}, M_{2B} and since they have also the same size, neglecting channel length modulation they set a quiescent current $I_B/2$ in M_{1A}, M_{1B}, M_{2A}, and M_{2B}. When a differential signal V_{id} is applied, currents in in M_{1A}, M_{1B}, M_{2A}, and M_{2B} are not limited by $I_B/2$ due to the large currents that can be sourced by the FVFs. Moreover, the differential pair transconductance in Fig. 1(b) is twice that of Fig. 1(a) as the input signal is applied both to the gate and source of M_{1A}, M_{1B}, M_{2A}, and M_{2B}.

B. Nonlinear Current Scaling

Instead of using extra local common-mode feedback loops with active [6], [9] or passive resistors [3], [8], [11], differential pair current boosting in Fig. 1(b) is simply done by suitably decreasing the bias current of cascode transistors M_{3C} and M_{4C} in Fig. 1(a). The new voltage V_{BIAS} is such that in quiescent operation M_{3B} and M_{4B} are in saturation but near ohmic region [5], [7], [10]. Hence for small-signal operation the NMOS current mirrors operate linearly, as in Fig. 1(a).

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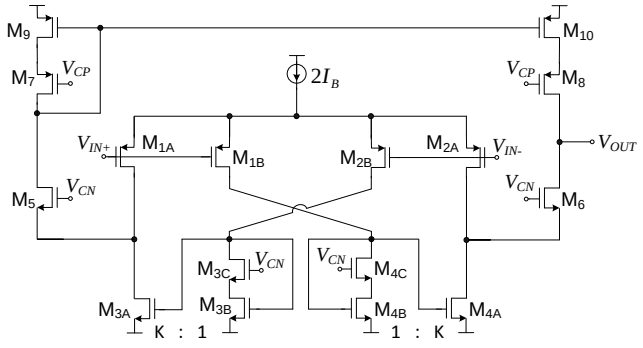
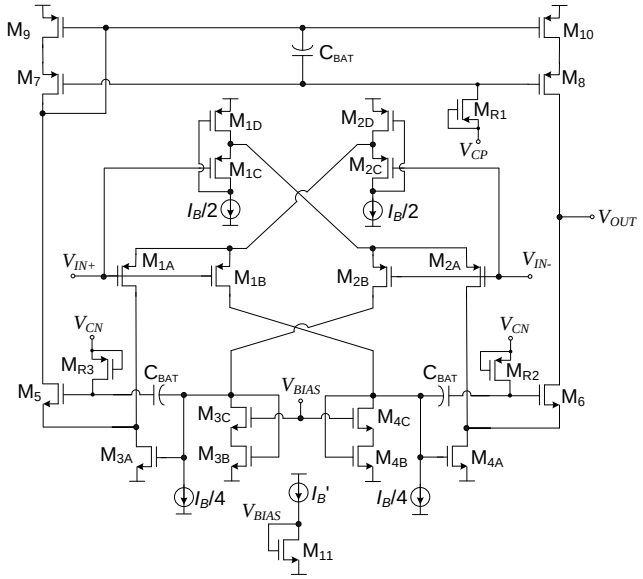


(a)



(b)

Fig. 1. (a) Class A RFC OTA (b) Enhanced super class AB RFC OTA.

However, for V_{id}>0 the drain current I_{2B} of M_{2B} increases, and M_{3B} enters ohmic region. As a result a large voltage appears at the gate of M_{3A}, which leads to a large current I_{3A} since M_{3A} is in saturation. This large current is copied by M_9-M_{10} and delivered to the load. For V_{id}<0, M_{4B} enters triode region provoking a large current in M_{4A} which is sinked from the load. Hence transition between saturation/ohmic region of M_{3B}-M_{4B} is used to get nonlinear current scaling in the NMOS current mirrors.

As shown in Fig. 1(b), V_{BIAS} can be generated by a diode-connected transistor with suitable I_B' and W/L. Voltage $V_{DS3B,4B}$ remains slightly larger than $V_{DS3B,4B,sat}=V_{GS3B,4B}-V_{TH}$ even with PVT variations as M_{11} is a scaled replica of $M_{3B,4B}$.

C. Current Starving

Current starving is implemented in Fig. 1(b) by two dc current sources that subtract part of the dc input current to the NMOS current mirrors. For a fixed current mirror gain K, current starving allows decreasing the quiescent current of the current mirror output, thus increasing the amplifier output resistance R_{out} and dc gain [4]. However, here we use current starving to increase K without increasing static power. The starving factor used is 0.5, so half of the bias current I_B/2 is subtracted. As a result K can be doubled in Fig. 1(b) (from 3 to 6) for the same quiescent current. Unfortunately, increasing current starving and K raises the inpedance and capacitance, respectively, of the internal nodes corresponding to the drains of M_{1B}-M_{2B}, reducing phase margin (PM). So proper design is required to keep PM degradation within acceptable limits.

D. Dynamic Cascode Biasing

For large dynamic currents cascoded transistors can enter ohmic region since the cascode transistor restricts their V_{DS}. This effect is exploited in M_{3B}-M_{4B} to get dynamic current boosting, but it must be avoided in M_{3A}, M_{4A}, M_9 and M_{10} to allow the large currents generated in M_{3A}-M_{4A} reach the load. To achieve it Quasi-Floating Gate (QFG) techniques [11], [14] have been employed. In quiescent operation cascode transistors are biased as in Fig. 1(a) since capacitors C_{BAT} are open circuits and hence there is no voltage drop through pseudo-resistors M_{R1}, M_{R2} and M_{R3}. However, in dynamic conditions capacitors C_{BAT} act as floating dc level shifters that translate voltage variations from the gates of transistors M_{3A}, M_{4A}, M_9 and M_{10} to the gates of their corresponding cascode transistors M_5, M_6, M_7 and M_8.

III. Circuit Analysis

A. Small Signal Analysis

The transconductance G_m and GBW of the super class AB OTA of Fig. 1(b) are:

$$G_m=2g_{m1A}\,(1+K) \tag{1}$$

$$GBW = 2(1+K)\frac{g_{m1A}}{2\pi C_L} \tag{2}$$

with g_{m1A} the transconductance of $M_{1A,1B}$. The dominant pole ω_{p1} = -1/(R_{out} C_L) is set by the output node. The active NMOS current mirrors M_{3A}-M_{3B} and M_{4A}-M_{4B} lead to the main non-dominant pole $\omega_{p2}\approx -g_{m3B}/(C_{gs3A}+C_{gs3B}) \approx -g_{m3B}/[(1+K)C_{gs3B}]$ and a zero $\omega_{z1} \approx -(1+K)\omega_{p2}$. There is also another non-dominant pole $\omega_{p3}\approx -g_{m5}/C_{p5}$ at the source of M_5 and M_6, with C_{p5} the parasitic capacitance at the source of M_5. The single ended version has an extra non-dominant pole and zero set by M_9-M_{10}. For relatively large K and with current starving, the PM is

$$PM \approx 90º - tan^{-1}\left(\frac{GBW}{f_{p2}}\right) \approx \tag{3}$$
$$90º - tan^{-1}\left[2(K+1)^2\frac{g_{m1A}}{g_{m3B}}\frac{C_{gs3B}}{C_L}\right]$$

Note that higher K and starving factors (which decrease g_{m3B}) can be used for larger C_L and that both factors decrease PM.

B. Large Signal Analysis

Using for simplicity the square law model for the MOS transistor in strong inversion and saturation, and the expression $I_D = \beta\cdot(V_{GS} - V_{TH})\cdot V_{DS}$ for ohmic region, for V_{id} > 0 current in M_{3A} is

$$I_{3A} = \frac{\beta_{3A}}{2}\left(\frac{I_{2B}}{\beta_{3B}V_{DS,3B}}\right)^2 \tag{4}$$

with $\beta_i=\mu C_{ox}(W/L)_i$ and $V_{DS,3B} = V_{BIAS} - \sqrt{2I_{2B}/\beta_{3C}} - V_{TH}$. Replacing I_{2B}, it leads to

$$I_{3A} = \frac{\beta_{3A}}{2}\left[\frac{\beta_{2B}}{2\beta_{3B}V_{DS,3B}}\left(\sqrt{\frac{I_B}{\beta_{1B}}} + V_{id}\right)^2\right]^2 \quad . \tag{5}$$

If an input step of A Volts is applied, current in M_{1A} and M_{4A} is negligible and M_{2A} is in deep ohmic region, so $I_{out} \approx I_{3A}$ and

$$SR_+ \approx \frac{\beta_{3A}}{2C_L}\left[\frac{\beta_{2B}}{2\beta_{3B}V_{DS,3B}}A^2\right]^2 \approx \frac{K}{8C_L}\frac{\beta_{2B}^2}{\beta_{3B}V_{DS,3B}^2}A^4 \quad . \tag{6}$$

Similarly, for $V_{id} < 0$:

$$I_{4A} = \frac{\beta_{4A}}{2}\left[\frac{\beta_{1B}}{2\beta_{4B}V_{DS,4B}}\left(\sqrt{\frac{I_B}{\beta_{2B}}} - V_{id}\right)^2\right]^2 \tag{7}$$

and a negative input step of $-A$ Volts yields $I_{out} \approx -I_{4A}$ and

$$SR_- \approx \frac{\beta_{4A}}{2C_L}\left[\frac{\beta_{1B}}{2\beta_{4B}V_{DS,4B}}A^2\right]^2 \approx \frac{K}{8C_L}\frac{\beta_{1B}^2}{\beta_{4B}V_{DS,4B}^2}A^4 \quad . \tag{8}$$

Practical SR values are significantly lower due to second-order effects not considered in the ideal square-law model.

IV. Measurement Results

The amplifiers of Fig. 1 were fabricated in unity-gain negative feedback using a 130 nm CMOS process. Dual nitride MiM C_{BAT} capacitors of 500 fF were employed. The microphotograph is shown in Fig. 2, with the layout superimposed due to the opaque passivation layer. Transistor dimensions W/L (in µm/µm) are 72/0.24 (M_{3A}, M_{4A}), 24/0.24 (M_5, M_6), 0.16/0.12 (M_{R1}, M_{R2}, M_{R3}) and 12/0.24 for others.

Supply voltage was ±0.5 V and I_B = 3 µA. Figure 3 shows the measured response of the class OTA of Fig. 1(a) and the super class AB OTA of Fig. 1(b) to a 1 MHz 0.4 V_{pp} square input signal with 0 dc level. An external load capacitor of 47 pF was used, which added to the pad, package traces, PCB and active probe capacitance, leads to $C_L \approx 70$ pF. The measured average SR = (SR_++SR_-)/2 of the OTA of Fig. 1(a) is 0.19 V/µs and that of the amplifier of Fig. 1(b) is 21.3 V/µs, i.e. an increase factor of 112.

The measured frequency response of the fabricated OTAs of Fig. 1 in unity gain feedback is shown in Fig. 4. The bandwidth is 380 kHz for the OTA of Fig. 1(a) and 9.95 MHz for the OTA of Fig. 1(b), i.e. about 26 times higher. This is a good estimation of the GBW considering non-dominant poles well above the unity-gain frequency. For this measurement an external buffer was used prior to the active probe of the network analyzer, so the estimated load capacitance is C_L =50 pF.

Fig. 5 shows the measured THD of the class A OTA of Fig. 1(a) and the super class AB OTA of Fig. 1(b). A 10 kHz input with different amplitude is employed. The proposed OTA shows improved linearity due to the enhanced dc gain and better dynamic performance.

The main measurement results of the class A and super class AB RFC OTAs of Fig. 1 are summarized in Table I, as well as results from previously reported class AB amplifiers. Note the reduced input-referred noise of Fig. 1(b) vs Fig. 1(a) due to the enhanced dc gain. To the authors' knowledge, the proposed amplifier shows the largest FoM_{AVG} reported to date.

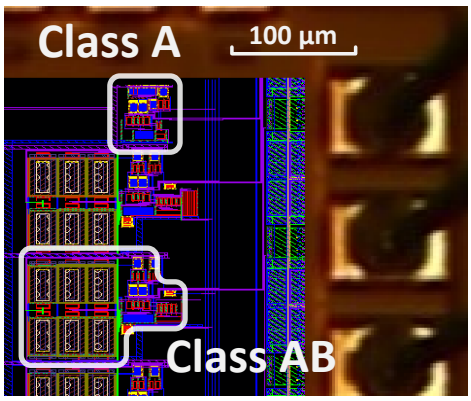


Fig. 2. Test chip microphotograph

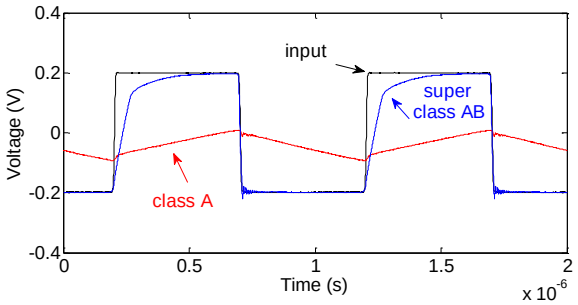


Fig. 3. Measured response of the OTAs of Fig. 1 to a square input signal

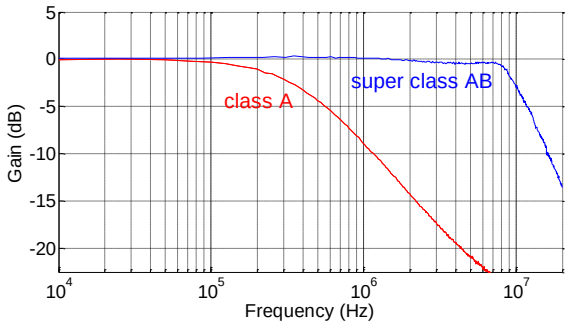


Fig. 4. Measured frequency response of the OTAs of Fig. 1.

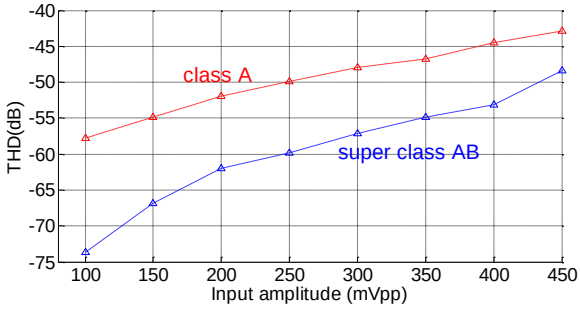


Fig. 5. Measured THD vs input amplitude at 10 kHz of the OTAs of Fig. 1.

TABLE I – SUMMARY OF MEASUREMENT RESULTS AND PERFORMANCE COMPARISON

Parameter (units)	Fig. 1(a)	Fig. 1(b)	[3]	[5]	[7]	[8]	[11]	[15]	[16]	[17]	[18]	[19]
CMOS process (nm)	130	130	500	500	180	500	130	180	180	180	130	500
Supply voltage (V)	±0.5	±0.5	±1	±1	±0.9	±1	±0.5	0.8	0.7	1.8	1.2	±1
Capacitive load (pF)	70/50	70/50	80	80	23	70	70/50	8	20	200	5.2	70
SR+ (V/µs)	0.085	4.1	100	20	24.11	13.2	3.72	0.14	1.8	74.1	98.7	9.8
SR- (V/µs)	-0.110	-38.6	-78	-54	-23.33	-25.3	-34.8	--	-3.8	--	--	-7.6
DC gain (dB)	38.19 [a]	47.24 [a]	43	39	67	76.8	58.72 [a]	51	57.5	72	75.4	81.7
PM (º)	89.8 [a]	86.4 [a]	89.5	58	84	75.1	78.8 [a]	60	60	50	82.5	60
GBW (MHz)	0.38	9.95	0.725	3.46	0.57	3.4	10.43	57	3	86.5	166.1	4.75
CMRR @DC (dB)	97	110	68	70	73.2	112	111	--	19	--	--	78
PSRR+ @DC (dB)	48	46	55	37	44.1	92	65	--	52.1	--	--	72
PSRR-@DC (dB)	46	45	58	70	41.8	113	56	--	66.4	--	--	74
Eq. input noise @1MHz (nV/√Hz)	147	57	230	--	--	23	41	--	100	--	--	35
Power (µW)	12	15	120	140	14.5	100	15	1.2	25.4	11900	236.4	120
Area (mm^2)	0.002	0.007	0.024	0.054	0.030	0.030	0.008	0.057	0.020	0.070	--	0.024
FoM_L (µA/µA)	1.13	99.63	118.67	42.29	67.72	26.95	89.88	0.75	1.54	2.24	2.61	10.15
FoM_S (MHz·pF/mA)	1583	33167	966.7	3954.3	1627.4	4760	34767	304	1653.5	2616.8	4384.4	5541.7
FoM_{AVG}	42.3	1817.8	338.7	408.9	332	358.1	1767.7	15.1	50.5	76.6	106.9	237.1

[a] Simulation

V. CONCLUSION

A power-efficient super class AB RFC OTA has been proposed, exploiting current starving and transition between ohmic and saturation region for dynamic current boosting. The amplifier can find application in energy-autonomous devices where very high power efficiency is required.

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