Super-Gain-Boosted Miller Op-Amp based on Nested Regulated Cascode Techniques with FoM_{AOLDC} =24,614kV/V.MHz.pF/µWatt

Anindita Paul
Electrical & Computer Eng.
NMSU
Las Cruces,USA
aninditapaul08@gmail.com

Jaime Ramirez-Angulo
Electrical & Computer Eng.
NMSU and INAOE
Las Cruces,USA
Pueblo,Mexico
jairamir@nmsu.edu

A. J. López-Martin
Electrical & Electronic Eng.
Public Univ of Navarra
Pamplona City, Spain
antonio.lopez@unavarra.es

R. G. Carvajal
Electronic Engineering
University of Seville
Sevilla, Spain
carvajal@ us.es

Alejandro Díaz Sánchez
Dept. of Electronics
INAOE
Pueblo, Mexico
adiazsan@inaoep.mx

***Abstract*—A simple technique to greatly enhance the DC open-loop gain of a Miller op-amp is introduced here. It is based on the utilization of nested regulated cascode amplifiers. It uses conventional Miller compensation and does not increase the supply voltage. The proposed scheme has a DC open-loop gain Figure of Merit FoM_{AOLDC}=24,614kV/V.pF.MHz/µWatt. It is especially appropriate for utilization in modern deep sub-micrometer CMOS technologies with low intrinsic gain.**

Keywords— Miller-Compensation, Class-AB amplifier, Regulated cascode, Differential Amplifier, Common-mode feedback

I. Introduction

As CMOS technology has scaled-down, the intrinsic gain A_i of MOS transistors has degraded continuously. It is currently in the order of $A_i=g_m r_o$~20 V/V (where g_m is the transconductance of the transistor and r_o is the output impedance of the MOS transistor). The DC open-loop gain is one of the most important parameters of an op-amp since it determines the accuracy of many systems. Among others, it determines the resolution of some D/A converters or the gain error of an amplifier. One and two-stage (Miller) op-amps (Figs. 1(a) and (b)) have been used for many years in most applications. They have a DC open-loop gain on the order of A_{OLDC}~$(A_i/2)^2$. This gain is insufficient for most applications in modern technology. Supply voltages have been also reduced as the technology scaled-down. This prevents the usage of cascoding devices in the output stage since they limit the output swing significantly. Non-cascoded one stage op-amps (also denoted OTAs) have a very low open-loop gain on the order of $A_i/2$ (~20dB) and for this reason, the only choice to achieve higher open-loop gain and high output swing with low supply voltages is the utilization of two-stage or multi-stage cascaded amplifiers. The latter requires complex nested Miller compensation schemes and are in practice limited (for stability reasons) to a maximum of three stages[1, 2]. Two-stage Miller op-amps can increase their gain by increasing the gain of their input stage using cascoded and regulated cascoded techniques [3]-[5]. Fig. 1c) shows the example of a Miller op-amp with a

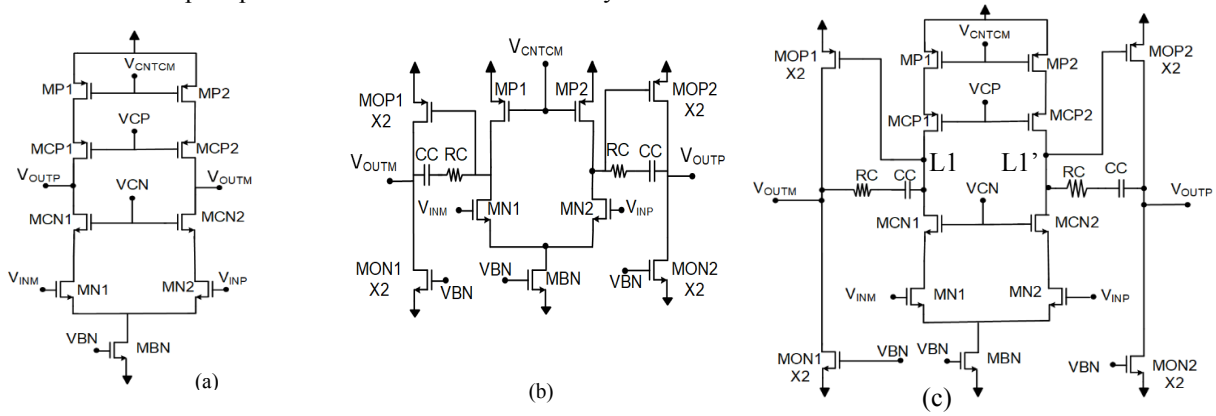

Fig.1 (a) Conventional one stage op-amp b) Conventional Two Stage Miller op-amp c) Telescopic input 2-stage Miller op-amp

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telescopic input stage that has a gain on the order of $A_{OLDC}=(A_i)^3/4$. In this op-amp, the presence of cascode transistors in the 1st stage provides higher impedance at the internal nodes L_1, L_1' which increases the gain of the first stage. It is possible to further enhance the gain of the first stage by adding more cascode transistor stages in series, but this increases the supply requirements. A non-cascoded push-pull output stage does not limit the output swing and provides modest additional gain $A_{II}=A_i/2$. Another possibility to further enhance the gain of a Miller op-amp without increasing supply requirements is the utilization of regulated-cascode techniques[4-6]. This technique enhances the effective gain of a cascode transistor by the gain of auxiliary amplifiers AuxP, AuxN used in a local negative feedback loop connected between the gate and source of the cascode transistors. Fig. 2 shows an example of a fully differential Miller op-amp with a telescopic input stage that uses regulated-cascode transistors with auxiliary amplifiers AuxP, AuxN (assumed to have similar gains $A_{AuxP}=A_{AuxN}=A_{Aux}$). These increase the open-loop gain of the op-amp by the factor A_{Aux} to a value $A_{OLDC}=((A_i)^3/4)A_{Aux}$.

In this paper, a super-gain-boosted Miller op-amp based on nested regulated cascode techniques with a DC open-loop gain on the order of $A_{OLDC}=(A_i^6/24)$ is introduced. Very high gain auxiliary amplifiers are implemented using single-ended folded cascode amplifiers in combination with a flipped voltage follower acting as a DC floating voltage source. The cascode transistors within the auxiliary amplifiers also use regulated cascode amplifiers in order to achieve very high gain. The circuits are explained in detail in the following section.

II. Amplifier Architecture

A. The topology of the proposed op-amp

The proposed super-gain-boosted fully differential two-stage Miller op-amp is shown in Fig.2. It uses a super-gain-boosted telescopic input stage incorporating nested regulated cascode technique and a non-cascoded push-pull free class AB output stage. The principle behind the super gain boosting of the first stage is to increase the impedance at nodes L_1, L_1' by a very large factor without including more cascode transistors in series. Gain boosted auxiliary amplifiers AuxN and AuxP are used to implement regulated cascode transistors M_{CP1}, M_{CP2} and M_{CN1}, M_{CN2}, respectively. The auxiliary amplifiers with gains A_{AuxN} and A_{AuxP} use two single-ended folded cascode amplifiers in combination with a cascoded flipped voltage follower (CASFVF) that acts as a DC floating voltage source to set the voltages at nodes Y_1, Y_1', X_1, X_1'. Gain boosted auxiliary amplifier use simple differential amplifiers to implement the nested regulated cascode technique for the cascode transistors used within the auxiliary amplifiers. For simplicity, it is assumed that A_{AuxN} and A_{AuxP} have equal values i.e. $A_{AuxN}=A_{AuxP}=A_{Aux}$. The auxiliary amplifiers enhance the output impedance (and open-loop DC gain of the op-amp) of the first stage at nodes L_1(L_1') by the factor A_{Aux}. The voltages applied at the terminals $V_{ref\text{-}X1}$ and $V_{ref\text{-}Y1}$ of the auxiliary amplifiers set accurately the values of the drain voltages of M_{N1}, M_{N2}, and M_{P1}, M_{P2}. This is required in order to keep all transistors in saturation with low supply voltage. The impedance at nodes L_1, L_1' at the output of the first stage

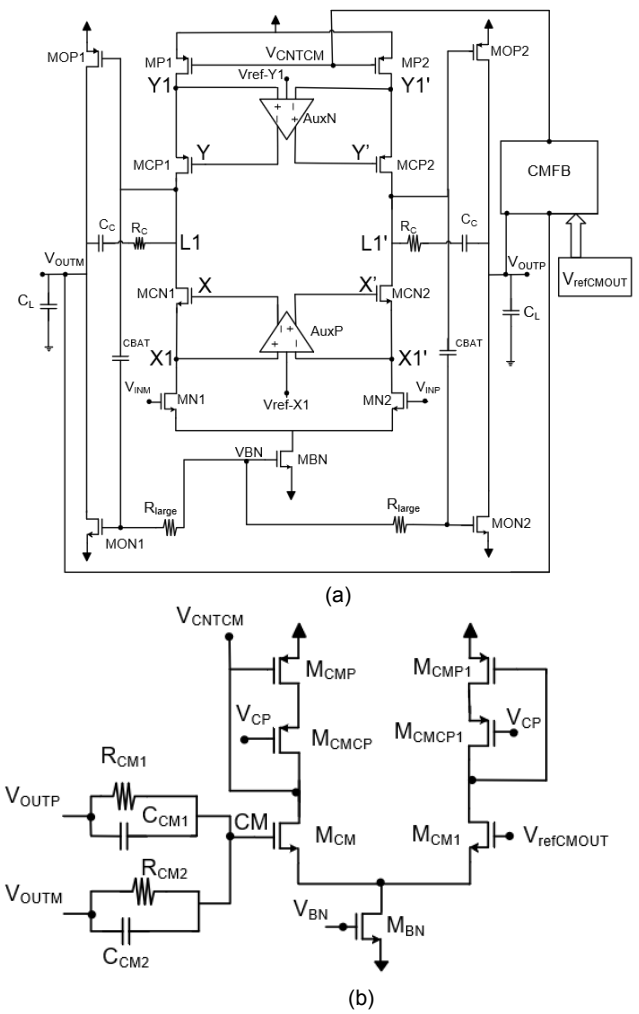

Fig. 2 a) Proposed topology of the gain boosted op-amp b) common-mode feedback network

($R_{outL1,1'}$) is given by $R_{outL1,1'}=\left(A_{Aux}g_{mCP1,2}r_{oCP1,2}r_{oP1,2}\right)\|\left(A_{Aux}g_{mCN1,2}r_{oCN1,2}r_{oN1,2}\right)$. Where g_{mCP1}, g_{mCN1} are the transconductance gains of the cascode transistors M_{CP1} and M_{CN1} of the input-stage. r_{oN1}, r_{oCN1}, r_{oCP1}, r_{oP1} are the output resistances of M_{N1}, M_{CN1}, M_{CP1}, M_{P1}. Assuming for simplicity that all transistors have similar g_m and r_o values then $R_{outL1,1'}$ becomes

$$R_{outL1,1'}=\left(A_{Aux}g_m r_o^2\right)\|\left(A_{Aux}g_m r_o^2\right)=\left(A_{Aux}A_i r_o\right)/2 \quad (1).$$

To provide high output swing and high current-efficiency a non cascoded free class AB push-pull output stage is used [7] that incorporates dynamic elements R_{large} and C_{BAT} to achieve symmetrical output currents that have much larger peak values than the output stage quiescent current.

The impedance of the output stage R_{outA2} is given by $R_{outA2}=r_{oP1,2}\|r_{oN1,2}=r_o/2$. The DC open-loop gain of the op-amp A_{OLDC} is given by (2).

$$A_{OLDC}=g_{mN1}R_{outL1}g_{mOP}R_{outA2}=g_m{}^2\left(A_{Aux}A_i r_o\right)r_o/4=\left(A_{Aux}A_i^3\right)/4 \quad (2)$$

From (2) it can be asserted that the open-loop gain of the op-amp increases by the gain A_{Aux} of the auxiliary amplifier. In the

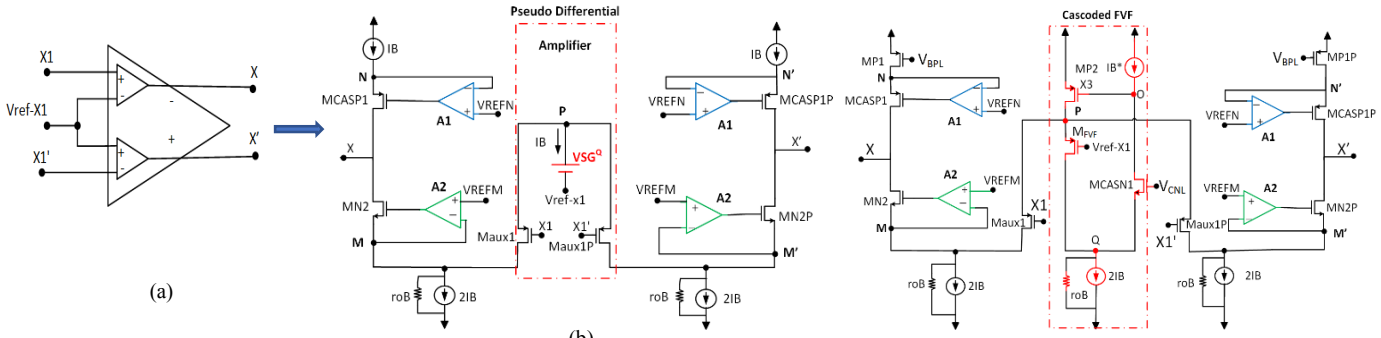

Fig.3. (a), (b) Block and (c) Schematic diagram of the AuxP amplifier

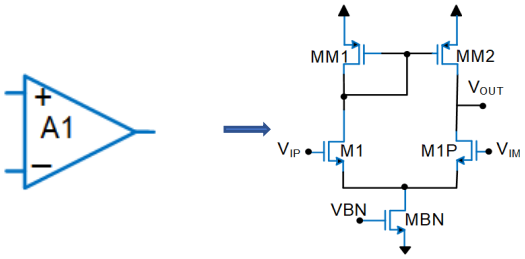

Fig. 4 NMOS differential pair auxiliary amplifier

next section, the implementation of the auxiliary amplifiers with very high gain A_{Aux}~A_i^3 based on ***nested regulated cascode techniques is shown***. These lead to an extremely high op-amp's DC open-loop gain A_{OLDC}~A_i^6.

As the op-amp is fully differential a common-mode feedback (CMFB) network is used to set the output common-mode voltage to a mid-supply value $V_{refCMOUT}=0$. The CMFB loop has the similar DC open-loop gain, phase margin as the differential loop. The CMFB circuit is shown in Fig. 2(b).

B. Auxiliary Amplifier

In order to provide enough headroom, an auxiliary amplifier with NMOS (PMOS) input stage is used to drive the PMOS (NMOS) cascode transistors M_{CP1}, M_{CP2} (M_{CN1}, M_{CN2}). Both A_{uxN} and A_{uxP} use Pseudo-differential amplifiers with a DC level shifter implemented using a Cascoded Flipped Voltage Follower (CASFVF) [8-10]. These set accurately the voltages V_{X1}, V_{X1}' to a reference value $V_{X1}=V_{X1}'=V_{ref\text{-}X1}$ and V_{Y1}, V_{Y1}' to a value $V_{Y1}=V_{Y1}'=V_{ref\text{-}Y1}$ respectively. These values are selected to keep all transistors in the input stage in saturated mode. In Fig.3 transistors M_{aux1} and M_{aux1P} implement single-ended folded cascode amplifiers with an AC signal ground at node P. A cascoded flipped voltage follower (CASFVF, enclosed in a dotted red box) is used for this purpose. Due to the use of the CASFVF the impedance at node P is very low $(R_P\sim 3/g_m(g_m r_0)^2)$ and this node acts approximately as a virtual AC ground with a quiescent voltage $V_P=V_{ref\text{-}X1}+V_{SGQ}$. Negative feedback sets the voltages at the output nodes X, X' of the auxiliary amplifiers until the conditions $V_{X1}=V_{X1}'=V_{ref\text{-}X1}$ are satisfied. The auxiliary amplifiers require a minimum supply voltage V_{DD}-$V_{SS}=3V_{DSsat}+|V_{TP}|$. To increase the output resistance of the auxiliary amplifiers another two auxiliary amplifiers (A1, A2) are used within the auxiliary amplifiers to provide nested regulated cascode operation to transistors $M_{CASP1,\ P1P,}$ and $M_{N2,2P}$. The auxiliary amplifiers A_1 (A_2) are NMOS (PMOS) differential amplifiers with a current mirror load. NMOS auxiliary amplifier is shown in Fig. 4. Auxiliary amplifier A2 (complement of A1) and A_{uxN} (complement of A_{uxP}) are not shown here. The gain A_1 is given by $A_1 = g_{mn1}\left(r_{oM1} \| r_{oMM1}\right) \approx g_m r_o/2 \approx A_i/2$.

The output impedance at nodes X, X' of the auxiliary amplifiers (assuming for simplicity equal gains $A=A_1=A_2$) is $R_{outX,X'} = \left(\left(r_{oaux1} \| r_{oB}\right) A g_{mN2} r_{oN2}\right) \| \left(r_{oP1} A g_{mCASP} r_{oCASP}\right)$. Considering for simplicity that all transistors' have equal g_m and r_o parameters $R_{outX,\ X'}$ becomes $R_{outX,X'} = r_o A A_i/3$. Thus, gain A_{Aux} of the auxiliary amplifiers is given by (3).

$$A_{Aux} = g_{maux1,1P} R_{outX,X'} = A A_i^2/3 \approx A_i^3/6 \qquad (3)$$

Hence from (2) and (3) the DC open-loop gain of the proposed op-amp is given by $A_{OLDC} = A_i^6/24$. As shown in the simulations in the next section A_{OLDC} can be greater than 140dB in 130nm CMOS technology.

C. Pole/ Zero analysis and Stability

Conventional Miller compensation is used to obtain stability of the op-amp. The main op-amp has 2 poles and a zero. The dominant pole is at nodes L1 (L1') is given by $f_{pDOM} = 1/\left(2\pi R_{outL1}\left(1+A_{II}\right)C_C\right)$ where $A_{II} = (g_{mOP})R_{out}$ is the DC gain of the output stage and C_C is the Miller capacitance. The 1st high-frequency pole is at the output node and given by $f_{HFp} = 1/\left(R_{Out}{}^{HF} C_L\right) = g_{mouteff}/\left(2\pi C_L\right)$ where $R_{out}{}^{HF} = 1/g_{mouteff}$ is the effective output resistance at high frequencies and the value $g_{mouteff} = g_{mOP}+g_{mON}$ is due to the presence of the C_{BAT} capacitor which shorts the gate of the M_{OP} and M_{ON} at high frequencies. The zero is given by $f_z = 1/\left(2\pi\left(R_C - g_{mouteff}^{-1}\right)C_C\right)$. The gain-bandwidth product GBW is given by $GBW = A_{OLDC} f_{pDOM} = A_I A_{II}/\left[2\pi\left(1+A_{II}\right)C_C R_{outL1}\right] \approx g_{mN1}/\left(2\pi C_{C1}\right)$. The high-frequency poles in the local feedback loops of the regulated cascode amplifiers are not considered in the analysis since they are high-frequency poles that have a negligible effecton the phase margin. This is verified by the simulations shown in the next section.

A gain boosted Miller op-amp with GBW=44MHz was designed in 130nm CMOS technology. Values C_C=2.5pF,

R_C=1.8kΩ, g_{mOP}=1.53mA/V, g_{mON}=1.73mA/V, g_{dsOP}=31.4µA/V, g_{dsON}=44.8µA/V, g_{mN1}=705µA/V were used. R_C was selected so that the zero would approximately match the output pole. The gain of both auxiliary amplifiers (A_{uxN} and A_{uxP}) is approximately 3000V/V. R_{outL1} is 1.3GΩ and the gain A_{II} of the output stage is A_{II}=20V/V. Theoretical values f_{pDOM}=2.3Hz, f_z=42MHz, f_{HFp}=35MHz, and GBW=44MHz were obtained. As the pole-zero doublets are very close to GBW and they are close to each other it will not affect the settling response of the op-amp significantly according to $V_{out}(t) = V[1-\exp(-GBW*t)+[(\omega_z-\omega_p)/GBW]\exp(-\omega_z t)]$.

III. Simulation Results

The proposed gain boosted op-amp was simulated in 130nm CMOS technology with NMOS and PMOS unit transistor sizes $(W/L)_N$=10µm/0.27µm and $(W/L)_P$=50µm/0.27µm respectively. The op-amp was simulated with I_B=30µA. To reduce quiescent power dissipation (P^Q) the transistor sizes of the auxiliary amplifiers were scaled-down by a factor 5 compared to the unit transistor size used in the main op-amp. The value of the supply voltage was ± 0.6V and the load capacitance C_L=15pF. The open-loop magnitude and phase responses of the proposed nested gain-boosted, gain-boosted with only one regulated cascode, telescopic, and conventional two-stage op-amps are shown in Fig. 5. The proposed op-amp

TABLE I Summary of Simulation Results and Comparison

	[11]	[12]	[13]	[14]	[15]	**Proposed**
Process (µm)	0.18	0.35	SMIC 0.25	0.8	0.18	**0.13**
Supply(V)	1.8	3.3	2.5	3.3	1.8	**1.2**
I_{Qtotal}(µA)						**330**
P^Q(W)	3.8 m	3.89m	35m	4.8m	7.34m	**396µ**
C_L (pF)	1	2	4	3.65	1	**15**
Gain(dB)	80	129	102	105	105.4	**144**
PM (degree)	73	70	62.5	78	74	**70**
GBW(MHz)	660	161	822	93	1440	**41**
SR+(V/µs)	-	92	839	125	-	**24**
SR- (V/µs)	-	-	-	-	-	**23**
1% settling time	-	23.5ns	3.5ns	26ns	-	**65ns/ 64ns**
CMRR (dB)@dc/1k/100k	-	89.8	-	57	-	**250/ 200/178**
PSRR+/- (dB) @dc,1k,100k	-	-	-	-	-	**284/200, 150/250, 200/153**
FOM_{AOLDC} kV/V.pF.MHz/µW	2	233	12	13	37	**24,614**
FOM_{LS}(V/µs)(pF/µW)	-	0.04	0.09	0.09	-	**0.9**
Equivalent input noise(nV/√Hz)	-	-	-	-	-	**109**

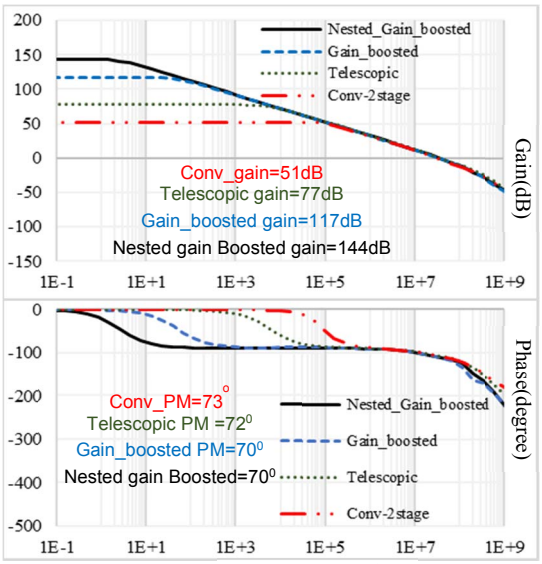

Fig.5 Op-amp's open loop gain and phase comparison in 130nm CMOS technology

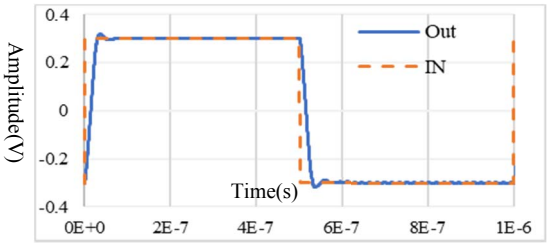

Fig.6 Transient response of the proposed op-amp for a 1MHz pulse input

has A_{OLDC}=144dB, PM=70°, unity gain frequency f_u=35MHz, f_{3dB}=2.6Hz, and gain-bandwidth product GBW=41MHz. The Phase Margin (PM) of all op-amps is very similar. Hence, it can be asserted that the introduction of the nested regulated cascode technique using two auxiliary amplifiers does not degrade the phase margin. The transient response of the op-amp in the unity-gain closed-loop configuration is shown in Fig.6. Positive and negative slew rates (SR) obtained from the transient response are 24 and 23V/µs. The DC open-loop gain figure of merit of the proposed op-amp is given by $FoM_{AOLDC} = (A_{OLDC}.GBW.C_L)/P_Q$ =24,614(kV/V).(MHz.pF)/µW and $FoM_{LS} = SR.C_L/P_Q$ =1(V/µs).(pF/µW) which is the highest among the references. Common mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) are simulated by introducing 2% mismatch in the output transistors. The corresponding values are given in TABLE I.

IV. Conclusion

Utilizing nested regulated cascode techniques a Miller op-amp with significantly enhanced open-loop DC gain, high PM, with minimum effect in settling time, and by just moderate increase in power dissipation, were introduced and verified with simulations.

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