Public University of Navarre

Electrical and Electronic Engineering Department

POWER-EFFICIENT CURRENT-MODE ANALOG CIRCUITS FOR HIGHLY INTEGRATED ULTRA LOW POWER WIRELESS TRANSCEIVERS

PhD. dissertation prepared to obtain the Doctor degree

By

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Pamplona, September 2014

UNIVERSIDAD PÚBLICA DE NAVARRA

DEPARTAMENTO DE INGENIERÍA ELÉCTRICA Y ELECTRÓNICA

Tesis doctoral:	Power-Efficient Current-Mode Analog Circuits for Highly Integrated Ultra Low Power Wireless Transceivers
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Tribunal nombrado para juzgar la Tesis Doctoral citada:

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Pamplona, a de de 2014

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ABSTRACT

In this thesis, current-mode low-voltage and low-power techniques have been applied to implement novel analog circuits for zero-IF receiver backend design, focusing on amplification, filtering and detection stages. The structure of the thesis follows a bottom-up scheme: basic techniques at device level for low voltage low power operation are proposed in the first place, followed by novel circuit topologies at cell level, and finally the achievement of new designs at system level.

At device level the main contribution of this work is the employment of Floating-Gate (FG) and Quasi-Floating-Gate (QFG) transistors in order to reduce the power consumption. New current-mode basic topologies are proposed at cell level: current mirrors and current conveyors. Different topologies for low-power or high performance operation are shown, being these circuits the base for the system level designs.

At system level, novel current-mode amplification, filtering and detection stages using the former mentioned basic cells are proposed. The presented current-mode filter makes use of companding techniques to achieve high dynamic range and very low power consumption with for a very wide tuning range. The amplification stage avoids gain bandwidth product achieving a constant bandwidth for different gain configurations using a non-linear active feedback network, which also makes possible to tune the bandwidth. Finally, the proposed current zero-crossing detector represents a very power efficient mixed signal detector for phase modulations. All these designs contribute to the design of very low power compact Zero-IF wireless receivers.

The proposed circuits have been fabricated using a 0.5µm double-poly n-well CMOS technology, and the corresponding measurement results are provided and analyzed to validate their operation. On top of that, theoretical analysis has been done to fully explore the potential of the resulting circuits and systems in the scenario of low-power low-voltage applications.

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LIST OF ACRONYMS

Acronym	Significance
A/D	Analog/Digital
AC	Alternating Current
ACG	Automatic Gain Control
ADSL	Asymmetric Digital Subscriber Line
BJT	Bipolar-Junction Transistor
BW	Bandwidth
CCII	Second-generation Current Conveyor
CMC	Common-Mode-Control
CMFB	Common-Mode Feedback
CMOS	Complementary Metal-Oxide-Semiconductor
CMRR	Common-Mode Rejection Ratio
D/A	Digital/Analog
DC	Direct Current
DVB	Digital Video Broadcasting
EPROM	Erasable Programmable Read-Only Memory
FGMOS	Floating-Gate Metal-Oxide-Semiconductor
FG	Floating-Gate
FGT	Floating-Gate Transistor
FoM	Figure of Merit
GB	Gain-Bandwidth Product
G_m-C	Transconductor-Capacitor
IF	Intermediate Frequency
IM3	3rd -order Intermodulation Distortion

LAN	Local Area Network
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect-Transistor
MOSFET-C	MOSFET- Capacitor
nMOS	Negative-Channel Metal-Oxide-Semiconductor
opamp	Operational Amplifier
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
pMOS	Positive-Channel Metal-Oxide-Semiconductor
PpP	Power-per-Pole
PSRR-	Negative Power-Supply-Rejection-Ratio
PSRR+	Positive Power-Supply-Rejection-Ratio
QFG	Quasi-Floating-Gate
QFGMOS	Quasi-Floating-Gate Metal-Oxide-Semiconductor
QFGT	Quasi-Floating-Gate Transistor
RSSI	Received Signal Strength Indication
SFDR	Spurious-Free Dynamic Range
SNR	Signal-to-Noise Ratio
THD	Total Harmonic Distortion
UV	Ultraviolet
V-I	Voltage-Intensity
VDSL	Very high bit-rate Digital Subscriber Line
VGA	Variable Gain Amplifier
VLSI	Very-Large-Scale Integration
WiMAX	Worldwide Interoperability for Microwave Access

PARAMETER GLOSSARY

Parameter	Significance
C_{GB}	Gate-Bulk capacitance
C_{GD}	Gate-Drain capacitance
C_{GS}	Gate-Source capacitance
C_{ox}	Gate Oxide capacitance per unit area
f_c	Cutoff frequency
g_m	MOS transistor transconductance defined as $\partial I_D/\partial V_{GS}$
G_m	Total transconductance of an OTA or transconductor
I_B	Bias current
i_D	MOS transistor drain current
K	1) Current scaling factor
	2)MOS transistor transconductance coefficient
K_B	Boltzmann constant ($1.38 \cdot 10^{-23}$ J/K)
L	Channel length of a MOS transistor
n	Subthreshold slope factor
P_n	Input-referred noise power
q	Electron charge
r	Channel resistance of a triode transistor
Q_0	Initial electric charge
T	Temperature
U_T	Thermal voltage
V_{CM}	Common-mode voltage

V_{cn}	Bias voltage in an nMOS cascode transistor
V_{cp}	Bias voltage in a pMOS cascode transistor
V_{DD}	Positive supply voltage
V_{SD}, V_{DS}	Source-drain/ Drain-source voltage of a MOS transistor
V_{SG}, V_{GS}	Source-gate/ Gate-source voltage of a MOS transistor
V_{SS}	Negative supply voltage
V_t	Threshold voltage of a MOS transistor
W	Channel width of a MOS transistor
μ_n	Electron mobility parameter

CHAPTER 1

Introduction

This chapter introduces the reader into the how's and why's of this thesis. First, the motivations behind this work are discussed, paying special attention to answering the big questions: Why analog? Why low voltage? Why low power? Why current mode? Afterwards, a brief overview of the most commonly used short distance communication standards is presented followed by a discussion on low power receivers. Finally, the objectives of this thesis are outlined, and a summary of the thesis' structure is given.

1.1 Motivation

As its own title states, the motivation behind this thesis is simple: developing new analog current-mode circuits for wireless receivers that can operate at very low voltages and with ultra-low power consumption.

The previous paragraph has some important key words: Analog, current-mode, low-voltage, low-power and wireless receivers. All these points are discussed next.

1.1.1 Why Analog?

Since the digital revolution started to take place, year after year, modern communication circuits have been gradually migrating more functions from the analog world to the digital domain. Once the signal is in the digital domain, it is

easy to do pretty much anything with it, with better precision, performance and dynamic range than in the analog domain. However, transforming a signal from the analog to digital domain and vice versa can be very complex and power consuming. Besides the analog to digital conversion (ADC) and digital to analog conversion (DAC), digital designs have faster time-to-market, lower development cost and they are easier to test than their analog counterparts [Lat09]. For these reasons, in many applications, analog circuits are only used for interfacing the digital systems to the real world.

Nevertheless, there are applications where analog electronics are preferred, proving to be more convenient than digital processing in terms of power consumption, size or cost [Vit94]. Using low power analog blocks can lead to simpler ADCs / DACs, and a more power efficient implementation. This thesis is focused in this mixed signal approach, where all the signal processing is done in the analog domain using ultra low power blocks. Afterwards, the digital message is obtained using a very simple ADC.

1.1.2 Why Low-Voltage?

As it is explained in Chapter 2, lower supply voltages lead to lower overall power consumption. Only for that reason, it is worth to reduce the voltage supplies. Nevertheless, this is not the main reason behind the low voltage trend. CMOS circuits are at the forefront of Very Large Scale Integration (VLSI). Modern CMOS technologies have smaller transistors with reduced gate oxide transistors thickness. As the gate oxide thickness is shorter, the maximum voltage supplies are also reduced to avoid an excess of electric fiend intensity in the devices [Fay03].

Since the 90's, transistors supply voltage has decreased from 5V in 500nm technologies to 0.9V in 65nm processes, and it is supposed to keep decreasing according to SIA Roadmap predictions [Sia13]. Table 1.1 [Pek04] exemplifies this trend showing the main parameters of various CMOS processes.

A critical problem when designing analog circuits in modern deep submicron technologies is that while the supply voltage scales linearly with the minimum transistor length, the threshold voltage scales as a square root function [Bul00]. As a result of this fact, the threshold voltages are getting closer to the supply voltages. Although this is not a problem in digital circuits, most of the typical analog circuits architectures can't be directly implemented in newer technologies as transistors may not be biased in saturation anymore, degrading

both dynamic range and signal to noise ratio [Ste97, Ann99]. Moreover, it is interesting to use the same voltage supplies for both digital and analog parts, avoiding the complexity involved in generating various voltage supplies [Ram09]. Therefore, novel low voltage topologies are needed in order to accommodate to the newer CMOS processes. In chapter 2, some of these techniques are explained: dynamic cascode biasing [Ram08, Esp12, Esp14], sub threshold operation [Bar72, Tro73, Nas74, Tro75, Bar76, Vit76, Vit77, Vit91, Enz95, Enz96, Vit03, Wan06] and companding [Cla28, Mat34, Ada79, Bel82, Tsi90, Tsi95].

1.1.3 Why Low-Power?

Modern lifestyle is now, more than ever, bounded to portable devices: smart phones, laptops, tablets, e-book readers, wireless sensors networks, wristwatches, cameras, portable music devices, etc. Everybody wants to be permanently connected to the internet anywhere. It is funny to think that wasting energy was never a problem for most inhabitants of the first world, but running out of battery in your smart phone is for some people a matter of life and death. Low power operation is a must not only in consumer electronics, but in wireless sensors networks, where sensor nodes must be autonomous for a long period of time, either with small batteries [Wai03, Kun07] or without batteries using energy harvesting techniques [Can06, Rou06, Pri09, Kha14]. Moreover, deep CMOS technology beyond 65nm node represents a real challenge for keeping power density low enough, which requires decreasing the overall power. For these reasons, it is very important to develop low power techniques. In Chapter 2, how to implement the class AB operation [Kaw96, Ram06] (a very useful low-power technique) with Quasi-Floating Gate MOS [Ram03, Ram04, Ram06] transistors is explained.

1.1.4 Why Current-Mode?

Much has been said about the current mode approach since the first works on this topic were presented [Gil68a, Gil68b, Gil68c, Smi68, Sed70, Gil75, Tou90]. Although more than 40 years have passed since then, even now there isn't a clear definition agreed by the scientific community about what a current-mode circuit is. A widespread definition is that a current-mode circuit is one where its inputs and outputs are currents; Gilbert defined the current-mode circuits in a very specific manner, formulating a few characteristics that a current-mode circuit should have, being the most important one that "a current-mode (CM) circuit is one whose signal states are completely and unambiguously defined by its branch currents." [Gil04]. Schmid claimed that the current-mode should

not be strictly defined and that both current-mode and voltage-mode (VM) knowledge should merge together in order to apply all the state of the art from the current-mode way into the mainstream circuit design community [Sch03].

Besides of the "definition" problem, there is also the "what is better: VM or CM?" question. Although plenty of the current-mode published papers [Kum10, Li10, Zha10] claimed that current-mode circuits have higher bandwidth, simpler architecture, better dynamic range, lower voltage operation, better linearity and lower power consumption, others [Gil04, Sch03] said that this is a fallacy. [Sch03] traced back around 100 references in the current-mode state of the art concluding that there is no evidence at all that proves that in general, current-mode circuits are better than voltage mode circuits.

Moreover, current-mode circuits have some drawbacks with respect to the voltage-mode circuits. Generating on-chip accurate current references without an accurate voltage source is not an easy task [Gil04]; measuring currents is not as easy as measuring voltages; in digital voltage-mode circuits several gate-input stages can be driven without concerning much about the loads, etc.

That being said, even not strictly defining what a current-circuit is, neither claiming that current-mode circuits are better that voltage-mode circuits, the current-mode approach has demonstrated himself to be a useful tool. Within the current-mode approach philosophy is to try to design simpler circuits, avoid feedback and have low impedance internal nodes. This philosophy can be translated into high bandwidth, low-voltage, simple and elegant circuit solutions that can be very useful in applications where it is preferred to process the signal in the form of a current.

Table 1.1. Downscaling of CMOS processes [Pek04]

	250nm	180nm	130nm	90nm	65nm
L_{gate}(nm)	180	130	92	63	43
t_{ox}(nm)	6.2	4.45	3.12	2.2	1.8
g_m(μS/μm)	335	500	720	1060	1400
g_{ds}(μS/μm)	22	40	65	100	230
g_m/g_{ds}	15.2	12.5	11.1	10.6	6.1
V_{DD}(V)	2.5	1.8	1.5	1.2	1
V_{TH}(V)	0.44	0.43	0.34	0.36	0.24
f_T(GHz)	35	53	94	140	210

1.2 Short distance low-power wireless communication standards

Short distance wireless communications have become a key area in the last years. There are a great number of communication standards that can be used for short distance low power wireless communications, used in a wide range of applications such as cell phones, health and fitness devices, home automation, ventilating, heating, and air conditioning (HVAC), gaming, payment, remote controls, human interface devices (HID) or smart meters.

Some of the most employed communication standards for short distance low-power wireless communications are Bluetooth Low Energy (BLE) [Ble14], ANT (+) [Ant14], ZigBee [Zig14], Wi-Fi [Wif14], Nike+ [Nik14] and Infrared Data Association (IrDA) [Ird14]. Comparing all these low-power wireless technologies [Smi11] could be a thesis by itself, and it is not the goal of this section. Therefore, a very brief summary of these technologies is presented.

ANT(+) and Nike+ are proprietary wireless technologies developed by Dynastream and Nike&Apple respectively, used mainly in the fitness industry, and within a very small range (<30m / <10m) and providing very small data rates (20kbps / 272 bps). For these reasons, they are not very interesting as general communication systems.

IrDA can provide up to 1Gbps, but, as it requires line-of-sight operation and its range is less than 2m, becoming a very application-specific standard (multimedia wireless communications).

BLE, ZigBee and Wi-Fi are very versatile all-purpose standards, compared in Table 1.2. ZigBee is a low-power wireless specification, targeting applications such as home automation, smart meters and remote control units. ZigBee adopted the IEEE 802.15.4 standard for the PHY and MAC layers. This standard was developed by the IEEE 802 standards committee and was initially released in 2003 (standard IEEE 802.15.4-2003) and later on updated in 2006 (standard IEEE 802.15.4-2006). Over these two layers, ZigBee defines the protocols and procedures for the upper layers to develop the ZigBee specification (officially named ZigBee 2007). ZigBee is mainly targeted for battery-powered devices requiring low cost, low data rate, and long battery lifetime. These devices are typically used in low-latency applications, where the percentage of time the device is active performing any sensing or data transmission task is very small, spending most of the time in sleep mode to save power.

WiFi is based on IEEE standard 802.11. It allows wireless data transfer between devices in relatively large areas such as a campus or a building. Devices usually connect using unlicensed RF bands to an access point which provides internet access. Typical WiFi users are static or move at pedestrian speed. It is widely used worldwide, but even though Wi-Fi is a very efficient wireless technology (see table 1.2), it is optimized for large data transfer. Therefore, it is not suitable for ultra-low power applications.

Bluetooth Low Energy started as a Nokia Research Centre project called Wibree. In 2007 this technology was adopted by the Bluetooth Special Interest Group (SIG) and renamed as BLE. This technology includes features designed to enable products that require lower power consumption, lower complexity and lower cost than conventional Bluetooth Basic Rate or Enhanced Data Rate. The BLE system is also designed for use cases and applications with lower data rates and has lower duty cycles, such as several wireless sensor network applications, where devices operate for large periods of time using a simple coin cell, like the popular CR2032.

1.3 Low Power Receivers

In general, receivers can be grouped into two main categories: Heterodyne and homodyne architectures [Raz98].

Homodyne receivers, also called direct conversion [Dur02, Duv03, Mak04, Yoo04, Yan07, Tom09, Bal10, Syu11, Hsi12, Mas13] or Zero Intermediate Frequency (Zero-IF) down convert the incoming RF signal to baseband using an oscillator frequency equal to the RF carrier frequency, therefore using an intermediate frequency equal to zero. Because of its simplicity Zero-IF architecture can lead to a very compact and power efficient design.

Table 1.2. Wireless standards comparison

	BLE	ZigBee	Wi-Fi
Radio frequency (GHz)	2.4	2.4	2.4/5
Channel BW (MHz)	1	2	20/40
Typical distance range (m)	280	100	150
Max. data rate (Mbps)	1	0.2	54
Peak current consumption (mA)	12.5	40	116
Power per bit (μW/bit)	0.153	185.9	0.00525

Heterodyne receivers have been used extensively since the first wireless devices were invented. These topologies are based on progressively down converting the incoming RF signal to one or several intermediate frequencies (each time at a lower frequency) amplifying and filtering at each stage. Using various stages, these receivers achieve high sensitivity and selectivity, but they require highly selective filters for image rejection and channel selection. The high power consumption associated with multiple down-converting amplification and filtering stages, together with the impossibility of implementing these filters on chip, requiring external ceramic or surface acoustic wave (SAW) resonators [Mon04, Daw03, Con02, Sat06] make these topologies non suited for low power low cost devices. Nevertheless, there is one kind of heterodyne receiver, the Low-IF receiver [Cro95, Cro98, Zen03, Crip04, Her06, Nam07], which is simple (as it only has one down-converting stage) and can lead to very power efficient designs.

Both Low-IF and Zero-IF architectures are explored in this section, paying special attention to the latter, as it is the chosen topology.

1.3.1 Low-IF receiver

A typical Low-IF receiver is shown in Figure 1.1. As it can be seen, this architecture consists on a RF stage where the input signal is band pass filtered and amplified using a low noise amplifier (LNA). Then the signal is down-converted to the intermediate frequency and split into the in phase (I) and quadrature (Q) branches. These signals are amplified and filtered before going into the demodulator. The main advantage of this solution is that the signal spectrum is kept out of baseband, overcoming two important signal degradations: The DC offsets and the flicker Noise.

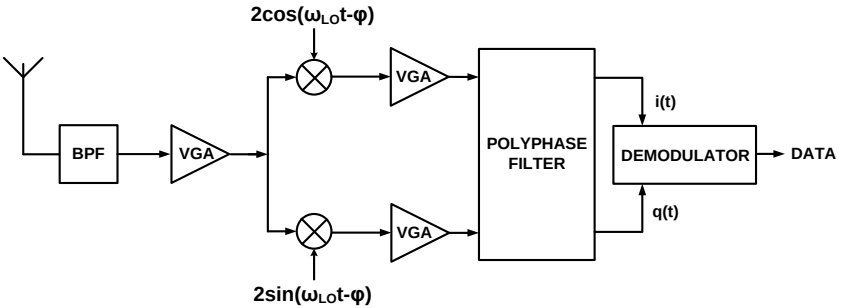

Figure 1.1. Low-IF receiver architecture

The DC offset is caused by the inherent offset of baseband signal processing circuits and the self-mixing of the local oscillator signal at the mixer. As the level of this offset can be orders of magnitude larger than the incoming signal, if it is not removed it can lead to strong signal degradation or saturation of the baseband circuits. In Low-IF receivers, if the signal is processed at a sufficient high intermediate frequency the bandpass response of the baseband circuits can efficiently remove this offset.

The flicker or 1/f noise is dominant in CMOS circuits up to moderately high frequencies (up to hundreds of kHz). As in the case of the DC offset, if the IF frequency is set appropriately, the IF chain signal processing can remove most of the flicker noise power. Nevertheless, the power consumption increases with the IF, being a tradeoff between flicker noise, DC offset reduction and overall power consumption. In Bluetooth, it is typical to choose IF=2MHz.

Despite of these advantages, the low-IF solution has two main shortcomings: increased power consumption due to the nonzero IF signal processing and need for image rejection. As in all the heterodyne receivers, the image spectrum must be rejected. In the Low-IF receiver the image spectrum can be rejected using complex polyphase bandpass filter processing both I and Q signal components [Che01, Kir08, Li11]. Nevertheless, this approach requires a good linearity and gain and phase matching between I and Q components, increasing the system sensitivity to I and Q gain/phase mismatch. It is also possible to use conventional image rejection filtering in the RF front-end, but as explained before, it comes with an increase of cost, complexity and circuit integration limitations.

1.3.2 Zero-IF Receiver

Figure 1.2 shows a typical Zero-IF receiver with direct conversion of the RF signal to baseband. Due to its simplicity, it has two main advantages with respect to other receivers: No image rejection is required (as the signal itself is its own image) and simpler channel filtering. These advantages directly impact on the receiver's power consumption, making this topology a promising choice in terms of cost, integration density and power consumption. However, as the signal is processed in baseband, this receiver suffers from the degradations mentioned in the previous section: the DC offset and the flicker noise. Both problems can be solved using a simple RC highpass filter after the mixer in modulations with negligible near-DC components, like the FSK signals with high modulation index [Wil91]. When the employed modulations have significant spectral content near

DC other solutions, typically based on feedback loops, can be employed. Nevertheless, they are more complex and usually they don't remove completely the time-varying offset.

The zero-IF receiver was selected versus the low-IF receiver because in spite of its constraints [Abi95] this approach can lead to more compact, simpler, and more power efficient implementations. As seen in Figure 1.2, this thesis is focused on implementing the backend part of a Zero-IF receiver framed in red: filtering, amplification and detection stages. All these blocks operate in the current-mode domain, so an input current signal is assumed. The output of the detector is a digital signal which is fed into the digital processor, whom provides the dispatched data. The order, number and specifications of the filtering and amplification stages, as well as the specifications of the rest of the receiver chain can vary, as it is the mission of the designer to accomplish the standard specifications. Table 1.3 [Bal10] shows the radio specifications for Bluetooth and ZigBee operating in the 2.4-GHz ISM Band. The mission of the system designer is to extract the concrete specifications of each block so the overall receiver accomplishes the specifications. In order to do so, system level software such as Agilent Advanced Design System (ADS) can be used. As the specifications of each block affect the entire system, many iterations may be necessary until the final specifications for each block are defined. In this manner, it is possible to relax the specifications of a specific block by increasing the performance of the other system blocks.

Table 1.3. Radio specifications for Bluetooth and ZigBee in 2.4-GHz ISM Band [Bal10]

	Bluetooth	ZigBee
Frequency band (MHz)	2400-2480	2400-2483
SNR at demodulator (dB)	15	7
Channel bandwidth (MHz)	1	2
Data rate (Mbps)	1	0.25
Min. receiver sensitivity (dBm)	-70	-85
Receiver noise figure (dB)	<28	<19
Channel spacing (MHz)	1	5
Alternate channel rejection (dB)	30	30
Receiver IIP_3 (dBm)	-21	-20
Received signal power (dBm)	<20	<20
Synthesizer phase noise (@1MHz offset)	-110	-88

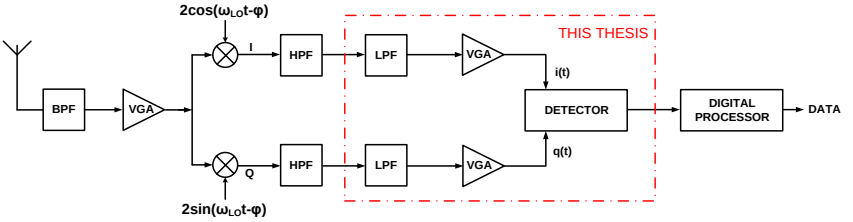

Figure 1.2. Zero-IF receiver architecture

1.4 Objectives

The general objective of this thesis is to develop novel current-mode circuits for the backend of Zero-IF receivers. It is mainly focused on the Bluetooth Low Energy standard, although multi-standard capability is sought, especially ZigBee. More precisely, the objectives of this work are:

- Familiarize with the Cadence custom IC design software and the 0.5µm design kit. All the circuits proposed in this thesis have been designed using this software.

- Study the state-of-the-art of current-mode low-power low-voltage:

  - General techniques, focusing on the ones using Floating Gate and Quasi-Floating Gate MOS transistors.

  - Channel selection filtering techniques.

  - Variable gain amplification techniques.

  - Demodulation strategies based on limiters and zero crossing detection.

- Develop a family of basic cells for current-mode circuits, specifically current mirrors and second generation current conveyors. It is important to develop cells focusing in different key parameters such as low voltage, low power, high performance, high speed, etc, so it is possible to choose the proper cell for a particular application.

- Implement novel architectures for current-mode channel selection filtering based on these basic cells.

- Design novel current-mode variable gain amplification topologies based on these basic cells.

- Develop novel current-mode zero-crossing detectors circuits based on these basic cells.

By fulfilling the afore mentioned objectives, this thesis tries to contribute to current-mode low-voltage low-power Zero-IF receiver design at both cell and system level, a very important topic taking into account the amount of this kind of devices which are fabricated every year.

1.5 Structure of the thesis

This thesis is organized in 7 chapters, being the first one this introductory chapter. In this chapter the motivations behind this work have been explained, making an special effort to reply to the question: Why current mode analog low-power low-voltage design? Afterwards, a short discussion about short distance communication circuits has been done, followed by the description of the main two low power receiver architectures: Zero-IF and Low-IF. Finally, the objectives of the thesis were summarized.

Chapter 2 presents the low-power and low-voltage techniques utilized during the following chapters. It starts presenting the Floating Gate and Quasi Floating gate MOS transistors, which are used in some of the techniques explained during the rest of the chapter: Class AB operation, dynamic cascode biasing, sub threshold operation and companding.

The basic class AB current-mode blocks: current mirrors and second generation current conveyors (CCII) are introduced in Chapter 3. For both blocks, different implementations focusing on different goals (low power operation, high performance, low voltage, etc.) are shown.

Low-power tunable current-mode filter design for channel selection is treated in Chapter 4. The chapter starts presenting the different methods available

for sinh filter design. Finally, the proposed sinh filter implementation validated with measurements is shown.

Chapter 5 is focused on the current-mode constant bandwidth variable gain amplifier design. First, a discussion about the gain-bandwidth product trade-off and how to avoid it is given. Next, the most common current operational amplifiers: the current operational amplifier and the voltage feedback current operational amplifier (VFCOA) are introduced. Finally, the proposed design for a constant bandwidth variable gain VFCOA validated with measurement results is shown.

The current mode detector design for ultra-low power receivers is presented in Chapter 6. The chapter starts introducing the Gaussian frequency shift keying modulation used in the Bluetooth Low Energy standard. Afterwards, some of the most common low power phase detection demodulators are explained, taking special emphasis on the chosen design, the zero-crossing detector. Afterwards the proposed design validated with simulation results is shown.

Finally, Chapter 7 provides a summary of this work conclusions and most significant results, followed by an analysis of the thesis future research lines.

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CHAPTER 2

Low-Power and Low-Voltage design techniques

There are only two ways to increase a device battery lifetime: increasing the battery energy or reducing the device power consumption. The former option impacts in the device weight, size and cost, while the latter usually comes with a performance reduction. Reducing the static or quiescent power consumed by a circuit is a very useful approach when trying to reduce its overall power consumption, because this power is consumed even when no input signal is processed. The quiescent power consumption P_q is given by the following equation:

$$P_q = I_q V_{DD} \tag{2.1}$$

with I_q the quiescent bias current and V_{DD} the supply voltage. From Equation (2.1) it is seen that there are only two ways to reduce P_q: reducing I_q or decreasing V_{DD} (or both). Reducing the bias currents is not trivial, because the transistor bias current influences parameters such as the transistor's transconductance, bandwidth, output resistance, etc. [Joh07]. On the other hand, reducing the supply voltage usually comes with other shortcomings such as dynamic range reduction; therefore, there is no easy way to decrease the power consumption.

This chapter is devoted to present techniques aimed to reducing power consumption. The chapter starts introducing the floating gate MOS (FGMOS)

and the quasi-floating gate MOS (QFGMOS) transistors. Next, low quiescent current and low voltage techniques are presented, some of them using the above mentioned devices.

2.1 The Floating Gate and Quasi Floating Gate MOS Transistors

The FGMOS and QFGMOS transistors have been extensively employed for a wide range of applications in the last decades. In this section both devices are presented and their main applications are highlighted.

2.1.1 The Floating Gate MOS Transistor

The Floating Gate MOS Transistor (FGMOS) has been widely used in industry for memories, neural networks and logic control on analog design since its first report in 1967 [Kah67]. This device is very similar to the well-known MOS transistor. The only difference is that while the latter has a single gate terminal, the former has n input gate terminals capacitively coupled with the internal gate node. As the gate node doesn't have any low resistance path to charge/discharge it, the internal gate node is floating in dc. For this reason, this device is called *floating gate* MOS transistor. Figure 2.1 shows the layout, symbol and equivalent circuit of a two-input FGMOS transistor. As it can be seen from Figure 2.1(a), in order to create the capacitive coupling between the input nodes and the floating gate, a second polysilicon layer is used forming capacitors C_1 and C_2. As the total charge at the floating gate must be conserved, the n inputs form a capacitive divider, and the floating-gate voltage is [Ram01]:

$$V_{FG} = \frac{1}{C_T}\left(\sum_{i=1}^{N} C_i V_i + C_{GS}V_S + C_{GD}V_D + C_{GB}V_B + Q_0\right) \qquad (2.2)$$

where $C_T = \sum_{i=1}^{N} C_i + C_{GS} + C_{GD} + C_{GB}$ and Q_0 is the initial charge trapped in the floating gate. Q_0 can't be controlled during fabrication so it could produce undesired dc offsets or large threshold voltage variations. Traditionally, this trapped charge is removed after fabrication using UV radiation [Gla85, Ker91], tunnel effect [Len69] or hot electron injection [Has97, Has98]. In this thesis Q_0 has been removed during fabrication with the technique proposed in [Rod03]. This method solves the problem during fabrication without extra masks or processing costs. [Rod03] proposed to connect the gate polysilicon layer with the top metal layer using stacked dummy contacts in all the metal layers. As the floating gate remains isolated from any other part of the circuit, given that the

contact stack does not create any new connection after fabrication, its functionality remains constant. However, during deposition of each metal layer and before selective etching, all nodes sharing each metal layer are connected to the floating gate, offering a low-impedance path to discharge the trapped charge. After the top metal etching, the floating gate condition is restored. Therefore, by using this solution the trapped charge is removed during fabrication, becoming negligible.

Besides the trapped charge problem, the FGMOS transistor has other two drawbacks. One is related to the simulation of FGMOS circuits, the other to the performance of FGMOS transistors in new technologies. It is unclear if FGMOS transistors will be usable with modern technologies because the gate leakage current could nullify the floating gate effect.

Simulating FGMOS transistors circuits is not trivial because most simulation software tools present dc convergence errors when a node is floating in dc. To solve this problem, several techniques have been proposed [Ram97, Yin97, Tom99, Rod01]. In this work the method proposed in [Yin97] has been used for its simplicity. Although it has some drawbacks, they can be minimized by oversizing the floating gate capacitors [Yin97].

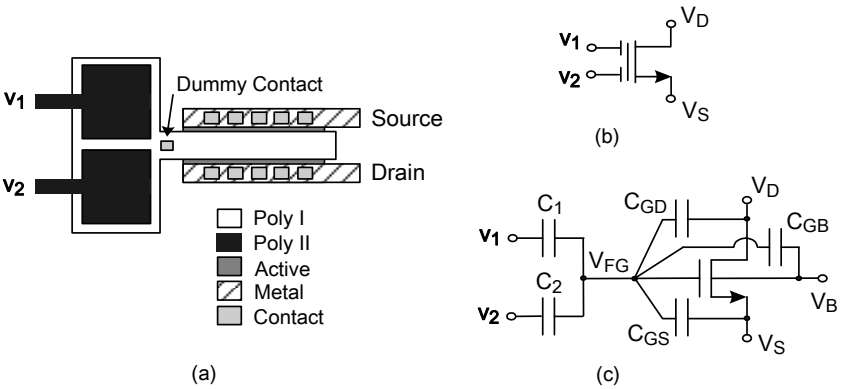

Figure 2.1. Two-input FGMOS transistor (a) Layout (b) Symbol (c) Equivalent circuit

2.1.2 The Quasi-Floating Gate MOS Transistor

The Quasi-Floating gate MOS (QFGMOS) transistor [Ram03] is a device that operates in a very similar way to the FGMOS, but it allows biasing the floating gate at a specific dc voltage while maintaining all the ac properties of the FGMOS. Unlike the FGMOS device, the QFGMOS doesn't have issues with trapped charge, simulation or new technologies. Figures 2.2 (a) and (b) show a 2-input QFGMOS transistor layout and equivalent circuit, respectively. As in the FGMOS device case, the input terminals V_1 and V_2 are capacitively coupled to the quasi-floating gate using a second polysilicon layer in order to create capacitors C_1 and C_2. The dc gate voltage is set to V_B independently of the dc levels of the input voltages by weakly connecting the floating gate to a proper dc voltage using a large-valued resistance. This large resistance R_{large} can be implemented by the leakage resistance of a reverse-biased pn junction of a diode-connected MOS transistor operating in cutoff region [Nae03, Ram04, Seo06] as seen in Figure 2.2. Although there are several ways to implement this large valued resistance [Seo06], each of them has advantages and disadvantages. The employed implementation minimizes the dc offset but requires gate voltage swings to be limited to less than a diode turn-on voltage above or below a supply rail voltage, which may be a limitation in ultra low voltage open-loop configurations.

The ac gate voltage at the floating gate in the s-domain is [Ram04]:

$$V_{QFG} = \frac{sR_{large}}{1+sR_{large}C_T}\left(\sum_{i=1}^{N} C_i V_i + C_{GS}V_S + C_{GD}V_D + C_{GB}V_{bias}\right) \quad (2.3)$$

where $C_T = \sum_{i=1}^{N} C_i + C_{GS} + C_{GD} + C_{GB} + C_{pR}$ and C_{pR} is the parasitic capacitance of the large-valued resistive element seen from the gate.

Note from Equation (2.3) that inputs are high-pass filtered with a cutoff frequency $1/(2\pi R_{large}C_T)$ which can be made very low (below 1 Hz). Therefore, even for very low frequencies, (2.3) becomes a weighted averaging of the ac input voltages determined by capacitance ratios, plus some parasitic terms. Note also that the exact value of R_{large} or its temperature and voltage dependence are not relevant as long as R_{large} remains large enough to not influencing the circuit's operation at the lowest frequency required. The exact value of C_T is also unimportant.

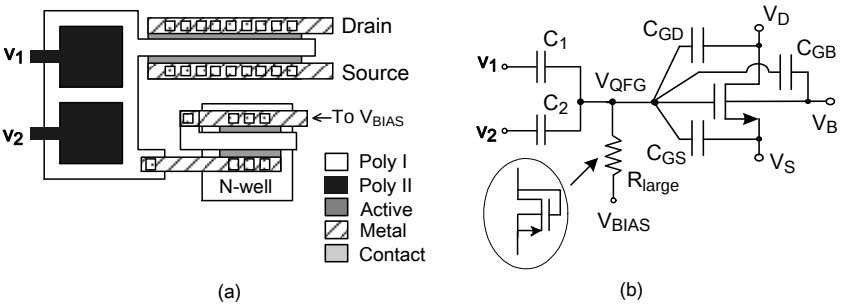

Figure 2.2. Two-input QFGMOS transistor (a) Layout (b) Equivalent circuit

2.2 Low quiescent current techniques

2.2.1 Class AB operation

In class A circuits, the signal current swing is limited by the bias current, leading to a tradeoff between dynamic performance and quiescent power consumption. When low power operation is needed, class AB operation can be implemented in order to achieve a similar performance with less power consumption [Kaw96]. There are different ways to implement class AB operation but they usually come with the cost of increasing the transistor count and circuit complexity [Wan90, Pal00]. In this subsection a method to achieve class AB operation using the Quasi-Floating Gate MOS Transistor is explained. The compact implementation of floating dc level shifts achievable by these devices allows obtaining class AB operation in a simple way [Ram06]. Figure 2.3 (a) shows a typical class AB output stage. The quiescent current is set by the bias voltage at node A and the dc level shift V_{bat}. Under dynamic conditions, signal variations at node A are transferred to node B allowing output currents not limited by the quiescent current. The dc level shift has been implemented in several ways, for instance using diode-connected transistors or resistors biased by dc currents. However, these solutions require extra quiescent power consumption and may increase supply voltage requirements. Moreover, the quiescent current is often not accurately set and dependent on process and temperature variations, and the parasitic elements added by this extra circuitry may limit bandwidth.

Figure 2.3(b) shows an efficient implementation of this dc level shift that avoids these drawbacks, making M_2 a QFGMOS transistor [Ram04, Ram06]. In quiescent operation C_{bat} has no effect and there is not current flowing through R_{large}, so that the quiescent current of the output branch is accurately set to the

bias current I_B, regardless of thermal and process variations as it is set by a current mirror. Under dynamic conditions, voltage at node A is transferred to node B after being attenuated by a factor $C_{bat}/(C_{bat}+C_B)$ and high-pass filtered with cutoff frequency $1/[2\pi R_{large}(C_{bat}+C_B)]$, where C_B is the capacitance at node B. Due to the large resistance employed (in the order of GigaOhms) this cutoff frequency is typically below 1 Hz, so in practice only the dc component of voltage at node A is not transferred to node B. Notice that the implementation of the floating battery does not increase static power or supply voltage requirements. The increase in silicon area is modest as R_{large} is made by a minimum-size MOS transistor (see Section 2.1.2 for more information) and C_{bat} can be small (with the minimum value imposed by the parasitic capacitance C_B).

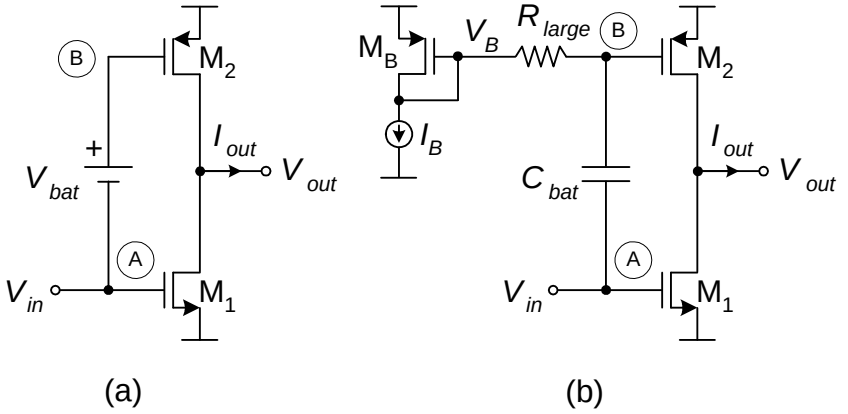

Figure 2.3. Class AB output stage (a) Conventional (b) QFG implementation

2.3 Low voltage techniques

In this section, some techniques aimed to reducing the required supply voltage are briefly described.

2.3.1 Dynamic Cascode biasing

Figure 2.4(a) shows a typical cascode topology. A voltage variation at node A generates a varying current through transistors M_{N1} and M_{CN1}. As node B is fixed to a constant dc voltage, this current makes voltage at node C to swing as well, modifying the V_{DS} of M_{N1} and therefore degrading linearity. Moreover, as the current increases, node C voltage decreases, and transistor M_{N1} can enter into triode region, limiting the dynamic range of the circuit. Figure 2.4 (b) shows a way

to solve this problem [Ram08]. If a floating battery is connected between nodes A and B, node B will track the voltage variations of node A, and therefore, voltage at node C will remain almost constant, increasing linearity and dynamic range.

As in the former section, a compact implementation of the floating battery can be achieved using QFG techniques. Figure 2.4(c) presents the QFGMOS implementation of Figure 2.4(b). M_{CN1} becomes a QFGMOS transistor. In dc, voltage at node B is set to V_{cn} because there is not current flowing through R_{large}. Under dynamic conditions, the voltage swing at node A is transferred to node B through the high pass filter formed by C_{bat} and R_{large} (as explained before, the cutoff frequency is lower than 1 Hz) with a pass band gain of $C_{bat}/(C_{bat}+C_B)$,where C_B is the parasitic capacitance at node B. As the pass band gain should be close to one in order to have the same voltage swing at both nodes, $C_{bat} >> C_B$. This fact limits C_{bat}'s minimum value. In this way, the swing experienced by both gates is equal, and therefore, because of the equal current that crosses both transistors, voltage at node C remains approximately constant. Preserving the V_{DS} of M_{N1} almost constant leads to improved linearity, and allows M_{N1} to remain in saturation region for a wider input range, increasing dynamic range and allowing a lower voltage operation.

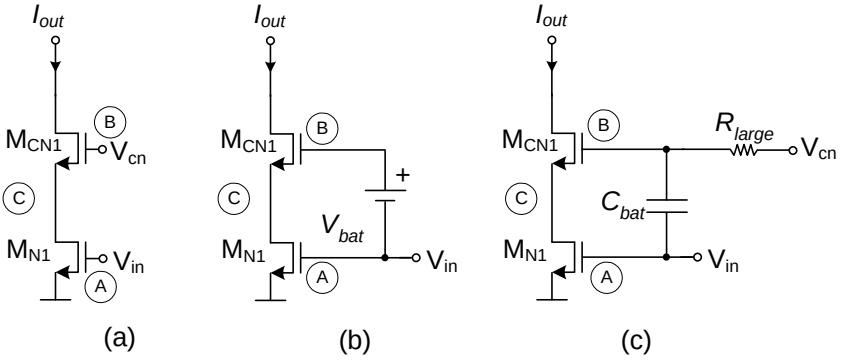

Figure 2.4. Wide swing cascode (a) Conventional (b) Dynamic Cascode biasing (c) QFGMOS dynamic cascode biasing implementation

2.3.2 Sub threshold operation: weak inversion

More than 40 years have passed since the first efforts to model the weak inversion operation of a CMOS transistor [Bar72, Tro73, Tro75, Mas74, Bar76] and the first experimental circuits [Vit76, Vit77]. At that time the scientific

community didn't understand the importance of this topic. In the old times minimum supply voltage requirements were not a problem. Circuit designers were used to design using MOS transistors operating in strong inversion and cascoding stages. Nowadays, due to the fast downscaling of supply voltages in CMOS processes but not so fast downscaling of threshold voltages (see Table 1.1), these design procedures aren't feasible anymore. Sub-threshold operation enables biasing transistors with very low V_{GS} voltages, allowing lower voltage operation.

At the present time, both hand calculation and circuit simulation of weak inversion transistor are possible. In the circuit simulation domain, the EKV compact MOST model [Enz96b] allows computer accurate calculations for circuits working in weak, moderate and strong inversion. As comparing weak and strong inversion operation using the EKV model would be very complex, it is more convenient to perform the comparison using the hand calculation formulas for two of the most important parameters in transistor design, the drain current and the transconductance gain. Both parameters for saturation operation are shown in Equations (2.4)-(2.5) and (2.6)-(2.7) for weak inversion and strong inversion operation, respectively [Vit77, Enz96a, Vit91, Enz95, Vit03, Wan06].

$$I_{D,wi} = 2n\beta U_T^2 e^{\left(-V_{T0}/nU_T\right)} e^{\left(V_{GS}/nU_T\right)} \tag{2.4}$$

$$g_{m,wi} = \frac{I_D}{nU_T} \tag{2.5}$$

$$I_{D,si} = \frac{\beta}{2n}(V_{GS} - V_{T0})^2 \tag{2.6}$$

$$g_{m,si} = \sqrt{2\beta I_D / n} \tag{2.7}$$

and

$$\beta = (\mu_n C'_{ox} W)/L \tag{2.8}$$

where n is the slope factor, μ_n is the mobility of electrons near the surface, C'_{ox} is the gate capacitance, W and L are the transistor dimensions, V_{T0} is the threshold voltage and $U_T = kT/q$ is the thermal voltage.

The previous equations provide some insight about weak inversion operation. Regarding the drain current, the weak inversion model relationship between V_{GS} and I_D is exponential, while in the strong inversion model it is

quadratic. With respect to the transconductance, the weak inversion model depends linearly on I_D and is independent of β while in the strong inversion model the relationship is root-squared and depends on β.

The exponential relationship between $I_{D,wi}$ and V_{GS} is very important as it makes possible to design translinear loops [See91] and exponential/log domain circuits [Fre93], achieves maximum I_{on}/I_{off} for a given voltage swing and reduces the intermodulation in RF front ends. The exponential relationship also makes g_m/I_D larger for weak inversion, achieving maximum intrinsic voltage gain, minimum input noise density, maximum bandwidth, minimum input offset voltage, maximum output noise current and maximum current mismatch dominated by V_T mismatch: $\Delta I_D/I_D = \Delta V_{T0}/nU_T$ for a given kT/C and I_D. On top of that, weak inversion operation permits minimum gate voltages, as $V_{GS,wi} << V_{T0}$ and the saturation drain voltage is as low as $5U_T$.

The main disadvantage of the weak inversion operation is that as the bias currents are smaller, the speed is also reduced being the transistor cutoff frequency $f_c \approx \mu_n U_T/2\pi L^2$. Even though, this bandwidth is enough for some applications (such as the design of Bluetooth Low Energy Zero-IF receivers) and allows very low voltage operation, becoming a very beneficial technique to take into account.

2.3.3 Companding

Companding is a fancy word standing for **comp**ressing – exp**anding**. Although the concept was formally introduced in 1990 [Tsi90], companding was extensively used in transmission and storage [Mat34, Bel82] since A. B. Clark of AT&T patented the concept in 1928 [Cla28] and the first report related with its use in analog signal processing circuits dates from 1979 [Ada79].

This technique is based on compressing the input signal dynamic range before processing it, afterwards, the resulting signal dynamic range is expanded again to provide the output signal. The compression block is a non-linear block; Small input signals are amplified while large input signals are attenuated. The expansion block, also non-linear, expand the processed signal in a way that the overall system is kept linear, even though internally it is non-linear. This approach contributes to reduce the overall distortion as the larger inputs are attenuated before processing. On top of that, the signal to noise ratio is improved because the small signals are amplified. Therefore, the dynamic range is enhanced.

If the companding technique is combined with the current-mode approach, the input current is transformed into a compressed voltage. Having compressed internal voltages makes the voltage swing across the processing block almost independent of the supply voltage, being possible to reduce the supply voltage the minimum required for the circuit's proper operation without a loss in dynamic range.

Besides of companding main advantages, which are enhanced dynamic range, wide frequency tuning range, low voltage operation and high speed [Lop99], due to its internal non-linear behavior, this approach suffers from noise modulation, high mismatch sensibility, intermodulation by interference signals and increased bandwidth requirements [Lop99].

Due to its mathematical complexity, explaining the insights of externally linear internally non-linear circuits in detail [Fre96, Tsi97] would take a chapter by itself. In order to exemplify the companding operation a simple current-mode integrator is shown in Figure 2.5 where the expanding block f() is a non-linear function dependent on the integrator capacitor voltage v_{cap}

$$f(v_{cap}) = i_{out} \tag{2.9}$$

and the compression block is a non-linear current amplifier with gain dependent on the voltage across the capacitor v_{cap}, so the integrator capacitor current is

$$i_{cap} = C\frac{dv_{cap}}{dt} = i_{in}g(v_{in}) \tag{2.10}$$

In order to preserve a global linear transfer function, the relationship between the input i_{in} and the output i_{out} is

$$i_{out}(t) = \frac{1}{\tau}\int_{-\infty}^{t} i_{in}(\tau)d\tau \tag{2.11}$$

where τ^{-1} is the integrator unity gain frequency. As explained in [TSI95], Equation (2.11) is satisfied when the compression and expansion blocks accomplish:

$$g(v_{cap}) = \frac{C}{\tau}\left[\frac{df}{dv_{cap}}\right]^{-1} \tag{2.12}$$

Even though any compression / expansion rule that follows Equation (2.12) is valid, in practice, three approaches rules are commonly used: log-domain, sinh-domain and root-domain.

The log-domain approach [Fre93, Tsi95, Dra99, Enz99] is the most used companding method in analog signal processing by far, being this caused both by mathematical and technological reasons. In the mathematical field, the derivate of an exponential function is also an exponential function, and the product or quotient of exponential functions is equal to their arguments sum or difference. On the technological ground, the exponential function is easily implemented using BJTs or MOST in weak inversion. These arguments make possible to implement log-domain circuits easily and in a compact way. The main drawback in log-domain circuits is that, due to the positive nature of the logarithmic function, only unipolar inputs can be processed. In order to solve this problem several class AB implementations have been proposed [Fre99, Fox00] but they increase the circuit complexity and the transistor and capacitor area by two.

The root-domain approach was first proposed in 1996 [Mul96, Pay96] and is typically implemented using CMOS translinear loops [See91]. Due to the quasi-quadratic large-signal characteristics of MOS transistors in strong inversion-saturation region, it is possible to use translinear loops operating in this region [Mul96, Mul98, Esk00], where all the drawbacks of weak inversion operation are avoided (see section 2.3.2). Even though synthesis methods have been proposed [Lop01, Psy02], root-domain circuits have the same drawback than log-domain circuits: unipolar input signal operation, and, on top of that, they usually have more complex implementations.

Hyperbolic-sine-domain circuits [Tsi95, Fre96, Kat08] are (as well as log-domain systems) a kind of exponential-domain circuits. Instead of using an exponential expansion block, a sinh expansion function is employed. This function has the advantage of being an odd function from a mathematical point of view, allowing both positive and negative input/output signals, therefore functioning by default in class AB operation. This approach allows class AB operation with half the capacitor area than in the pseudo-differential log-domain approach. In spite of its' promising features and the existence of synthesis methods [Tsi95, Fre96], only one sinh filter validated with measurement results has been presented so far [Kur13].

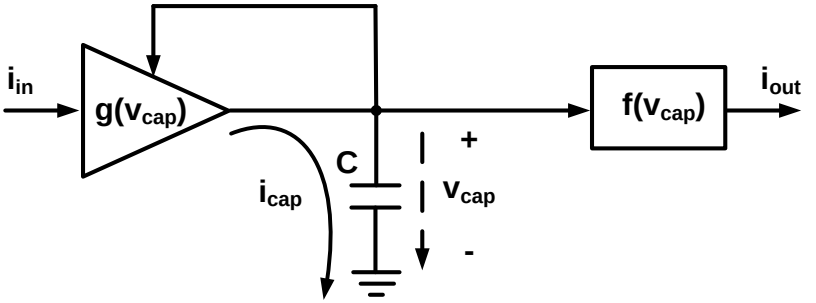

Figure 2.5. Current mode companding integrator

2.4 Conclusions

In this chapter the reasons behind the low power trend have been explained. Two different approaches for reducing circuits' overall power consumption have been analyzed: decreasing the quiescent currents and decreasing the supply voltage. Different techniques for each alternative have been presented, and the devices involved in some of these techniques, named floating gate and quasi floating gate transistors have been introduced

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CHAPTER 3

Basic class AB current-mode blocks

In this chapter basic building blocks in the current-mode approach (the current mirror and the current conveyor) are presented. Current mirrors have been extensively used in circuit design to generate the bias currents, but they are capable of much more tasks, as it is described in this chapter. Current conveyors were presented 40 years ago with promising features. Since then, a lot of research has been done in the field, becoming one of the most versatile devices together with the operational amplifier.

Both devices are able to achieve class AB operation in a simple and efficient manner using the technique explained in section 2.2.1. These implementations, together with the state of the art and the circuit applications, are explained in this chapter.

3.1 Current Mirrors

Current mirrors have been used for decades in analog circuit design, becoming one of the most utilized blocks. Although they are mainly used to generate and replicate currents, they are also employed as a basic building block in current-mode circuits [Tou90] such as current conveyors, voltage-current converters, current operational amplifiers or current-mode filters. Hence the availability of current mirrors with adequate performance in terms of linearity,

power consumption, supply voltage requirements and input and output resistance is critical nowadays in analog and mixed-signal design.

During the nineties, a few class AB current mirrors were proposed [Wan90, Ram94, Kaw96]. However, all of them increase the circuit complexity, number of transistors and minimum supply voltage requirements with respect to class A current mirrors. The circuit in [Kaw96] has been extensively used because it allows to accurately set the quiescent currents (unlike [Wan90]) and is simpler than [Ram94]. At the same time, [Pal95, Zek97] proposed methods to improve the performance of the class AB current output stages in terms of linearity and output resistance. More recently, with the aim of achieving low voltage operation, different approaches have been proposed. In [Pal00] a class AB current mirror which employs switched capacitor (SC) techniques for dynamic biasing was presented. The main drawbacks of this topology are the need of additional circuitry to create two nonoverlapping clock signals and the inherent switching effects associated to SC circuits, namely, clock feedthrough and charge injection. In [Lop08] it was proposed a compact class AB current mirror based on Quasi-Floating Gate MOS transistors (QFGMOST) [Ram04, Ram06a] which features both low supply voltage requirements and low circuit complexity. Later on, there were proposed improved versions of [Lop08] maximizing the linearity and output resistance using auxiliary amplifiers [Esp12a] and improving the linearity while maintaining the low supply voltage using dynamic cascode biasing [Esp12b, Esp12c, Esp14].

This section starts presenting the class A and class AB mirrors are presented. Afterwards, two different implementations of class AB current mirrors with different design approaches; one of them looking forward low voltage low power operation and the other focusing on the high performance are presented and validated with theoretical analysis and measurement results. Finally, some current-mirror applications are shown.

3.1.1 Class A and class AB current mirrors

In this section, the conventional class A cascode current mirror is briefly outlined. Then the basic class AB cascode current mirror with conventional cascode biasing formerly reported [Lop08] is revised.

Figure 3.1(a) shows a simple class A wide-swing cascode current mirror. The operation of this circuit is well known. Transistors M_{N1}-M_{N2} copy the input

signal, and are biased by M_{P1}-M_{P3}. Cascode transistors M_{CN1}-M_{CN2} and M_{CP1}-M_{CP3} are used to increase linearity, current copy accuracy and output resistance.

Because of the equal gate-source voltage of M_{N1} and M_{N2}, and their very similar drain-source voltage due to the cascode transistors M_{CN1}-M_{CN2}, the current through M_{N1} (I_{in}+I_B) is accurately copied to M_{N2}. The cascode transistors M_{CN2}-M_{CP2} also increase the output resistance. The main drawback of this configuration is that because of its class A operation, the amplitude of I_{in} is limited by I_B, and therefore, in order to handle high current swings, the bias current should be high, increasing the static power consumption.

Figure 3.1(b) shows the class AB current mirror presented in [Lop08]. This current mirror is the result of applying the technique shown in section 2.2.1 [Ram06b] to the class A current mirror. It allows obtaining class AB operation in a simple way. In static conditions, the circuit is equivalent to that of Figure 3.1(a) due to the dc open circuit equivalence of the C_{bat} capacitor, leading to the same operating point in both circuits. On the other hand, under dynamic conditions, the configuration achieves class AB operation transforming transistors M_{P1} and M_{P2} (now QFGMOST) into dynamic current sources. If I_{in} becomes negative, the current through M_{N1} decreases, decreasing the gate voltage of M_{N1} as well. This voltage decrease is transferred to the gate of M_{P1}-M_{P2} through the high pass filter formed by the capacitor C_{bat} and resistor R_{large}, increasing the current provided by these transistors, and therefore achieving class AB operation. In order to achieve a very low cutoff frequency for the high pass filter with relatively small C_{bat} values, R_{large} should be very large. As stated before, this resistor can be implemented easily using the leakage resistance of a transistor in the cutoff region. Although this circuit achieves higher dynamic range and linearity than the class A current mirror for the same supply voltage and static power consumption, the price to pay is the extra area occupied by the capacitor C_{bat}.

It is interesting to note that the input and output resistances of both circuits are equal and given by:

$$R_{in} = \frac{1}{g_{mN1}} \tag{3.1}$$

$$R_{out} = g_{mCN2} r_{dsN2} r_{dsCN2} || g_{mCP2} r_{dsP2} r_{dsCP2} \tag{3.2}$$

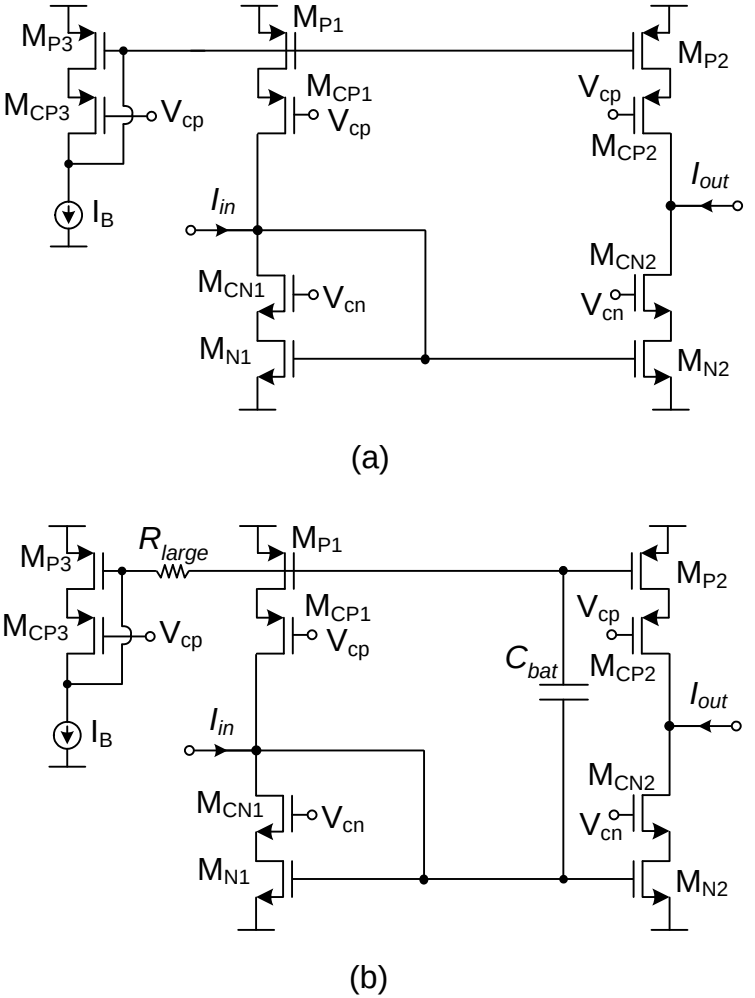

Figure 3.1. Basic cascode current mirror (a) Class A (b) Class AB

3.1.2 Class AB current mirror with dynamic cascode biasing

One of the drawbacks of the topologies of Figure 3.1 is that the bias voltages of the cascode transistors are fixed to a constant dc value which limits linearity and dynamic range. To overcome this drawback, the technique shown in section 2.3.1 [Ram08] can be applied to the previous class AB current mirror, obtaining the circuit shown in Figure 3.2(a). Another possible arrangement for the floating capacitors that achieve dynamic biasing is shown in Figure 3.2(b).

Under static conditions, all the circuits of Figures 3.1 and 3.2 are equivalent. Thus, in all the class AB QFGMOST current mirrors, quiescent currents are accurately controlled and are the same as in the class A topology. Under dynamic conditions, when an ac current signal is applied to the input in the proposed topologies of Figure. 3.2, the voltage swing generated at the gates of transistors M_{N1}-M_{N2} is transferred through the three floating capacitors to the gates of M_{CN1}-M_{CN2}, M_{CP1}-M_{CP2} and M_{P1}-M_{P2}, which makes the voltage drop between the drain and source of transistors M_{N1}-M_{N2} and M_{P1}-M_{P2} to remain almost constant, increasing linearity and dynamic range. In the basic class AB current mirror, this variation is just transferred to the gate of M_{P1}-M_{P2}.

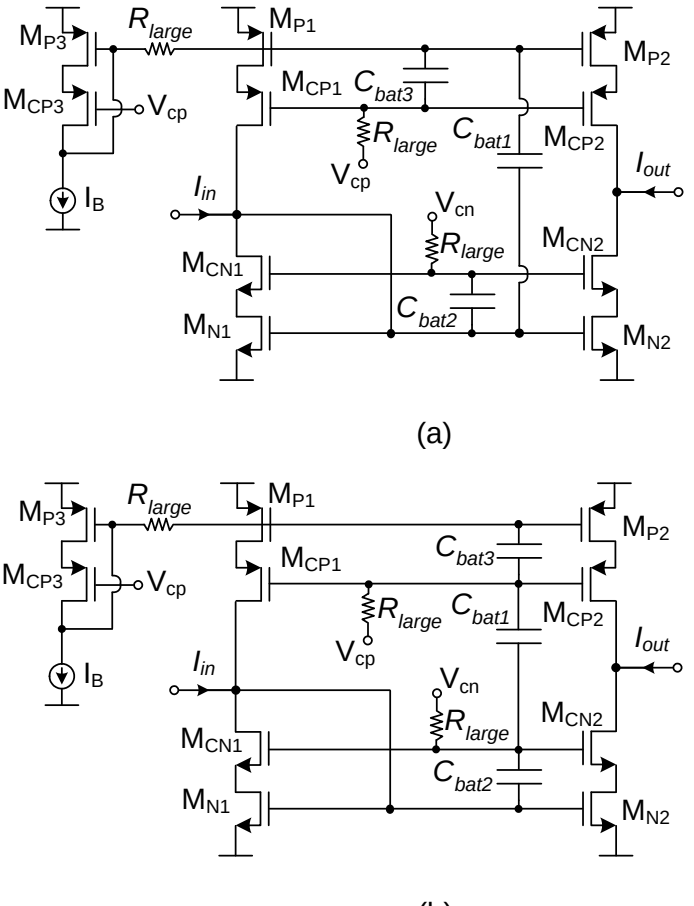

Figure 3.2. Dynamic cascode class AB current mirrors (a) Topology 1 (b) Topology 2

Although both circuits on Figure 3.2 are based on the same principle, the way they behave is slightly different. In Figure 3.2(b) circuit, the capacitive divider formed by the series connection of C_{bat1}, C_{bat2} and C_{bat3} leads to higher attenuation in the voltage transfer from M_{N1}-M_{N2} transistors' gates and the rest of the quasi-floating nodes than in Figure 3.2(a), leading to a slightly worse linearity and dynamic range. On the other hand, the capacitance at the common gate nodes of M_{N1}-M_{N2} and M_{P1}-M_{P2} is smaller in Figure 3.2(b) than in Figure 3.2(a), achieving a slightly higher bandwidth.

In summary, the proposed topologies of Figure 3.2 improve performance versus the previous class AB cascode current mirror in terms of dynamic range and linearity, preserving supply voltage requirements, static power consumption and accuracy in quiescent currents. The price paid is the extra area and parasitic capacitance associated to the two additional floating capacitors included. Concerning input and output resistances, they are the same as in the previous circuits.

3.1.2.1 Second order effects and noise

Concerning geometric and parametric mismatch, the proposed topologies of Figure 3.2, as well as the basic classA/classAB current mirrors of Figure 3.1, require accurate matching between transistors M_{N1}-M_{N2} and M_{P1}-M_{P3}. If these transistors are not matched, there is degradation in current copy accuracy, linearity and noise. In order to minimize these effects, proper layout techniques should be applied. Note that the circuits of Figure 3.2 do not require extra matching requirements, since there is no need to match the floating capacitors C_{bat1} to C_{bat3} or resistances R_{large}. Mismatch in these devices only slightly modifies the minimum frequency component that is transferred by the ac coupling achieved by the R_{large}-C_{bat} high-pass network.

Temperature variations do not affect quiescent currents since they are set by current mirrors, so if the bias current source I_B is independent of these variations, quiescent currents are independent too. Regarding supply variations, v_{DD} and v_{SS} are considered as the upper and lower voltage supply variations respectively. In order to analyze the influence of these glitches, the output current generated by these variations must be calculated.

As both supply variations are independent, they can be considered separately. First, the circuit of Figure. 3.1(a) is considered. Analyzing the small signal equivalent circuit it can be seen that AC gate voltages of M_{P2} and M_{N2} are

connected to v_{DD} and v_{SS}, respectively. Therefore, the output current generated by supply glitches is zero regardless of transistor matching. On the other hand, class AB current mirrors' supply variations insensitivity depends on perfect matching. Analyzing the small signal equivalent circuits considering the capacitors as short-circuits, it is easy to arrive to the following relationship.

$$I_{out,AB}(v_{DD}, v_{SS}) = \left(\frac{g_{mP2}g_{mN1} - g_{mN2}g_{mP1}}{g_{mP1} + g_{mN1}}\right)(v_{DD} - v_{SS}) \tag{3.3}$$

where g_{mi} is the transconductance of transistor M_i.

As it can be seen from Equation (3.3), the circuits of Figure 3.1(b) and Figure 3.2 are insensitive to supply variations when perfect matching is achieved ($g_{mN1} = g_{mN2}$ and $g_{mP1} = g_{mP2}$). This can be explained intuitively taking into account that the current generated by v_{DD}/v_{SS} in the input branch is mirrored to the output branch by the N/P current mirrors, eliminating the output current.

Concerning the bulk effect, it has no relevance in the proposed circuits because it only affects the cascode transistors M_{CN1}-M_{CN2} and M_{CP1}-M_{CP3}, and its influence is negligible. The rest of transistors have the source tied to the corresponding supply rail, thus not suffering from this effect.

Regarding noise, the main sources in CMOS analog circuits are thermal and Flicker noise. Considering thermal noise, the approximate expression for Figure 3.1(a) circuit's equivalent input noise current density is

$$\overline{I^2_{TN,inA}} = \frac{8k_bTg^2_{mN1}}{3g^2_{mN2}}\left[\frac{1}{g_{mP3}}\left(\frac{g_{mN2}g_{mP1}}{g_{mN1}} - g_{mP2}\right)^2 + g_{mP2} + g_{mN2} + \frac{g^2_{mN2}}{g_{mN1}} + \frac{g_{mP1}g^2_{mN2}}{g^2_{mN1}}\right] \tag{3.4}$$

The corresponding expression for all the class AB current mirrors (Figures 3.1(b) and 3.2) is

$$\overline{I^2_{TN,inAB}} = \frac{8k_bT}{3}(g_{mN1} + g_{mP1})\left(1 + \frac{g_{mN1}+g_{mP1}}{g_{mN2}+g_{mP2}}\right) \tag{3.5}$$

where k_B is the Boltzmann's constant and T the absolute temperature.

In equation (3.4), the first term in the sum between brackets is the noise from the current bias circuit. If perfect matching between transistors is achieved, this term disappears. In the class AB current mirrors there isn't noise from the

current bias circuit because it is low pass filtered with extremely low cutoff frequency. Thus, the proposed current mirrors not only preserve noise performance, but they even improve it as compared to their class A counterpart in presence of mismatch, since they filter the noise coming from the biasing circuits. In case of perfect matching both circuits have the same equivalent input thermal noise where all transistors have the same influence. A possible design procedure in order to reduce the thermal noise current is to reduce transistors transconductance.

Regarding flicker noise, the equivalent input noise density for the class A current mirror is

$$\overline{I^2_{FN,inA}(f)} = \frac{g^2_{mN1}}{C_{ox} f g^2_{mN2}} \left[\frac{K_{P3}}{W_{P3} L_{P3}} \left(\frac{g_{mN2} g_{mP1}}{g_{mN1}} - g_{mP2} \right)^2 + \frac{g^2_{mP1} g^2_{mN2} K_{P1}}{g^2_{mN1} W_{P1} L_{P1}} + \frac{g^2_{mN2} K_{N1}}{W_{N1} L_{N1}} + \frac{g^2_{mN2} K_{N2}}{W_{N2} L_{N2}} + \frac{g^2_{mP2} K_{P2}}{W_{P2} L_{P2}} \right] \quad (3.6)$$

For the class AB current mirrors it is:

$$\overline{I^2_{FN,inAB}(f)} = \frac{1}{C_{ox} f} \left[\left(\frac{g_{mN1} + g_{mP1}}{g_{mN2} + g_{mP2}} \right)^2 \left(\frac{g^2_{mP2} K_{P2}}{W_{P2} L_{P2}} + \frac{g^2_{mN2} K_{N2}}{W_{N2} L_{N2}} \right) + \frac{g^2_{mN1} K_{N1}}{W_{N1} L_{N1}} + \frac{g^2_{mP1} K_{P1}}{W_{P1} L_{P1}} \right] \quad (3.7)$$

where constant K_i is dependent on transistor M_i and can vary widely for different devices in the same process. C_{ox} is the capacitance per unit area and W_i and L_i are transistor M_i width and length respectively.

In case of perfect matching, both circuits have the same equivalent input flicker noise, and all the transistors have the same contribution. Considering the results from equations (3.4) to (3.7), it is clear that class AB operation and regulated cascode don't degrade the noise performance. In case of noise constraints, the best way to reduce noise is increasing the length of M_{N1}, M_{N2}, M_{P1} and M_{P2}. This will reduce the noise and increase the current copy accuracy, but on the other hand, the bandwidth will be reduced.

3.1.2.2 Simulation and Measurement results

Both topologies of Figure 3.2 have been fabricated in a 0.5μm CMOS technology with nominal NMOS and PMOS threshold voltages of 0.67 V and –0.96 V, respectively. Capacitors C_{bat1} to C_{bat3} were implemented as poly-poly capacitors with a nominal value of 1 pF. Resistors R_{large} were implemented with

minimum size PMOS transistors (1.5μm/0.6μm) with v_{gd} and v_{sb} equal to 0. The rest of the transistors' dimensions W/L (in μm/μm) were: 100/0.6 (M_{P1}, M_{P2}, M_{P3}, M_{CN1}, M_{CN2}), 200/0.6 (M_{CP1}, M_{CP2}, M_{CP3}), and 60/1 (M_{N1}, M_{N2}). I_B (10μA) was implemented with an NMOS wide swing cascode current source. Both circuits were measured for supply voltages of 1.5 V and 1.2 V, achieving a static power consumption of 45 μW and 36 μW, respectively.

Figure 3.3 shows the measured THD for both topologies of Figure 3.2 and the simulated THD for the circuit of Figure 3.1(b) for a supply voltage of 1.5 V. As it can be seen from the figure, both topologies perform better than the previous one in all the input range. The THD improvement is better than 32 dB for Figure 3.2(a) and 23 dB for Figure 3.2(b). Figure 3.4 shows the measured THD for both topologies of Figure 3.2 and the simulated THD for the circuit of Figure 3.1(b) but now for a supply voltage of 1.2 V. As it can be noticed, also in this case both proposed topologies outperform the previous one in all the input range. Note that as expected, Figure 3.2(a) circuit is slightly more linear than Figure 3.2(b) topology, achieving for amplitudes up to 100 times the bias current THD values of less than -35 and -30 dB for 1.5V and 1.2V supply voltage, respectively.

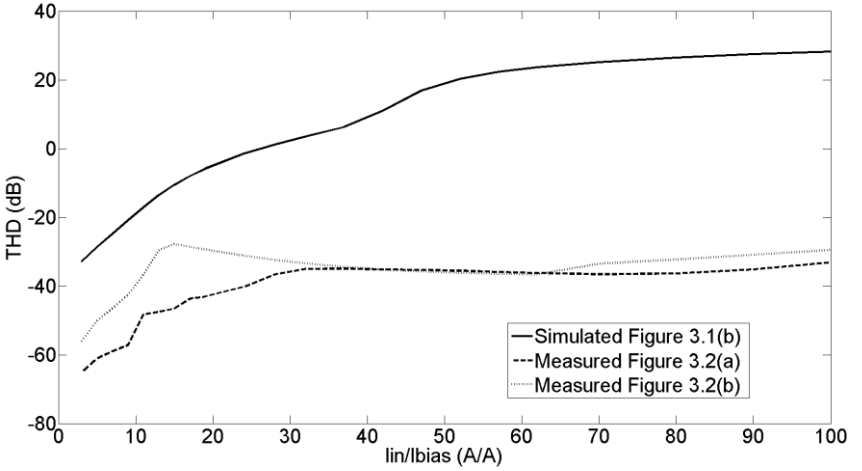

Figure 3.3. THD versus normalized input amplitude for V_{DD} = 1.5V

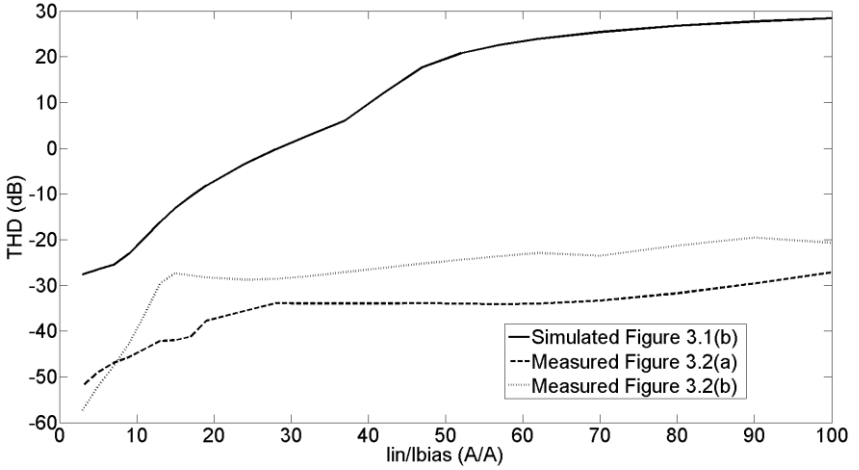

Figure 3.4. THD versus normalized input amplitude for V_{DD}=1.2V

Table 3.1 shows the simulation results of other important parameters. As expected, the proposed topologies have the same input and output resistance and equivalent input noise, but on the other hand, less bandwidth than the basic class AB current mirror due to the extra capacitance associated to the internal nodes.

Table 3.1. Figures 3.1(b) and 3.2 simulation results

	Figure 3.1(b)	Figure 3.2(a)	Figure 3.2(b)
R_{in}@V_{DD} = 1.5V (kΩ)	4.88	4.88	4.88
R_{in}@V_{DD} = 1.2V (kΩ)	4.892	4.892	4.892
R_{out}@V_{DD} = 1.5V (MΩ)	8.486	8.486	8.486
R_{out}@V_{DD} = 1.2V (MΩ)	7.176	7.176	7.176
BW@V_{DD} = 1.5V (MHz)	104.4	75.2	76.3
BW@V_{DD} = 1.2V (MHz)	101.4	72.42	75.2
Eq. Input Noise@V_{DD}=1.5V (pA/√Hz)	3.19	3.19	3.19
Eq. Input Noise@V_{DD}=1.2V (pA/√Hz)	3.19	3.19	3.19

Figure 3.5 shows the output current simulation for an input triangular signal of 1 mA amplitude for the three class AB current mirrors. As it can be

seen, both proposed topologies have a wider input range than the previous topology due to the effect of the dynamic cascode biasing. It can also be noticed that Figure 3.2(a) topology features a wider input range than Figure 3.2(b) circuit. As mentioned before, this is due to the increased attenuation of the capacitive divider that sets the voltage at the gates of the cascode transistors.

Finally, Figure 3.6 shows the microphotograph of the proposed topologies. The silicon area is 127x139 μm for the circuit of Figure 3.1(b) and 180x139 μm for each proposed topology of Figure 3.2.

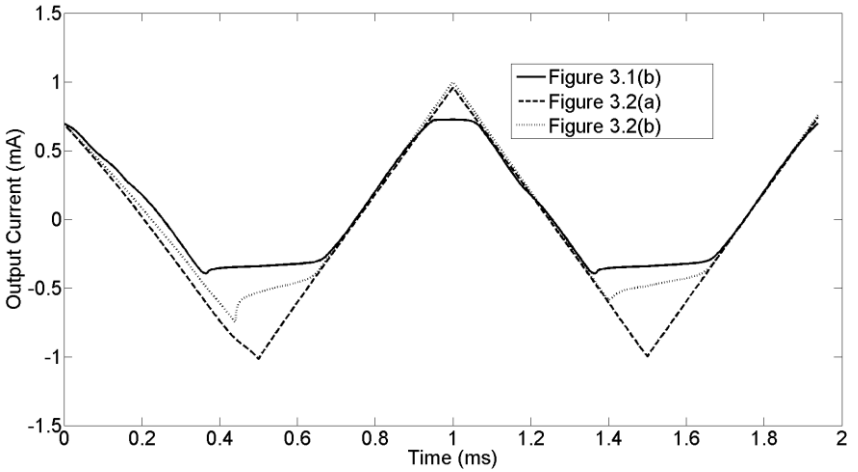

Figure 3.5. Simulated transient response of Figures' 3.1(b) and 3.2 circuits

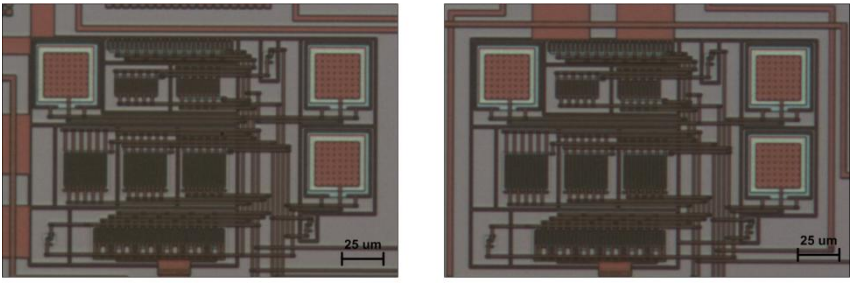

Figure 3.6. Microphotograph of (a) Figure 3.2(a) (b) Figure 3.2(b)

3.1.3 High performance class AB current mirrors

When current mirrors are used to build more complex blocks, often a higher performance could be needed. Desirable characteristics of current mirrors are low input impedance, high output impedance, high linearity and high current handling capability together with low power consumption.

Figure 3.7 shows two techniques that can be applied to achieve some of these characteristics. Figure 3.7(a) employs an error amplifier in order to decrease the input resistance by a factor A, and at the same time, increases the overall linearity stabilizing the input node voltage. Figure 3.7(b) makes use of a regulated cascode topology that increases the output resistance by a factor (1+A). On top of that, the amplifier enhances the current mirror dynamic range in a similar way as in the circuits of Figure 3.2. Due to the high gain of amplifier A, the drain of M_2 is accurately set to V_{bias}, increasing the overall linearity, while allowing the gate voltage of M_{2C} to dynamically change with I_{out}. It is worth saying that if the structure of Figure 3.7(b) is replicated into the input branch, both transistors forming the current mirror are equally biased, and therefore, the linearity and current accuracy improve even more.

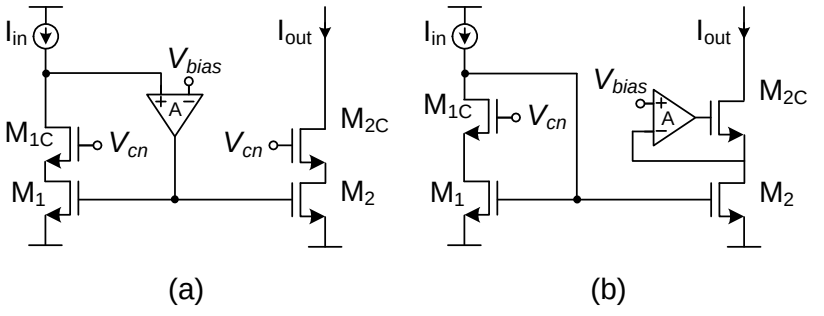

Figure 3.7. Techniques to improve current mirror performance
(a) input branch (b) output branch

The technique from Figure 3.7(b) admits a wide range of design possibilities as it is shown below. Figure 3.8 shows some different ways to apply Figure 3.7 techniques to the class AB current mirror. All topologies have the input error amplifier and they have regulated cascodes both in the P and N cascodes so the output resistance is enhanced in both sides. Figure 3.8(a) and (b) topologies are the direct implementation of Figure 3.7. One of the drawbacks of these topologies is that two bias voltages V_{biasp} and V_{biasn} are needed. In order to

resolve this issue, topologies 3.8(b), (c) and (d) show how to automatically bias the amplifiers.

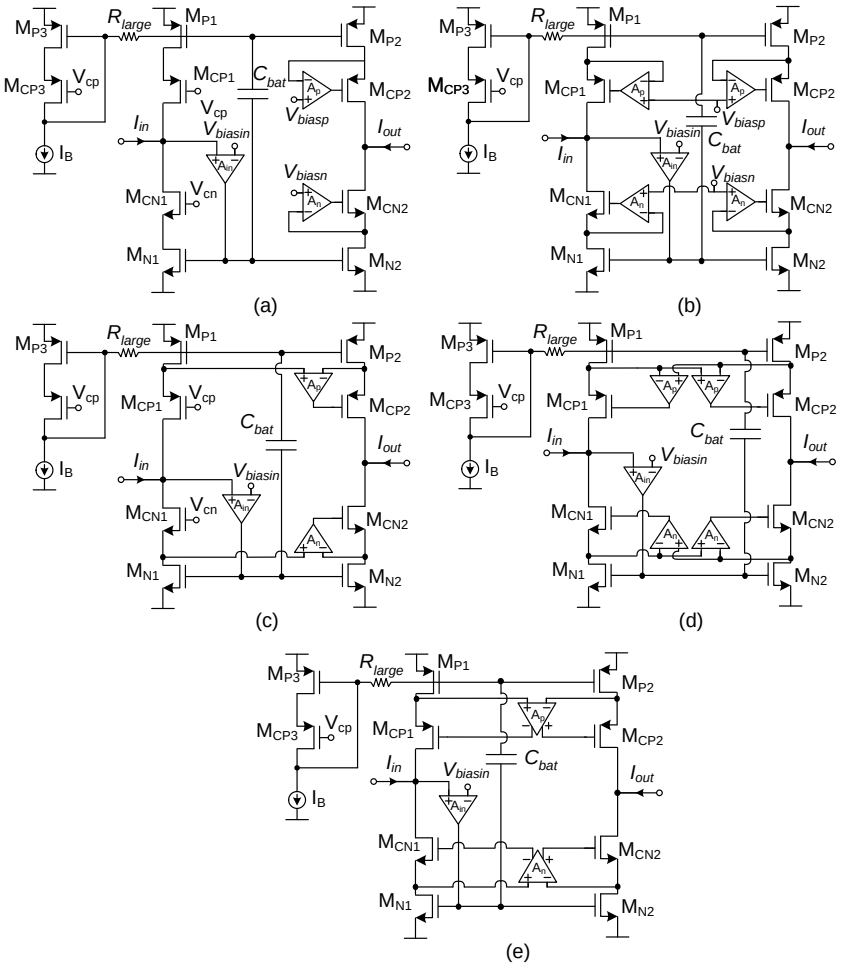

Figure 3.8. High performance current mirrors with input error amplifier and
(a) output regulated cascode in the output branch
(b) regulated cascode in the input and output branches
(c) auto-polarized regulated cascode in the output branch
(d) auto-polarized regulated cascode in the input and output branches
(e) fully differential auto-polarized amplifier regulated cascode in the in. and out. branches.

3.1.3.1 Proposed high performance current mirror

All these possibilities with different amplifier implementations were explored by the author in [Esp11], and the best performance implementation is shown in Figure 3.9. The input error amplifier is implemented by the common gate amplifier M_{P4}. Four transistors (M_{N3}, M_{N4}, M_{P5} and M_{P6}) have been added to create a regulated cascode current mirror based on the Säckinger implementation [Sac90]. M_{N4} and M_{P6} increase the output resistance by a factor $(g_{mN4\text{-}P6}r_{dsN4\text{-}P6})/2$ while M_{N3} and M_{P5} are used to guarantee that all transistor bias voltages of the input branch are matched to those of the output branch. Therefore, the current mirror input and output resistances are equal to:

$$R_{in} = \frac{1}{g_{mN1}g_{mP4}(R_{0B}||r_{dsP4})} \tag{3.8}$$

$$R_{out} = \frac{g_{mCN2}r_{dsN2}r_{dsCN2}g_{mN4}r_{dsN4}}{2} || \frac{g_{mCP2}r_{dsP2}r_{dsCP2}g_{mP6}r_{dsP6}}{2} \tag{3.9}$$

where R_{oB} is the resistance of current source I_B.

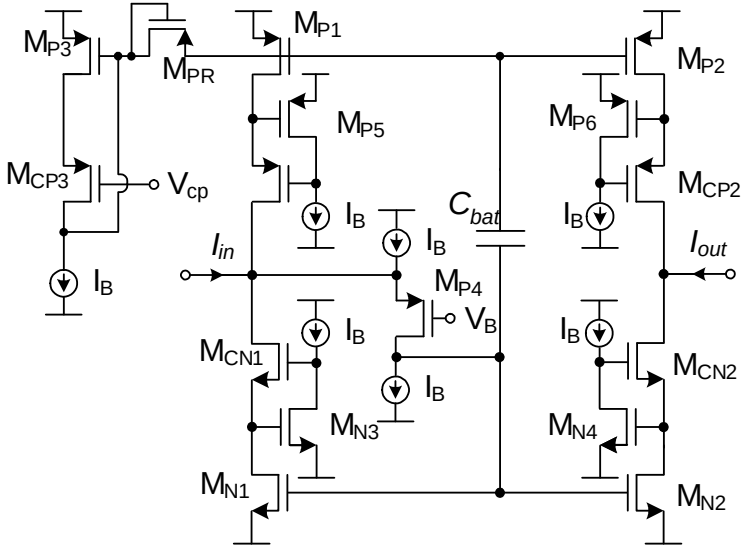

Figure 3.9. High performance current mirror implementation.

3.1.3.2 Measurement and simulation results

The circuit of Figure 3.9 was fabricated in a 0.5µm CMOS technology, with nominal NMOS and PMOS threshold voltages of 0.64 V and -0.91 V respectively. Capacitor C_{bat} was a poly-poly capacitor of 1 pF. High swing cascode current sources were employed. Transistor dimensions W/L (in µm/µm) were 100/0.6 (M_{P1}, M_{P2}, M_{P3}, M_{CN1}, M_{CN2}, M_{P5}, M_{P6}, M_{N3}, M_{N4}) 200/0.6 (M_{CP1}, M_{CP2}, M_{CP3}), 30/1 (M_{N1},M_{N2}), 100/1 (M_{P4}) and 1.5/0.6 (M_{PR}). Supply voltages were V_{DD} = 1.65V and V_{SS}= -1.65V, and the bias current I_B was 10 µA.

Figure 3.10 shows the measured THD for an input signal of 100 kHz and different values of input current amplitude normalized to the bias current (I_{in}/I_B). It is shown that THD is -85.7 dB for an input amplitude 5 times larger than the bias current, while measured THD of the [Lop08] current mirror is -78.4 dB for the same input. Simulated parameters of the proposed high performance class AB current mirror are compared with [Lop08] and results are presented in Table 3.2. It can be seen that input resistance, bandwidth and equivalent input noise are very close. On the other hand, the output resistance is approximately 65 times larger in the proposed circuit. The silicon area of the proposed class AB current mirror is approximately 295 µm x 75 µm and quiescent power consumption is 264 µW.

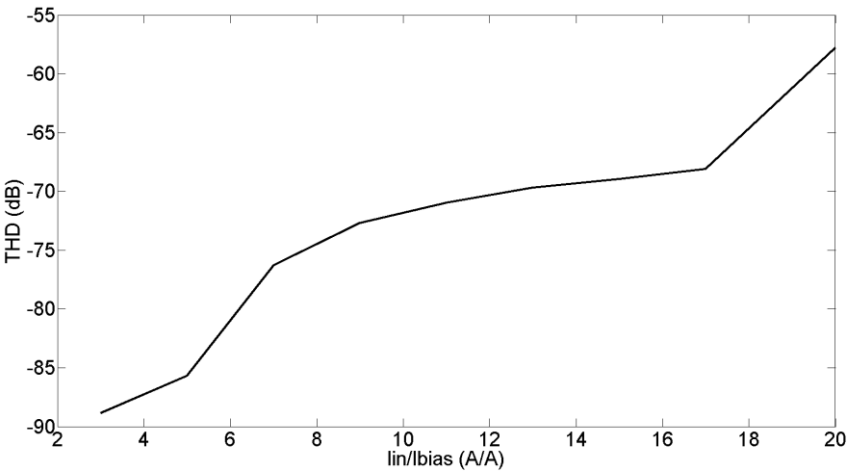

Figure 3.10. Measured total harmonic distortion of Figure 3.9 circuit for different input amplitudes (normalized to bias current IB).

Table 3.2. Comparison between [Lop08] and Figure 3.9 circuits simulation results

	[Lop08]	Figure 3.9
R_{in} (Ω)	17.61	15.79
R_{out} (MΩ)	11.73	650.8
BW (MHz)	96.97	97.58
Eq. Input Noise (pA/√Hz)	4.34	4.41

3.1.4 Typical current mirror applications

As it was stated above, current mirrors have several applications in analog circuit design. In this section, two of the most common applications for current mirrors: the dc biasing current source and the current linear combiner are shown

The main application within current mirrors is current replication and generation of DC bias currents. Figure 3.11 shows how to use current mirrors in order to do so. The output currents are replicas of the input current multiplied by the relationship between the mirror transistors sizes:

$$I_{out1} = I_{in}\frac{(W/L)_{N2}}{(W/L)_{N1}} \tag{3.10}$$

$$I_{out2} = I_{in}\frac{(W/L)_{N3}(W/L)_{P2}}{(W/L)_{N1}(W/L)_{P1}} \tag{3.11}$$

where $(W/L)_i$ are the aspect ratios of the M_i transistor. Note that it is very easy to implement a current amplifier simply dimensioning the transistors in order to have the desired current gain.

Other direct application of the current mirror is a current mode linear combiner. Figure 3.12 shows how simple is to implement the following function

$$I_{out} = I_{in1}\frac{(W/L)_{N2}}{(W/L)_{N1}} + I_{in2}\frac{(W/L)_{N4}}{(W/L)_{N3}} - I_{in3}\frac{(W/L)_{N6}(W/L)_{P2}}{(W/L)_{N5}(W/L)_{P1}} \tag{3.12}$$

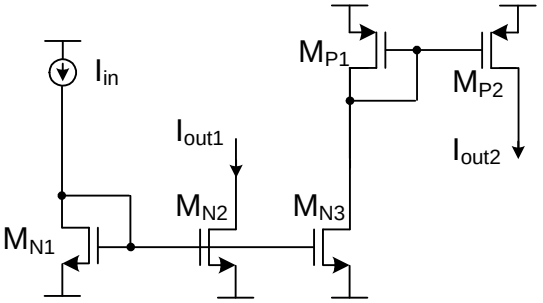

Figure 3.11. Current mirror as DC bias current source.

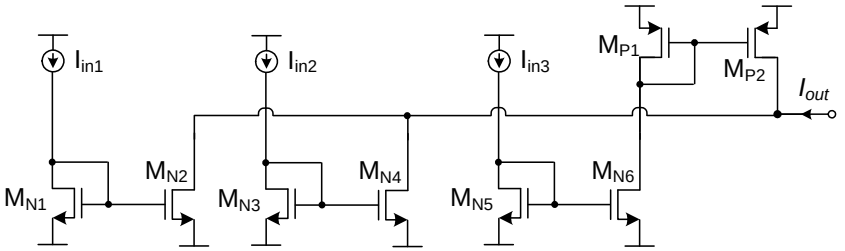

Figure 3.12. Current mirror as current linear combiner.

3.2 Current Conveyors

In 1968, the first generation current conveyor (CCI) was introduced by K.C. Smith and A.S Sedra [Smi68]. This three-terminal device is described by the following relationship:

$$\begin{pmatrix} i_y \\ v_x \\ i_z \end{pmatrix} = \begin{pmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{pmatrix} \begin{pmatrix} v_y \\ i_x \\ v_z \end{pmatrix} \tag{3.13}$$

As it can be seen from equation (3.13), a CCI copies the voltage from terminal Y to terminal X, and conveys the current supplied to terminal X to terminals Y and Z. For this reason it is called current conveyor.

This circuit was widely used as wideband current measuring device [Smi69] and negative impedance converter (NIC) [Bre88]. Several implementations both in BJT and CMOS were proposed [Fab84, Tem87].

The second generation current conveyor (CCII) was presented in a conference in 1968 but later published in a journal with much greater diffusion in 1970 [Sed70]. The CCII increased the versatility of its predecessor converting Y into infinite an input impedance terminal with no current flow. The device is described by:

$$\begin{pmatrix} i_y \\ v_x \\ i_z \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{pmatrix} \begin{pmatrix} v_y \\ i_x \\ v_z \end{pmatrix} \tag{3.14}$$

The voltage sensed at Y is copied to X while the current supplied to X is conveyed to the high impedance node Z, where it is supplied with positive polarity (CCII+) or negative polarity (CCII-). It is important to state that, ideally, node X has zero input impedance (voltage source), node Y has infinite input impedance (voltage sensor) and node Z has very high output impedance (current source).

The CCII has been found to be one of the most versatile blocks in the history of circuit theory, being able to realize controlled sources, impedance convertors, impedance inverters, gyrators, non-linear blocks and almost all known active network building blocks, such as in active RC filters [Sed70, Smi70, Sed90]. For this reason the device became very popular and a great number of different implementation have been reported, first implemented with operational amplifiers [Bla76, Wil84, Lid85, Tou85] and later on fully integrated in CMOS technology [Nis85, Go88]. A good review of about this topic was done by B. Wilson in 1990 [Wil90].

Finally, the third generation current conveyor was introduced by A. Fabre in 1995 [Min06]. This device is similar to the CCI but with the difference that the current supplied by i_x is inverted with respect to the one supplied by i_y. The CCIII operation is determined by the following relationship:

$$\begin{pmatrix} i_y \\ v_x \\ i_z \end{pmatrix} = \begin{pmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{pmatrix} \begin{pmatrix} v_y \\ i_x \\ v_z \end{pmatrix} \tag{3.15}$$

CCIII conveys the current supplied to node X to nodes Y and Z, and copies the voltage at node Y to node X. This device was presented as a floating current sensing device, but other applications such as filters or inductance simulator have been proposed [Hor97, Abu98, Wan00, Cho01, Kun02, Min03].

3.2.1 The class AB second generation current conveyor

The class AB current mirror presented in section 3.1 can be also used as a CCII. Figure 3.13 shows the resulting circuit. The voltage at node Y is accurately copied to node X by the input error amplifier. At the same time, the amplifier reduces the input resistance in a factor of A, being able to easily achieve values around 15Ω. As a current mirror is implemented between terminals X and Z, the current supplied to X is conveyed to Z, a high impedance output node. Using the techniques explained in section 3.1.3, output resistances of hundreds of MΩ can be achieved. Therefore, a very compact, simple, low power and high performance CCII can be designed.

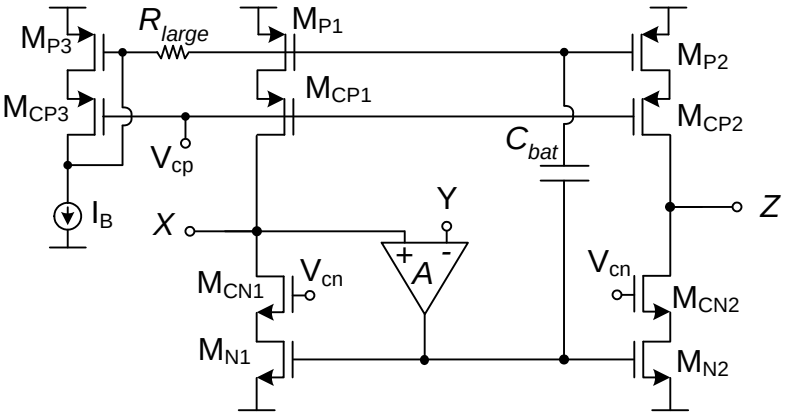

Figure 3.13. Class AB CCII.

3.2.2 The class AB second generation current conveyor

Several CCII applications were cited above. In this section, two simple direct applications of CCII that have been used in this work will be outlined: the current follower and the V/I converter.

Both circuits are shown in Figure 3.14. The current follower (Figure 3.14(a)) is achieved by simply connecting the Y terminal to the DC voltage input desired at the X terminal. Afterwards, the input current is supplied to node X, and it is conveyed to Z. In the V/I converter (Figure 3.14(b)), the input voltage is applied to the node Y. This voltage is copied to node X, which is converted into the current V_{in}/R at the resistor R. This current is afterwards conveyed to terminal Z.

Other more complex applications of the CCII such as the Voltage Feedback Current Operational Amplifier (VFCOA) are shown in next chapters.

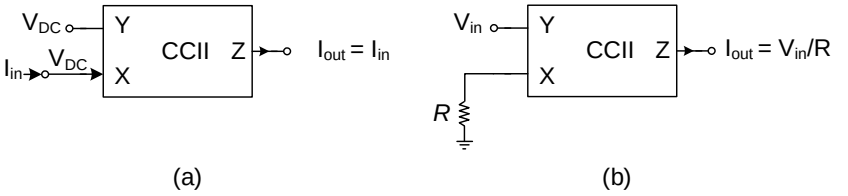

Figure 3.14. (a) Current Follower (b) V/I Converter.

3.3 Conclusions

In this chapter, two basic building blocks of current mode circuits, namely the current mirror and the current conveyor have been presented. Class AB implementations for both circuits have been shown. Both low-power low-voltage and high performance implementations have been shown, allowing a wide range of possibilities in current mode design.

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CHAPTER 4

Ultra low power tunable current mode filter design for channel selection

Externally linear internally nonlinear [Tsi97] (ELIN) current-mode [Tou90] companding filters are a very interesting option in high dynamic range low voltage filter design because the internal node's voltages are compressed, allowing reduced supply rails [See90]. As explained in section 2.2.3, these circuits are also called *companding* circuits, as the input is *com*pressed before the signal is processed, being ex*pand*ed afterwards. The compression function employed dictates the relationship between internal and external signals, being the logarithmic law the most widely used one [Fre93, Fre96, Tsi95, Dra99, Enz99]. In the last years a lot of research has been done in log-domain circuits, presenting a large variety of implementations [Bak03, Elg98, Fox04, Him97, Pyt01, Kri01, Pun97, Lop05]. The main limitation in log-domain circuits is their inherent class A behavior. Although it is possible to design class AB log-domain circuits [Fox00, Fre99] they have two main limitations. First, the synthesis of biquadratic structures is not straightforward because all the currents should remain positives at all times. Second, class AB implementations increment the transistor and integrating capacitor count by a factor of two. Furthermore, as this approach duplicates the system blocks, it requires good matching, and as transistor matching in weak inversion operation is very dependent of threshold voltage, large device areas must be used in order to minimize the threshold voltage variations, increasing the overall chip area and reducing bandwidth.

Hyperbolic sine (sinh) filters [Kat08] form another subclass of ELIN exponential companding circuits. The compression/expansion function is the hyperbolic sine which is an odd function from a mathematical point of view, allowing both positive and negative input and output signals. For this reason, class AB operation can be achieved with half the capacitor area than in the pseudo-differential log-domain approach.

Even though sinh filters have promising features and the synthesis procedures were presented 20 years ago [Fre96, Tsi95], there has not been done as much research in this topic as in the log-domain approach. In the theoretical field, besides of the two above mentioned general synthesis procedures, in [Lop99] it was presented a method to synthesize sinh systems from Gm-C systems by component to component substitution, and in [Kha12] a systematic method for designing Sinh-Domain linear transformation filters. In the practical field, even though several simulated sinh filter designs have been presented [Kat05, Had06, Kat07, Gla08, Pil11, Kas12, Kar13, Psy13, Kaf14, Tsi14] up to date, only one of them was validated with measurement results [Kur13].

This chapter presents an ultra-low power tunable current mode filter for channel selection. First, the two predominant systematic procedures for sinh filters synthesis are introduced. Afterwards, the proposed implementation is shown followed by the experimental and simulation results. Finally, some conclusions are exposed.

4.1 Hyperbolic sin filter synthesis

The two main synthesis procedures for sinh filters were presented in 1996 and 1997 by D.R. Frey [Fre96] and Y. Tsividis [Tsi95], respectively. In this section, the step-by-step synthesis of a first order sinh lossy integrator using both methods is shown. Other filter topologies such as high pass filters or band pass filters can be easily derived using the same methods.

Both methods have the same goal, which is to implement the state-space description of a first order lossy integrator:

$$\frac{dI_{out}}{dt} = \omega_0(I_{in} - I_{out}) \tag{4.1}$$

where I_{out} and I_{in} are the output and input currents, respectively, and ω_0 is the integrator pole frequency.

The synthesis methods consist on generating the integrating capacitor current I_C, and using the voltage across the capacitor V_C to feed a transconductor (expansion block) that provides the output signal.

$$I_C = C\frac{dV_C}{dt} \tag{4.2}$$

4.1.1 D.R Frey method [Fre96]

The method proposed in [Fre96] consists on applying a nonlinear mapping to the state variables of a linear state-space description (4.1) as shown in Figure 4.1. The non-linear mapping is imposed by the compression and expansion rules. The compression rule relates the input current and the input voltage (V_{in}). The expansion rule links the integrator capacitor voltage and the output current.

$$I_{in} = I_0 \sinh(aV_{in}) \tag{4.3}$$

$$I_{out} = I_0 \sinh(aV_C) \tag{4.4}$$

where *a* is a constant dependent of the implementation with dimensions Volts^{-1} and I_0 is a bias current.

Figure 4.1. Method [Fre96] filter structure

Combining Equations (4.3) and (4.4) into (4.1) and multiplying both sides by C, the current trough the integrating capacitor is obtained.

$$C\frac{dV_C}{dt} = -\frac{C\omega_0}{a}\tanh(aV_C) + \frac{C\omega_0}{a}\frac{\sinh(aV_{in})}{\cosh(aV_C)} \tag{4.5}$$

Rearranging the terms using the followings relationships

$$\frac{\sinh(aV_i)}{\cosh(aV_j)} = \cosh\left(a(V_i - V_j)\right)\tanh(aV_j) + \sinh\left(a(V_i - V_j)\right) \tag{4.6}$$

$$I_0 = \frac{C\omega_0}{a} \tag{4.7}$$

The final form for I_C is obtained

$$I_C = I_o\left(-1 + \cosh\left(a(V_{in} - V_C)\right)\right)\tanh(aV_C) + I_o \sinh\left(a(V_{in} - V_C)\right) \quad (4.8)$$

The block diagram that implements Equation (4.8) is shown in Figure 4.2. The input current I_{in} is compressed generating the input voltage V_{in} by S_1. Afterwards, the integration current is generated by S_3 and T. The output current is produced by S_1. S and T are sinh and tanh transconductors respectively, and both implementations are presented in [Fre96].

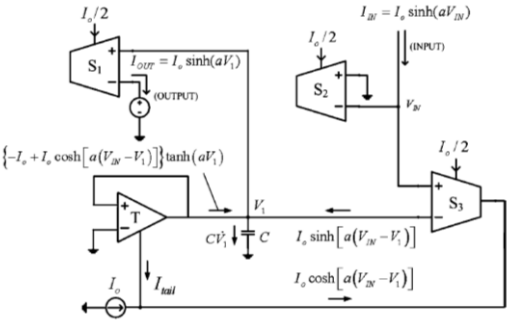

Figure 4.2 Lossy integrator block diagram with Frey method [Fre96, Kat08]

4.1.2 Y. Tsividis method [Tsi95]

The method proposed by Tsividis is represented in Figure 4.3. This procedure consist on setting the expansion rule that relates the output current and the voltage across the integrator capacitor

$$I_{out} = g(V_C) = I_{DC}\sinh(aV_C) \quad (4.9)$$

And afterwards finding the pre-distortion block that preserves the input-output linearity, being the integrator capacitor current the pre-distortion block output

$$f(I_{in}, I_{out}) = I_C = C\frac{dV_C}{dt} \quad (4.10)$$

In order to do so, the procedure starts applying the chain rule to the first term in Equation (4.1) obtaining:

$$\frac{dI_{out}}{dt} = \frac{dI_{out}}{dV_C}\frac{dV_C}{dt} = aI_0\cosh(aV_C)\frac{I_C}{C} \tag{4.11}$$

Combining Equations (4.11), (4.1) and (4.7) and solving for $f(I_{in}, I_{out})$:

$$f(I_{in}, I_{out}) = \frac{I_0(I_{in}-I_{out})}{I_{DC}\cosh(aV_C)} \tag{4.12}$$

Equation (4.12) represents the necessary and sufficient condition satisfied by the pre-distortion block so the system is externally linear, shown in Figure 4.4.

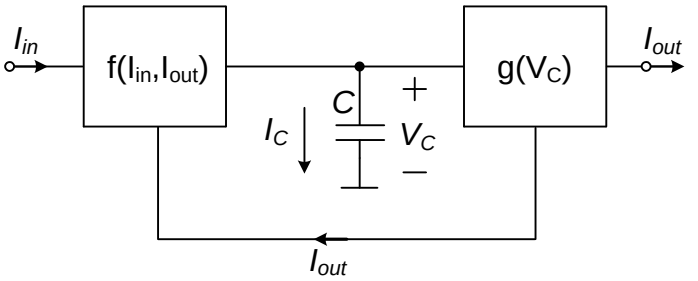

Figure 4.3 Generic block diagram for Tsividis method [Tsi95]

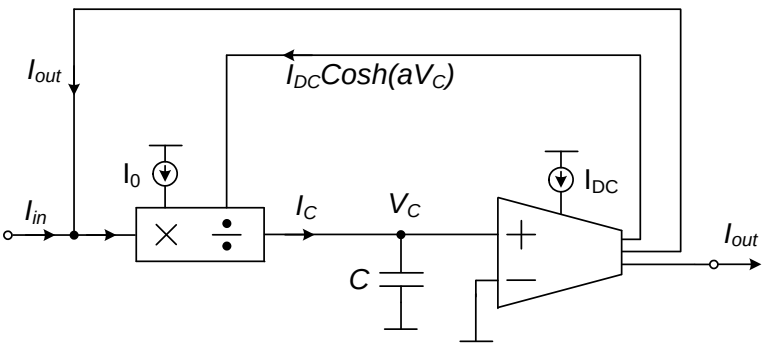

Figure 4.4. Lossy integrator block diagram by Tsividis method [Tsi95]

Figure 4.4 circuit uses a 4 quadrant current multiplier/divider. Depending on the implementation it could be convenient to use a two quadrant current multiplier/divider. Figure 4.5 shows this implementation, where a

geometric mean splitter (GMS) is used to transform the bipolar input current into two unipolar input currents I_{in}^{u} and I_{in}^{l} which meet the following rules:

$$I_{in} = I_{in+} - I_{in-} = I_{in}^{u} - I_{in}^{l} \tag{4.13}$$

$$I^{2}{}_{DC\_GMS} = I_{in}^{u} I_{in}^{l} \tag{4.14}$$

with I_{DC_GMS} being the GMS bias current, equal to the geometric mean of the input currents. The output current can also be split into two unipolar currents I_{out}^{u} and I_{out}^{l}. In order to do so, it is convenient to expand the sinh and cosh functions into their exponential relationships:

$$I_{DC}\sinh(aV_C) = \frac{I_{DC}}{2}(e^{aV_C} - e^{-aV_C}) \tag{4.15}$$

$$I_{DC}\cosh(aV_C) = \frac{I_{DC}}{2}(e^{aV_C} + e^{-aV_C}) \tag{4.16}$$

And then define the output currents as:

$$I_{out}^{u} = \frac{I_{DC}}{2} e^{aV_C} \tag{4.17}$$

$$I_{out}^{l} = \frac{I_{DC}}{2} e^{-aV_C} \tag{4.18}$$

Combining (4.15) and (4.16) with (4.17)-(4.18) a more convenient form for these equations is achieved

$$I_{out} = I_{DC}\sinh(aV_C) = I_{DC}\frac{e^{aV_C}}{2} - I_{DC}\frac{e^{-aV_C}}{2} = I_{out}^{u} - I_{out}^{l} \tag{4.19}$$

$$I_{DC}\cosh(aV_C) = I_{DC}\frac{e^{aV_C}}{2} + I_{DC}\frac{e^{-aV_C}}{2} = I_{out}^{u} + I_{out}^{l} \tag{4.20}$$

Finally, combining Equations (4.13), (4.19) and (4.20) into Equation (4.21) the predistortion block for this implementation is:

$$f(I_{in}, I_{out}) = I_C = \frac{I_0\left(I_{in}^{u} + I_{out}^{l}\right)}{I_{out}^{u} + I_{out}^{l}} - \frac{I_0\left(I_{in}^{l} + I_{out}^{u}\right)}{I_{out}^{u} + I_{out}^{l}} = I_{C1} - I_{C2} \tag{4.22}$$

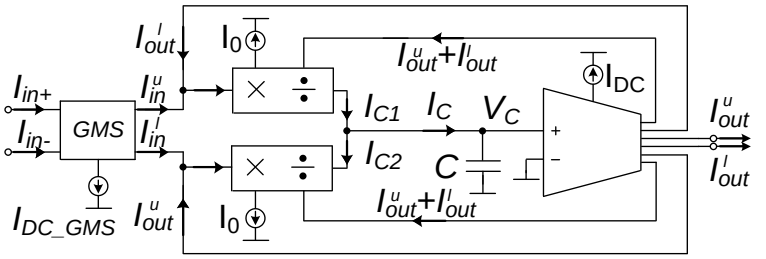

Figure 4.5. Lossy integrator block diagram with Tsividis method [Tsi95] using two quadrant current multipliers/dividers.

4.1.3 Comparison of the two methods

Comparing Figures 4.2 and 4.4, it is clear that [Tsi95] proposed a much simpler implementation than [Fre96]. Although the starting point in both methods is Equation (4.1), [Fre96] imposes that the input current has to be compressed into an input voltage, while [Tsi95] is more flexible and doesn't force that input stage. Besides that, the main difference between both methods is the application of the trigonometric relationship in Equation (4.6). In [Fre96], this relationship leads to a more expanded chain with 4 transconductors. On the other hand, [Fre96] only needs a single transconductor, but in return it requires a current multiplier/divider.

4.2 Hyperbolic sin channel selection filter implementation

The first step towards the filter design is choosing a synthesis method. In this case, the Tsividis method [Tsi95] was chosen because it leads to a more compact and simpler design than the Frey [Fre96] method. Figure 4.5 diagram was chosen over Figure 4.4 circuit because although the latter offers a more compact design, due to technological constraints the former is more convenient as will be explained below.

As explained in Chapter 2, there are different design techniques and approaches available when designing low voltage low power circuits. One of these approaches is using CMOS transistor operating in weak inversion. The matching between two MOS transistors operating in weak inversion is extremely dependent of the V_{sb} voltage. In order to minimize these matching errors, V_{sb} has to be equal to 0. If the design needs matching in both NMOS and PMOS transistors, this can only be possible using triple-well processes, increasing the fabrication cost. A four quadrant current multiplier/divider design needs matching between

N and P transistors, while a two quadrant current / multiplier needs only matching between same type transistor. For this reason, the Figure 4.5 design was chosen.

The proposed filter is designed using 2-input FGMOS transistors. This device was explained in Chapter 2, but, for convenience, some of its features are shown next. The two-input FGMOS transistor layout, symbol and equivalent circuit are shown in Figure 2.2. The drain current of a two-input FGPMOS with its bulk and source terminals connected to V_{DD} operating in weak inversion / saturation, and with $C_1=C_2 >> C_{GD}$ is

$$I_D = I_S e^{\frac{V_{GS}}{nU_T}} = I_S K e^{\frac{\alpha(V_1+V_2)}{nU_T}} \tag{4.23}$$

where I_S is a constant current dependent on transistor geometry and technology, n is the slope factor ($1 < n < 2$), $U_T = kT/q$ is the thermal voltage, $\alpha = C_1/C_T = C_2/C_T$, $C_T = \sum_{i=1}^{N} C_i + C_{GS} + C_{GD} + C_{GB}$ and

$$K = e^{\left(\frac{C_{GS}+C_{BG}}{C_T}-1\right)\frac{V_{DD}}{nU_T}} \tag{4.24}$$

Now that the basis of QFGT transistors has been explained, the different blocks that form the sinh filter following Figure 4.5 are explained.

4.2.1 The Geometric Mean Splitter

The first block to be introduced is the geometric mean splitter. Its implementation is shown in Figure 4.6. As it is formed by two identical structures in a differential arrangement only one of them is analyzed, and the result is extended to the whole circuit afterwards. The gate terminals interconnections of the P-type FGMOS transistors form the main processing core while NMOS transistor are used as current mirrors. Assuming matched PMOS and NMOS transistors ($I_{SP1} = I_{SP2} = I_{SP3} = I_S$, $n_{P1} = n_{P2} = n_{P3} = n$, $K_{P1} = K_{P2} = K_{P3} = K$ and $I_{DN1} = I_{DN2}$) and using (4.23) to calculate the currents through $M_{P1\text{-}3}$ transistors:

$$I_{DP1} = I_{DC\_GMS} = I_S K e^{\frac{\alpha(V_{DP1}+V_{DP2})}{nU_T}} \tag{4.25}$$

$$I_{DP2} = I_{DP3} - I_{in+} = I_S K e^{\frac{2\alpha V_{DP2}}{nU_T}} \tag{4.26}$$

$$I_{DP3} = I_S K e^{\frac{2\alpha V_{DP1}}{nU_T}} \tag{4.27}$$

where V_{DPi} is the drain voltage of transistor M_{Pi}. Solving the equation system (4.25)-(4.27) for I_{DP3}, the following relationship is obtained:

$$I_{DP3}^2 - I_{DP3}I_{in+} - I_{DC}^2 = 0 \tag{4.28}$$

which leads to the final I_{DP3} form

$$I_{DP3} = \frac{I_{in+} \pm \sqrt{I_{in+}^2 + 4I_{DC}^2}}{2} \tag{4.29}$$

Although (4.29) gives two different solutions, as I_{DP3} has to be positive, only the additional numerator solution makes sense. As both half circuits are equal, the final expressions for I^u_{in} and I^l_{in} are:

$$I_{in}^u = \frac{I_{in+} + \sqrt{I_{in+}^2 + 4I_{DC}^2}}{2} \tag{4.30}$$

$$I_{in}^l = \frac{I_{in-} + \sqrt{I_{in-}^2 + 4I_{DC}^2}}{2} \tag{4.31}$$

Combining (4.30)-(4.31) into (4.13)-(4.14), it can be seen that the circuit follows the GMS behavior. Note that if $(W/L)_{N3\text{-}4} = (W/L)_{N1\text{-}2,5\text{-}6}$ then I^u_{in}-$I^l_{in} = I_{in}/2$; this can be avoided simply by making $W_{MN3\text{-}MN4} = 2W_{MN1\text{-}3,5\text{-}6}$. It is also interesting to highlight that under static operation all transistors are biased with I_{DC_GMS} with a total quiescent current consumption of $6I_{DC\_GMS}$, and the minimum supply voltage is as low as $V_{gsn} + |V_{dsp,sat}|$, allowing low voltage operation.

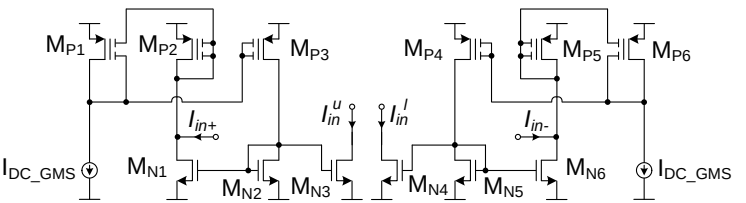

Figure 4.6 Proposed geometric mean splitter

4.2.2 The current multiplier / divider

After the input is split, both inputs and outputs are processed through the current multipliers / dividers, creating the integrator capacitor current. This circuit was presented in [Lop05] and is shown in Figure 4.7. It uses the FGPMOS device. Using Equation (4.23) the drain voltages of transistors M_1, M_2 and M_3 are:

$$I_{DP7} = I_{in1,m/d} = I_S K e^{\frac{\alpha(V_{DP7}+V_{DP9})}{nU_T}} \tag{4.32}$$

$$I_{DP8} = I_{in2,m/d} = I_S K e^{\frac{\alpha(V_{DP8}+V_{DP9})}{nU_T}} \tag{4.33}$$

$$I_{DP9} = I_{in3,m/d} = I_S K e^{\frac{2\alpha V_{DP9}}{nU_T}} \tag{4.34}$$

$$I_{DP10} = I_{out,m/d} = I_S K e^{\frac{\alpha(V_{DP7}+V_{DP8})}{nU_T}} \tag{4.35}$$

The output current can be calculated combining equations (4.32) to (4.35) and solving for $I_{out,m/d}$

$$I_{out,m/d} = \frac{I_{in1,m/d} I_{in2,m/d}}{I_{in3,m/d}} \tag{4.36}$$

Considering that the circuit is driven by current mirrors with the same dc current I_{DC} it is easy to see that the total power consumption is $4I_{DC}$ and the minimum supply voltage is as low as $V_{gsn} + |V_{dsp,sat}|$, allowing low voltage operation. For more information about this circuit the reader is referred to [16].

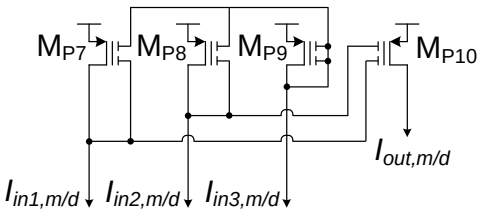

Figure 4.7 Current multiplier / divider [16]

4.2.3 The sinh transconductor

The last block in the filter is the sinh transconductor. It is shown in Figure 4.8, and it converts the integrator capacitor voltage into the output currents. As stated before, the transconductor has to provide the outputs according to (4.17)-(4.18). In order to do so, a differential pair is combined with the current multiplier / divider. Considering that the differential pairs are biased in weak inversion, the currents through M_{N9} and M_{N10} are:

$$I_{DN9} = \frac{I_{DC}}{1+e^{\frac{V_{cap}}{nU_T}}} \tag{4.37}$$

$$I_{DN10} = \frac{I_{DC}}{1+e^{-\frac{V_{cap}}{nU_T}}} \tag{4.38}$$

Therefore, the output currents are:

$$I_{out}^{u} = \frac{\frac{I_{DC}}{1+e^{-\frac{V_{cap}}{nU_T}}} - \frac{I_{DC}}{2}}{1+e^{+\frac{V_{cap}}{nU_T}}} = \frac{I_{DC}}{2} e^{+\frac{V_{cap}}{nU_T}} \tag{4.39}$$

$$I_{out}^{l} = \frac{\frac{I_{DC}}{1+e^{+\frac{V_{cap}}{nU_T}}} - \frac{I_{DC}}{2}}{1+e^{-\frac{V_{cap}}{nU_T}}} = \frac{I_{DC}}{2} e^{-\frac{V_{cap}}{nU_T}} \tag{4.40}$$

Comparing Equations (4.39)-(4.40) with (4.17)-(4.18) it is clear that the proposed circuit satisfies the required sinh transconductor specification with

$$a = \frac{1}{nU_T} \tag{4.41}$$

Combining equations (4.41) and (4.7) the filter's bandwidth can be calculated as

$$\omega_0 = \frac{I_0}{CnU_T} \tag{4.42}$$

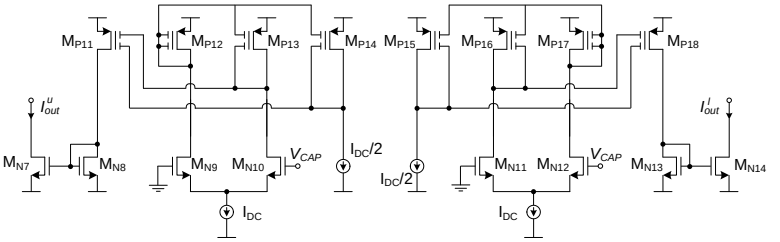

Figure 4.8 Proposed sinh transconductor implementation

4.3 Hyperbolic sin channel selection filter design

The analysis in Section 4.1.2 was done assuming that the pole introduced by the integrating capacitor is the dominant pole. Although this is plausible in low frequency operation, as transistors are operating in weak inversion, their bandwidth is limited, and when the filter cutoff frequency is set at higher frequencies the dominant pole assumption is no longer valid.

In order to calculate the filter transfer function taking into account all the active blocks, each active block small signal transfer function should be calculated. Considering a single (dominant) pole behavior for each block, these transfer functions are:

$$i_{in}^{u} = \frac{I_{in+}}{1+s/\omega_{GMS}} \tag{4.43}$$

$$i_{in}^{l} = \frac{I_{in-}}{1+s/\omega_{GMS}} \tag{4.44}$$

$$i_{out,m/d} = \frac{i_1+i_2-i_3}{1+s/\omega_{m/d}} \tag{4.45}$$

$$i_{out}^{u} = \frac{g_{mN}V_{cap}}{1+s/\omega_{trans}} \tag{4.46}$$

$$i_{out}^{l} = \frac{-g_{mN}V_{cap}}{1+s/\omega_{trans}} \tag{4.47}$$

Once the transfer functions of each block are calculated, the overall filter transfer function can be expressed as:

$$H_{filter} = \frac{1}{\left(1+\frac{s}{\omega_{GMS}}\right)\left(1+\frac{s}{\omega_0}\left(1+\frac{s}{\omega_{trans}}\right)\left(1+\frac{s}{\omega_{m/d}}\right)\right)} = \frac{1}{\left(1+\frac{s}{\omega_{GMS}}\right)\left(1+\frac{s}{\omega_0}+\frac{s^2}{\omega_0}\left(\frac{1}{\omega_{trans}}+\frac{1}{\omega_{m/d}}\right)+\frac{s^2}{\omega_0\omega_{trans}\omega_{m/d}}\right)} \quad (4.48)$$

As seen in (4.48), the overall system behaves as a first order filter (the GMS) in cascade with a third order filter. It is interesting to consider that when ω_{GMS}, $\omega_{m/d}$, ω_{trans} >> ω_0 Equation (4.48) is equivalent to (4.1), and if $\omega_{trans} \cong \omega_{GMS} \cong \omega\frac{m}{d} \cong \omega_0$ the system operates as a fourth order filter with the power and area consumption of a first order filter. This approach is very interesting in ultra-low power design. Nevertheless, there are some conditions that have to be accomplished for this design to operate properly. First, the active blocks should have a dominant pole behavior. Second, the active blocks cutoff frequencies have to be insensible to temperature or process variations. Third, active blocks' bandwidths have to be proportional to I_0, so the filter transfer function maintains its shape when it is tuned by I_0.

These conditions can be verified either solving the small signal ac equivalent circuit of Figures 4.6, 4.7 and 4.8 or through simulations. Because of the floating gate transistors, it is very complex to solve those circuits by hand, so simulations have been done to analyze their frequency response. The mechanism used to set the frequency response of the active blocks is the value of the floating gate capacitors. These capacitors are implemented as poly-poly capacitors, and matching techniques are used in the layout. Thus, these capacitances are matched between them and to the integrating capacitance, so that they experience the same process, voltage and temperature (PVT) variations which can be compensated by the proper automatic tuning circuit. This fact makes the poles generated by the FGMOS blocks as reliable as that of the integrating capacitor. Other approaches in the technical literature that employ parasitic capacitances to achieve extra poles in the frequency response often do not feature this advantage.

Figures 4.9, 4.10 and 4.11 show the frequency responses of the circuits of Figures 4.6, 4.7 and 4.8, respectively, for different values of the floating gate capacitors. Starting with the GMS frequency response (Figure 4.9), at a first look it can be seen that this circuit don't show a dominant pole behavior, becoming not usable for the proposed circuit. The current multiplier / divider frequency response shown in Figure 4.10 has a similar behavior than the geometrical mean splitter but in this case the pole is at a lower frequency than the zero, being also

not usable for this design. Lastly, the transconductor frequency response is shown in Figure 4.11. In this case, the frequency response shows a dominant pole behavior with its cutoff frequency controlled by the floating gate capacitor.

Taking into account the previous analysis, the idea behind this design is to track the transconductor cutoff frequency with ω_0 and maintain the GMS first zero as far as possible from this frequency so it doesn't interfere with the overall system frequency response.

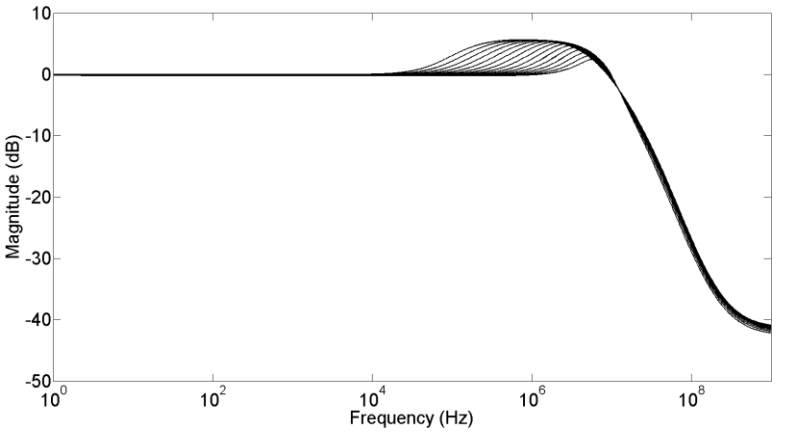

Figure 4.9 Geometric mean splitter simulated frequency response for different values of floating gate capacitor

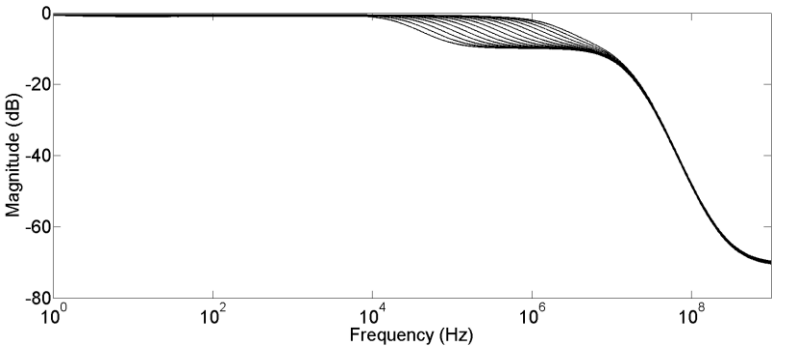

Figure 4.10 Current multiplier / divider frequency response for different values of floating gate capacitor

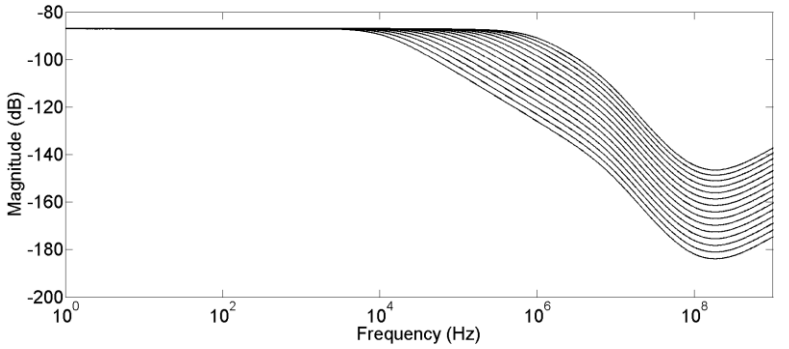

Figure 4.11 Sinh transconductor simulated frequency response for different values of floating gate capacitor

4.4 Measurement results

The filter of Figure 4.5 has been fabricated in a 0.5µm CMOS technology with nominal NMOS and PMOS threshold voltages of 0.67 V and -0.96 V respectively. FGMOS and C capacitors were implemented as poly-poly capacitors with a nominal value of 1 pF and 20 pF, respectively. Transistor's dimensions W/L (in µm/µm) were: 75/1 ($M_{P1\text{-}6,11\text{-}18}$), 150/1 ($M_{P7\text{-}10}$), 40/1.35 ($M_{N1\text{-}8,13\text{-}14}$) and 200/1 ($M_{N9\text{-}12}$). I_0, I_{DC} and I_{DC_GMS} were implemented as single-transistor NMOS current sources (60/3 µm/µm). The circuit was measured for 1.5 V supply voltage. The silicon area is 0.256 mm², where 75% of the area corresponds to capacitors.

Fig. 4.12 shows the measured filter's magnitude response for different bandwidths, showing a second order filter response. As it can be seen, the cut-off frequency can be continuously varied from 50 kHz up to 2 MHz. Table 1 summarizes the measured performance for 1.2MHz bandwidth, and compares it with the only measured sinh implementation previously reported to date. A well-known figure of merit (FoM) has been used to compare both filters, defined as

$$\mathrm{FoM} = \mathrm{P}/(8\,\mathrm{k\,T\,BW\,N\,DR}) \tag{4.49}$$

where P is the static power consumption, k is the Boltzmann constant, T is the room temperature (300K), BW is the filter's bandwidth, N is the number of poles and DR is circuit's dynamic range. Note that the proposed filter shows improved FoM.

Table 4.1. Summary of measured performance

	This work	[Kur13]
CMOS Technology (μm)	0.5	0.35
Supply Voltage (V)	1.5	2
Topology	Sinh Filter	Sinh Filter
Integrator capacitor (pF)	20	20
Tuning range	50kHz-2000MHz	20 Hz – 2 kHz
Bias current (nA)	2000	10
Cutoff frequency	1.2MHz	2kHz
IIP3@300-310kHz (μA)	8.4	NA
Eq. Input Noise (fA/√Hz)	68.3	NA
Dynamic Range@THD4% (dB)	99.7	110
Die area (mm^2)	0.256	0.074
Quiescent power consumption (μW)	45	0.3
FoM	5860	14322

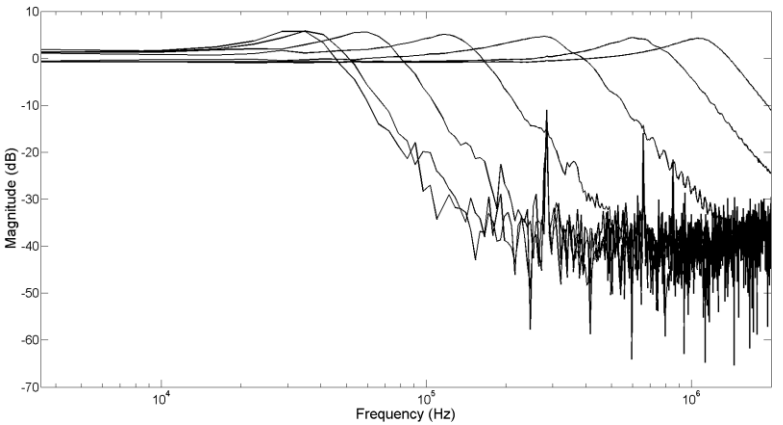

Figure 4.12. Measured frequency response

4.4 Conclusions

A novel current mode ELIN low pass sinh filter implementation has been presented. The proposed filter uses the internal sinh transconductor transfer function to have a second order filter response with only one integrating capacitor, achieving very low power consumption. The circuit is validated with measurement results and it represents the second fabricated and measured sinh filter reported so far. Comparing with the first one [Kur13], it requires less supply voltage and achieves higher bandwidth and improved FoM by a factor of 2.5, at the expense of more silicon area.

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CHAPTER 5

Current mode constant bandwidth variable gain amplifier design

Nowadays, the most popular analog building block is the Voltage Operational Amplifier (VOA). It provides a very high open loop gain, and a controllable closed loop gain only dependent of the feedback network. Because of the wide variety of achievable transfer functions, it is used to implement high complexity circuits such as filters, amplifiers, A/D and D/A converters, oscillators, power regulators, V-I/I-V converters, etc. [Fra03, Jun05, Sed10]. When designing wideband circuits, the main VOA limitation is its constant gain-bandwidth product. On the other hand, the Current Feedback Voltage Operational Amplifier (CFVOA) has constant bandwidth independent of the gain [Sen13, Sol96, Pal01, Pen11].

Since some sensors and transducers provide an output signal in current form, it is desirable in these cases to process the signal directly in the current mode (CM) domain. High-performance implementations of the CM equivalents of the VOA and CFVOA, (named Current operational amplifier, COA [Pal00a, Pen02] and Voltage Feedback Current Operational Amplifier, VFCOA [Bru91, Kau93, Pal98], respectively) are therefore required. Note that being COAs the CM counterpart of VOAs, they are still bounded to the constant gain bandwidth product. Instead, the VFCOA combines the constant bandwidth property with the possibility of using non-linear resistors in the feedback loop without penalty

in the overall circuit linearity [Mag94], becoming a very interesting option for designing wideband circuits.

In this chapter the gain-bandwidth product trade-off is reviewed. Afterwards, the current operational amplifier and the voltage feedback current operational amplifier are shown. The chapter finalizes presenting a current mode constant bandwidth variable gain amplifier design.

5.1 Avoiding the gain-bandwidth product trade-off

Figure 5.1 shows the general block diagram for a linear feedback circuit, where X_{IN} and X_{OUT} are the input and output signals, respectively, $-1<\alpha<1$ is the scaling factor, $A_d(s)$ is the amplifier open loop differential gain and $0<\beta<1$ is the feedback factor. Both β and α are considered frequency independent and $\beta A_d \gg 1$. Considering $A_d(s)$ as a single pole function with pole frequency ω_p

$$A_d(s) = \frac{A_d}{1+\frac{s}{\omega_p}} \tag{5.1}$$

The transfer function of Figure 5.1 diagram is:

$$A_{CL}(s) = \frac{\alpha/\beta}{1+\frac{1}{\beta A_d}+\frac{s}{\beta A_d \omega_p}} \approx \frac{\alpha/\beta}{1+\frac{s}{\beta\omega_{GBW}}} = \frac{A_{CL}(0)}{1+\frac{s}{\omega_{CL}}} \tag{5.2}$$

being $\omega_{GBW} = A_d\omega_p$ a constant called the gain bandwidth product.

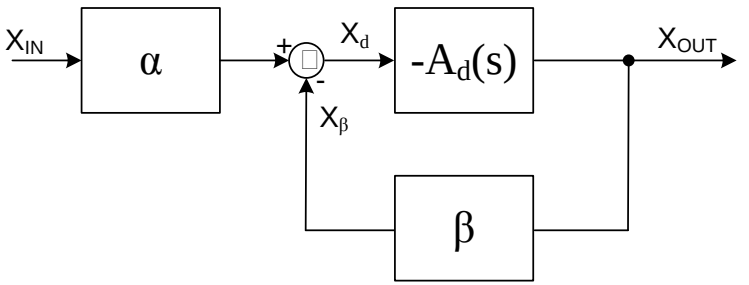

Figure 5.1. Linear feedback circuit general block diagram

The closed loop bandwidth and closed loop gain are

$$\omega_{CL} = \beta\omega_{GBW} \tag{5.3}$$

$$A_{CL}(0) = \frac{\alpha}{\beta} \tag{5.4}$$

Considering $\alpha = 1$ a constant, from Equations (5.3) and (5.4) it can be seen that the maximum closed loop bandwidth is achieved for $\beta = 1$, but this provides the minimum closed loop gain. Therefore, ω_{CL} and $A_{CL}(0)$ are interchangeable, and related by

$$A_{CL}(0)\omega_{CL} = \alpha\omega_{GBW} \tag{5.5}$$

Equation (5.5) dictates that it is possible to increase the gain, but at the cost of reducing the bandwidth, being their product the constant $\alpha\omega_{GBW}$ (constant gain bandwidth product). Figure 5.2 shows the closed loop transfer function magnitude for the system of Figure 5.1 and different β values.

The constant gain bandwidth tradeoff can be avoided [Pen11] by considering a variable α. Thus, β sets the bandwidth and α sets the gain. Therefore, it is possible to achieve different gains having the same bandwidth, as shown in Figure 5.3. The drawback of this approach is that the maximum gain is fixed once a bandwidth is selected, because the maximum gain and the selected bandwidth are still bounded to the gain bandwidth product.

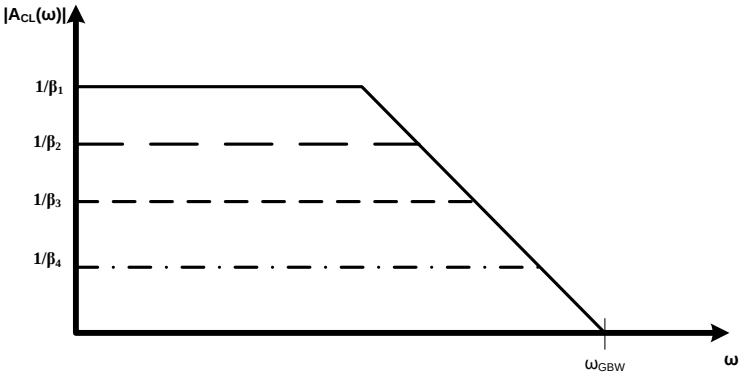

Figure 5.2. Constant gain bandwidth product trade-off

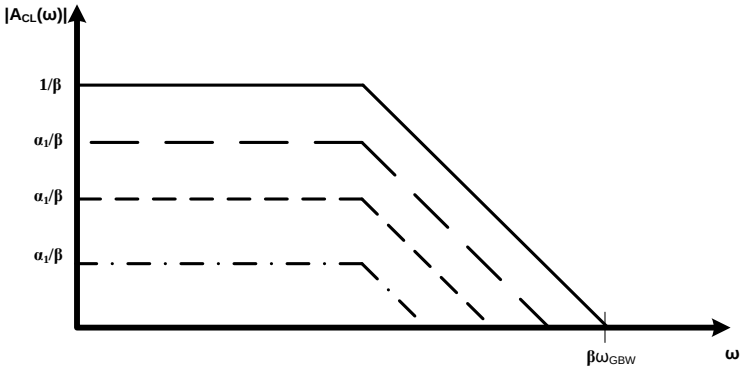

Figure 5.3. Constant bandwidth variable gain

5.2 Current operational amplifiers

5.2.1 The Current Operational Amplifier

The current mode equivalent of the voltage operational amplifier is the current operational amplifier (COA). The COA symbol and equivalent circuit with typical feedback network are shown in Figure 5.4(a) and (b) respectively. The COA can be modelled as a as a single-ended input differential-output floating current controlled current source, with (ideally) zero input impedance and infinite differential output impedance.

According to the Rosenstark formulation [Ros74], the exact closed-loop current gain, G_F, is related to the return ratio, T, the asymptotic gain, G_∞, and the direct transmission gain, G_0:

$$G_F = G_\infty \frac{T}{1+T} + G_0 \frac{1}{1+T} \tag{5.6}$$

All these quantities must be calculated with respect to one controlled source within the feedback amplifier (in this case the current controlled current source). The asymptotic gain, G_∞, is given by

$$G_\infty = \lim_{A_I \to \infty} \left(\frac{i_{out}^+}{i_{in}} \right) = 1 + \frac{R_2}{R_1} \tag{5.7}$$

where R_1 and R_2 are the feedback network resistors.

The return ratio T results to be

$$T(s) = A_I(s)\frac{R_1 r_0}{(R_1+r_0)(R_2+r_i)+R_1 r_0} \tag{5.8}$$

The forward gain G_o is lower than 1 and, being divided by 1+T in (5.6), is negligible.

If $R_2>>r_i$ and $R_1<<r_0$, T(s) can be approximated as

$$T(s) = A_I(s)\frac{1}{1+\frac{R_2}{R_1}} = \frac{A_I(s)}{G_\infty} \tag{5.9}$$

and the closed loop bandwidth ω_{CL} expressed as a function of the open loop bandwidth, ω_{OL}, is

$$\omega_{CL} \cong \big(1 + T(0)\big)\omega_{OL} \cong T(0)\omega_{OL} = \frac{A_I(0)\omega_{OL}}{G_\infty} \tag{5.10}$$

Comparing Equations (5.10) and (5.5) it is easy to see that the COA is also bounded to the constant gain bandwidth trade off.

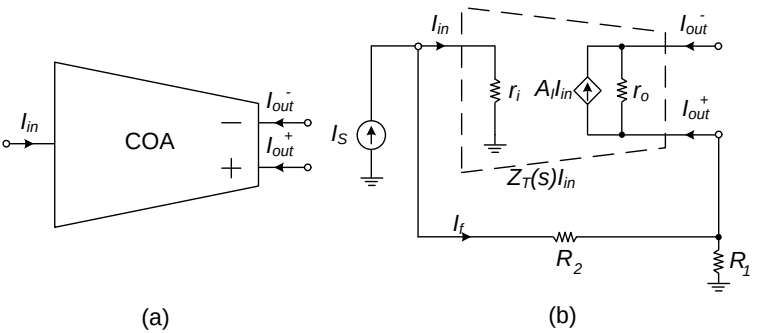

Figure 5.4. The COA: (a) symbol, (b) equivalent circuit with typical feedback configuration for accurate current gain.

5.2.2 The Voltage Feedback Current Operational Amplifier

Figure 5.5 shows the VFCOA's symbol and equivalent circuit with the feedback configuration used to achieve accurate current gain. The VFCOA can be modeled as a single-ended input differential-output current controlled current source, where the input and positive output terminal are low impedance nodes and the negative output terminal is a high impedance node.

The VFCOA can be represented with the block diagram in Figure 5.5(b) made up of a trans-impedance amplifier and a current follower. The trans-impedance amplifier converts the input current into a voltage, $Z_T(s)I_{in}$. The current follower senses the current driven by the trans-impedance amplifier and mirrors it to the negative output terminal.

The asymptotic gain, as in the case of the COA, is given by Equation (5.7). The return ratio is

$$T(s) = \frac{Z_T(s)R_1}{(R_2+r_i)(R_1+r_0^+)+R_1r_0^+} = \frac{Z_T(s)}{r_i+r_0^+G_\infty+R_2+\frac{r_ir_0^+}{R_2}(G_\infty-1)} \tag{5.11}$$

The forward gain G_o is lower than 1 and, being divided by 1+T in (5.6), is again negligible.

If $R_2,R_1>>r_i,r_0$, T(s) can be approximated as

$$T(s) = \frac{Z_T(s)}{R_2} \tag{5.12}$$

and the closed loop bandwidth ω_{CL} expressed as a function of the open loop bandwidth, ω_{OL}, is

$$\omega_{CL} \cong \big(1+T(0)\big)\omega_{OL} \cong T(0)\omega_{OL} = \frac{Z_T(0)\omega_{OL}}{R_2} \tag{5.13}$$

Comparing Equations (5.13) and (5.7), we see that while the asymptotic gain depends on both feedback network elements (R_1 and R_2), the closed loop bandwidth only depends on R_2. Therefore, this system behaves like a CFVOA with constant closed-loop bandwidth provided that different gains are set by changing R_1 alone.

Finally, it is worth mentioning that another advantage of VFCOAs is the possibility of using non-linear resistors in the feedback loop without worsening the linearity of the system [Mag94]. This is possible because the virtual ground at the input enforces equal voltage drops across both resistors, allowing cancellation of nonlinear terms.

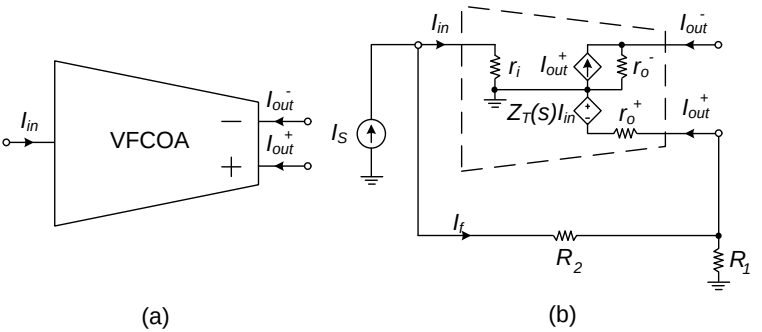

Figure 5.5. The VFCOA: (a) symbol, (b) equivalent circuit with typical feedback configuration for accurate current gain.

If the feedback resistors R_1 and R_2 are simultaneously changed in such a way that their ratio R_2/R_1 remains constant, the asymptotic gain (i.e., the ideal gain) in Equation (5.7) remains constant, but return ratio in Equation (5.12) goes through a maximum. This maximum occurs for two optimum values of R_1 and R_2 so that

$$R_{1,opt}R_{2,opt} = r_i r_0^+ \tag{5.14}$$

thus, evaluating R_2 from Equation (5.7) and substituting into Equation (5.14) we get

$$R_{1,opt} = \sqrt{\frac{r_i r_0^+}{G_\infty - 1}} \tag{5.15}$$

$$R_{2,opt} = \sqrt{r_i r_0^+ (G_\infty - 1)} \tag{5.16}$$

This means that for any G_∞ there is a different optimum setting of R_1 (and R_2). It is hence apparent that there is no possibility to set a constant R_2 for different G_∞ while maximizing the return ratio. Moreover, the resulting value of $R_{1,opt}$ is not practical because it is in general too small (for instance, if $r_i = r_o^+ = 50\Omega$ and $G_\infty = 11$, then $R_{1,opt}$ is around 16 Ω. Such low values are not convenient because a low R_1 value causes both poor matching with R_2 and large output offset current, V_{os}/R_1, where V_{os} is the input offset voltage.

The use of non-optimum resistances determines a return ratio reduction with respect to the maximum return ratio, $T_{MAX}(s)$,

$$T_{MAX}(s) = \frac{Z_T(s)}{r_i + r_0^+ G_\infty + 2\sqrt{r_i r_0^+ (G_\infty - 1)}} \tag{5.17}$$

given by

$$\frac{T(s)}{T_{MAX}(s)} = \frac{1 + \frac{r_0^+}{r_i} G_\infty + 2\sqrt{\frac{r_0^+}{r_i}(G_\infty - 1)}}{1 + \frac{r_0^+}{r_i} G_\infty + 1 + \frac{R_2}{r_i} + 1 + \frac{r_0^+}{R_2}(G_\infty - 1)} \tag{5.18}$$

Relationship (5.18) is plotted in Figure 5.6, where the reduction is expressed in dB versus R_2/r_i, for four different asymptotic gains ($r_i = r_o^+$ is assumed for simplicity).

As expected, the return ratio reduction, from its minimum value, increases with R_2/r_i and is greater for lower closed-loop gains. A tradeoff must hence be met to avoid excessive loop gain reduction while obtaining a nearly constant closed loop bandwidth. From Figure 5.6, it is seen that an acceptable maximum loop gain reduction less than 15 dB is obtained by choosing $R_2/r_i=20$ (for instance, if $r_i=50\Omega$, $R_2=1k\Omega$ can be set).

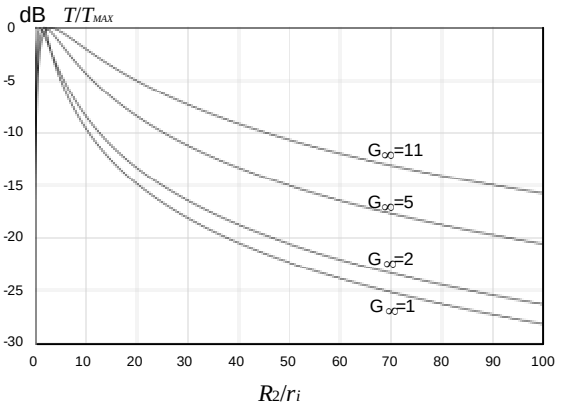

Figure 5.6. T/TMAX versus R2/ri for different values of G∞

5.3 Constant bandwidth variable gain voltage feedback current operational amplifier design

5.3.1 Block diagram

Figure 5.7 shows the block diagram of a VFCOA designed using the most versatile current mode circuit: the second generation current conveyor (CCII±) [Smi68, Sed70, Pal99]. As described in Chapter 3, it is a three terminal block whose mathematical relationship between the X, Y, and Z terminals is represented by the following equation.

$$\begin{pmatrix} i_y \\ v_x \\ i_z \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{pmatrix} \begin{pmatrix} v_y \\ i_x \\ v_z \end{pmatrix} \tag{5.19}$$

where $i_z = i_x$ and $i_z = -i_x$ represent the CCII+ and CCII-, respectively (note that positive currents are considered the ones "entering" into the node).

The trans-impedance amplifier is implemented by $CCII_1$+ and resistor R_T. Terminal Y_1 is connected to a proper DC voltage for biasing purposes (ground if a dual supply voltage is used), which is replicated at the virtual ground terminal X_1. The current entering terminal X_1 is mirrored to terminal Z_1. As Z_1 is connected to the compensation capacitor C_c and node Y_2 has very high impedance (ideally infinite, usually that of a MOS gate terminal), the Z_1 output current is driven to the parallel equivalent of the output impedance of Z_1, R_T and C_C. Considering dominant pole behavior in the $CCII_1$+, the voltage at node Z_1 is

$$v_{Z1}(s) = -I_{in} \frac{R_T}{1+sR_TC_C} \tag{5.20}$$

Subsequently, the voltage follower inside $CCII_2$± copies $V_{Z1}(s)$ from Y_2 to X_2. The cutoff frequency of this voltage follower sets the feedback-loop second pole, which should be much higher than the dominant pole in order to have enough phase margin and keep the loop stable. For this reason, $CCII_2$±'s voltage follower bandwidth becomes an important design parameter. The only way to achieve high current driving capability while maintaining low power consumption is using a class AB topology [Pal00b, Mit03].

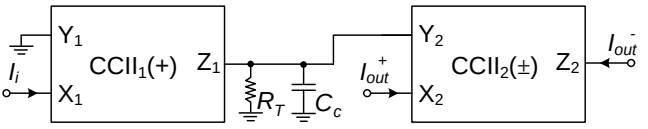

Figure 5.7. Block diagram of the VFCOA [Kau93].

5.3.2 Implementation

Figure 5.8 shows the class AB CCII+ implementation, based on the ideas described in Chapter 3. The circuit combines very low input impedance at node X, very high output impedance at node Z, ideally infinite input impedance at node Y, low power consumption and high linearity and current capability. The structure is based on the typical wide-swing cascode NMOS current mirror. Cascode configuration has been chosen because it increases both linearity and output resistance with respect to the non-cascode configuration. Although there are output stages capable of achieving higher output resistance and linearity [Pal00a, Esp12, Alo05], they are less power efficient.

The class AB operation is achieved transforming the PMOS static bias current circuit $M_{P1\text{-}2}$ into a quasi-floating gate (QFG) dynamic bias current mirror [Lop08]. The DC voltage at the gates of $M_{P1\text{-}3}$ is equal because there is no DC current going through capacitor C_{bat}, therefore, the DC voltage drop across R_{large} is zero. Thus in DC C_{bat} and R_{large} have no effect, and $M_{P1\text{-}2}$ act as conventional current sources of value I_B. This way the static currents are accurately set and can be made very low. Under dynamic operation, the voltage swing at $M_{N1\text{-}2}$'s gate is transferred to $M_{P1\text{-}2}$'s gate through the high pass filter formed by C_{bat} and R_{large}. Using the R_{large} implementation shown in the inset of Figure 5.8 (PMOS transistor in cutoff region) extremely high resistance values can be achieved, obtaining a cutoff frequency below 1 Hz. Thus in practice C_{bat} acts as a floating battery in AC, transferring any AC signal. This can lead to currents in M_{P2} much larger than I_B, achieving class AB operation. For more information about this technique the reader is referred to Chapters 2 and 3.

The error amplifier in the input loop, A, is used to create a virtual ground at the input X with DC input voltage accurately set by the DC voltage at node Y. Input resistance at node X and output resistance at node Z are given by

$$r_{inX} = g_{mCP1} r_{dsP1} r_{dsCP1} \| \frac{1}{A g_{mN1}} \cong \frac{1}{A g_{mN1}} \tag{5.21}$$

$$r_{outZ} = g_{mCN2} r_{dsN2} r_{dsCN2} || g_{mCP2} r_{dsP2} r_{dsCP2} \quad (5.22)$$

With suitable dimensioning and biasing, values around 50Ω and 10MΩ for r_{inX} and r_{outZ}, respectively, are easy to achieve. Figure 5.8 also shows how Miller compensation is employed to stabilize the loop.

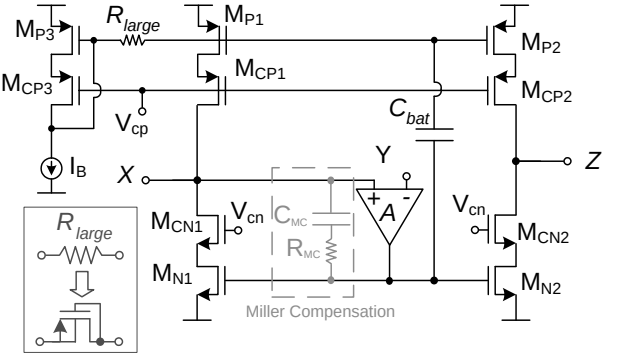

Figure 5.8. The class AB CCII+ [Lop08].

5.3.2.1 CCII$_1$+ implementation

The CCII$_1$+ should combine very low input resistance at node X (virtual ground condition, allowing minimum R_2 values), accurate DC voltage copy between Y and X (proper biasing and low offset voltage) and high output resistance (to achieve high trans-resistance gain). High current copy accuracy (enabling good linearity) is also needed but only for small currents. Figure 5.9 shows the adopted error amplifier implementation for the circuit of Figure 5.8. The well-known differential pair with active load has been chosen due to its simplicity and low current requirements. It provides a gain equal to $A = g_{mP5}(r_{dsP4}||r_{dsN3})$. Combining the amplifier gain with Equation (5.21) we obtain the VFCOA input resistance as

$$r_{in} = r_X = \frac{1}{g_{mN1} g_{mP5} (r_{dsP4}||r_{dsN3})} \quad (5.23)$$

It is important to highlight that in order to stabilize the input loop, Miller compensation (C_{MC}, R_{MC}) is used between the amplifier output and node X.

It is easy to see that the trans-resistance gain is

$$Z_T(s) = \frac{r_{outZ}}{1+sr_{outZ}C_C} \tag{5.24}$$

Where C_C is the compensation capacitor and r_{outZ} is the output resistance of the CCII given by Equation (5.22).

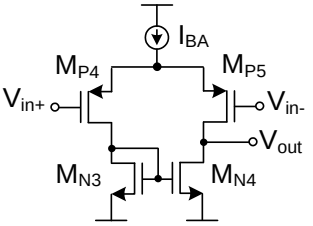

Figure 5.9. Implementation of CCII1+ error amplifier.

5.3.2.2 CCII$_2$+ implementation

In order to achieve a good performance, it is important that the CCII$_2$+ combines wideband voltage following capability between nodes Y and X (to avoid stability problems), very low input resistance at node X (allowing minimum R_1 and R_2 values), high current driving capability and linearity. The proposed CCII$_2$+ is the circuit of Figure 5.8 with the error amplifier implementation shown in Figure 5.10. The input loop amplifier is a common gate amplifier (M_{P7}) with gain $A = g_{mP7}(r_{dsP7}||r_{0B})/2$ where r_{0B} is the current source output resistance. Therefore, the positive output resistance of the implemented VFCOA is given by

$$r_{out}^{+} = r_{X2} = \frac{2}{g_{mN1}g_{mP7}(r_{dsP7}||r_{0B})} \tag{5.25}$$

M_{P6} is a DC level shifter and together with M_{P7} form a fast and accurate voltage follower between nodes Y_2 and X_2. As the current that flows across both transistors is equal, their gate voltage is also equal, and therefore, the voltage at node Y_2 is accurately copied to node X_2. This topology offers less gain than the differential pair and frequency compensation is not needed. The output resistance at node Z_2 is equal to that of the CCII+ described in Equation (5.22),

As stated before, using a CCII$_2$+ as output stage makes the overall system current gain DC A_{cl} to be negative (in sign). If input and output are intended to be in phase, the proposed CCII$_2$+ can be transformed into a CCII$_2$- inverting the output current.

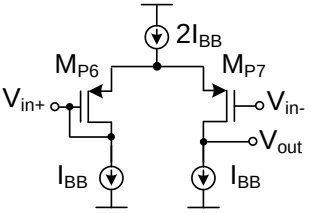

Figure 5.10. Implementation of CCII2+ error amplifier.

5.3.2.2 The feedback network

As mentioned above, it is possible to use non-linear elements in the feedback network without degrading the circuit linearity [13]. Figure 5.11 shows the feedback network used in this amplifier. Transistors M_{SW} are used as switches, while transistors $M_{PR1\text{-}2}$ are used as active resistors. If we compare Figure 5.11 and Figure 5.5(b) we see that R_1 and R_2 are implemented with M_{PR1} and M_{PR2} transistors respectively. If $M_{PR1\text{-}2}$ are matched and biased by V_R, their equivalent resistance $R(V_R)$ is equal. Therefore, $R_2 = R(V_R)$ and $R_1 = R(V_R)/n$, where n $(n \propto 0{:}N)$ is the number of M_{PR1} active transistors. If we substitute these relationships into Equations (5.7) and (5.13) the gain and closed loop bandwidth of the VFCOA are given by

$$G_\infty = 1 + \frac{R_2}{R_1} = 1 + \frac{nR(V_R)}{R(V_R)} = 1 + n \tag{5.26}$$

$$\omega_{CL} \cong T(0)\omega_{OL} = \frac{Z_T(0)\omega_{OL}}{R(V_R)} \tag{5.27}$$

From Equations (5.26) and (5.27) we see that the closed-loop gain depends solely on the number of active transistor while the closed loop bandwidth depends on the tuning voltage V_R. Therefore the possibility of having constant, but tunable, closed-loop bandwidth is achieved.

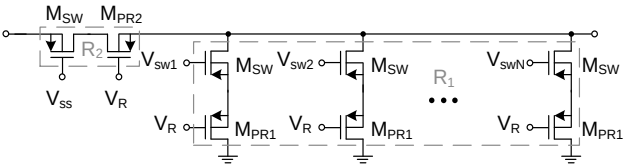

Figure 5.11. Adopted transistorized feedback network.

5.3.3 Measurement and simulation results

The proposed VFCOA has been fabricated in a 0.5-μm CMOS technology. C_{bat}, C_C and C_{MC} were implemented as poly-poly capacitors with a nominal value of 1pF, 18pF and 1.5pF respectively. Resistors R_{large} (M_{PR}) were implemented with minimum-size PMOS transistors (1.5μm/0.6μm) and R_{MC} has a nominal value of 2.5kΩ. The rest of the transistor's dimensions W/L (in μm/μm) were: 100/0.6 (M_{P1}, M_{P2}, M_{P3}, M_{CN1}, M_{CN2}) 200/0.6 (M_{CP1}, M_{CP2}, M_{CP3}), 60/1 (M_{N1}, M_{N2}, M_{N3}, M_{N4}), 100/1 (M_{P4}, M_{P5}), 50/0.6 (M_{SW}) and 13.5/1 (M_{PR1}, M_{PR2}).

Bias currents I_B, I_{BA} and I_{BB} have been implemented as wide swing cascode current sources with a nominal value of 10μA, 5 μA and 10μA, respectively. The supply voltage was 3.3V achieving a total static power consumption of 280.5μW. The total silicon area occupied by the whole circuit was 0.127mm^2, where the VFCOA and feedback network areas were 296×380 μm^2 and 285×50 μm^2, respectively. In Fig. 5.12 the VFCOA die microphotograph is shown.

Preliminary simulations showed a loop gain of 76 dB and gain-bandwidth product of 5.6 MHz with a phase margin of 60°. Input resistance was 53Ω and resistance R_2 was set nominally to 3500Ω.

Figure 5.13 shows the measured VFCOA's magnitude response for different gain configurations. As it can be seen, the amplification range goes from 0 up to 23.63 dB with the bandwidth ranging from 1.8 MHz to 2.9MHz for minimum and maximum gain respectively.

Figure 5.14 shows that the bandwidth can be tuned between 1 and 3 MHz using V_R. If lower/higher bandwidth values are needed, they can be easily achieved at the design stage by proper M_{PR} dimensioning. Although tunable bandwidth is not commonly employed in amplifiers, it can be used for instance in some low-cost low-power transceivers where a tunable bandwidth amplifier can help in the channel selectivity of the baseband section of the receiver, saving die area and power consumption.

The harmonic distortion for a 300-kHz input signal is shown for minimum and maximum gain in Figures 5.15 and 5.16 respectively (being the amplifier loaded with R_L=5.6 kΩ). As it can be seen, as usual in single-ended circuits, HD_2 dominates over HD_3. Class AB operation and high linearity can be

noticed by the fact that output total harmonic distortion is less than -40dB for output current amplitudes up to $5I_B$ for minimum gain and $23I_B$ in maximum gain configuration. Figure 5.17 shows the step response of the VFCOA for maximum and minimum gain. Finally, Table 5.1 reports a comparison of the circuit performance parameters with those of the other two existing fabricated designs reported. Note that due to the class AB operation, this proposal achieves similar settling performance with less power consumption. Table 5.2 shows additional measurement results.

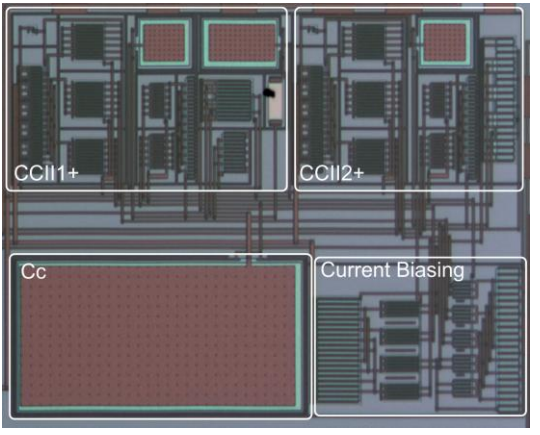

Figure 5.12. VFCOA die microphotograph.

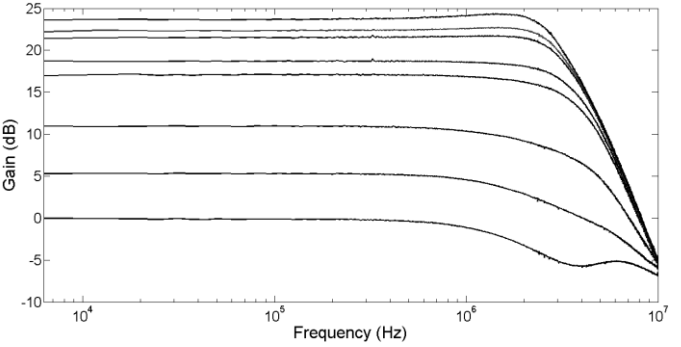

Figure 5.13. Measured magnitude response of the VFCOA.

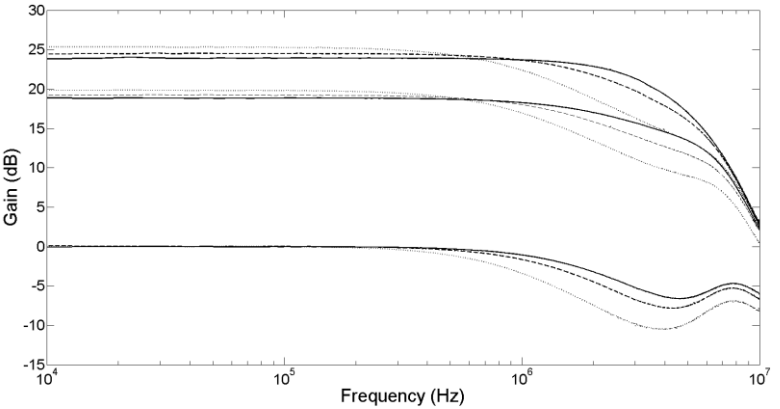

Figure 5.14. Measured magnitude response of the VFCOA for different bandwidths.

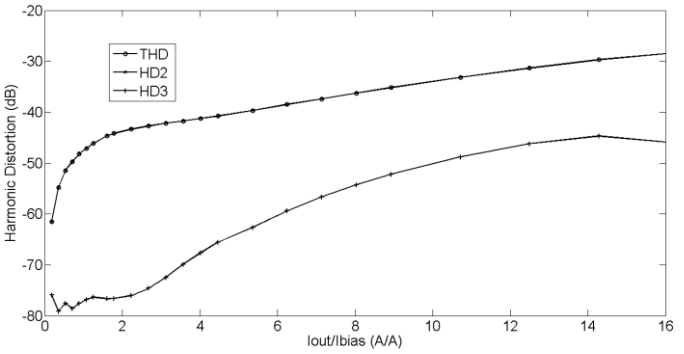

Figure 5.15. VCFOA measured harmonic distortion for 0 dB gain @300kHz.

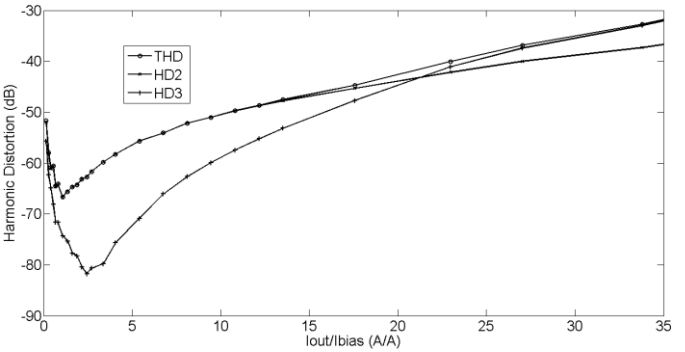

Figure 5.16. VFCOA measured harmonic distortion for 23.6 dB gain @300kHz.

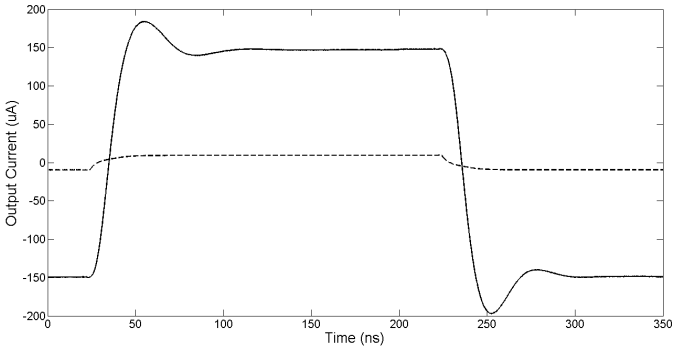

Figure 5.17. Measured VCFOA step response for minimum (dotted curve) and maximum gain (continuous curve).

Table 5.1. Performance comparison

	This work	[Pal98]	[Kau93]
CMOS Technology (μm)	0.5	1.2	2.4
Die Area (mm^2)	0.127	0.26	NA
Power Supply (V)	3.3	5	5
DC Power Consumption (μW)	280.5	4000	>1500
Open-Loop Gain (dB)	76*	100	72
GBW (MHz)	5.6*	10	3
Phase Margin (deg)	60*	>60	60
Output Load	5.6 kΩ	100 Ω	NA
IO,MAX (μA)	±500	±700	±700
IO,MAX /IStandby	58.8	8.75	<2.3
TSettl(0.1%), unity gain (ns)	47	165	35
SR, unity gain (μA/ns)	3.3	200	NA
Input noise voltage (nV/ √Hz)	0.54	7.5	NA
Output noise current (pA/ √Hz)	5.7 (1kΩ load)	20 (100Ω load)	NA
TSettl(0.1%)· IO,MAX /IStandby (ns)	2764	1443	<81
Die Area (mm2)	0.127	0.26	NA

* simulated results

Table 5.2. Summary of additional measured performance

	This work
BW Range (MHz)	1-3
Gain Range (dB)	0-23.6
0.1% Settling time, max gain (ns)	138.4
Slew rate, max gain (μA/ns)	28.4
$\Delta I_{out}/\Delta V_{DD}$, unity gain, @100kHz (μA/V)	24.6
$\Delta I_{out}/\Delta V_{SS}$, unity gain, @100kHz (μA/V)	27.3
IIP_3, unity gain (dBm)	29.3
P_{1dB}, unity gain (dBm)	10
IIP_3, max gain (dBm)	12.6
P_{1dB}, max gain (dBm)	-6.5
DR, THD@300kHz 1%, NBW 2.9MHz, max gain (dB)	87.5
DR, THD@300kHz 1%, NBW 1.7MHz, min gain (dB)	100.1

5.4 Conclusions

In this chapter, the gain-bandwidth product trade-off has been discussed. Afterwards, the current operational amplifier and the voltage feedback operational amplifier have been introduced. Finally, a class AB CMOS VFCOA that combines both variable gain and constant tunable bandwidth has been described, where the design strategy for the feedback resistors has also been discussed in detail. Measurement results confirm that the VFCOA is a versatile active block that can be used in high performance low power consumption current-mode circuit design. Measurement results show improved performance compared to similar circuits in literature.

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CHAPTER 6

Current mode detector design for ultra-low power receivers

The detector or demodulator block has a tremendous impact on the overall receiver design, as it determines the minimum signal to noise ratio (SNR) required at its input for a specific bit error rate (BER), directly influencing in the total receiver noise figure (NF) and gain requirements. It also determines if multibit analog-to-digital converters (ADCs) are needed, the gain control strategy, the tolerance to AC coupling in base band, and to other non-idealities such as I/Q mismatch errors.

As stated in chapter 1, the main objective of this work is to design the baseband chain of a Bluetooth 4.0 [Blu10] zero intermediate frequency (Zero-IF) receiver with a Gaussian Frequency Shift Keying (GFSK) modulation scheme.

There are several possibilities for zero-IF GFSK detection, from fully-analog to fully-digital implementations, and all in between. In general, fully-analog implementations suffer from high power consumption (in the order of several mW). On the other hand, All-Digital detectors are insensitive to mismatch, compact and efficient, but they usually require multibit ADCs operating at high speed and featuring high power consumption as well. Mixed-signal solutions can provide enough performance for this application with lower power consumption.

One important decision is whether to use amplitude limiters or not. Constant envelope modulations like GFSK allow using amplitude limiters before

detection, removing any amplitude modulation due to channel and receiver non idealities. Amplitude limiters also simplify the design of RSSI circuits and relax the receiver gain control as it has not to enforce a certain signal level at the detector input but to ensure that the receiver doesn't saturate. On the other hand, amplitude limiters cause odd order distortion, which can't be removed in zero-if receivers. Conventional cross-differentiate multiply detectors or limiter-discriminator detectors are very sensitive to this kind of distortion, becoming non-utilizable together with amplitude limiters. However, zero-crossing detectors are insensitive to odd order distortion, becoming an interesting alternative when using amplitude limiters. When amplitude limiters are not employed, accurate adaptive gain control (which requires a large amount of power) is required because the detector needs a constant level at its input.

Taking into consideration all the previous considerations, a zero-crossing detector has been selected as solution because it can lead to the most compact, cheaper and low power implementation.

This chapter is organized as follows. First, an overview of the GFSK modulation is given. Afterwards, some of the most common mixed-signal GFSK demodulators are briefly presented, followed by a detailed explanation of the adopted design, the zero-crossing detector. Next, the proposed zero-crossing detector implementation is shown. Finally, some conclusions are drawn.

6.1 The Gaussian Frequency Shift Keying Modulation

The Gaussian Frequency Shift Keying (GFSK) is a digital modulation method used in many wireless standards, being one of them Bluetooth. This modulation is a Frequency Shift Keying (FSK) modulation with its digital baseband input low pass filtered by a Gaussian shaped low pass filter. A GFSK signal at the receiver's input can be expressed as:

$$s(t) = \sqrt{2S}cos(\omega_{RF}t + \phi(t)) \tag{6.1}$$

where S is the mean signal power, $\omega_{RF} = 2\pi f_{RF}$ is the radian frequency of the transmitter oscillator, and $\phi(t)$ is the instantaneous phase deviation

$$\phi(t) = 2\pi f_d \int_{-\infty}^{t} m(t)dt \tag{6.2}$$

with f_d the frequency sensitivity of the GFSK modulator (in Hz/V assuming m(t) in Volts) and m(t) the modulating signal

$$m(t) = \sum_{n=-\infty}^{n=\infty} d_n g(t - nT) \tag{6.3}$$

where the data sequence is $\ldots d_{-2} d_{-1} d_0 d_1 d_2 \ldots$ with $d_n \epsilon \{-1,1\}$, T=1/R_b is the bit duration, and g(t) is the pulse shaping function. In GFSK, g(t) is a Gaussian pulse shape

$$g(t) = \frac{1}{\sqrt{2\pi}\delta T} e^{\frac{-t^2}{2\delta^2 T^2}} \tag{6.4}$$

with

$$\delta = \frac{\sqrt{ln2}}{2\pi BT} \tag{6.5}$$

and B the bandwidth of g(t). If the maximum value of |m(t)| is 1, then the maximum frequency deviation is f_d and the modulation index is defined as h=2f_dT=2f_d/R_b. In Bluetooth $0.28 \leq h \leq 0.35$ and BT = 0.5. The shift in $\phi(t)$ due to the bit d_k is:

$$\Delta\phi_k = \phi_k(kT) - \phi_k(kT - T) = 2\pi f_d \int_{kT}^{T} d_k g(t - kT) dt \tag{6.6}$$

Figure 6.1 shows the four possible phase paths in a GMSK phase trajectory during T seconds, being this phase shift bounded between π/6 and π/2.

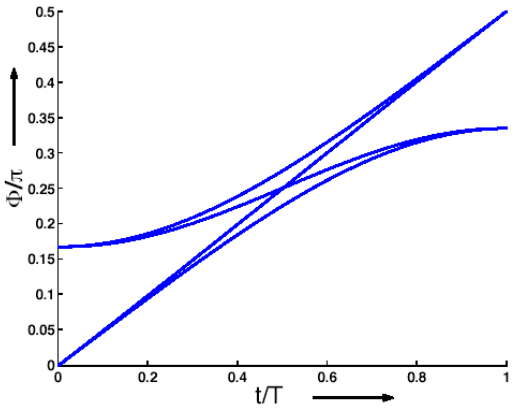

Figure 6.1. Four possible basic paths in the GMSK phase trajectory

After the RF processing, the incoming signal is mixed with the quadrature oscillator signals $2cos(\omega_{LO}t - \varphi)$ and $2sin(\omega_{LO}t - \varphi)$ and down-converted to baseband into the in phase I and in quadrature Q branches. Considering that $\omega_{RF} = \omega_{LO}$ the baseband signals are

$$i(t) = \sqrt{2S}cos(\phi(t) - \varphi) \tag{6.7}$$

$$q(t) = -\sqrt{2S}sin(\phi(t) - \varphi) \tag{6.8}$$

where the random constant φ reflects the phase incoherence between s(t) and the local oscillator. Once the signal is in baseband, the demodulator mission is to extract the phase $\phi(t)$ and demodulate it to get the original data sequence $\ldots d_{-2}d_{-1}d_0d_1d_2$ ....

The exact value of $\phi(t)$ is not needed to extract the message; it can be obtained calculating if $\phi(t)$ is increased or decreased over a bit period. An increase of $\phi(t)$ is a '1' and a decrease of $\phi(t)$ is a '0'. Therefore, the message can be extracted by calculating $d\phi(t)/dt$.

6.2 Low power phase detection demodulators

In this section some of the most commonly used low power GFSK demodulators are briefly presented. Next, the adopted architecture, named the zero-crossing detector, is explained in detail. The topologies shown don't include the RF or baseband processing parts; only the detector is shown for convenience.

6.2.1 The arctan-differentiated demodulator

The arctan-differentiated demodulator [Hag86] has been widely utilized in FM receivers. As shown in Figure 6.2, this architecture consist on dividing the inputs q(t) and i(t) obtaining $\tan(\phi(t))$. Afterwards, the $\tan^{-1}$ function extracts $\phi(t)$, which is derived and feed into the decision circuit. Although simple, this topology has some drawbacks such as saturation for low values of q(t) which were solved in [Hag85] and [Eis02].

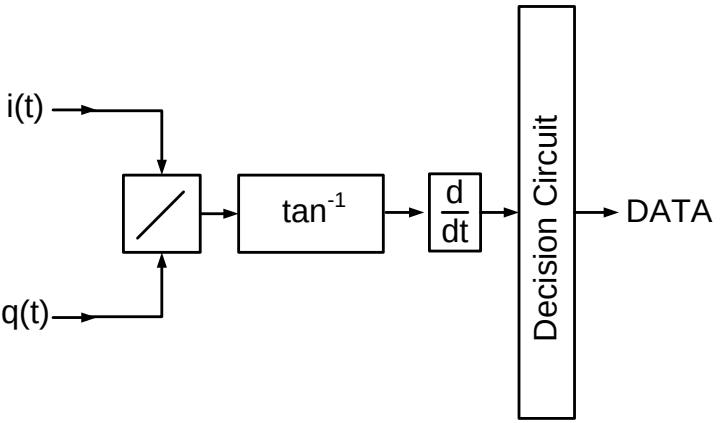

Figure 6.2. Conventional arctan-differentiated receiver

6.2.2 Correlation demodulator

The optimum FSK demodulator is the correlation detector [Pro00] shown in Figure 6.3. However, it is barely used in practical applications due to its complexity. The incoming signals are cross-correlated with the $S_{'1'}(t)$ and $S_{'0'}(t)$ functions, which are the modulated signals corresponding to the 1 and 0 symbols, respectively. Afterwards, the signals are squared and added. The decision circuits compare the '1' and '0' outputs and the larger value is selected as data. In [Min95] a new correlation type detector was proposed. This method avoids the use of multipliers (reducing the complexity of the system) using XNOR logic gates. Nevertheless, this receiver is very sensitive to oscillator frequency synchronization errors [Lop05].

6.2.3 Cross-difference multiply demodulator

The cross-differentiate multiply (CDM) demodulator has been widely used in industry, e.g., in pager applications. Figure 6.4 shows the conventional analog CDM demodulator and Figure 6.5 the digital CDM demodulator proposed in [Sai5]. The conventional analog architecture obtains $d\phi(t)/dt$ at the output using two integrators, 4 multipliers and a divider:

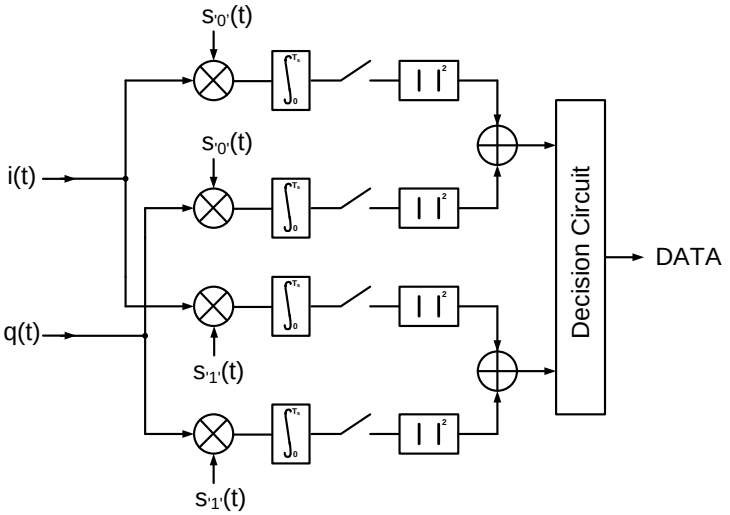

Figure 6.3. Conventional correlation demodulator

$$\frac{i(t)\frac{dq(t)}{dt}-q(t)\frac{di(t)}{dt}}{i(t)^2+q(t)^2}=\frac{d\phi(t)}{dt}\frac{2S\cos^2(\phi(t))+2S\sin^2(\phi(t))}{2S\cos^2(\phi(t))+2S\sin^2(\phi(t))}=\frac{d\phi(t)}{dt} \tag{6.9}$$

Note that if the output signal processor can demodulate $2S\frac{d\phi(t)}{dt}$ the divider and the squarer circuits can be removed as $\cos^2(\phi(t))+\sin^2(\phi(t))=1$.

The digital CDM demodulator output is the sign of $\Delta\phi(t)/\Delta t$. The amplifier limiters can be approximated as a signum (sgn) function. Remembering that the XOR function is '0' when both inputs are equal and '1' for different inputs, it is easy to see that the output of XOR_1 is '0' for $\frac{d\phi(t)}{dt}>0$ and '1' for $\frac{d\phi(t)}{dt}<0$. On the other hand, the output of XOR_2 is '1' for $\frac{d\phi(t)}{dt}>0$ and '0' for $\frac{d\phi(t)}{dt}<0$. Therefore, the demodulator output is '1' for $\frac{d\phi(t)}{dt}>0$ and '0' for $\frac{d\phi(t)}{dt}<0$, achieving a more simple accurate demodulator without multipliers or dividers.

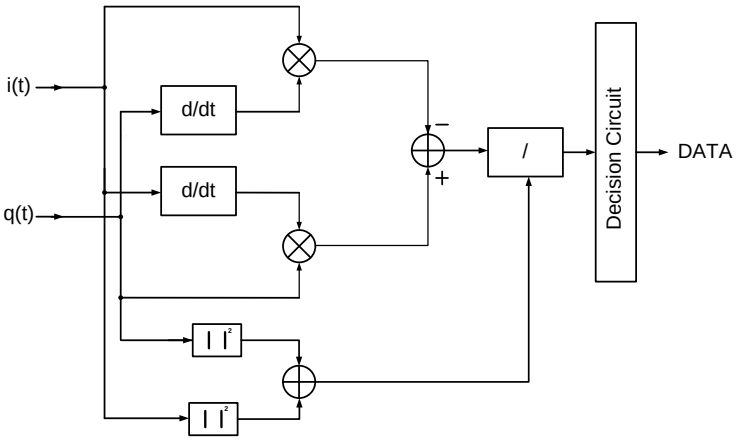

Figure 6.4. Analog cross-differentiate multiply demodulator

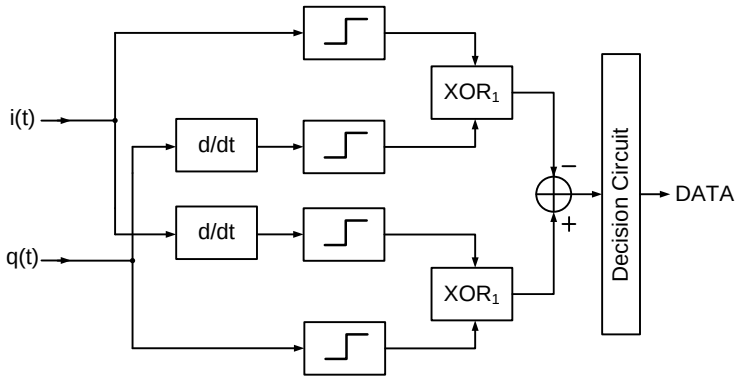

Figure 6.5. Digital cross-differentiate multiply demodulator

6.2.4 Zero-crossing detector

The zero-crossing detector [Lee94a,Lee94b,Kwo96] can estimate the instant phase of the incoming signal. Figure 6.6 depicts the IQ-plane representation of the phase modulated signal. The vertical and horizontal axes projection of this vector correspond to the i(t) and q(t) components, and its instantaneous angle with the horizontal axis is $\phi(t) - \varphi$. As stated before, it is not needed to extract the exact value of $\phi(t)$ but the direction of the phase shift, representing a positive shift a '1' and a negative shift a '0'.

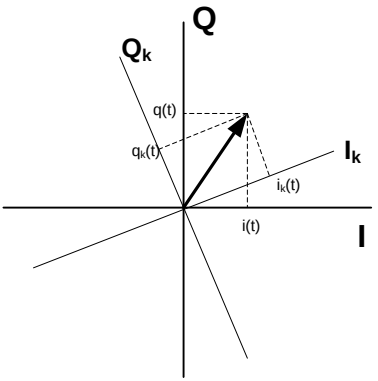

Figure 6.6. Vector representation of a phase modulated signal

Figure 6.7 represents the polarity of i(t) and q(t) when the signal vector is in each quadrant of the I/Q plane. When the signal vector changes from one quadrant to another i(t) or q(t) suffers a zero-crossing. Therefore, by detecting the zero-crossings the phase change can be estimated and the message recovered. Nevertheless, if the phase change for a bit period is less than $\pi/2$, the bit may not be correctly demodulated as the zero-crossing may not happen. In order to solve this problem a finer quantization of the instantaneous phase is required. This finer quantization improves the BER for a given SNR, but leads to a more complex implementation of the detector.

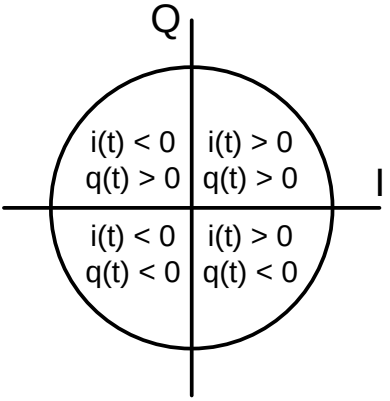

Figure 6.7. Polarity of i(t) and q(t) in each quadrant of the IQ-plane

Figure 6.8 shows a division of the instantaneous phase in 4*N sectors. Each sector is delimited by two axes $\pi/(2N)$ far apart, and each axis I_k and Q_k (k=0, 1, …N) is forming an angle $\theta_k = \pi k/2N$ with its fundamental axis. Therefore, the projection of the modulation vector on each axis is a linear combination of i(t) and q(t) given by

$$i_k(t) = i(t)cos\theta_k + q(t)sin\theta_k \tag{6.10}$$

$$q_k(t) = -i(t)sin\theta_k + q(t)cos\theta_k \tag{6.11}$$

Using Equations (6.10) and (6.11) it is possible to detect when the input vector crosses the axes between sectors, i.e. a cross through I_k happens for $q_k(t) = 0$. The direction of the crossing is determined by the sign of $i_k(t)$ and the sign change of $q_k(t)$.

As seen in Figure 6.1, in Bluetooth, GFSK phase shifts are between $\pi/6$ and $\pi/2$. A zero-crossing detector with N=4 detects shifts greater than $\pi/8$, being accurate enough for this application. Figure 6.9 shows a possible implementation of a detector based on this technique for N=4. First, the linear combiners generate the signals $i_k(t)$ and $q_k(t)$ (k=0,1,2,3) as in Equations (6. 10) and (6.11). Afterwards, these signals are feed into zero crossing detectors with amplitude hard-limiters, providing a digital output dependent of the input signal sign. This digital signal can be processed to obtain the transmitted message.

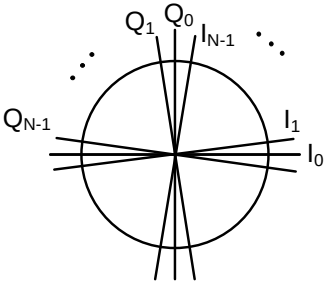

Figure 6.8. Quantization of the phase in the complex plane

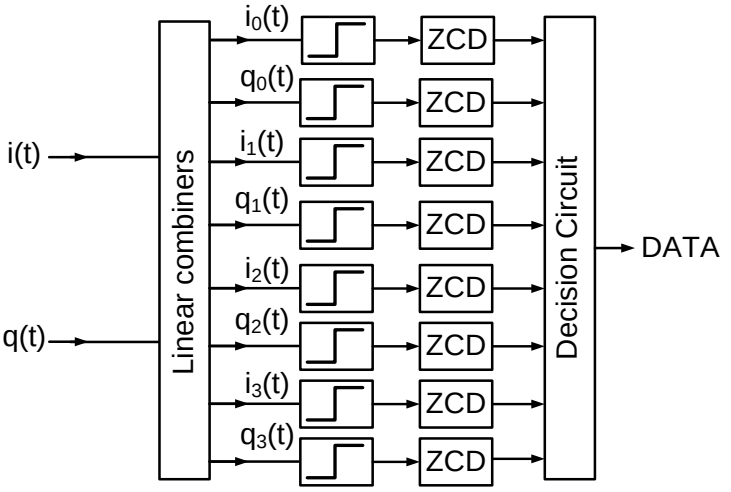

Figure 6.9 A possible implementation of the detector based on zero-crossings

6.3 Low power current mode zero-crossing detector design

In this section the implementation of the 4-axes zero-crossing detector shown in Figure 6.9 is presented.

6.3.1 The linear current combiner

The first step towards the receiver design is to expand Equations (6.10) and (6.11) transforming them into a more convenient form

$$i_0(t) = i(t) \tag{6.12}$$

$$i_1(t) = i(t)cos\frac{\pi}{8} + q(t)sin\frac{\pi}{8} = sin\frac{\pi}{8}(Ki(t) + q(t)) \tag{6.13}$$

$$i_2(t) = i(t)cos\frac{\pi}{4} + q(t)sin\frac{\pi}{4} = sin\frac{\pi}{4}(i(t) + q(t)) \tag{6.14}$$

$$i_3(t) = i(t)cos\frac{3\pi}{8} + q(t)sin\frac{3\pi}{8} = cos\frac{3\pi}{8}(i(t) + Kq(t)) \tag{6.15}$$

$$q_0(t) = q(t) \tag{6.16}$$

$$q_1(t) = -i(t)sin\frac{\pi}{8} + q(t)cos\frac{\pi}{8} = sin\frac{\pi}{8}(Kq(t) - i(t)) \tag{6.17}$$

$$q_2(t) = -i(t)sin\frac{\pi}{4} + q(t)cos\frac{\pi}{4} = sin\frac{\pi}{4}(q(t) - i(t)) \quad (6.18)$$

$$q_3(t) = -i(t)sin\frac{3\pi}{8} + q(t)cos\frac{3\pi}{8} = cos\frac{3\pi}{8}(q(t) - Ki(t)) \quad (6.19)$$

with $K = cos\frac{\pi}{8}/sin\frac{\pi}{8} = cos\frac{3\pi}{8}/sin\frac{3\pi}{8} \approx 2.4142$. As the receiver is based on detecting crossings by zero, the constant terms multiplying the linear combination of i(t) and q(t) are not important and don't need to be implemented.

The proposed way of implementing the current linear combiner is using class AB current mirrors, in particular the topology 1 dynamic cascode biasing class AB current mirror shown in Figure 3.2(a). This topology has been chosen because it features high linearity with very low power consumption and supply voltage requirements. For more information about this circuit the reader is referred to section 3.1.2. As seen in Equations (6.12)-(6.19) the currents that must be generated are:

- 3 times i(t)
- 2 times –i(t)
- 1 time Ki(t)
- 1 time –Ki(t)
- 5 times q(t)
- 2 times Kq(t)

Figures 6.10 show the schematic of the proposed current linear combiner. As it can be seen, the schematic is general. In the case of the i(t) linear combiner, the branch 1:1 has to be replicated 3 times, and the 1:-1 branch two times. In the q(t) current combiner, the 1:-1 and 1:-K branches are not needed, but the 1:1 and 1:K branches may be replicated 5 and 2 times respectively. Apart from this, some important points have to be highlighted.

The first one is related to the 1:K amplification. As it is well known, it is easy to amplify a current signal with current mirrors simply by making the relation between the output stage transistors dimensions and the input stage transistors dimensions equal to K: $(W/L)_{out}/(W/L)_{in}$ =K. Maintaining $L_{in}=L_{out}$ for convenience, W_{out}/W_{in} = K. In the used technology, the transistors width W = n*0.15μm with n an integer larger than 10. Therefore:

$$K = \frac{n_{out}}{n_{in}} \quad (6.20)$$

As K is equal to 2.41421356237… it has to be approximated by a fractional number. For very accurate results very big transistors have to be used, i.e. K=2.4142 = 408/169. For this implementation K=2.4 = 12/5 has been used, achieving a more compact implementation.

As seen in Figure 6.10 reversing a current with current mirrors is as easy as breaking the output stage into two output currents: the P current and the N current, which are fed into an N and P current mirror, respectively, connecting their outputs together to obtain the inverted output. Note that this current inverter stage is also made with regulated cascodes, using C_{batN2} and C_{batP2} quasi-floating gate capacitors.

Finally, as explained in section 3.1.2, the minimum quasi-floating gate capacitance is related to the parasitic capacitance at the quasi-floating gate node. As in these linear combiners several output stages have been cascaded, the parasitic capacitance is greater than in a regular 1 output stage current mirror. For this reason, the quasi-floating gate capacitances values have been increased. The drawback of this approach is that the current mirror bandwidth is reduced. The optimum value for these floating gate capacitances has been found through simulations.

The general structure of the proposed linear current combiner implementation is shown in Figure 6.10. The current inversion is done as explained previously. Note that this current inverter stage is also made with regulated cascodes, using C_{batN2} and C_{batP2} quasi-floating gate capacitors.

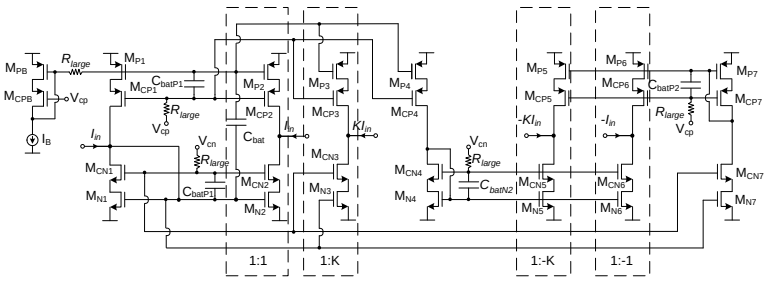

Figure 6.10 Linear current combiner

6.3.2 The amplitude limiter / zero crossing detector

Once $q_i(t)$ and $i_i(t)$ (i=0,1,2,3) are generated at the linear current combiners, the final stage is to detect these signals' crosses by zero and the direction of the cross. As seen in Figure 6.9, this can be done using an amplitude limiter followed by a zero crossing detector. Both of these functions can be implemented using current comparators.

The conventional current comparator used [Tra92] is shown in Figure 6.11. The operation of this circuit is very simple. The input stage is formed by a class AB source-follower (M_{Na} and M_{Pa}) forming a positive feedback loop with the CMOS inverter (M_{Nb} and M_{Pb}). Although this configuration achieves very low input resistance and short response time, it has a deadband for small input signals where both M_{Na} and M_{Pa} transistors are turned off, worsening the dynamic response. This problem was solved by [Tan94, Min98, Che00] at a cost of increasing the circuit complexity, voltage supply and current consumption. As those are the main goals of this work, these implementations are discarded.

Other commonly used current comparator is the current mirror shown in Figure 3.1(a). This circuit can be biased with very small bias currents achieving a very compact, power efficient and low voltage current comparator. Nevertheless, the input resistance of this solution is larger than in [Tra92], and its slew rate is limited by the bias current.

In this work the adopted solution has been the simple class AB current mirror from figure 3.1(b). As this circuit is dynamically biased, its slew rate is much larger than the conventional class A current mirror, achieving a faster response. By dimensioning the transistors with their minimum dimensions, the circuit saturates for small input currents, acting as an amplitude limiter. As the output stage is connected to a high impedance node (voltage sensor) the input current is mirrored to the equivalent output resistance of the output stage, saturating close to $-V_{DD}$ and $+V_{DD}$ for small positive and negative currents respectively, achieving therefore accurate zero crossing detection.

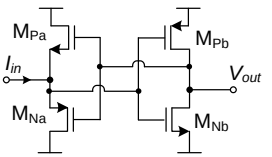

Figure 6.11 Conventional current comparator [TRA92]

6.4 Current operational amplifiers

The proposed zero-crossing demodulator has been fabricated in a 0.5-μm CMOS technology. In the linear combiners, C_{bati}, C_{batP1i}, C_{batP2i}, C_{batN1i}, C_{batN2i}, C_{batq}, C_{batP1q}, and C_{batN1q} were implemented as poly-poly capacitors with a nominal value of 4pF, 2pF, 2pF, 1pF, 1pF, 5pF, 2pF and 2pF respectively. In the current comparators C_{bat} was implemented as well as a poly-poly capacitor with a nominal value of 0.5pF. Resistors R_{large} (M_{PR}) were implemented with minimum-size PMOS transistors (1.5μm/0.6μm). In the linear combiners, the transistor's dimensions W/L (in μm/μm) were: 99.75/0.6 (M_{PB}, M_{P1}, M_{P2}, M_{P4}, M_{P6}, M_{P7}, M_{CN1}, M_{CN2}, M_{CN4}, M_{CN6}, M_{CN7}) 199.5/0.6 (M_{CPB}, M_{CP1}, M_{CP2}, M_{CP4}, M_{CP6}, M_{CP7}), 60/1.05 (M_{N1}, M_{N2}, M_{N4}, M_{N6}, M_{N7}), 239.4/0.6 (M_{P3}, M_{P5}, M_{CN3}, M_{CN5}), 478.8/0.6 (M_{CP3}, M_{CP5}), 144/1.05 (M_{N3}, M_{N5}). In the current comparators all transistors are minimum length transistors (1.5 μm /0.6 μm)

The bias currents I_B have been implemented as wide swing cascode current sources with a nominal value of 10μA and 500nA for the current linear combiners and current comparators, respectively. The supply voltage was 1.5V achieving a total static power consumption of 404.4 μW. The total silicon area occupied by the whole circuit was 0.2415mm^2. In Figure 6.12 the zero-crossing detector die microphotograph is shown.

The Cadence design kit used in this work doesn't provide digital modulated signals, for this reason system level simulations are very complex to do. To verify that the system demodulates GFSK signals correctly, a GFSK modulated signal was generated in Matlab. Afterwards, this signal was imported into cadence, and the simulation was performed. The output signal was processed in Matlab obtaining the original message without errors. Although a SNR vs BER simulation was intended to be done, due to computer limitations it was impossible be performed. At the time of the thesis writing, the chip was not measured, but it is expected that measurement results are provided at the thesis dissertation.

As a general statement, the linear combiner should be very linear so the zero crosses of $i_i(t)$ and $q_i(t)$ (i=0,1,2,3) are where they should be. The zero crossing detectors may be accurate and fast. To test the proper functioning of the circuit, several simulations were done.

Figure 6.13 shows the total harmonic distortion for the linear current combiner inverted and non-inverted outputs. As it can be seen, both outputs are

very linear even for very high input currents. Figure 6.14 shows the IM3 value for varying input amplitude for the i(t) linear current combiner. Note that for the q(t) linear current combiner the results are similar to the 1:1 and 1:K branches of the i(t) linear current combiner.

A comparison between the performances of the current comparators for large input currents is shown in Figures 6.15 and 6.16. As it can be seen, the class AB current mirror is way faster than the others in negative zero crossing and only a little slower in the positive zero crossing detection. For small inputs (<1uA), [Tra92] circuit doesn't work properly, while the proposed class AB current mirror detects zero-crossings even for very small signals.

Finally, Figure 6.17 shows the zero-crossing detectors output signals for $i(t) = \cos(2\pi ft)$ and $q(t) = \sin(2\pi ft)$ with f=100KHz. As it can be seen, the input signal phase is accurately detected for $\pi/8$ steps. Although i(t) and q(t) are currents, and they are not in scale, they have been introduced into the Figure 6.17 for clarity.

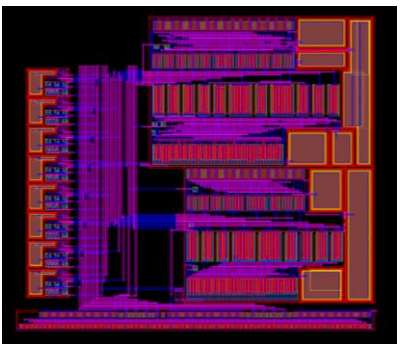

Figure 6.12. Zero-crossing detector die microphotograph

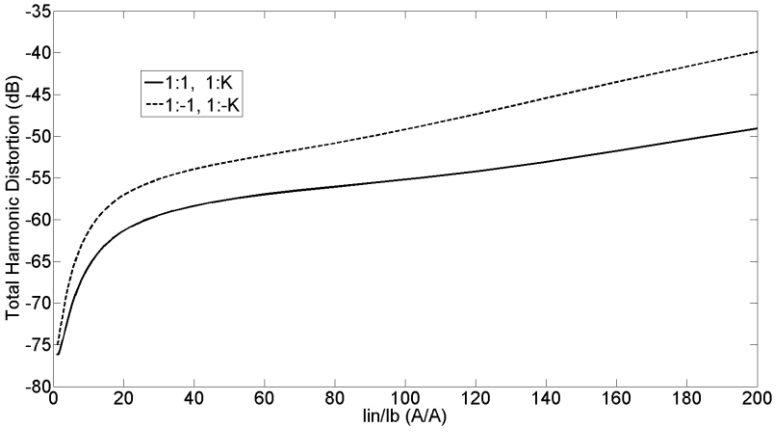

Figure 6.13. i(t) linear current combiner total harmonic distortion

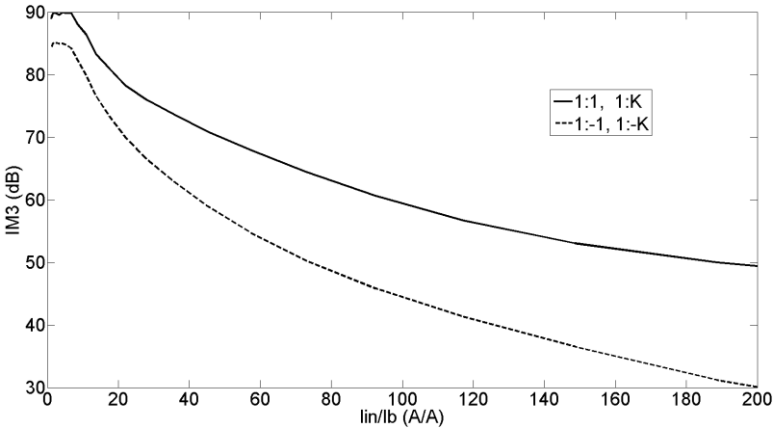

Figure 6.14. i(t) IM3 for 75kHz and 125kHz input sinusoidal signals

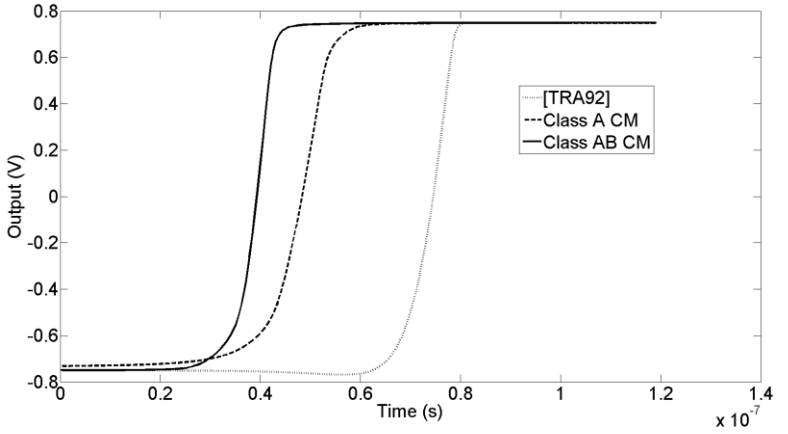

Figure 6.15. Current comparator simulated performance for negative zero crossing of a 100uA@100kHz sinusoidal signal (a) Conventional [TRA92] (b) Class A current mirror (c) Class AB current mirror

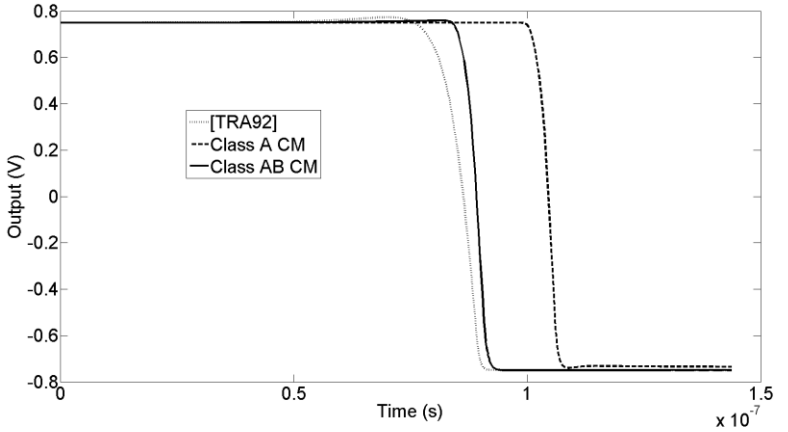

Figure 6.16. Current comparator simulated performance for positive zero crossing of a 100uA@100kHz sinusoidal signal (a) Conventional [TRA92] (b) Class A current mirror (c) class AB current mirror

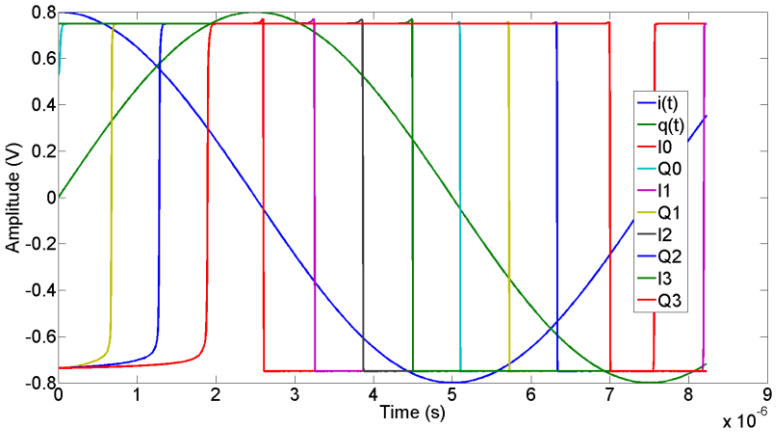

Figure 6.17. Linear current combiner simulated outputs

6.5 Conclusions

In this chapter a novel zero crossing detector implementation for Bluetooth 4.0 zero-IF receivers has been introduced. The circuit, which operates with 1.5V supply voltage, is based on class AB current mirrors, has been validated through simulations combining very low power consumption and good performance. The circuit has been fabricated in 0.5um CMOS technology and the measurement results are expected to be presented during the thesis dissertation.

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CHAPTER 7

Conclusions and future work

The most significant results of this thesis are overviewed during this chapter. Section 7.1 provides a compilation of the main contributions of this work and validates the fulfillment of the objectives proposed in Chapter 1. Afterwards, section 6.2 explores the future research trends related to this thesis.

7.1 Conclusions

The motivation behind this work has been the increasing number of wireless communication systems limited by battery life issues, and the growing integration factor of electronic circuits which forces the voltage supply to be reduced. In order to address this problem, this work has been focused on the design of analog current-mode low voltage low power circuits for the backend for zero-IF receivers, specifically in baseband amplification, filtering, and detection stages.

Chapters 1 and 2 have been centered on the why's and how's of this work, respectively. The questions behind the motivation of this thesis were replied first, i.e. why current-mode low power low voltage analog design?. Afterwards a brief review about the most common short distance low-power wireless communication standards and their most used receiver architectures (the

low-IF and the zero-IF receivers) was done. Chapter 2 explained the insights of Floating and Quasi-Floating Gate devices, followed by low power and low voltage the techniques that are employed during the following chapters: class AB operation, dynamic cascode biasing, sub threshold operation and companding.

After these introductory chapters, the real contributions take place. First, Chapter 3 has presented different implementations for the two basic current-mode cells (current mirror and current conveyor), focusing on both low-voltage low-power and high performance operation. Next, the proposed designs for the filtering, amplification and detection stages in Chapters 4, 5 and 6, respectively, have been shown.

Chapter 4 has addressed the design of ultra low power tunable current mode filters for channel selection. The proposed filter operates in the sinh domain using Floating Gate, companding and sub-threshold operation techniques. Measurement results show a better figure of merit than the state of the art and validate the design for multi-standard operation due to its tunability and micropower operation.

A current-mode constant bandwidth variable gain amplifier design has been shown in Chapter 5. The proposed amplifier is also valid for multi-standard operation due to its bandwidth tunability. The amplifier, composed by class AB second generation current conveyors, avoids the constant gain-bandwidth product issue being its bandwidth constant for the different gain configurations.

Finally, Chapter 6 presents the design of a current-mode low-power zero-crossing detector. After explaining Gaussian frequency shift keying modulation and the state of the art in low power phase detection demodulators, the proposed design is shown. The circuit, validated with simulation results, makes uses of different class AB current mirrors configured as linear current combiners and current comparators to implement the zero-crossing detection architecture.

7.2 Future Work

Even though this thesis has treated different threads in cell and system design, much work in both worlds is still to be made.

In the cell domain, much research can be done looking for more efficient implementations of class AB current mirrors and current conveyors.

Moreover, it would be very interesting to re-design and validate the proper function of the proposed designs in newer technologies with remarkable short-channel effects. After this experiment, the usability of the quasi floating and floating gate techniques in the future could be taken into consideration.

At system level, there are several things to be done. The filtering topic can be extended in several ways. First, the possibility of designing higher order architectures simply by cascading stages to achieve higher selectivity can be explored. Other kind of filters such as high pass filters or band pass filters can also be designed using a similar topology. On top of that, it would be interesting to implement a filtering with amplification stage, as shown in [Kat08]. Besides of that, an automatic frequency-tuning system could be implemented.

The proposed current-amplifier can be improved by combining it with an automatic gain control circuit and an automatic frequency-tuning system. The possibility of using this device as a single stage backend filter/amplifier for very low cost transceiver implementation can be explored as well.

The current mode zero-crossing detector has to be validated with measurements with different phase modulations.

Finally, it would be very interesting to implement the whole receiver backend in a single chip and test its viability in a multi-standard zero-if low power receiver.

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List of Publications

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3. F. Esparza-Alfaro, A. J. Lopez-Martin, R. G. Carvajal and J. Ramirez-Angulo, "Highly linear micropower class AB current mirrors using Quasi-Floating Gate transistors," *Microelectronics Journal*, in Press, pp. 1-7, 2014.

4. F. Esparza-Alfaro, A. J. Lopez-Martin, J. Ramirez-Angulo and R. G. Carvajal, "Low-voltage highly-linear class AB current mirror with dynamic cascode biasing," *Electronics Letters*, vol. 48, no. 31, pp. 1336-1338, 2012.

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1. F. Esparza-Alfaro, A. J. Lopez-Martin, R. G. Carvajal and J. Ramirez-Angulo, "Low-Voltage Highly-Linear Class AB current mirror with dynamic cascode biasing," Conference on Design of Circuits and Integrated Systems (DCIS), Avignon, France, 2012.

2. F. Esparza-Alfaro, A. J. Lopez-Martin, R. G. Carvajal and J. Ramirez-Angulo, "Power-Efficient High-Performance class AB current mirror," Conference on Design of Circuits and Integrated Systems (DCIS), Albufeira, Portugal, 2011.

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