Low-Power Class-AB CMOS Voltage Feedback Current Operational Amplifier with Tunable Gain and Bandwidth

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***Abstract*— A CMOS class AB variable gain Voltage Feedback Current Operational Amplifier (VFCOA) is presented. The implementation is based on class AB second generation current conveyors and exploits an electronically tunable transistorized feedback network. The circuit combines high linearity, low power consumption and variable gain range from 0 to 24 dB with nearly constant bandwidth, tunable from 1 to 3 MHz. A prototype has been fabricated in a 0.5-µm technology and occupies a total area of 0.127 mm^2. The VFCOA operates using a 3.3-V supply with static power consumption of 280.5µW. Measurements for maximum gain configuration show a dynamic range (1% THD@300kHz) of 87.5 dB and a THD lower than -40dB for an output current 23 times the bias current.**

***Index Terms*— CMOS analog integrated circuits, voltage feedback operational amplifier, current mode, class AB, current amplifier, quasi-floating gate transistor, current mirror, current conveyor, operational amplifiers.**

I. Introduction

The most popular analog building block is the Voltage Operational Amplifier (VOA). Because of the wide variety of achievable transfer functions, it is used to implement high complexity circuits such as filters, amplifiers, A/D and D/A converters, V-I/I-V converters, etc. [1]-[3]. When designing wideband circuits, the main VOA limitation is its constant gain-bandwidth product. On the other hand, the Current Feedback Voltage Operational Amplifier (CFVOA) has constant bandwidth independent of the gain [4]-[7].

Since some sensors and transducers provide an output signal in current form, it is desirable in these cases to process the signal directly in the current mode (CM) domain. High-performance implementations of the CM equivalents of the VOA and CFVOA, (named Current operational amplifier, COA [8]-[9] and Voltage Feedback Current Operational Amplifier, VFCOA [10]-[12], respectively) are therefore required. Note that being COAs the CM counterpart of VOAs, they are still bounded to the constant gain bandwidth product. Instead, the VFCOA combines the constant bandwidth property with the possibility of using non-linear resistors in the feedback loop without penalty in the overall circuit linearity [13], becoming a very interesting option for designing wideband circuits.

In this paper a novel low-power class AB VFCOA with transistorized feedback network is presented. Section II introduces its basic operation. The proposed implementation is shown in Section III, followed by the experimental results in Section IV. Conclusions are drawn in Section V.

II. Voltage Feedback Current Operational Amplifier

A. General considerations

The VFCOA can be modeled as a single-ended input differential-output current controlled current source, where the input and positive output terminal are low impedance nodes and the negative output terminal is a high impedance node. Fig. 1 shows the VFCOA's symbol and equivalent circuit with the feedback configuration used to achieve accurate current gain. Main properties of this amplifier will be outlined below.

The VFCOA can be represented with the block diagram in Fig. 1b made up of a trans-impedance amplifier and a current follower. The transimpedance amplifier converts the input current into a voltage, $Z_T(s)I_{in}$. The current follower senses the current driven by the transimpedance amplifier and mirrors it to the negative output terminal.

According to the Rosenstark formulation [14], the exact closed-loop current gain, G_F, is related to the *return ratio*, T, the *asymptotic gain*, G_∞, and the *direct transmission gain*, G_o:

$$G_F = G_\infty \frac{T}{1+T} + G_o \frac{1}{1+T} \tag{1}$$

All these quantities must be calculated with respect to one controlled source within the feedback amplifier (in this case the current controlled voltage source). The asymptotic gain, G_∞, is given by

$$G_\infty = \left.\frac{i_{out}^+}{i_{in}}\right|_{Z_T\to\infty} = 1 + \frac{R_2}{R_1} \tag{2}$$

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where R_1 and R_2 are the feedback network resistors.

The return ratio T results to be

$$T(s)=\frac{Z_T(s)R_1}{(R_2+r_i)(R_1+r_o^+)+R_1r_0^+}= \\ =\frac{Z_T(s)}{r_i+r_o^+G_\infty+R_2+\frac{r_ir_o^+}{R_2}(G_\infty-1)} \tag{3}$$

The forward gain G_o is lower than 1 and, being divided by $1+T$ in (1), is negligible.

If $R_1, R_2 >> r_i, r_0^+$, $T(s)$ can be approximated as

$$T(s)\cong\frac{Z_T(s)}{R_2} \tag{4}$$

and the closed loop bandwidth ω_{CL} expressed as a function of the open loop bandwidth, ω_{OL}, is

$$\omega_{CL}\cong(1+T(0))\omega_{OL}\cong T(0)\omega_{OL}=\frac{Z_T(0)\omega_{OL}}{R_2} \tag{5}$$

Comparing (2) and (5), we see that while the asymptotic gain depends on both feedback network elements (R_1 and R_2), the closed loop bandwidth only depends on R_2. Therefore, this system behaves like a CFVOA with constant closed-loop bandwidth provided that different gains are set by changing R_1 alone.

Finally, it is worth mentioning that another advantage of VFCOAs is the possibility of using non-linear resistors in the feedback loop without worsening the linearity of the system [13]. This is possible because the virtual ground at the input enforces equal voltage drops across both resistors, allowing cancellation of nonlinear terms.

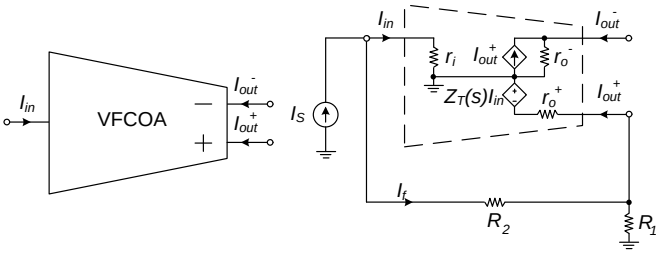

Fig. 1. The VFCOA: (a) symbol, (b) equivalent circuit with typical feedback configuration for accurate current gain.

B. Feedback resistors design

If the feedback resistors R_1 and R_2 are simultaneously changed in such a way that their ratio R_2/R_1 remains constant, the asymptotic gain (i.e., the ideal gain) in (2) remains constant, but return ratio in (3) goes through a maximum. This maximum occurs for two optimum values of R_1 and R_2 so that

$$R_{1,opt}R_{2,opt}=r_ir_0^+ \tag{6}$$

thus, evaluating R_2 from (2) and substituting into (6) we get

$$R_{1,opt}=\sqrt{\frac{r_ir_o^+}{G_\infty-1}}\ \text{and}\ R_{2,opt}=\sqrt{r_ir_o^+(G_\infty-1)} \tag{7}$$

This means that for any G_∞ there is a different optimum setting of R_1 (and R_2). It is hence apparent that there is no possibility to set a constant R_2 for different G_∞ while maximizing the return ratio. Moreover, the resulting value of $R_{1,opt}$ is not practical because it is in general too small (for instance, if $r_i = r_o^+ = 50\Omega$ and $G_\infty = 11$, then $R_{1,opt}$ is around 16 Ω[1].

The use of non optimum resistances determines a return ratio reduction with respect to the maximum return ratio, $T_{MAX}(s)$,

$$T_{MAX}(s)=\frac{Z_T(s)}{r_i+r_o^+G_\infty+2\sqrt{r_ir_o^+(G_\infty-1)}} \tag{8}$$

given by

$$\frac{T(s)}{T_{MAX}(s)}=\frac{1+\frac{r_o^+}{r_i}G_\infty+2\sqrt{\frac{r_o^+}{r_i}(G_\infty-1)}}{1+\frac{r_o^+}{r_i}G_\infty+\frac{R_2}{r_i}+\frac{r_o^+}{R_2}(G_\infty-1)} \tag{9}$$

Relationship (9) is plotted in Fig. 2, where the reduction is expressed in dB versus R_2/r_i, for four different asymptotic gains ($r_i = r_o^+$ is assumed for simplicity).

As expected, the return ratio reduction, from its minimum value, increases with R_2/r_i and is greater for lower closed-loop gains. A tradeoff must hence be met to avoid excessive loop gain reduction while obtaining a nearly constant closed loop bandwidth. From Fig. 2, it is seen that an acceptable maximum loop gain reduction less than 15 dB is obtained by choosing R_2/r_i=20 (for instance, if r_i=50Ω, R_2=1kΩ can be set).

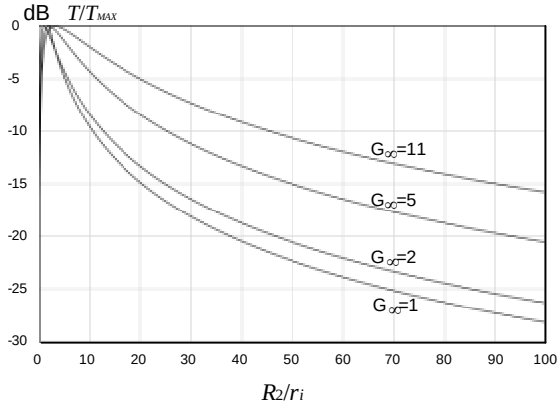

Fig. 2. T/T_{MAX} versus R_2/r_i for different values of G_∞

III. The Designed Circuit

A. Block diagram

Fig. 3 shows the block diagram of a VFCOA designed using the most versatile current mode circuit: the second generation current conveyor (CCII±) [15]-[17], a three port network whose mathematical relationship between the X,Y, and Z terminals is represented by the following equation.

$$\begin{pmatrix}I_Y\\V_X\\I_Z\end{pmatrix}=\begin{pmatrix}0&0&0\\1&0&0\\0&\pm1&0\end{pmatrix}\begin{pmatrix}V_Y\\I_X\\V_Z\end{pmatrix} \tag{10}$$

where $I_Z=+I_X$ and $I_Z=-I_X$ represent the CCII+ and

[1] A low R_1 value causes both poor matching with R_2 and large output offset current, V_{os}/R_1, where V_{os} is the input offset voltage.

CCII-, respectively (note that positive currents are considered the ones "entering" into the node).

The transimpedance amplifier is implemented by $CCII_1$+ and resistor R_T. Terminal Y_1 is connected to a proper DC voltage for biasing purposes (ground if a dual supply voltage is used), which is replicated at the virtual ground terminal X_1. The current entering terminal X_1 is mirrored to terminal Z_1. As Z_1 is connected to the compensation capacitor C_c and node Y_2 has very high impedance (ideally infinite, usually that of a MOS gate terminal), the Z_1 output current is driven to the parallel equivalent of the output impedance of Z_1, R_T and C_C. Considering dominant pole behavior in the $CCII_1$+, the voltage at node Z_1 is

$$V_{Z1}(s) = -I_{in}\frac{R_T}{1+sR_TC_C} \tag{11}$$

Subsequently, the voltage follower inside $CCII_2\pm$ copies $V_{Z1}(s)$ from Y_2 to X_2. The cutoff frequency of this voltage follower sets the feedback-loop second pole, which should be much higher than the dominant pole in order to have enough phase margin and keep the loop stable. For this reason, $CCII_2\pm$'s voltage follower bandwidth becomes an important design parameter. The only way to achieve high current driving capability while maintaining low power consumption is using a class AB topology [18], [19].

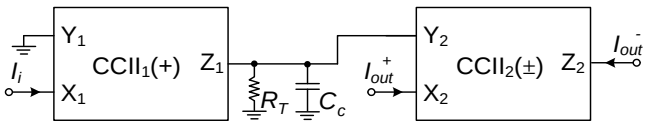

Fig. 3. Block diagram of the VFCOA [11].

B. Implementation

Fig. 4 shows the class AB CCII+ implementation. It was presented as a current mirror in [20], but it will be shown that it can also be used as a CCII+. The circuit combines very low input impedance at node X, very high output impedance at node Z, ideally infinite input impedance at node Y, low power consumption and high linearity and current capability. The structure is based on the typical wide-swing cascode NMOS current mirror, which was chosen since it increases both linearity and output resistance. Although there are output stages capable of achieving higher output resistance and linearity [8], [21], [22], they are less power efficient.

The class AB operation is achieved transforming the PMOS static bias current circuit $M_{P1\text{-}2}$ into a quasi-floating gate (QFG) dynamic bias current mirror [20]. The DC voltage at the gates of $M_{P1\text{-}3}$ is equal because there is no DC current going through capacitor C_{bat}, therefore, the DC voltage drop across R_{large} is zero. Thus in DC C_{bat} and R_{large} have no effect, and $M_{P1\text{-}2}$ act as conventional current sources of value I_B. This way the static currents are accurately set and can be made very low. Under dynamic operation, the voltage swing at $M_{N1\text{-}2}$'s gate is transferred to $M_{P1\text{-}2}$'s gate through the high pass filter formed by C_{bat} and R_{large}. Using the R_{large} implementation shown in the inset of Fig. 4 (PMOS transistor in cutoff region) extremely high resistance values can be achieved, obtaining a cutoff frequency below 1 Hz. Thus in practice C_{bat} acts as a floating battery in AC, transferring any AC signal. This can lead to currents in M_{P2} much larger than I_B, achieving class AB operation. For more information about this technique the reader is referred to [20].

The error amplifier in the input loop, A, is used to create a virtual ground at the input X with DC input voltage accurately set by the DC voltage at node Y. Input resistance at node X and output resistance at node Z are given by

$$r_{inX} = g_{mCP1}r_{dsP1}r_{dsCP1} \parallel \frac{1}{Ag_{mN1}} \cong \frac{1}{Ag_{mN1}} \tag{12}$$

$$r_{outZ} = g_{mCN2}r_{dsN2}r_{dsCN2} \parallel g_{mCP2}r_{dsP2}r_{dsCP2} \tag{13}$$

With suitable dimensioning and biasing, values around 50Ω and 10MΩ for r_{inX} and r_{outZ} respectively are easy to achieve. Fig. 4 also shows how Miller compensation is employed to stabilize the loop.

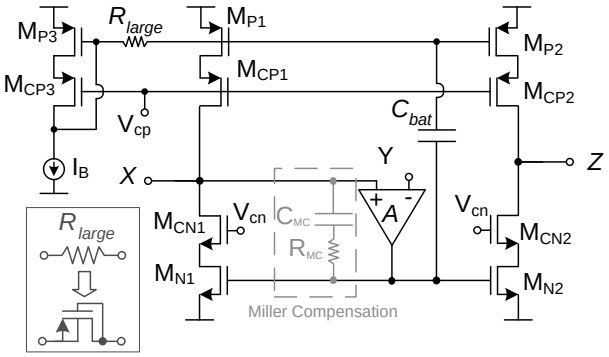

Fig. 4. The class AB CCII+ [20].

Fig. 5 shows the error amplifier used in $CCII_1$. The well-known differential pair with active load has been chosen due to its simplicity and low current requirements. It provides a gain A, equal to $g_{P5}(r_{dsP4} // r_{dsN3})$. A similar solution is adopted for the implementation of $CCII_2$.

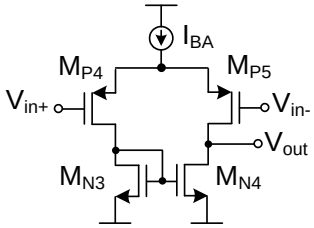

Fig. 5. Implementation of error amplifier in Fig. 4.

C. The Feedback Network

As mentioned above, it is possible to use non-linear elements in the feedback network without degrading the circuit linearity [13]. Fig. 6 shows the feedback network used in this work. Transistors M_{SW} are used as switches, while transistors $M_{PR1\text{-}2}$ are used as active resistors[2]. If $M_{PR1\text{-}2}$ are matched and biased by V_R, their equivalent resistance $R(V_R)$ is equal. Therefore, $R_2 = R(V_R)$ and $R_1 = R(V_R)/n$, where n (

[2] Due to the larger switching transistors, a slightly lower capacitance at node X_2 (Fig. 3) is obtained by exchanging the position of M_{PR1} with M_{SW}.

$n \subset 0:N$) is the number of M_{PR1} active transistors. If we substitute these relationships into (2) and (5) the gain and closed loop bandwidth of the VFCOA are given by

$$G_\infty \cong 1+\frac{R_2}{R_1} = 1+\frac{nR(V_R)}{R(V_R)} = 1+n \quad (14)$$

$$\omega_{CL} \cong T(0)\omega_{OL} = \frac{Z_T(0)\omega_{OL}}{R(V_R)} \quad (15)$$

From (14) and (15) we see that the closed-loop gain depends solely on the number of active transistor while the closed loop bandwidth depends on the tuning voltage V_R. Therefore the possibility of having constant, but tunable, closed-loop bandwidth is achieved.

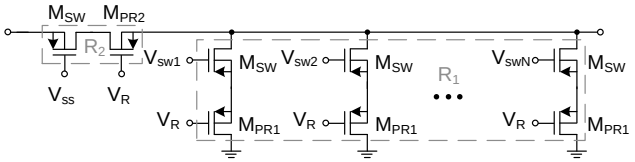

Fig. 6. Adopted transistorized feedback network.

IV. Measurement Results

The proposed VFCOA has been fabricated in a 0.5-µm CMOS technology. C_{bat}, C_C and C_{MC} were implemented as poly-poly capacitors with a nominal value of 1pF, 18pF and 1.5pF respectively. Resistors R_{large} (M_{PR}) were implemented with minimum-size PMOS transistors (1.5µm/0.6µm) and R_{MC} has a nominal value of 2.5kΩ. The rest of the transistor's dimensions W/L (in µm/µm) were: 100/0.6 (M_{P1}, M_{P2}, M_{P3}, M_{CN1}, M_{CN2}) 200/0.6 (M_{CP1}, M_{CP2}, M_{CP3}) 60/1 (M_{N1}, M_{N2}, M_{N3}, M_{N4}), 100/1 (M_{P4}, M_{P5}), 50/0.6 (M_{SW}) and 13.5/1 (M_{PR1}, M_{PR2}).

Bias currents I_B and I_{BA} have been implemented as wide swing cascode current sources with a nominal value of 10µA and 5 µA respectively. The supply voltage was 3.3V achieving a total static power consumption of 280.5µW. The total silicon area occupied by the whole circuit was 0.127mm^2, where the VFCOA and feedback network areas were 296×380 µm^2 and 285×50 µm^2 respectively. In Fig. 7 the VFCOA die microphotograph is shown.

Preliminary simulations showed a loop gain of 76 dB, gain-bandwidth product of 5.6 MHz with a phase margin of 60°. Input resistance was 53Ω and resistance R_2 was set nominally to 3500Ω.

Figure 8 shows the measured VFCOA's magnitude response for different gain configurations. As it can be seen, the amplification range goes from 0 up to 23.63 dB with the bandwidth ranging from 1.8 MHz to 2.9MHz for minimum and maximum gain respectively.

Measurement results also show that the bandwidth can be tuned between 1 and 3 MHz using V_R. If lower/higher bandwidth values are needed, they can be easily achieved at the design stage by proper M_{PR} dimensioning[3].

The harmonic distortion for a 300-kHz input signal is shown for minimum and maximum gain in Figs. 9 and 10, respectively (being the amplifier loaded with R_L=5.6 kΩ). As it can be seen, as usual in single-ended circuits, HD2 dominates over HD3. Class AB operation and high linearity can be appreciated by the fact that output total harmonic distortion is less than -40dB for output current amplitudes up to $5I_B$ for minimum gain and $23I_B$ in maximum gain configuration. Fig. 11 shows the step response of the VFCOA for maximum and minimum gain. Finally, Table I reports a comparison of the circuit performance parameters with those of the other two existing fabricated designs reported. Note that due to the class AB operation, this proposal achieves similar settling performance with less power consumption. Table II shows additional measurement results.

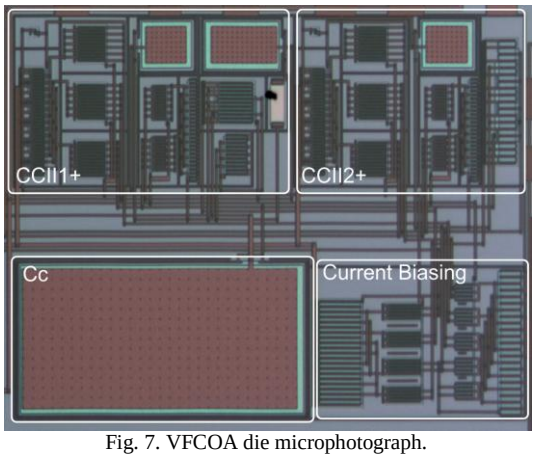

Fig. 7. VFCOA die microphotograph.

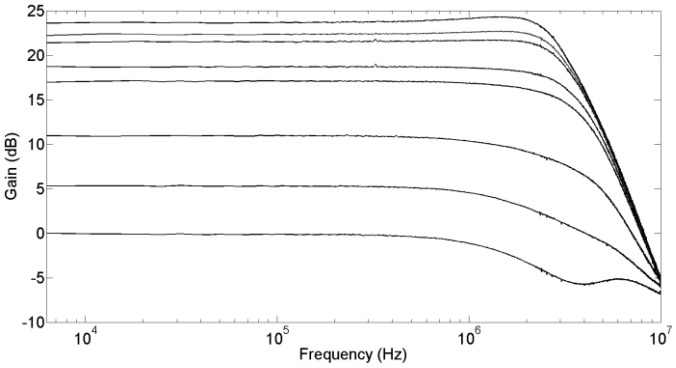

Fig. 8. Measured magnitude response of the VFCOA.

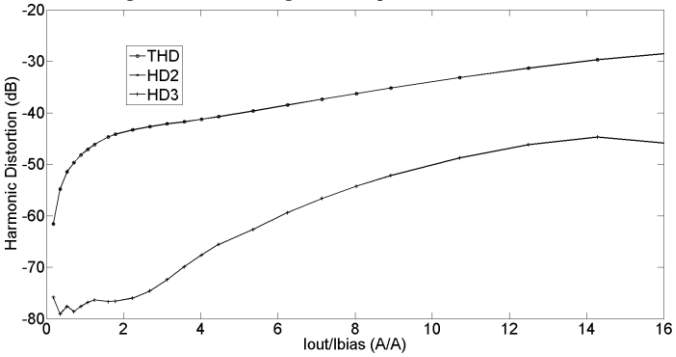

Fig. 9. VFCOA measured harmonic distortion for 0 dB gain @300kHz.

[3] Although tunable bandwidth is not commonly employed in amplifiers, it can be used for instance in some low-cost low-power transceivers where a tunable bandwidth amplifier can help in the channel selectivity of the baseband section of the receiver, saving die area and power consumption.

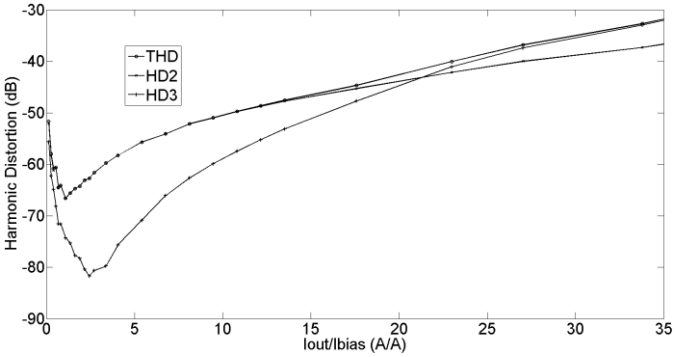

Fig. 10. VFCOA measured harmonic distortion for 23.6 dB gain @300kHz.

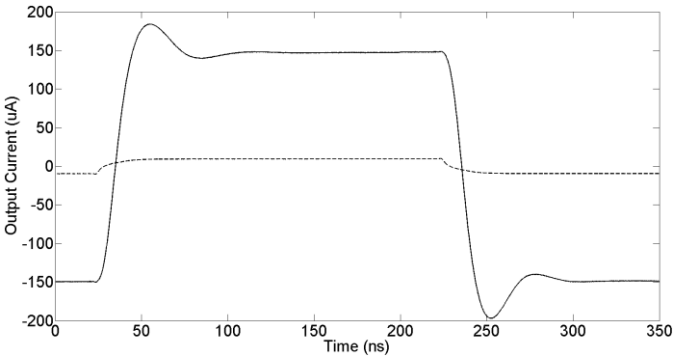

Fig. 11. Measured VCFOA step response for minimum (dotted curve) and maximum gain (continuous curve).

V. Conclusion

A class AB CMOS VFCOA that combines both variable gain and constant tunable bandwidth has been described in this brief, where the design strategy for the feedback resistors has also been discussed in detail. Measurement results confirm that the VFCOA is a versatile active block that can be used in high performance low power consumption current-mode circuit design. Measurement results show improved performance compared to similar circuits in literature, as apparently indicated by the figure of merit reported in the last row of Table I.

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TABLE I
Performance Comparison

Parameter	**This work**	**[12]**	**[11]**
CMOS Technology (μm)	0.5	1.2	2.4
Die Area (mm^2)	0.127	0.26	NA
Power Supply (V)	3.3	5	5
DC Power Consumption (μW)	280.5	4000	>1500
Open-Loop Gain (dB)	76*	100	72
GBW (MHz)	5.6*	10	3
Phase Margin (deg)	60*	>60	60
Output Load	5.6 kΩ	100 Ω	NA
$I_{O,MAX}$ (μA)	±500	±700	±700
$I_{O,MAX}$ /$I_{Standby}$	58.8	8.75	<2.3
$T_{Settl(0.1\%)}$, unity gain (ns)	47	165	35
SR, unity gain (μA/ns)	3.3	200	NA
Input noise voltage (nV/ √Hz)	0.54	7.5	NA
Output noise current (pA/ √Hz)	5.7 (1kΩ load)	20 (100Ω load)	NA
$T_{Settl(0.1\%)}$· $I_{O,MAX}$ /$I_{Standby}$ (ns)	2764	1443	<81

*simulated results

TABLE II
Summary of Additional Measured Performance

Parameter	**Value**
BW Range (MHz)	1-3
Gain Range (dB)	0-23.6
0.1% Settling time, max gain (ns)	138.4
Slew rate, max gain (μA/ns)	28.4
$\Delta I_{out}/\Delta V_{DD}$, unity gain, @100kHz (μA/V)	24.6
$\Delta I_{out}/\Delta V_{SS}$, unity gain, @100kHz (μA/V)	27.3
IIP3, unity gain (dBm)	29.3
P1dB, unity gain (dBm)	10
IIP3, max gain (dBm)	12.6
P1dB, max gain (dBm)	-6.5
DR, THD@300kHz 1%, N_{BW} 2.9MHz, max gain (dB)	87.5
DR, THD@300kHz 1%, N_{BW} 1.7MHz, min gain (dB)	100.1