Strategies for improving the efficiency and grid-connection stability of power converters for wind energy systems

Ph. D. dissertation prepared to obtain
the Doctor of Philosophy degree by

Javier Samanes Pascual

Supervisor

Eugenio Gubía Villabona

upna
Universidad Pública de Navarra
Nafarroako Unibertsitate Publikoa

Department of Electrical, Electronic and Communication Engineering

Pamplona, November 2018

Summary

Wind power is one of the most extensive renewable energies, which continues to grow, powered by the cost reduction of the technology and a greater societal environmental awareness. This worldwide expansion brings new challenges, such as the connection of wind turbines to weak grids, raising new stability issues. In addition, the efficiency of wind energy conversion systems, and consequently, of the power converter, becomes a key aspect to keep reducing the cost of energy. The last challenge to be highlighted is the increase of the rated power of the flagship wind turbines among the main manufacturers. This tendency is behind the interest of developing new conversion structures for modern wind turbines, which already reach 9 MW.

In this general context, the general research lines are:

- Detailed modeling of the control loops of a grid connected power converter.
- Improvement of the converter's dynamic response.
- Enhancement of the stability and efficiency of grid-connected power converters by damping the output filter through control techniques.
- Increasing the system efficiency by using specific modulations for power converters used in wind energy conversion systems.
- Analysis of the conversion structures for high power wind turbines and extension of the previous techniques to these systems.

Resumen

La energía eólica es una de las principales fuentes de generación renovable, una tecnología que continúa expandiéndose gracias a la reducción de costes y a la mayor concienciación ambiental de la sociedad. Esta expansión a nivel mundial está provocando que las turbinas eólicas se conecten a redes débiles, que plantean nuevos problemas de estabilidad. Asimismo, para continuar avanzando en la reducción del coste de la energía generada, la eficiencia de los sistemas de generación eólica, y consecuentemente del convertidor de potencia, se convierte en un aspecto clave. Por último, existe una tendencia entre los principales fabricantes de aerogeneradores a incrementar el tamaño de las turbinas, aprovechando las economías de escala existentes. Esta tendencia está forzando a buscar nuevas estructuras de conversión para estas turbinas que alcanzan hoy en día los 9 MW.

Dentro de este contexto general, en esta tesis se abordan las siguientes líneas de investigación:

- Modelo detallado de los lazos de control de un convertidor de conexión a red.
- Mejora de la respuesta dinámica del convertidor.
- Mejora de la estabilidad y de la eficiencia de convertidores de conexión a red al amortiguar el filtro de salida mediante el control.
- Incremento de la eficiencia gracias a la utilización de modulaciones especificas para convertidores eólicos.
- Análisis de las estructuras de conversión para turbinas eólicas de gran potencia y extensión a estos sistemas de las técnicas anteriores.

Agradecimientos

No me podía imaginar cuando empecé la tesis que iba a aprender tanto a lo largo de este tiempo. En gran parte, esto ha sido posible gracias a mucha gente que me ha acompañado durante este camino. Aprovecho esta ocassión para darles las gracias.

En primer lugar, tengo que agradecer a mi director de tesis, Eugenio, el haber confiado en mi para realizar este trabajo, siendo paciente y cercano durante todo el proceso. A lo largo de estos años he aprendido mucho gracias a él y me ha conseguido contagiar su pasión por descubrir nuevas ideas y entender nuevos conceptos.

En segundo lugar, quiero agradecer a la empresa Ingeteam Power Technology su colaboración y apoyo constante. En especial, quiero agradecer a Alberto, Xabier y Carlos su dedicación, las contribuciones en todas las reuniones y todo el trabajo en las sesiones de valiación de resultados en Mutilva. Sin duda, han contribuido a mejorar esta tesis y a darle una visión más realista.

En tercer lugar, quiero agradecer a todos los compañeros del grupo de investigación INGEPER el buen ambiente que existe entre todos. Siempre que lo he necesitado ha habido alguien dispuesto a echar un mano con cualquier cosa. Desde luego, todo esto ayuda a que cueste menos madrugar los lunes. Por no hablar de los Ingebikes, intentos de Ingesky, congresos...

En último lugar, quiero agradecer a mi familia, especialmente a mis padres, el cariño que me han dado y el haberme enseñado la importancia de la educación y del esfuerzo personal, porque sin ello, habría sido imposible terminar esta tesis. También tengo que agradecer a mi hermana Leyre, no solo su ayuda con la portada, si no el buen ejemplo que ha sido siempre como hermana mayor. También quiero dar las gracias a esa segunda familia que son los amigos. Y por supuesto, tengo que agradecer a Irati su apoyo durante toda esta etapa, sus ánimos y todos los buenos momentos juntos.

Tampoco me quiero dejar a todos los compañeros de APERNA, por todos esos “sumideros de tiempo”. Gracias a esta experiencia en APERNA he podido descubrir que la universidad tiene que ser mucho más que un lugar de estudio

Muchas gracias a todos.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Energy and civilization

Human beings, as well as all life forms, require a continuous flow of energy for their survival. However, in contrast to any other creature, humanity has developed alternative tools and mechanisms to harvest energy from their surroundings. The first societies were able to increase their standard of living by transitioning from an energy supply based on hunting and gathering to an agricultural culture, which provides a more reliable primary energy source. By harnessing the workforce of animals, fewer human resources were required to achieve greater supplies, increasing the level of development and complexity of societies. Energy is not only involved in feeding, it is also involved in transportation, manufacture of tools and comfort. The invention of the steam engine marked the beginning of the Industrial Revolution and was the true game changer. From this moment, human energy consumption escalated thorough the 19^{th} century to levels never seen before, as the revolution spread to different countries. This access to power sources with greater energy densities brought an unprecedented development and created migration movements towards the cities, where greater living standards could be achieved now.

The Industrial Revolution was powered by fossil fuels; first by coal, and later by petroleum and gas, as represented in Figure 1.1 (a) and (b). Lead by fossil fuel consumption, in 2016 the world's primary energy consumption reached 150 PWh, or in a more practical and understandable set of units, 53 $kWh/person/day$. Nevertheless, it must be taken into account that the intensive use of fossil fuels implies a depletion of natural resources and a modification of the climate, whose consequences for future generations are

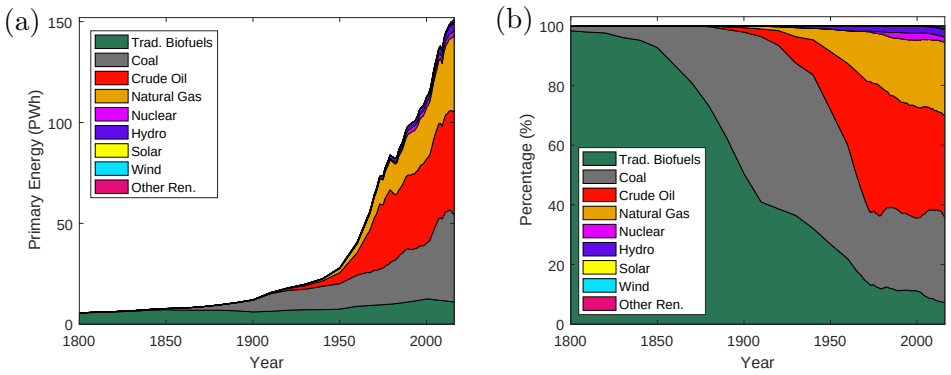


Figure 1.1: World total primary energy consumption per year (a) and share of global energy by fuel (b). Sources: [SMI16, GLO18].

hard to predict.

Even though our primary energy consumption is clearly dominated by fossil fuels, since the late 90s, modern renewable energies such as wind and solar, have steadily increased their generation in what it seems today as an unstoppable revolution. The exponential growth represented in Figure 1.2, was motivated, initially, by a greater societal environmental awareness which has driven the technological development of these technologies, and a dramatic cost reduction, mainly in wind and solar technologies. This cost reduction has motivated the impressive expansion since 2010.

Wind power is currently the modern renewable accounting for the

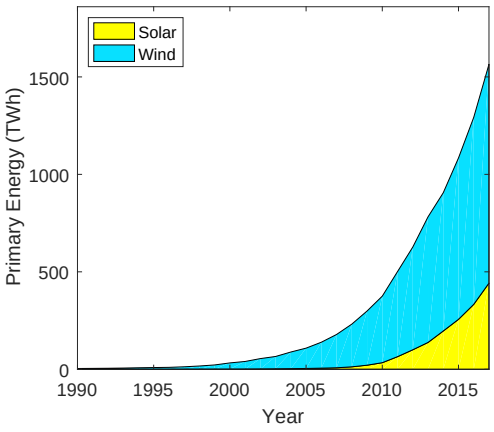


Figure 1.2: Contribution of modern renewables to the primary energy consumption.

greatest generation globally, with more than 1100 TWh, or 0.4 *kWh/person/day*, followed by solar energy, with more than 440 TWh [GLO18], or 0.15 *kWh/person/day*. The total installed capacity around the world in 2017 was 540 GW for wind power, 402 GW for photovoltaic power (PV) and 5 GW for concentrated solar thermal power (CSP) [REN18].

This thesis is focused on wind power generation, for this reason, in the following, the general trends in wind energy conversion systems (WECS) are analyzed.

1.2 Wind energy

1.2.1 General outlook

The world cumulative wind capacity has been growing in the last years at a sustained rate of 50 GW per year. This installation rate has allowed to advance from a cumulative power capacity equal to 240 GW in 2012 to the current 540 GW.

The majority of this cumulative capacity, 521 GW, is installed on land. This is called onshore wind power. However, offshore wind power is growing rapidly, as represented in Figure 1.4. This technology accounted at the end of 2017 for almost 19 GW around the world; nearly five times more than in 2011. Onshore wind power is already considered a cost-effective and competitive technology for electrical generation if compared with fossil fuel alternatives, while the general belief is that offshore wind power is still an expensive technology that requires subsidies in order to be developed. This statement about offshore wind power may not longer be true for too long. The Netherlands has already announced that a 350 MW offshore wind farm will be built by 2022 without any subsidies, confirming an unexpectedly fast cost reduction tendency. Moreover, an additional milestone has been

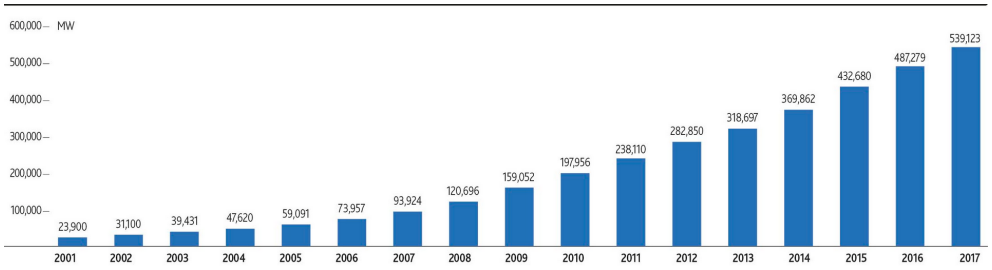


Figure 1.3: Global cumulative wind capacity 2001-2017 [GWE18].

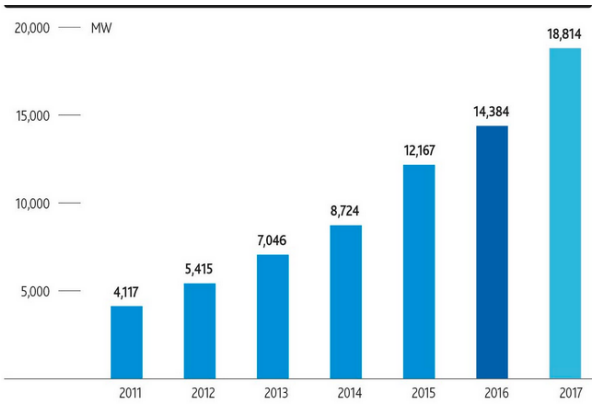


Figure 1.4: Global offshore cumulative wind capacity in MW from 2001-2017 [GWE18].

achieved in offshore wind power with the grid connection of a 30 MW commercial-scale floating wind farm in Scotland during 2017. This development opens new possibilities all around the world, as in the case of Spain. The majority of the Spanish coast depth is greater than 60 m, requiring floating structures in order to install wind turbines in the sea.

The majority of the wind capacity is concentrated in Europe, China and the USA. As shown in Figure 1.5 Spain still comes in fifth position, despite stagnation in the last years. If only offshore wind power is considered, the

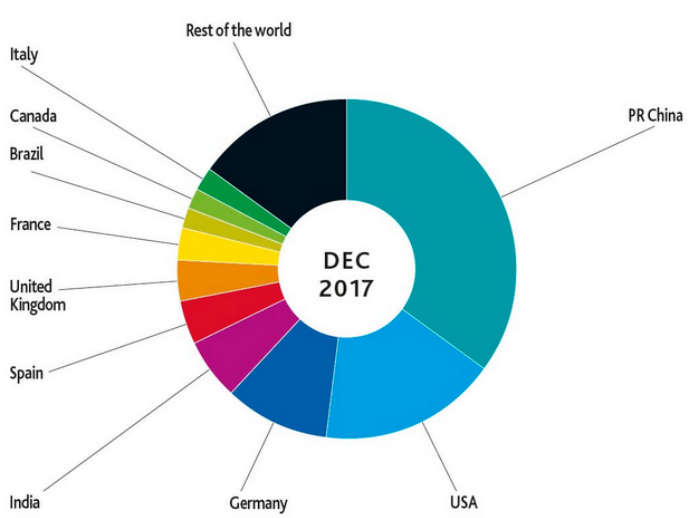


Figure 1.5: Global cumulative wind capacity by country [GWE18].

concentration of the cumulative power is greater: Europe, lead by United Kingdom and Germany, accounted, at the end of 2017, for 84% of the total cumulative power, while China accounted for almost 15% [GWE18].

In this general context, where both onshore and offshore wind power generation systems are steadily growing, the main trends and challenges that these systems are facing from the electrical perspective are analyzed in the following.

1.2.2 Trends and challenges

Motivated by the development of offshore wind power and the existing economies of scale, commercial wind turbines' rated power has steadily increased. In Figure 1.6 the evolution from 1980 to 2015 is represented, along with the predictions made in 2015 for 2020. In 25 years, the flagship wind turbines of the main manufacturers have evolved form a rated power of 50 kW in 1980 to 10 MW in 2015, having rotor diameters of more than 180 m. The tendencies predicted for 2020, with perspectives of commercial turbines from 15 to 20 MW, were too optimistic. To date, the biggest world turbine development, the Haliade-X 12 MW offshore wind turbine, by GE, will be available by 2021 falling behind the estimation.

These bigger wind turbines have brought changes in the electrical conversion structure. Traditionally, wind power has been dominated by the electrical conversion structure represented in Figure 1.7 (a): a doubly-fed induction generator whose stator is directly connected to the grid and a back-to-back (B2B) power converter connected to the rotor and used as an interphase with the grid. In this conversion structure, GSC stands for

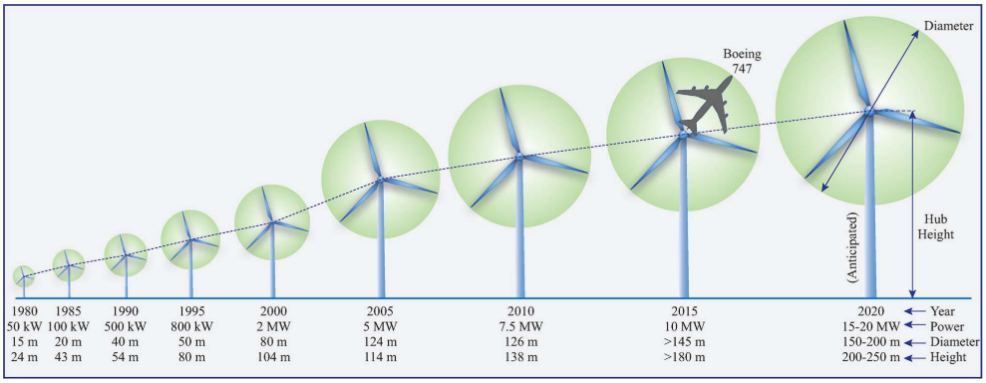


Figure 1.6: Evolution of the size and rated power of wind turbines [YAR15].

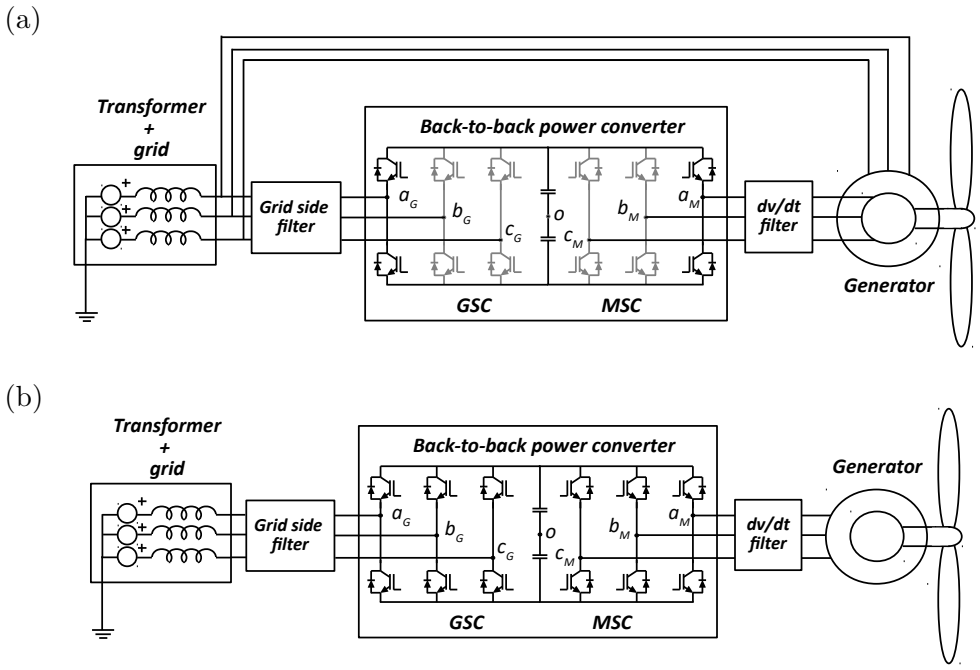


Figure 1.7: Structure of a wind turbine with a doubly-fed induction generator and a back-to-back power converter (a) and a full-converter topology for a permanent magnet generator (b).

grid-side converter while MSC stands for machine-side converter. DFIG wind turbines have largely dominated wind markets because they are a cost-effective solution. They use a high-speed compact generator, connecting its high-speed shaft to the slow main shaft through a gearbox. Moreover, the B2B power converter only has to transform a third of the rated power, consequently reducing the price of this stage if compared to the full-converter approaches. However, this conversion structure has one main drawback. In DFIG topologies the power converter is connected to the rotor. The common-mode voltage introduced by the B2B conversion structure can create transient currents through the gearbox bearings, reducing their lifetime. This is the main cause of failure in DFIG wind turbines with a rated power greater than 2 MW [ALE12]. Nevertheless it is still the predominant solution for onshore wind turbines.

Reliability is key to offshore wind turbines. The two main costs of offshore wind energy are logistics and maintenance of the wind turbine [GON17]. For this reason, minimizing the number of failures is an important

issue. The offshore wind turbine portfolio of the main manufacturers is based on permanent magnet generators (PMG) with a full-scale B2B power converter which does not require a gearbox. These turbines are called direct-drive. In these solutions, the PMG rotates at low speeds, requiring a high number of poles and increasing the cost of the generator. Moreover, the B2B power converter also becomes more expensive. However, this increase in the cost is justified by the higher availability of the wind turbine.

This trend – the transition to high power PMG direct-drive wind turbines – can be confirmed by reviewing the porfolio of the main offshore manufacturers. In 2017, 84% of the offshore power capacity added around the world was installed in Europe, as outlined in Subsection 1.2.1. For this reason, a general insight into the offshore market can be gained by simply analyzing the main manufacturers of the European market. According to [REM18] Siemens Gamesa leaded the European market with 51.3% of the installed power, MHI Vestas had a share equal to 24.7% and Senvion and Adwen a 14% and 11% respectively, as represented in Figure 1.8

Research has been performed through the portfolio of the three main manufacturers, summarizing the results in Table 1.1. The table contains the basic information, from the electrical conversion perspective, of the flagship turbines of each manufacturer for the offshore segment: rated power, generator used, including additional information related to the use of a gearbox (GB) or the absence of it (DD) and at last the generator output voltage. It can be seen that the rated power of the wind turbines is steadily increasing and the permanent magnet generator (PMG) at low voltage is the

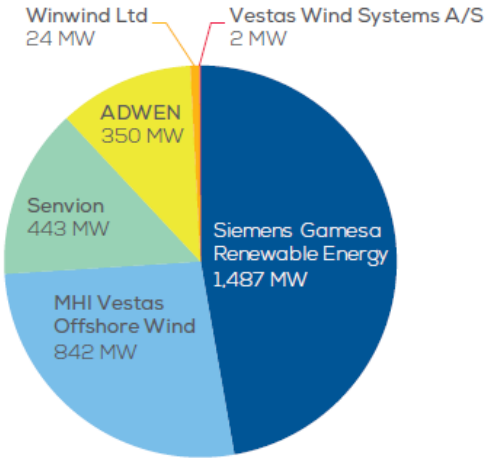


Figure 1.8: Manufacturers' share of 2017 annual installations in Europe [REM18].

Table 1.1: Offshore wind turbine portfolio of the main manufacturers.

Manufacturer	Wind turbine	Rated power (MW)	Generator	Voltage (V)
Siemens-Gamesa	SWT-6.0-154	6	PMG - DD	690
	SWT-7-154	7	PMG - DD	690
	SG 8.0-167 DD	8	PMG - DD	690
MHI Vestas	V117-4.2 MW	4.2	PMG - GB	690
	V164-8.0	8	PMG - GB	690
	V164-9.5	9.5	PMG - GB	690
Senvion	6.XM	6.1-6.3	DFIG - GB	690 (rotor)

dominant trend. Both Siemens-Gamesa and MHI Vestas have wind turbines with similarly rated powers and generator topologies, while Senvion uses a doubly-fed induction generator (DFIG) with a lower turbine rated power. An important difference between both manufacturers is that while Siemens-Gamesa has developed direct drive wind turbines, MHI Vestas has kept the gearbox with a reduced number of stages: two instead of three. With this solution they can increase the rotational speed of the generator, reducing the required number of poles and resulting in a more compact and cheaper solution. The same trend, high power with low voltage generator, can be found in other manufacturers such as GE Renewable Energy, who recently announced the release of Haliade-X: a 12 MW Wind turbine, using a PMG generator with direct-drive technology and an output voltage of 900 V.

The high power generated by the wind turbine at low voltage implies high currents. These high current levels increase the power losses. For this reason, a high efficiency in the power converter stage is specially important. By reducing the required switching orders in the power converter and eliminating or reducing the resistive passive components, interesting gains in the efficiency can be obtained. This approach helps to reduced the levelized cost of energy (LCOE), as the cooling requirements are reduced and more energy is injected to the grid. Moreover, as the power converter is connected to the stator windings in PMGs, the bearing currents are not as problematic as in DFIG wind turbines, which a key aspect from the maintenance point of view.

Not only the power of each individual turbine has grown over the last years, the overall size of wind farms has also seen a sustained growth. In the early developments of wind power, wind farms had a reduced power and were installed in developed countries, with strong grids. However, as wind power has been extended all over the world and the size of wind farms has grown, wind turbines are connected in many occasions to weak grids with extremely low SCRs. Some wind turbine manufacturers even demand the operation at

SCRs equal to 1, meaning that the turbine rated power is equal to the short circuit power. With the connection of the power converter to such weak grids, new stability challenges arise. These challenges are accompanied by the development of stringent grid codes, which impose additional requirements to modern wind turbines, limiting the grid current harmonic content and imposing faster transient responses against grid transients [BDE08, IEE08]. To limit the grid currents, an *LCL* filter is the most extended solution used at the output of GSC. This filter topology has a main drawback, it presents a resonance frequency that introduce stability issues, moreover, as it is connected to weak grids.

1.3 Goals

The main goals of this thesis are related with the challenges and trends introduced in the previous section. These goals are exposed according to the order in which they are tackled thorough the thesis.

The first goal is to guarantee the stability and the appropriate response of the wind turbines, regardless of the grid impedance at which it is connected, a proper control strategy is required. This control strategy should address the stability issues related to the instabilities created within the active and reactive power control bandwidths in high power converters.

The second goal is also focused in the power converter stability, but in this case, tackling the instability problems at high frequencies, related to the output filter resonance and the interactions with the grid impedance. This goal should be approached from the control perspective, allowing to achieve a solution that does not compromise the efficiency of the conversion structure, in opposition to other alternatives that include hardware resistors to guarantee the stability.

The third objective consists in the improvement of the efficiency of the conversion stage. The efficiency depends on the modulation strategy applied. Nevertheless, this modulation strategy has to take into account the common-mode and phase-to-ground voltages imposed at the generator terminals, which can deteriorate it and create early failures.

Finally, the fourth goal is to explore the parallel connection of power converters for offshore high power wind turbines. This conversion structure should respond to the market trends analyzed and be scalable and flexible to be used in different wind turbines, with different power ratings. The efficiency and the grid-connection stability of this conversion structures are

studied and improved.

The fulfillment of these four goals determines the structure of this thesis. After this introduction, in Chapter 2 the model required for the precise analysis of the power conversion structure is developed. In this chapter it is highlighted the influence of the voltages imposed by the power converter on the different current components. Several control approaches are reviewed, presenting a detailed modeling approach that will serve as a frame for the control strategies presented in the following chapters.

In Chapter 3 a control strategy is presented that achieves an improved dynamic response of the active and reactive power control in grid-connected power converters. This strategy takes into account the possible connection of the power converter to strong and weak grids, achieving a robust design. Both the reference tracking and the rejection to grid disturbances are studied. The results are validated in a three-phase power converter at the Public University of Navarre.

To solve the high frequency stability problems created by the use of an LCL filter, in Chapter 4 an active damping strategy robust to variations in the grid impedance is proposed. In this section, the delays within the control loop are carefully studied and adjusted, as it is a key aspect for the stability. With this strategy the harmonic code compliance is guaranteed, as well as achieving a reduction of the power losses by eliminating the passive resistor. This control strategy is validated in the facilities of Ingeteam Power Technologies SA.

The work covered in Chapter 5 is focused on the development of modulation strategies for B2B power converters. The efficiency of the conversion structure is improved without increasing the phase-to-ground and common-mode voltage peaks. Again, the results are validated in the same power converter at Ingeteam facilities, also used to validate the active damping strategy.

In the final part, Chapter 6, the use of parallel B2B conversion structures for offshore applications is considered. Firstly, a review of the parallelization alternatives is performed and the model to characterize the interaction of parallel conversion structures is shown. Secondly, a modulation to achieve a high efficiency is studied and the control approaches proposed in Chapter 3 and Chapter 4 are adjusted to improve the grid-connection stability of the modular conversion stage. This stage is referred as single-block.

Lastly, in Chapter 7 the conclusions of this thesis are highlighted, presenting the main contributions made in the development of this work. There are several future research lines that appeared in the development of this thesis, which are summarized at the end of the chapter.

Chapter 2

System modeling and characterization

2.1 General overview of the power generation system

The current trend in high power offshore wind turbines is the use of permanent magnet synchronous generators with a full-converter back-to-back (B2B) power converter. This topology is represented in Figure 2.1 (a). In contrast, the doubly-fed induction generator with a back-to-back power converter that handles a portion of the generated power is the most extended solution in onshore WECS, as it is a more cost-effective solution, Figure 2.1 (b).

The power generated by the wind turbine flowing through the back-to-back power converter is transformed and adapted to the requirements imposed by the grid operator. The back-to-back conversion structure is composed of two three-phase power converters, symmetrical located with respect to a capacitive DC-bus.

The machine side converter (MSC) is responsible of controlling the rotational speed of the electrical generator, maximizing the power generated by the wind turbine. MSC works as a rectifier; the power generated at a variable frequency and voltage level is transformed to DC. This converter is connected to the stator of the generator through a dv/dt filter. This filter is responsible of limiting the high voltage derivatives introduced by the fast switching characteristics of the IGBTs.

The pulses introduced by the converter, are not equally distributed in

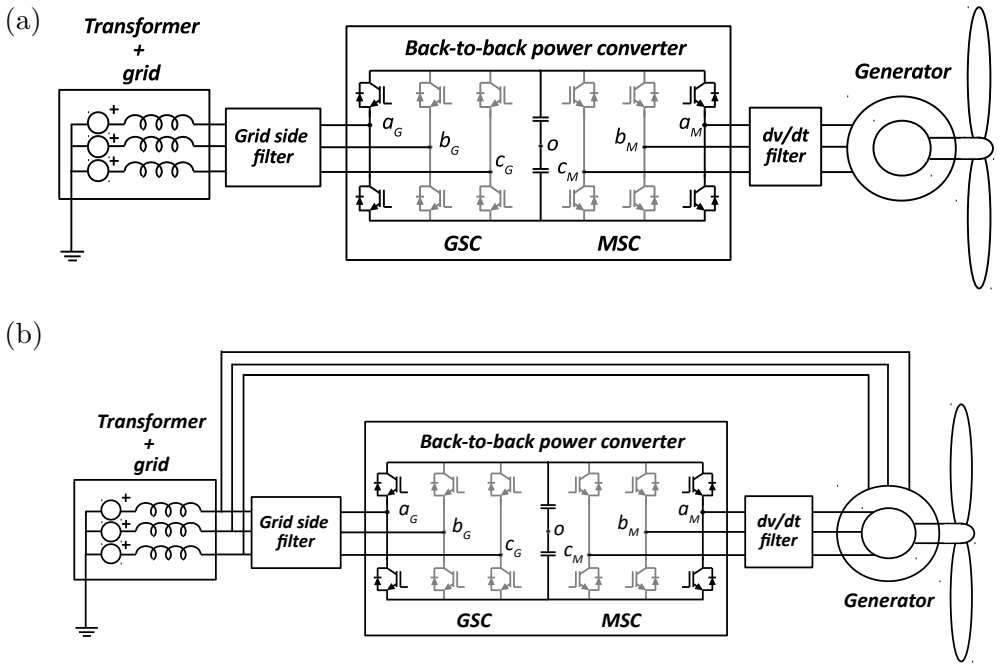


Figure 2.1: Structure of a full-converter back-to-back power converter for a permanent magnet generator (a) and for a doubly-fed induction generator (b).

the whole stator winding during the raising and falling voltage edges. The insulation of the first coils has to withstand a greater voltage, which can cause premature failures in the generator [MEL98]. Moreover, these fast pulses can create electromagnetic interference in the surrounding electronic equipment. These issues are alleviated by the addition of a *dv/dt* filter between the power converter and the generator, which limits the slope of the pulses introduced at the machine terminals. Different filtering solutions can be used, being the L-RC filter one of the most typical ones [SWA17]. This filter is shown in Figure 2.2. The size of the *dv/dt* filter is relatively small because it only has to slow down the rising and falling edges, and has an almost null effect at the switching frequency.

The grid side converter (GSC) controls the DC-bus voltage to a fixed value, injecting the power generated by the wind turbine into the grid. GSC is connected through a step-up transformer to the grid. This transformer is usually located inside the nacelle, and its parameters are known. The neutral point of the low voltage side is connected to the ground [IEE08], as represented in Figure 2.1.

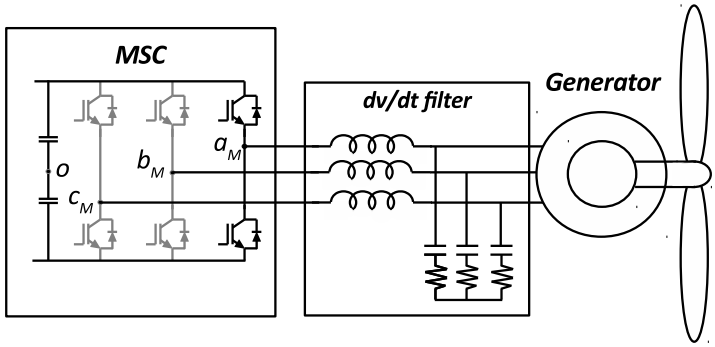


Figure 2.2: Classical *dv/dt* filter between the MSC and the generator.

The power injected to the grid has to comply with the standards set by the grid codes [BDE08, IEE08]. The voltage imposed by the power converter contains important harmonics at the switching frequency and its multiples. For this reason, a filter is included between GSC and the step-up transformer in order to limit the grid current harmonic content.

Several filtering solutions can be used to fulfill the grid codes. The most simple approach would be the addition of a purely inductive filter. However, the required inductor to comply with the grid codes is unacceptably bulky. To reduce the size and cost of the output filter of GSC, a LCL or a trap filter can be implemented [BER16a, BER16c]. The LCL filter is the most extended one, as it is a simple and cost effective option, with a reduced number of components if compared with trap filters. The typical LCL filter is shown in Figure 2.3. The inductance connected at the output of the converter receives the name of converter side inductance. The other inductor, the grid side inductor, is composed of the transformer leakage inductor, which is generally known, and the grid equivalent inductance, which is generally unknown. The unknown equivalent grid inductance creates an uncertainty that introduces some challenges in the design of the control loop.

2.2 System model from the point of view of the common-mode and differential mode components

In Figure 2.3 the ground current is the sum off the three currents flowing into the grid. This current is called common-mode current, i_{cm} and is equal in each of the three phases. The rest of the current in each phase is called differential-

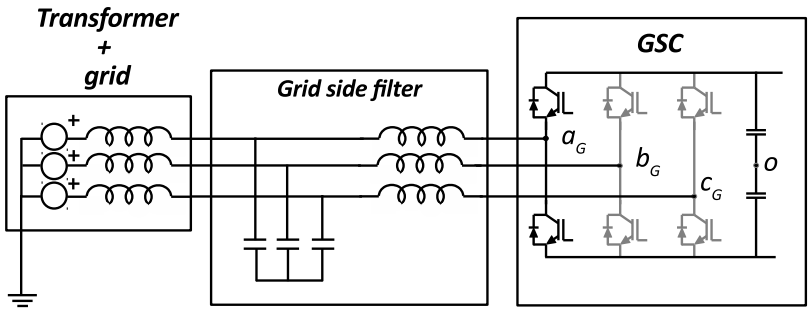


Figure 2.3: Classical *LCL* filter between the GSC and the grid.

mode current, i_{gdm} and add-up to zero. In Figure 2.4, these currents and the grid voltages are represented.

The instantaneous power transfer to the grid is given by the product of the grid currents and voltages.

$$p_g = p_{g_a} + p_{g_b} + p_{g_c} = i_{g_a} v_{g_a} + i_{g_b} v_{g_b} + i_{g_c} v_{g_c} \tag{2.1}$$

All the variables in this equation are a function of time. To simplify the notation, $v(t)$ is represented by simply v, $i(t)$ by i and the power, $p(t)$, by p.

Each phase current can be decomposed in its common-mode and differential-mode currents. The common-mode current is defined as

$$i_{cm} = i_{g_a} + i_{g_b} + i_{g_c} \tag{2.2}$$

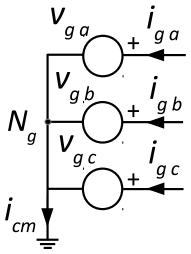


Figure 2.4: Three-phase balanced voltage source.

while the differential-mode current of phase i is

$$i_{gdm_i} = i_{g_i} - \frac{i_{cm}}{3} \tag{2.3}$$

Consequently, all the phase currents can be rewritten in terms of the common-mode and differential-mode components.

$$i_{g_a} = i_{gdm_a} + \frac{i_{cm}}{3} \tag{2.4}$$

$$i_{g_b} = i_{gdm_b} + \frac{i_{cm}}{3} \tag{2.5}$$

$$i_{g_c} = i_{gdm_c} + \frac{i_{cm}}{3} \tag{2.6}$$

Equation 2.1 can be rewritten expressing the currents in terms of their common mode and differential mode components.

$$p_g = i_{gdm_a} v_{g_a} + i_{gdm_b} v_{g_b} + i_{gdm_c} v_{g_c} + \frac{i_{cm}}{3}(v_{g_a} + v_{g_b} + v_{g_c}) \tag{2.7}$$

Under balanced conditions, the sum of the three grid voltages is equal to zero and the power transfer to the grid expressed as:

$$p_g = i_{gdm_a} v_{g_a} + i_{gdm_b} v_{g_b} + i_{gdm_c} v_{g_c} \tag{2.8}$$

The power transfer to the grid, and more generally, to any balanced three phase voltage source, depends only on the product of the differential currents, and not on the common-mode current. For this reason, to control the power transfer to the grid, and to the generator, the grid differential currents, and the machine differential currents, have to be controlled. In order to properly characterize how the voltages imposed by the power converter influence the common-mode and differential-mode currents, the equivalent common-mode and differential-mode models of the B2B power converter are developed.

Both GSC and MSC are three-phase two-level power converters. In a three-phase two-level power converter as the one shown in Figure 2.5, each phase is connected to a branch composed of two switches. Both switches have to be operated in a complementary way, if the upper switch is in the on-state, the lower switch has to be off and vice versa. Otherwise, the DC-bus capacitors would be short-circuited or the inductor open-circuited.

A variable F, named switching function, can be defined to describe analytically the switching state of each converter leg. This variable is equal

to 1 if the upper switch is connected, while it becomes -1 if the lower switch is connected. In this way, the voltage in phase i, defined with respect to the mid-point of the DC-bus, is:

$$v_{io} = F_i \frac{E}{2} \tag{2.9}$$

where E is the DC-bus voltage. This means that the three-phase power converter can be represented by three voltage sources, where each of these sources can have a value of $\pm E/2$. The three-phase power converter behaves as a voltage source converter (VSC). All the possible values of the switching functions of the three-phase VSC are summarized in Table 2.1.

The value of the switching function is determined through the modulation technique called pulse width modulation (PWM). The PWM is based on the comparison of three low frequency modulating waves (for a three-phase power converter), in this case, three sinusoidal waves phase shifted by 120 degrees at the grid fundamental frequency, with a high frequency carrier wave at the switching frequency. If the carrier wave is greater than the modulating wave in phase i at a given instant, the upper switch in leg i is turned on, and F_i is equal to 1. If the carrier wave is lower than the modulating wave in phase i, the lower switch is turned on and F_i is equal to -1. This working principle

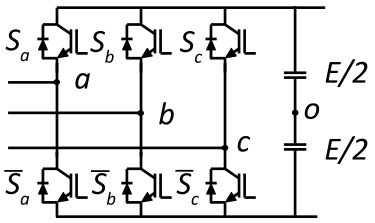


Figure 2.5: Three-phase two-level power converter.

Table 2.1: Possible switching states of a tree-phase two-level VSC.

F_a	F_b	F_c	v_{dm_a}	v_{dm_b}	v_{dm_c}	v_{cm}
-1	-1	-1	0	0	0	-E/2
-1	-1	1	-E/3	-E/3	2E/3	-E/6
-1	1	-1	-E/3	2E/3	-E/3	-E/6
-1	1	1	-2E/3	E/3	E/3	E/6
1	-1	-1	2E/3	-E/3	-E/3	-E/6
1	-1	1	E/3	-2E/3	E/3	E/6
1	1	-1	E/3	E/3	-2E/3	E/6
1	1	1	0	0	0	E/2

and the resulting leg voltage v_{io} are represented in Figure 2.6.

The *LCL* filter has to be added at the output of the VSC to filter the modulated voltage and obtain a waveform similar to the modulating fundamental frequency.

To characterize and analyze the common-mode and differential-mode currents, the converter voltages and currents are also decomposed in common-mode and differential-mode. As indicated by Figure 2.7, any three-phase voltage source, can be decomposed in a common-mode voltage source, v_{cm}, and three differential-mode voltage sources, v_{dm_a}, v_{dm_b} and v_{dm_c}. The common-mode voltage source can be defined as:

$$v_{cm} = \frac{1}{3}(v_{ao} + v_{bo} + v_{co}) \tag{2.10}$$

or equivalently as:

$$v_{cm} = \frac{E}{6}(F_a + F_b + F_c) \tag{2.11}$$

v_{cm} can have four different values $\pm E/2$ and $\pm E/6$. The differential-mode voltage in phase a is defined as:

$$v_{dm_a} = v_{ao} - v_{cm} \tag{2.12}$$

or equivalently as

$$v_{dm_a} = \frac{E}{6}(2F_a - F_b - F_c) \tag{2.13}$$

v_{dm_a} can have five different values $\pm 2E/3$, $\pm E/3$ and 0. The instantaneous value of the differential voltage can have these five discrete values, however, the average value can be adjusted by means of the PWM technique, modifying the amplitude of the modulating wave. The average value in every sampling period determines the control action, while the instantaneous value determines the harmonic content.

The grid voltage can also be decomposed in common-mode and differential mode. Under normal operation, the grid is a balanced three phase system with no common-mode. With this consideration, GSC can be modeled in terms of its common-mode and differential mode voltage sources as in Figure 2.8. The subindex g stands for the grid, while *conv* stands for the converter side variables.

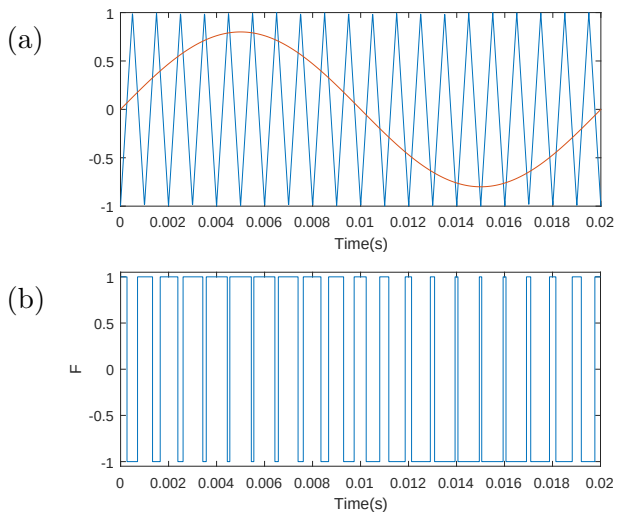


Figure 2.6: Comparison of the carrier and modulating wave (a) and switching function value (b).

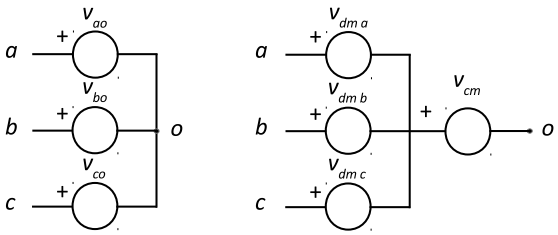


Figure 2.7: Decomposition of a three-voltage source in common-mode and differential-mode voltage sources.

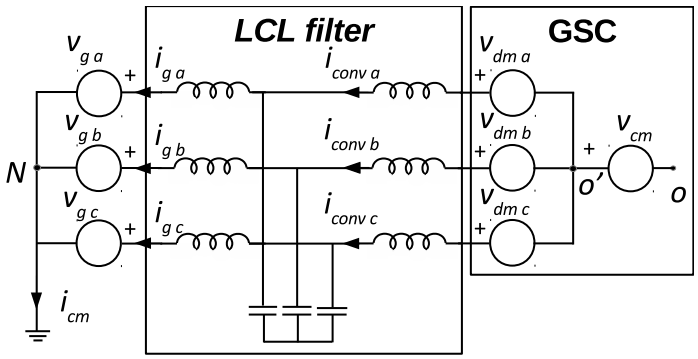


Figure 2.8: Common-mode and differential-mode decomposition of GSC.

By superposition, if v_{cm} in Figure 2.8 is 0 and the LCL filter components are balanced, the voltage between N and o is given by:

$$v_{No'} = \frac{1}{3} \sum_{i=a,b,c} (v_{dm_i} - v_{g_i}) \tag{2.14}$$

and is equal to 0 by definition. In this way, the differential current in each phase is controlled by the differential voltage of each phase. If the point o is connected to ground through a parasitic capacitance, the common-mode current, i_{cm}, would be determined by v_{cm} and the impedances seen in this path. The common-mode voltage does not affect the differential current, however, it is a degree of freedom that can be used to extend the modulation range of the power converter or to minimize the losses.

By extending the model developed for GSC to the back-to-back conversion structure, Figure 2.9 is obtained. From this model, it is clear that the differential currents of GSC and MSC are independently controlled by the differential voltages imposed by each three-phase power converter. The switching orders of GSC can be determined independently of those of MSC. However, the combined effect of the switching orders in GSC and MSC has an impact on the common-mode voltage. This common-mode voltage can create problems form the common-mode current point of view, due to the existing parasitic capacitances to ground. In this way, transient currents appear related to the problems outlined in the introduction, such as bearing currents and insulation stress.

The power transfer to the grid depends only on the differential currents, which are driven by the differential voltage, independent from those in MSC. In this way MSC can be eliminated from the stability analysis when GSC is studied.

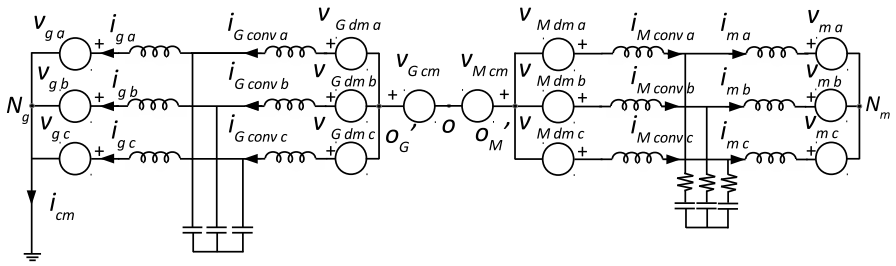


Figure 2.9: Common-mode and differential-mode decomposition of the B2B conversion structure.

2.3 Current control loop model of GSC

2.3.1 Current control approaches

It has been seen in Section 2.2 that the differential currents, and consequently, the power transferred to the grid and the machine, can be controlled independently with the differential voltages imposed in GSC and MSC, respectively. One of the main challenges of wind energy conversion systems (WECS) is the connection and control of new turbines to weak grids. For these reasons, in this subsection, the scope is focused on GSC, even though the current control approaches are also applicable to MSC.

2.3.1.1 Scalar current control

In the scalar current control, the real magnitude currents are controlled, as represented in Figure 2.10. Even though to control the power transferred to the grid, the grid current should be controlled, it is a common approach to control the converter side current, as in Figure 2.10. This can be done because at low frequencies, such as the grid fundamental frequency, both the grid-side and the converter-side currents are similar. Moreover, the filter capacitor voltage is also measured, and the capacitor reactive power can be compensated.

The DC-bus voltage control loop determines the active power that must be injected to the grid, while the reactive power is determined by the grid operator, under normal operation. Under voltage dips, sags and overvoltages the grid codes determine the reactive power.

With the capacitor voltage measurements, the current references are calculated. Note that there are only two reference currents. The three-phase differential currents cannot be controlled simultaneously, so only two of them are controlled. The action in the third phase is calculated depending on the modulating waves of the other two phases.

The current controller determines the voltage that has to be applied on each phase, and the modulator determines the switching states of the power converter.

Different current controllers can be used to determine the required action to follow the reference. The main alternatives are the use of a proportional integral controller (PI) or a resonant controller.

Proportional integral controller

A PI controller introduces infinite gain at 0 Hz, achieving zero tracking

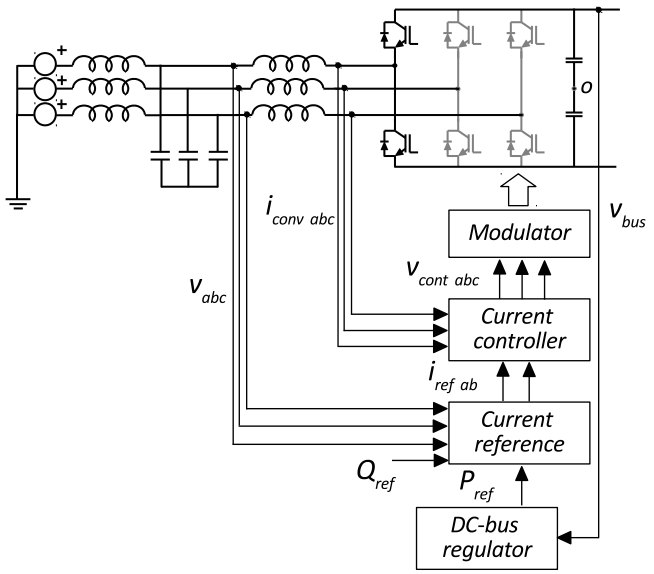


Figure 2.10: Diagram representation of the scalar current control.

error at that frequency. However, the reference that must be tracked oscillates at the grid fundamental frequency. At 50 Hz or 60 Hz (depending on the grid at which the power converter is connected), the gain of the PI is reduced.

To achieve good tracking characteristics, the bandwidth of the current control loop has to be increased, generally to a frequency ten times higher than the fundamental. However, in high power converters, where the switching frequency is limited, and consequently, the sampling frequency is also limited, the controller bandwidth cannot be increased without a significant reduction in the stability margins.

Resonant controller

To achieve zero tracking error in high power converters, a resonant controller can be used. This resonant controller can be adjusted to achieve an infinite gain at a given frequency, in this case, at the grid fundamental frequency. The resonant controller can be combined with a proportional or a PI controller, in order to control low frequency and DC components.

2.3.1.2 Vectorial current control

The vectorial current control applies transformations to the three-phase variables measured, decomposing them in two "differential" axis and a homopolar or common-mode axis. With these transformations, the power transfer to the grid can be controlled through the control of the currents in the two differential axis components.

First, the vectorial current control in the stationary reference frame is studied. In this reference frame, the variables oscillate at the fundamental frequency. For this reason, the vectorial control in the synchronous reference frame is later presented. This transformation converts the oscillating variables into a DC component that can be controlled by means of the classical PI controller.

Control in the stationary reference frame or $\alpha\beta$

To control the system in the stationary reference frame the Clarke transformation has to be applied to the measured variables [DUE51]. The Clarke transformation consists in the application of the following matrix:

$$[CLA] = K \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \tag{2.15}$$

to the electrical variables, obtaining the variables expressed in a different set of axis; $\alpha\beta z$. The constant K can be chosen to adjust the gain of this transformation. The gain introduced by the Clarke transformation in 3/2. To obtain a magnitude invariant transformation, K has to be equal to 2/3; this is called the American convention. If K is equal to $\sqrt{2/3}$ a power invariant transformation is obtained; this is called the European convention.

In this thesis, the European convention, or equivalently, the power invariant convention, is going to be used, as our main intention is the control of the power transferred to the grid. With this convention, the Clarke inverse transformation matrix is equal to the transpose of [CLA].

If the Clarke transformation is applied to the converter currents, decomposed in their differential-mode and common-mode components:

$$\begin{Bmatrix} i_\alpha \\ i_\beta \\ i_z \end{Bmatrix} = K \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \begin{Bmatrix} i_{conv\ dm_a} + \frac{i_{cm}}{3} \\ i_{conv\ dm_b} + \frac{i_{cm}}{3} \\ i_{conv\ dm_c} + \frac{i_{cm}}{3} \end{Bmatrix} \tag{2.16}$$

By operating:

$$\begin{Bmatrix} i_\alpha \\ i_\beta \\ i_z \end{Bmatrix} = K \begin{Bmatrix} i_{conv\ dm_a} + \frac{i_{cm}}{3} - \frac{1}{2} i_{conv\ dm_b} - \frac{i_{cm}}{6} - \frac{1}{2} i_{conv\ dm_c} - \frac{i_{cm}}{6} \\ \frac{\sqrt{3}}{2} i_{conv\ dm_b} + \frac{\sqrt{3} i_{cm}}{6} - \frac{\sqrt{3}}{2} i_{conv\ dm_c} - \frac{\sqrt{3} i_{cm}}{6} \\ \frac{i_{cm}}{6} + \frac{i_{cm}}{6} + \frac{i_{cm}}{6} \end{Bmatrix} \quad (2.17)$$

it can be found that the three-phase differential components are translated into the $\alpha\beta$ axis, while the common-mode component is translated into the z axis:

$$\begin{Bmatrix} i_\alpha \\ i_\beta \\ i_z \end{Bmatrix} = K \begin{Bmatrix} \frac{3}{2} i_{conv\ dm_a} \\ \frac{\sqrt{3}}{2} i_{conv\ dm_b} - \frac{\sqrt{3}}{2} i_{conv\ dm_c} \\ \frac{i_{cm}}{2} \end{Bmatrix} \quad (2.18)$$

In this way, the power transfer to the grid can be controlled by the control structure of Figure 2.11, where only the $\alpha\beta$ components are controlled. Moreover, the common-mode can be controlled independently of the differential components, as the common-mode voltage only introduces transient common-mode currents.

As in the scalar current control, the reference that must be tracked in both

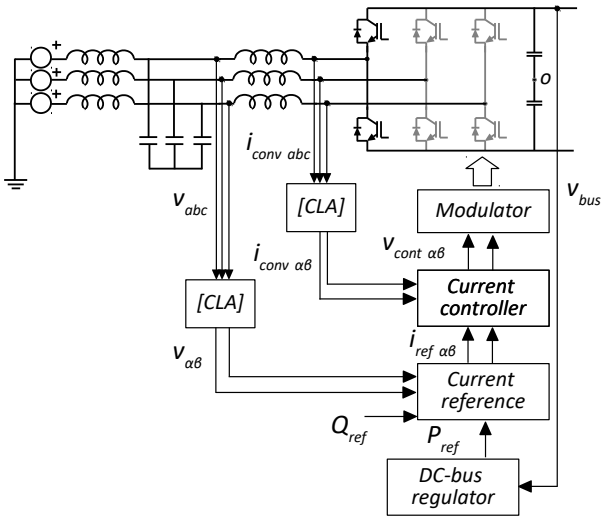


Figure 2.11: Diagram representation of the vectorial current control in the stationary reference frame.

axis is a sine wave at the grid fundamental frequency. For this reason, a **PI controller** suffer from the same problems that in the scalar current control and a **resonant controller** is a more suitable approach for high power converters.

Control in the synchronous reference frame or dq

A further transformation that converts the frequency spectrum of the signal, such that the given frequency now appears as DC, is the Park transformation [PAR33], or the direct-quadrature-zero (dqz) transformation. The Park transformation matrix is

$$[PAR] = \begin{bmatrix} cos(\omega_0 t) & sin(\omega_0 t) & 0 \\ -sin(\omega_0 t) & cos(\omega_0 t) & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{2.19}$$

where ω_0 is the frequency that is translated into a DC component.

The Clarke transformation and the Park transformation can be combined, obtaining the benefits from both transformations; the power transfer is controlled by two differential components, dq, while the magnitudes are seen as a DC component and can be controlled by means of a simple PI with zero tracking error.

The transformation matrix is obtained by multiplying [PAR] and [CLA]:

$$[T] = [PAR][CLAR] = \begin{bmatrix} cos(\omega_0 t) & sin(\omega_0 t) & 0 \\ -sin(\omega_0 t) & cos(\omega_0 t) & 0 \\ 0 & 0 & 1 \end{bmatrix} \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \tag{2.20}$$

Obtaining the transformation matrix [T]:

$$[T] = \sqrt{\frac{2}{3}} \begin{bmatrix} cos(\omega_0 t) & cos(\omega_0 t - \frac{2\pi}{3}) & cos(\omega_0 t + \frac{2\pi}{3}) \\ -sin(\omega_0 t) & -sin(\omega_0 t - \frac{2\pi}{3}) & -sin(\omega_0 t + \frac{2\pi}{3}) \\ \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} \end{bmatrix} \tag{2.21}$$

The inverse of [T] is again equal to its transpose.

The application of [T] directly converts the real magnitudes to its equivalent in a rotating frame, with an angular velocity ω_0.

$$i_{dqz} = [T] i_{abc} \tag{2.22}$$

This rotating frame is also called synchronous reference frame (SRF). The effects of the Clarke and Park transformations are represented in

Figure 2.12. The voltage v has three components; a,b and c. If this voltage is represented in the abc reference frame, it is seen as a rotational vector with an angular frequency equal to ω_0. If this voltage is projected in the $\alpha\beta$ reference frame, the vector can be decomposed in two components that also vary at the same angular frequency and a third component orthogonal to α and β. If v is transformed to the rotating axis dq, the projections are seen as a DC component.

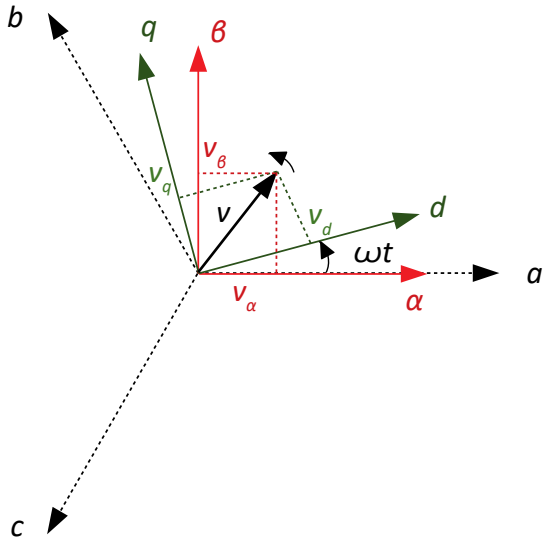


Figure 2.12: Clarke and Park transformations.

The current can be controlled in the SRF with the control structure shown in Figure 2.13. It can be seen in this schematic, that the angle θ ($\omega_0 t$) for the transformation is obtained by means of a phase-locked loop (PLL) from the capacitor voltage, which is mainly determined by the grid voltage. In this way, the grid fundamental component is seen in the SRF as a DC component.

In the SRF, the **PI** controller is the most interesting option, as it offers infinite magnitude at 0 Hz, achieving zero tracking error of the current references, which are also DC components. Moreover, in the modeling of permanent magnet generators with salient poles, it allows to achieve time-invariant parameters in the model, so the traditional transfer function approach can be used.

The control of the electrical variables in the SRF is widely extended to regulate the power transfer to both the machine and the grid. The plant dynamics between the converter voltage and the converter current are

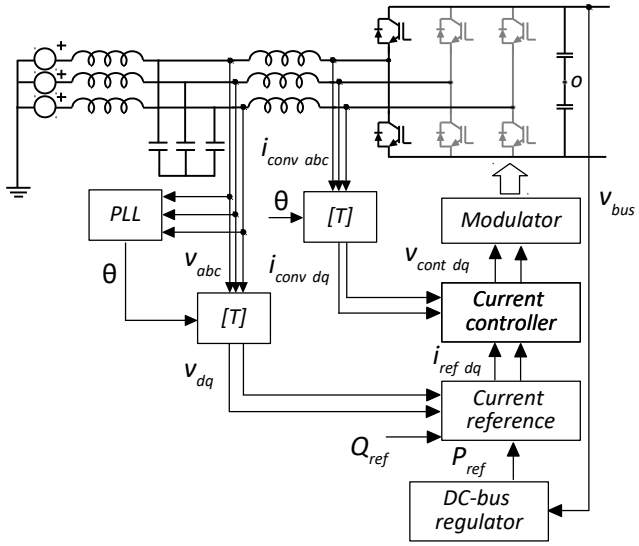


Figure 2.13: Diagram representation of the vectorial current control in the synchronous reference frame.

determined in Subsection 2.3.2 and Subsection 2.3.3, while the current regulator is studied in Subsection 2.3.4.

2.3.2 Model of the basic passive components

The *LCL* output filter of GSC contains all the basic elements of any electrical circuit: resistors inductor and capacitors, as represented in Figure 2.14. As a first step to obtain the plant, correlating the converter current with the converter voltage, the models in the SRF of the basic components are developed.

As we are interested in modeling the power transferred to the grid, only the *dq* axis are modeled in the following, neglecting the *z* axis. With this simplification, [T] becomes:

$$[T] = \sqrt{\frac{2}{3}} \begin{bmatrix} cos(\omega_0 t) & cos(\omega_0 t - \frac{2\pi}{3}) & cos(\omega_0 t + \frac{2\pi}{3}) \\ -sin(\omega_0 t) & -sin(\omega_0 t - \frac{2\pi}{3}) & -sin(\omega_0 t + \frac{2\pi}{3}) \end{bmatrix} \tag{2.23}$$

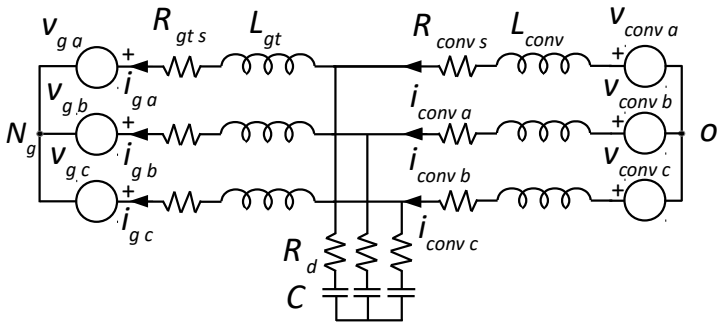


Figure 2.14: *LCL* filter.

2.3.2.1 SRF model of a three-phase resistor

If $v_{R\ dq}$ is the voltage across the resistor in the dq axis and $v_{R\ abc}$ is the real magnitude voltage:

$$v_{R\ dq} = [T]v_{R\ abc} \tag{2.24}$$

By substituting the basic equation of the resistor:

$$v_{R\ dq} = [T]v_{R\ abc} = [T][R]i_{R\ abc} = [T][R][T]^{-1}i_{R\ dq} \tag{2.25}$$

where $i_{R\ abc}$ and $i_{R\ dq}$ are the real currents and their dq projection, respectively and $[R]$ is a diagonal matrix:

$$[R] = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} \tag{2.26}$$

The product $[T][R][T]^{-1}$ is a two-by-two matrix:

$$v_{R\ dq} = \begin{bmatrix} R & 0 \\ 0 & R \end{bmatrix} i_{R\ dq} \tag{2.27}$$

An impedance matrix can be defined in the SRF for the resistor:

$$[Z_{R\ dq}] = \begin{bmatrix} R & 0 \\ 0 & R \end{bmatrix} \tag{2.28}$$

2.3.2.2 SRF model of three independent inductors

If $v_{L\ abc}$ and $v_{L\ dq}$ are the real magnitude voltages and dq voltages across the inductor, and $i_{L\ abc}$ and $i_{L\ dq}$ are the inductor real magnitude currents and in the dq axis:

$$v_{L\ dq} = [T]v_{L\ abc} = [T][L]\frac{di_{L\ abc}}{dt} = [T][L]\frac{d([T]^{-1}i_{L\ dq})}{dt} \tag{2.29}$$

with $[L]$ being equal to a diagonal matrix for three decoupled inductor.

$$[L] = \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{bmatrix} \tag{2.30}$$

$[T]$ depends on time, and consequently $[T]^{-1}$ is also time dependent, so the product $\frac{d([T]^{-1}i_{L\ dq})}{dt}$ must be derivated, obtaining:

$$v_{L\ dq} = \begin{bmatrix} L & 0 \\ 0 & L \end{bmatrix}\frac{di_{L\ dq}}{dt} + \begin{bmatrix} 0 & -L\omega_0 \\ L\omega_0 & 0 \end{bmatrix} i_{L\ dq} \tag{2.31}$$

$$v_{L\ dq} = \begin{bmatrix} L\frac{di_{L\ d}}{dt} & -L\omega_0 i_{L\ q} \\ L\omega_0 i_{L\ d} & L\frac{di_{L\ q}}{dt} \end{bmatrix} \tag{2.32}$$

From this equation, the equivalent circuit of Figure 2.15 can be obtained for three decoupled inductors in the SRF. It can be seen that a cross-coupling between the dq axis appears, and can be represented as current dependent voltage sources.

As the system is linear and time-invariant, it can be modeled in the Laplace

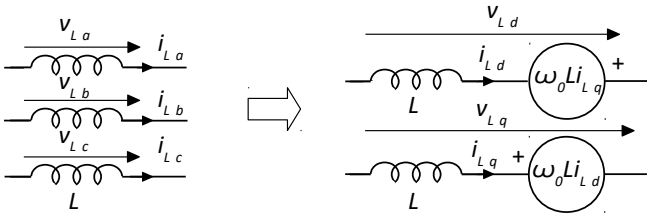


Figure 2.15: Equivalent model in the SRF of three decoupled inductances.

domain.

$$V_{L\ dq}(s) = \begin{bmatrix} Ls & -L\omega_0 \\ L\omega_0 & Ls \end{bmatrix} I_{L\ dq}(s) \tag{2.33}$$

So an impedance matrix in the SRF can be defined; $[Z_{L\ dq}(s)]$:

$$[Z_{L\ dq}(s)] = \begin{bmatrix} Ls & -L\omega_0 \\ L\omega_0 & Ls \end{bmatrix} \tag{2.34}$$

Expressing the current as a function of the voltage across the inductor:

$$I_{L\ dq}(s) = \begin{bmatrix} \frac{s}{L(s^2+\omega_0^2)} & \frac{\omega_0}{L(s^2+\omega_0^2)} \\ -\frac{\omega_0}{L(s^2+\omega_0^2)} & \frac{s}{L(s^2+\omega_0^2)} \end{bmatrix} V_{L\ dq}(s) \tag{2.35}$$

2.3.2.3 SRF model of a three-phase inductor

To derive the model of a three-phase inductor, the only change required is a change in the matrix [L], which becomes:

$$[L] = \begin{bmatrix} L & -L/2 & -L/2 \\ -L/2 & L & -L/2 \\ -L/2 & -L/2 & L \end{bmatrix} \tag{2.36}$$

This matrix is valid for a three-phase inductor whose reluctances are equal in the three legs and with negligible leakage inductances. This matrix is applicable to symmetric three-phase inductances, and in three-phase inductances with an air-gap that is dominant face to the core reluctances.

Developing Equation 2.29 for the three-phase inductor, the following expression is obtained:

$$v_{L\ dq} = \frac{3}{2}\begin{bmatrix} L & 0 \\ 0 & L \end{bmatrix} \frac{di_{L\ dq}}{dt} + \frac{3}{2}\begin{bmatrix} 0 & -L\omega_0 \\ L\omega_0 & 0 \end{bmatrix} i_{L\ dq} \tag{2.37}$$

This equation is similar to the one obtained for the three decoupled inductors, but in this occasion a gain of 3/2 multiplies the self-inductance.

The dq impedance matrix of the three-phase inductor; $[Z_{L\ dq}(s)]$ is equal to:

$$[Z_{L\ dq}(s)] = \frac{3}{2}\begin{bmatrix} Ls & -L\omega_0 \\ L\omega_0 & Ls \end{bmatrix} \tag{2.38}$$

2.3.2.4 SRF model of the capacitors

The same procedure can be developed for the capacitor. If $v_{C\ abc}$ and $v_{C\ dq}$ are the real magnitude phase voltages and dq voltages across the capacitor, and $i_{C\ abc}$ and $i_{C\ dq}$ are the inductor real magnitude currents and the dq currents respectively:

$$i_{C\ dq} = [T]i_{C\ abc} = [T][C]\frac{dv_{C\ abc}}{dt} = [T][C]\frac{d([T]^{-1}v_{C\ dq})}{dt} \tag{2.39}$$

with $[C]$ being equal to:

$$[C] = \begin{bmatrix} C & 0 & 0 \\ 0 & C & 0 \\ 0 & 0 & C \end{bmatrix} \tag{2.40}$$

By developing Equation 2.39:

$$i_{C\ dq} = \begin{bmatrix} C & 0 \\ 0 & C \end{bmatrix} \frac{dv_{C\ dq}}{dt} + \begin{bmatrix} 0 & -C\omega_0 \\ C\omega_0 & 0 \end{bmatrix} v_{C\ dq} \tag{2.41}$$

From this equation, the equivalent circuit of Figure 2.16 can be obtained for the capacitors. The cross-coupling between the axis appears as voltage dependent current sources.

As the system is linear and time-invariant, it can be modeled in the Laplace

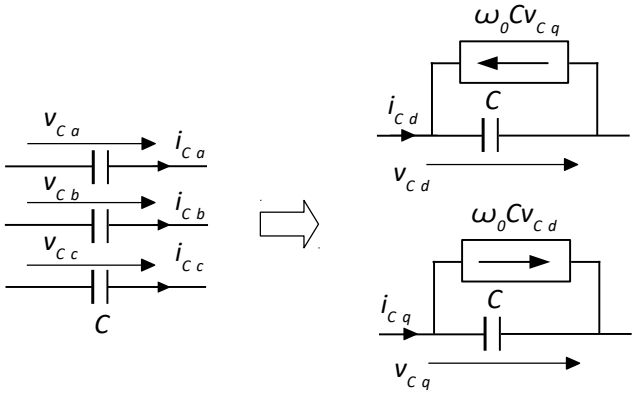


Figure 2.16: SRF model of three balanced capacitors.

domain.

$$I_{C\ dq}(s) = \begin{bmatrix} Cs & -C\omega_0 \\ C\omega_0 & Cs \end{bmatrix} V_{C\ dq}(s) \tag{2.42}$$

Expressing the voltage as a function of the current across the capacitor:

$$V_{C\ dq}(s) = \begin{bmatrix} \frac{s}{C(s^2+\omega_0^2)} & \frac{\omega_0}{C(s^2+\omega_0^2)} \\ -\frac{\omega_0}{C(s^2+\omega_0^2)} & \frac{s}{C(s^2+\omega_0^2)} \end{bmatrix} I_{C\ dq}(s) \tag{2.43}$$

So an impedance in the SRF can be defined; $[Z_{C\ dq}(s)]$:

$$[Z_{C\ dq}(s)] = \begin{bmatrix} \frac{s}{C(s^2+\omega_0^2)} & \frac{\omega_0}{C(s^2+\omega_0^2)} \\ -\frac{\omega_0}{C(s^2+\omega_0^2)} & \frac{s}{C(s^2+\omega_0^2)} \end{bmatrix} \tag{2.44}$$

2.3.3 Model of the *LCL* filter

Once the models for all the components that form the LCL filter have been developed in the SRF, the complete model for the filter can be built. In the LCL filter represented in Figure 2.14, the converter side inductance, L_{conv}, has a series equivalent resistance $R_{conv\ s}$, and the sum of the transformer leakage inductance, L_{transf}, and the grid inductance, L_g, denoted by L_{gt}, has a series equivalent resistance $R_{gt\ s}$. The filter capacitor branch includes a damping resistor, R_d, in series with the filter capacitor, C, in order to damp the LCL resonance.

This filter can be translated into the SRF using the equivalent models developed in Subsection 2.3.2 for each of the basic passive components, obtaining the equivalent circuit in Figure 2.17. The equivalent model in the dq components can be transformed into a Laplace domain model, in order to obtain the transfer functions that model the system dynamics, obtaining the representation in Figure 2.18.

Deriving the plant model in the Laplace domain, correlating the converter current and the converter voltage, from this diagram requires a great deal of algebraic manipulations, due to the existence of the cross-coupling terms. A six order transfer function is obtained, whose interpretation is not practical, for this reason, a different modeling approach is followed. Instead of manipulating the blocks, the dq impedances defined in Subsection 2.3.2, which already contain the cross-couplings, are going to be used to build a meaningful block diagram representation. By operating with

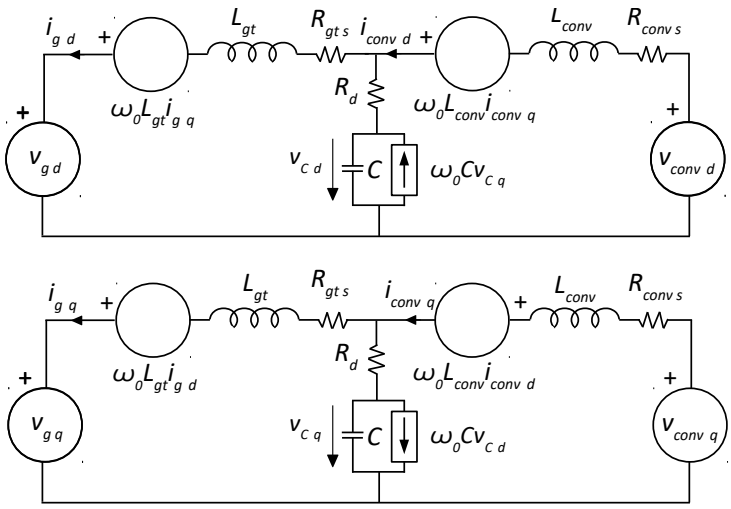


Figure 2.17: *LCL* filter in the synchronous reference frame.

the matrices of each component, the algebra is simplified, and the transfer functions can be derivated in a more intuitive and comprehensive way.

From Figure 2.14, the model in the SRF of the *LCL* filter represented in Figure 2.19 can be obtained by directly using the matrix impedances. This circuit is similar to the representation of a single phase *LCL* filter, except for the fact that the impedances are matrices and this circuit has the two

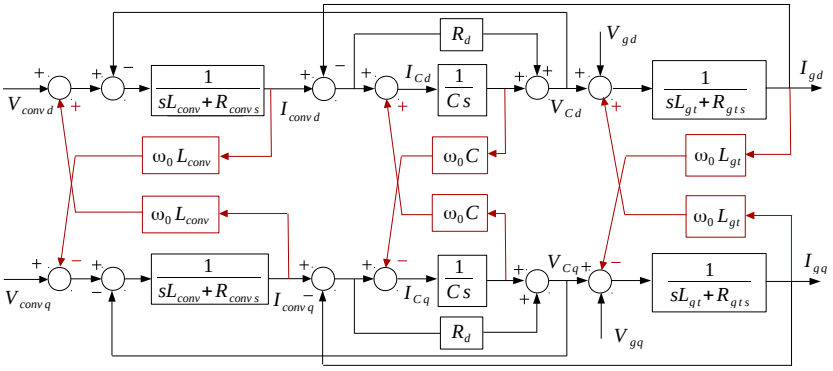


Figure 2.18: Laplace domain representation of the *LCL* filter modeled in the SRF.

components d and q. The impedances in Figure 2.19 are defined as:

$$[Z_{L\ conv}(s)] = \begin{bmatrix} L_{conv}s & -L_{conv}\omega_0 \\ L_{conv}\omega_0 & L_{conv}s \end{bmatrix} \tag{2.45}$$

$$[Z_{R\ convs}(s)] = \begin{bmatrix} R_{convs} & 0 \\ 0 & R_{convs} \end{bmatrix} \tag{2.46}$$

$$[Z_{L\ gt}(s)] = \begin{bmatrix} L_{gt}s & -L_{gt}\omega_0 \\ L_{gt}\omega_0 & L_{gt}s \end{bmatrix} \tag{2.47}$$

$$[Z_{R\ gts}(s)] = \begin{bmatrix} R_{gts} & 0 \\ 0 & R_{gts} \end{bmatrix} \tag{2.48}$$

$$[Z_C(s)] = \begin{bmatrix} \frac{s}{C(s^2+\omega_0^2)} & \frac{\omega_0}{C(s^2+\omega_0^2)} \\ -\frac{\omega_0}{C(s^2+\omega_0^2)} & \frac{s}{C(s^2+\omega_0^2)} \end{bmatrix} \tag{2.49}$$

$$[Z_{R\ d}(s)] = \begin{bmatrix} R_d & 0 \\ 0 & R_d \end{bmatrix} \tag{2.50}$$

In Figure 2.19 the impedances can be grouped, defining three impedances, $[Z_{LR\ conv}]$, $[Z_{LR\ gt}]$ and $[Z_{CRd}]$, equal to the sum of each inductance and capacitor with its series resistor:

$$[Z_{LR\ conv}(s)] = [Z_{L\ conv}(s)] + [Z_{R\ convs}(s)] = \begin{bmatrix} L_{conv}s + R_{convs} & -L_{conv}\omega_0 \\ L_{conv}\omega_0 & L_{conv}s + R_{convs} \end{bmatrix} \tag{2.51}$$

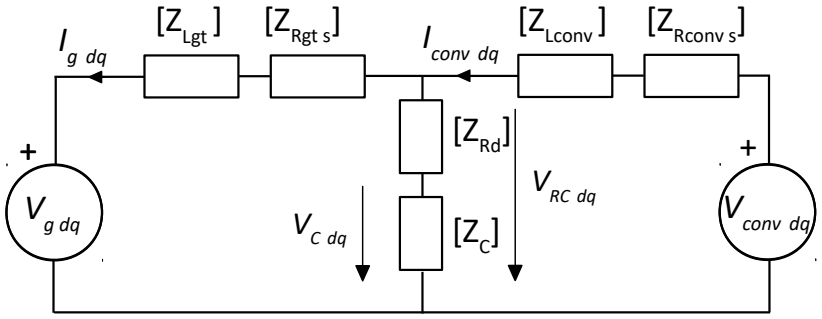


Figure 2.19: Matrix impedance representation of the LCL filter in the SRF.

$$[Z_{LR\ gt}(s)] = [Z_{L\ gt}(s)] + [Z_{R\ gts}(s)] = \begin{bmatrix} L_{gt}s + R_{gts} & -L_{gt}\omega_0 \\ L_{gt}\omega_0 & L_{gt}s + R_{gts} \end{bmatrix} \quad (2.52)$$

$$[Z_{CRd}(s)] = [Z_C(s)] + [Z_{R\ d}(s)] = \begin{bmatrix} \frac{s}{C(s^2+\omega_0^2)} + R_d & \frac{\omega_0}{C(s^2+\omega_0^2)} \\ -\frac{\omega_0}{C(s^2+\omega_0^2)} & \frac{s}{C(s^2+\omega_0^2)} + R_d \end{bmatrix} \quad (2.53)$$

Taking into account these considerations, the transfer matrix correlating the converter current and the converter voltage can be obtained:

$$I_{conv\ dq}(s) = \left([Z_{LR\ conv}(s)] + [Z_{CRd}(s)]\left([Z_{LR\ gt}(s)]^{-1}[Z_{CRd}(s)] + I\right)^{-1}\right)^{-1} V_{conv\ dq}(s) \quad (2.54)$$

This matrix, that correlates $I_{conv\ dq}(s)$ and $V_{conv\ dq}(s)$, is named $[G_{iv}(s)]$:

$$[G_{iv}(s)] = \left([Z_{LR\ conv}(s)] + [Z_{CRd}(s)]\left([Z_{LR\ gt}(s)]^{-1}[Z_{CRd}(s)] + I\right)^{-1}\right)^{-1} \quad (2.55)$$

The bode plot representation of $[G_{iv}(s)]$ is shown in Figure 2.20. It is clear from this representation that the diagonal terms of the resulting 2×2 matrix are equal, while the anti-diagonal terms have the same magnitude but are phase shifted by 180 degrees.

The terms of $[G_{iv}(s)]$ have the following symmetry:

$$I_{conv\ dq}(s) = [G_{iv}(s)]V_{conv\ dq}(s) = \begin{bmatrix} G_{iv\ 1}(s) & G_{iv\ 2}(s) \\ -G_{iv\ 2}(s) & G_{iv\ 1}(s) \end{bmatrix} V_{conv\ dq}(s) \quad (2.56)$$

where $G_{iv\ 1}(s)$ and $G_{iv\ 2}(s)$ are six order transfer functions, too long to be reproduced here, but calculated by means of Equation 2.54.

To better understand the grid connection of the power converter through the *LCL* filter and the model in the SRF, the transfer matrices obtained are represented for the parameters given in Table 2.2. These parameters correspond to a grid-connected three-phase power converter in the Renewable Energies Laboratory of the Public University of Navarre, used for general control tests. This system is going to be used for the validation of the decoupling strategy that will be presented in Chapter 3.

$G_{iv\ 1}(s)$ and $G_{iv\ 2}(s)$ are represented in Figure 2.20 and Figure 2.21. At low frequencies $G_{iv\ 2}(s)$ is dominant, showing that at low frequencies (50 Hz in real magnitude) the *LCL* filter behaves as an inductor. When a voltage is

Table 2.2: System parameters of a low power VSC.

Parameter	Symbol	Value
Converter inductance	L_{conv}	2.2 mH
Converter inductance series resistance	$R_{conv\ s}$	100 $m\Omega$
Grid side inductance	L_{gt}	1 mH
Grid side inductance series resistance	$R_{gt\ s}$	70 $m\Omega$
Filter capacitor	C	10 μF
Damping resistor	R_d	1Ω

applied in the d axis, a current is created, but lagged by 90 degrees, so it is seen in the q axis, while in the d axis a small current component appears, and is determined by the inductor series resistor. At 50 Hz in dq, the inductor shows a magnitude peak. This peak corresponds to the infinite gain that a pure inductor shows at 0 Hz, only limited by the inductor equivalent series resistance. As the frequency becomes higher, the capacitive branch is more important, and the resonance of the capacitor and the grid inductance can be appreciated, followed by the LCL resonance frequency. In the following, instead of representing the four Bode diagrams as in Figure 2.20, only the two elements of the matrix, the diagonal and anti-diagonal terms, would be represented, as this symmetry is maintained for the rest of transfer matrices.

The transfer matrix correlating the capacitor voltage and the converter current is also calculated, as it is going to be used later:

$$V_{RC\ dq}(s) = \left(I + [Z_{LR\ conv}(s)]\left([Z_{CRd}(s)]\left([Z_{LR\ gt}(s)]^{-1}[Z_{CRd}(s)] + I\right)^{-1}\right)^{-1}\right)^{-1} V_{conv\ dq}(s) \tag{2.57}$$

In this case, another matrix is defined $[G_{vv}(s)]$, which correlates $V_{RC\ dq}(s)$ and $V_{conv\ dq}(s)$, with the same symmetry as $[G_{iv}(s)]$. Its diagonal term is $G_{vv\ 1}(s)$ and its anti-diagonal term $G_{vv\ 2}(s)$.

$$V_{RC\ dq}(s) = [G_{vv}(s)]V_{conv\ dq}(s) = \begin{bmatrix} G_{vv\ 1}(s) & G_{vv\ 2}(s) \\ -G_{vv\ 2}(s) & G_{vv\ 1}(s) \end{bmatrix} V_{conv\ dq}(s) \tag{2.58}$$

Lastly, the influence of the grid voltage in the converter current, another important aspect in grid-connected power converters, is studied from the

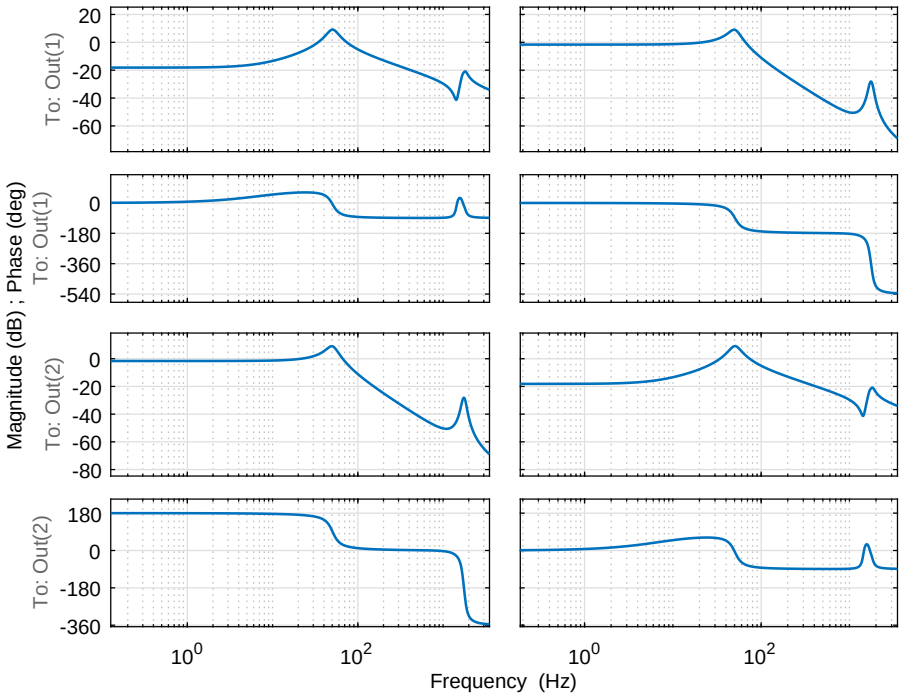


Figure 2.20: Bode plot of the transfer matrix correlating $I_{conv\ dq}(s)$ and $V_{conv\ dq}(s)$.

transfer matrix that correlates $I_{conv\ dq}$ with $V_{g\ dq}$:

$$I_{conv\ dq}(s) = -\left([Z_{LR\ conv}(s)] + [Z_{LR\ gt}(s)]\left(I + [Z_{CRd}(s)]^{-1}[Z_{LR\ conv}(s)]\right)\right)^{-1} V_{g\ dq}(s) \tag{2.59}$$

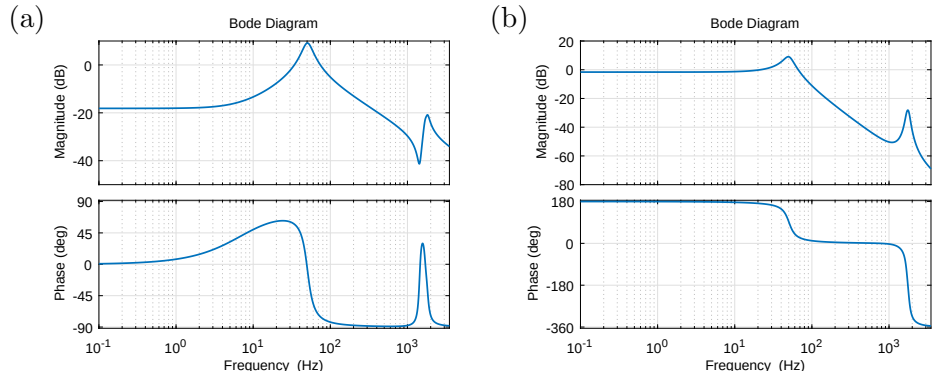


Figure 2.21: Bode plot representation of $G_{iv\ 1}(s)$ (a) and $G_{iv\ 2}(s)$ (b).

Once more, the same symmetry is obtained, and the matrix $[G_{dist}(s)]$ is defined, which correlates $I_{conv\ dq}(s)$ and $V_{g\ dq}(s)$, with a diagonal term $G_{dist\ 1}(s)$ and a anti-diagonal term $G_{dist\ 2}(s)$.

$$I_{conv\ dq}(s) = [G_{dist}(s)]V_{g\ dq}(s) = \begin{bmatrix} G_{dist\ 1}(s) & G_{dist\ 2}(s) \\ -G_{dist\ 2}(s) & G_{dist\ 1}(s) \end{bmatrix} V_{g\ dq}(s) \quad (2.60)$$

Influence of the variability of the grid inductance on the plant

In Subsection 2.3.3 all the parameters were known for the Bode plot representations, however, the grid inductance may suffer strong variations. The same power converter can be connected to strong and weak grids. Moreover for a given location, the effective grid inductance can vary at the point of common-coupling (PCC), depending on the power injected to the grid by the surrounding power converters [AGO11].

A parameter called short-circuit ratio (SCR) is normally used to define whether a grid is strong or weak. It is the ratio of the grid short-circuit power (S_{cc}) to the rated power connected at the PCC (S_R).

$$SCR = \frac{S_{cc}}{S_R} \quad (2.61)$$

By manipulating this expression, the grid inductance, L_g, can be found as a function of the grid line voltage, V_g, the grid fundamental frequency, F_g, and the rated power connected at the PCC.

$$L_g = \frac{V_g}{2\pi F_g SCR\ S_R} \quad (2.62)$$

If the SCR is low, for a given S_R the grid inductance is high and the grid is weak. If the SCR is high, for the same S_R the grid inductance is low and the grid is strong.

The variations in the grid inductance strongly modify the LCL filter frequency response. The frequency response of the converter current to the capacitor voltage in the dq axis is analyzed, what has been called $[G_{iv}(s)]$, by means of the Bode plots of $G_{iv\ 1}(s)$ and $G_{iv\ 2}(s)$ in Figure 2.22.

From this figure, it is clear that the variability of the grid inductance strongly influences the system dynamics. At low frequencies, the gain is highly reduced in weak grids. Moreover, the resonance of the capacitor and the grid inductance moves towards lower frequencies, what can strongly affect the

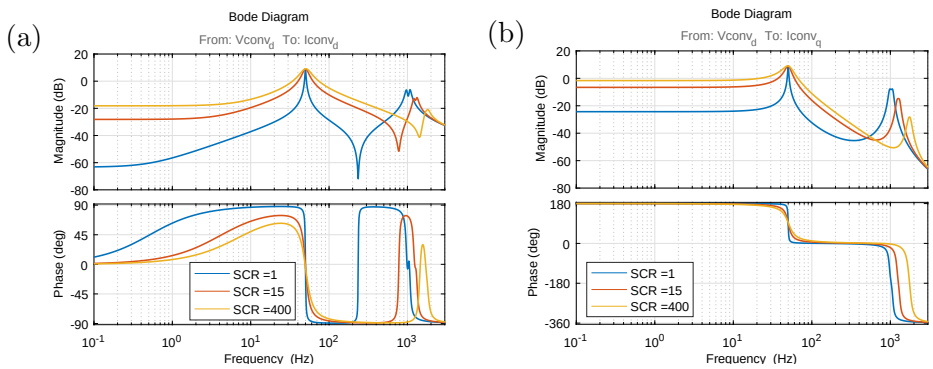


Figure 2.22: Bode plot representation of $G_{iv\ 1}(s)$ (a) and $G_{iv\ 2}(s)$ (b) for three different short-circuit ratios; 1, 15 and 100.

current loop stability. At last, the *LCL* resonance frequency is also moved towards lower frequencies with greater magnitude peaks, something that can compromise the stability.

In Chapter 3 the stability problems that may arise in the current control loop, within the control bandwidth, when a power converter is connected to weak grids, are faced through the design of a current controller that includes a multiple-input-multiple-output (MIMO) based decoupling strategy. In Chapter 4, the influence that the connection of power converters to weak grids has on the *LCL* resonance frequency, which is above the control bandwidth, and the corresponding stability problems are tackled, proposing an active damping (AD) strategy.

2.3.4 Description and modeling of the current control loop

A detailed representation of the current control loop in the synchronous reference frame, briefly introduced in Figure 2.13, is provided in Figure 2.23.

In this control loop, the capacitor voltage and the converter current measurements are filtered by a low pass analog filter, LPAF. These measurements are sampled by a digital signal processor (DSP), where the control loops are executed. The PLL, receiving the capacitor voltage filtered measurements through a SOGI filter [XIA17], used to select the fundamental component, provides the angle for the transformation to the SRF. In this thesis it is assumed that the PLL provides the correct angle for the transformations, ignoring the instabilities that may be originated in the PLL when the converter is connected to weak grids [DON15].

The filtered variables are transformed to the *dq* axis using matrix [T].

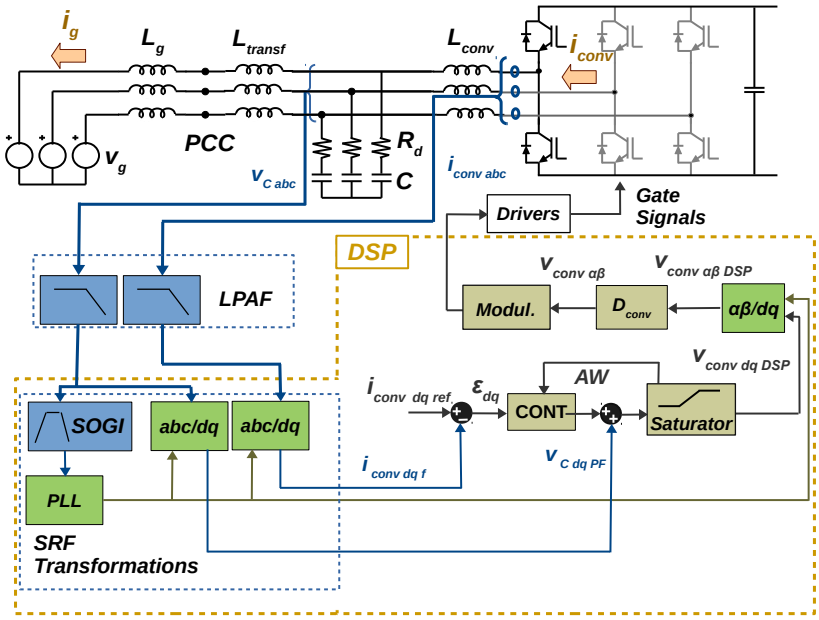


Figure 2.23: Detailed diagram of the current control loop.

Each current component is controlled by a PI controller. At the output of the controller, the capacitor voltage is added. The sum of the controller and the capacitor voltages is saturated to avoid overmodulation, using an anti-windup (AW) for the PI.

The required action in the SRF is transformed back to $\alpha\beta$ and the modulator determines the switching orders for every individual switch.

This general overview of the control loop is useful to identify all the elements. Nevertheless, to properly study the system stability, a detailed model of each of these elements is required and developed in the following.

2.3.4.1 Modeling the digital control implementation

Power converters are commonly controlled by means of a digital signal processor (DSP) or by means of a field-programmable-array (FPGA). The digital control of power converters offers multiple benefits, such as the possibility of implementing more complex algorithms, the simplicity to modify the control strategy, the reduction of the number of components, the higher reliability and the possibility of tracking the variables in a SCADA system.

The digital control implementation also introduces some limitations: the

computation times are increased, due to the sequential implementation of the calculations and the time that each of these calculations requires. Moreover, the measurements have to be converted to digital signals before using them in the DSP. As a consequence, delays are introduced in the current control loop that may degrade the control loop stability margins and impose limits on the control loop bandwidth. Moreover, to precisely study the stability of digital systems, the discrete domain z has to be used. Nevertheless, the discrete domain is less intuitive than the Laplace domain, making the identification of the possible stability problems and required ccontol strategies more difficult to identify. For this reason, it is common to approximate digital functions by their equivalent continuous transfer functions. In this thesis, the Laplace domain is used to model all the elements. Consequently, the singularities of the digitally controlled systems have to be carefully modeled:

1. Sampler. In a digitally controlled system, the electrical variables have to be sampled, so this effect has to be modeled in the continuous approximation of the digital system. Furthermore, it is a common approach sampling the converter variables once or twice per switching frequency, what it is called symmetrical or asymmetrical sampling. These sampling approaches introduce a lower harmonic content and lower noise is contained in the measurements if these samples are taken when the power converter does not introduce commutations, at the peaks and valleys of the carrier frequency [HOL03]. As proposed by [HOU99, HOU13] the sampling behavior can be modeled by a gain:
$$\frac{1}{T_{samp}} \tag{2.63}$$
where T_{samp} is the sampling time of the digital controller

2. Computational delay. The calculation time of the DSP is not negligible if compared with the sampling time, the time between two consecutive samples taken by the DSP. For these reasons, the computational delay is normally equal to a sampling period:
$$e^{-T_{samp}s} \tag{2.64}$$

3. In the discrete analysis of power converters, the LCL plant is discretized with the zero order hold transformation, modeling that the power converter keeps, during a sampling period, the control action at the same value [LIS04, LIS05, WU06]. It can be modeled in the continuous domain by [HOU99, HOU13]:
$$\frac{1 - e^{-T_{samp}s}}{s} \tag{2.65}$$

Taking into account 1-3, the modeling of the digital control is given by $D_{conv}(s)$:

$$D_{conv}(s) = \frac{e^{-T_{samp}s}(1 - e^{-T_{samp}s})}{T_{samp}s} \tag{2.66}$$

By using Equation 2.66, the transfer functions become non-rational, due to the existence of pure delays, and *Matlab* has some issues when operating with them. For this reason, this expression has been traditionally approximated. [BLA96] approximated Equation 2.66 by a first order low pass filter:

$$D_{conv}(s) \approx \frac{1}{1.5T_{samp}s + 1} \tag{2.67}$$

However, this approximation is not very rigorous. [AGO11] calculated a more accurate and rigorous expression to approximate Equation 2.66, by substituting the first order *Padé* approximation for the delay:

$$e^{-T_{samp}s} \approx \frac{1 - 0.5T_{samp}s}{1 + 0.5T_{samp}s} \tag{2.68}$$

in Equation 2.66, obtaining a second order transfer function:

$$D_{conv}(s) \approx \frac{1 - 0.5T_{samp}s}{(1 + 0.5T_{samp}s)^2} \tag{2.69}$$

Equation 2.69 provides a precise approximation for $D_{conv}(s)$ in a wider frequency range than Equation 2.67. However, if the stability has to be analyzed close to the DSP Nyquist frequency it does not provide accurate results. This is the case that will be analyzed in Chapter 4, for this reason, a more accurate representation of the digital control is required and developed in this thesis. To derive this approximation, the procedure presented in [AGO11] is followed. The second order *Padé* approximation is used to approximate the delay:

$$e^{-T_{samp}s} \approx \frac{1 - \frac{1}{2}T_{samp}s + \frac{1}{12}T_{samp}^2s^2}{1 + \frac{1}{2}T_{samp}s + \frac{1}{12}T_{samp}^2s^2} \tag{2.70}$$

By substitution of this second order approximation in Equation 2.66 a fourth order expression is derived:

$$D_{conv}(s) \approx \frac{12(T_{samp}^2s^2 + 12 - 6T_{samp}s)}{(T_{samp}^2s^2 + 6T_{samp}s + 12)^2} \tag{2.71}$$

The accuracy of the approximations in Equations 2.67, 2.69 and 2.71 is compared with the "exact" transfer function of Equation 2.66 in Figure 2.24. For the representation in Figure 2.24, a sampling frequency of 4 kHz has been used, meaning that the Nyquist frequency is 2 kHz, marked with the black line. The first order approximation of Equation 2.67 does not reproduce the emulation of the digital control, while the second order approximation of Equation 2.69 matches the "exact" representation up to a third of the control Nyquist frequency. The fourth order expression calculated in this thesis and provided in Equation 2.69, is able to perfectly reproduce the emulation of the digital control up to the Nyquist frequency. This expression would be the one used in the following sections.

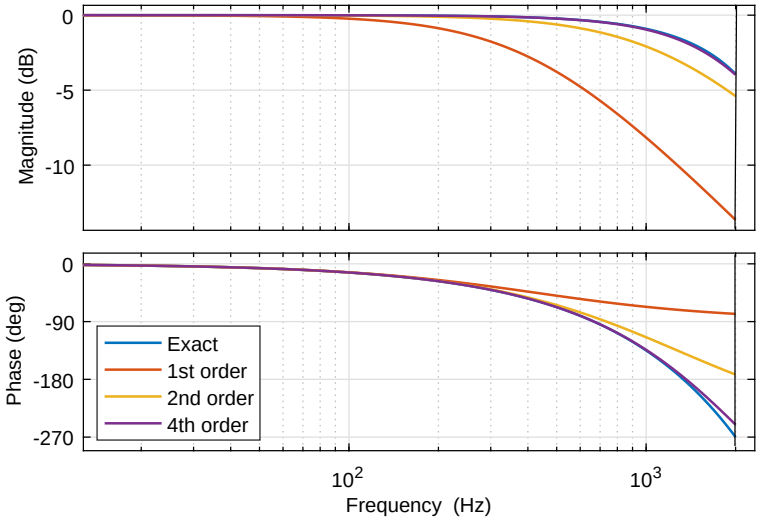


Figure 2.24: Bode plot of the different approximations for the emulation of the digital control.

2.3.4.2 Filters

All the currents and voltages measured in the power converter contain noise and undesired switching ripple. For this reason, all the measurements fed to the control loop must be filtered. In a digitally controlled power converter, both analog and digital filters may coexist.

Analog filter

Usually, all the measured variables are filtered by a low-pass first-order

analog filter, $LPAF(s)$:

$$LPAF(s) = \frac{1}{\tau_{lp}s + 1} \tag{2.72}$$

In high power converters, the filter cut-off frequency is located relatively close to the switching frequency. This is caused by the low switching frequency of these converters, normally between 2 and 5 kHz, and the negative effects that a filter located one decade below the switching frequency would have in the system stability. The attenuation introduced by the filter at the switching frequency is limited, however, it is really effective to eliminate the high frequency noise and the corresponding aliasing.

Digital filters

Many high power converters include an FPGA to filter the measurements fed to the DSP, where the controller is normally programmed [BUE09]. In this FPGA, running at a faster speed than the DSP, higher order digital filters, such as moving average filters, can be implemented in order to reduce the switching ripple and avoid aliasing in the measurements fed to the DSP. The moving-average filter (MAF) has the following expression:

$$MAF(z) = \frac{1 - z^{-N}}{N(1 - z^{-}1)} \tag{2.73}$$

where N is the ratio of the FPGA sampling frequency to the converter switching frequency. This filter has the frequency response plotted in Figure 2.25.

As seen in the magnitude plot, the switching harmonics can be attenuated. However, an important phase delay of 180 degree is introduced at the first switching harmonic family filtered, thus the MAF can compromise the stability margins. The transformation of this filter to the Laplace domain requires a high number of zeros and poles, so it is directly obtained through the *Matlab* tool *d2c()*.

The filters actuate on the real converter magnitudes, while D_{conv} is defined in $\alpha\beta$, however the control is performed in the SRF. To properly analyze the stability of the current control loop in Figure 2.23 all the elements must be modeled in the same reference frame: the SRF. In the following section, the elements applied to the real magnitudes, i.e. $LPAF(s)$ and the elements defined in $\alpha\beta$, i.e. $D_{conv}(s)$, have to be translated into the SRF.

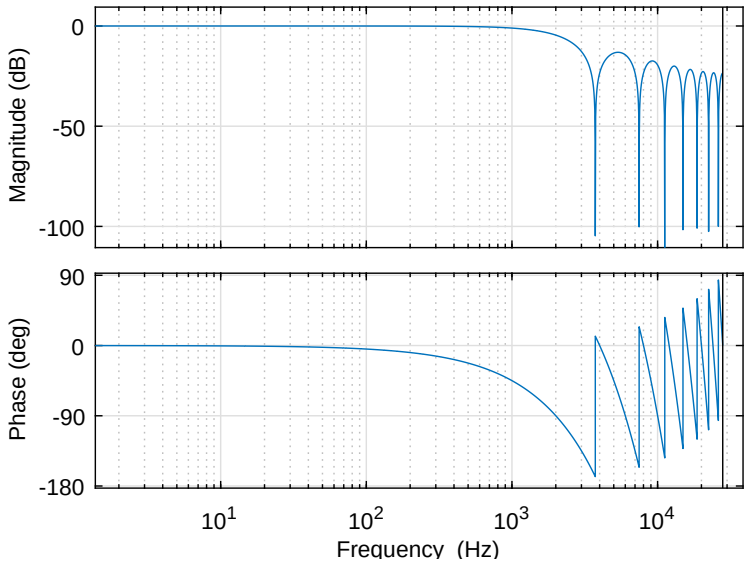


Figure 2.25: Bode plot of the moving-average filter.

2.3.4.3 Transformation of the elements within the current control loop to the SRF

$D_{conv}(s)$ and $LPAF(s)$ can be directly expressed in $\alpha\beta$ as diagonal matrices. As an example, the $\alpha\beta$ matrix of $LPAF(s)$ is shown:

$$\begin{Bmatrix} X_{f\alpha}(s) \\ X_{f\beta}(s) \end{Bmatrix} = \begin{bmatrix} LPAF(s) & 0 \\ 0 & LPAF(s) \end{bmatrix} \begin{Bmatrix} X_{\alpha}(s) \\ X_{\beta}(s) \end{Bmatrix} \tag{2.74}$$

This means that the filtered variable $X_{f\alpha}(s)$ is only affected by the component $X_{\alpha}(s)$, and similarly in the β axis.

Any diagonal matrix can be transformed to the SRF using the theory presented in [ZMO01]. According to this theory, the diagonal matrix is translated into the SRF as a symmetrical matrix, whose diagonal terms, $LPAF_1(s)$ in the case of the $LPAF(s)$, is obtained by calculating $LPAF(s + j\omega_0) + LPAF(s - j\omega_0)$, and the anti-diagonal term , $LPAF_2(s)$, from $(jLPAF(s + j\omega_0) - jLPAF(s - j\omega_0))$, ω_0 being the grid fundamental frequency:

$$\begin{Bmatrix} X_{fd}(s) \\ X_{fq}(s) \end{Bmatrix} = \frac{1}{2} \begin{bmatrix} LPAF_1(s) & LPAF_2(s) \\ -LPAF_2(s) & LPAF_1(s) \end{bmatrix} \begin{Bmatrix} X_{d}(s) \\ X_{q}(s) \end{Bmatrix} \tag{2.75}$$

In this way a matrix $[LPAF(s)]$ is defined that models $LPAF(s)$ in the

SRF. According to this matrix, when the filter is translated into the SRF, the filtered measurement in one axis is affected by the measurement in the other axis. By developing these terms, the components of $[LPAF(s)]$ are:

$$\begin{bmatrix} X_{fd}(s) \\ X_{fq}(s) \end{bmatrix} = \begin{bmatrix} \frac{\tau_{lp}s+1}{\tau_{lp}^2(s^2+\omega_0^2)+2\tau_{lp}s+1} & \frac{\tau_{lp}\omega_0}{\tau_{lp}^2(s^2+\omega^2)+2\tau_{lp}s+1} \\ -\frac{\tau_{lp}\omega_0}{\tau_{lp}^2(s^2+\omega_0^2)+2\tau_{lp}s+1} & \frac{\tau_{lp}s+1}{\tau_{lp}^2(s^2+\omega_0^2)+2\tau_{lp}s+1} \end{bmatrix} \begin{bmatrix} X_d(s) \\ X_q(s) \end{bmatrix} \tag{2.76}$$

note that the imaginary unit does not appear in any of the terms. By analyzing Equation 2.76 it is clear that if the cut-off frequency of this filter is increased, τ_{lp} is reduced, and the effect of the cross-coupling becomes weaker.

This procedure is similarly performed for $D_{conv}(s)$

$$\begin{bmatrix} V_{conv_d}(s) \\ V_{conv_q}(s) \end{bmatrix} = \begin{bmatrix} D_{conv1}(s) & D_{conv2}(s) \\ -D_{conv2}(s) & D_{conv1}(s) \end{bmatrix} \begin{bmatrix} V_{conv_{d_{DSP}}}(s) \\ V_{conv_{q_{DSP}}}(s) \end{bmatrix} \tag{2.77}$$

with $D_{conv1}(s) = D_{conv}(s+j\omega_0) + D_{conv}(s-j\omega_0)$ and $D_{conv2}(s) = jD_{conv}(s+j\omega_0) - jD_{conv}(s-j\omega_0)$.

2.3.4.4 Capacitor-voltage positive-feedback

The voltage difference across the inductor depends on the voltage imposed by the power converter and the capacitor voltage, the last being dominated by the grid voltage. For this reason, it is interesting making use of this information in the current control loop. The capacitor-voltage positive-feedback is commonly referred in the literature as capacitor-voltage feedforward. It basically consists in adding the capacitor voltage in the dq axis to the resulting PI action. In this way, the effect of the capacitor voltage is minimized. It is widely used to avoid high inrush currents during the converter connection [ZHO15], to improve the dynamic response during voltage dips, sags and overvoltages [ZHA16], and to suppress the current distortion caused by the presence of harmonics in the grid [ABE05, XU16].

2.3.4.5 Controller

The controller is programmed in the DSP, however, as the stability is studied in the Laplace domain, its equivalent continuous representation is used. One of the main advantages of controlling the converter current in the SRF is that a simple PI controller can be used to achieve zero tracking error. The

corresponding equation of the controller is:

$$PI(s) = K_p \frac{T_n s + 1}{T_n s} \tag{2.78}$$

The PI has a pole at the origin, to achieve an infinite gain in DC, and a zero, adjusted with T_n. In this way, a PI controller never adds phase. To increase the phase margins of the current controller some phase displacement might be added at some frequency ranges. With this aim, a lead-lag compensator is frequently included.

The lead-lag compensator, CLL, also has a pole and a zero, but the pole is located at higher frequencies than the zero, in such way that a positive phase can be added in a given range of frequencies. The expression of CLL is:

$$CLL(s) = \frac{s/z_l + 1}{s/p_l + 1} \tag{2.79}$$

where z_l and p_l can be adjusted to introduce the desired phase, φ_d, at the desired frequency, ω_d, by means of the following expressions:

$$p_l = \sqrt{\frac{\omega_d^2(1 + sin(\varphi_d))}{1 - sin(\varphi_d)}} \tag{2.80}$$

$$z_l = p_l \frac{1 + sin(\varphi_d)}{1 - sin(\varphi_d)} \tag{2.81}$$

2.3.5 Stability analysis and design of the controller

The control loop presented for the 5 kW power converter is considered, having a switching frequency equal to 3900 Hz and sampling the variables once per switching period (symmetrical sampling), as the sampling frequency of the digital controller, an Arduino Due, is limited by the high computational delay. The low pass analog filter has a cut-off frequency of 1 kHz.

As a first step the stability criterion used is presented and the transfer matrices that allow to study the system stability are characterized. The controller is later designed and the stability problems of the power converter outlined, being one of the goals of this thesis the solution of these instabilities.

2.3.5.1 Stability criterion

With the power converter and its control loops modeled in the SRF, cross-coupling terms appear between the different elements, and the system becomes a MIMO system. In a MIMO system, the closed-loop stability can be deduced from the open-loop transfer matrix, similarly to single-input single-output (SISO) systems. Nevertheless, it is convenient to introduce here some particular concepts concerning MIMO systems, which are relevant for the stability analysis.

The open-loop transfer matrix, $[H_{ol}(s)]$, of a general system with two inputs and two outputs, has the following form:

$$[H_{ol}(s)] = \begin{bmatrix} H_{d1}(s) & H_{a1}(s) \\ -H_{a2}(s) & H_{d2}(s) \end{bmatrix} \tag{2.82}$$

The eigenvalues of this matrix are equal to:

$$\lambda_{1,2}(s) = \frac{H_{d1}(s) + H_{d2}(s)}{2} \pm \sqrt{\left(\frac{H_{d1}(s) - H_{d2}(s)}{2}\right)^2 - H_{a1}(s)H_{a2}(s)} \tag{2.83}$$

and the closed-loop stability can be deduced from these eigenvalues by means of the *multivariable Nyquist stability criterion* [MAC89]. This criterion states that the number of closed-loop unstable poles, Z, is equal to the number of unstable poles in the open-loop transfer matrix, P, plus the number of clockwise encirclements around the (-1, 0) point of the the eigenvalues $\lambda_{1,2}(s)$. The Nyquist plot of the eigenvalues have to be represented for $s = j\omega$, with $-\infty < \omega < \infty$, at positive and negative frequencies.

$$Z = P + N \tag{2.84}$$

There is a straightforward relationship between the Nyquist diagrams and the Bode plots. The number of encirclements with (-1, 0) in the Nyquist diagram, are seen in the Bode plot as crossings with $\pm n180$ degree, with n equal to 1, 3, 5..., when the magnitude in the Bode plot is greater than 0 dB.

The eigenvalues can have all their coefficients real valued, having in these cases symmetric representation at positive and negative frequencies. However, they can have complex coefficients as a result of the root square calculation in Equation 2.83. In these cases, as the ones under consideration in this thesis, $\lambda_{1,2}(s)$ would have complex coefficients, and consequently, the Bode plots are not equal at positive and negative frequencies. For this reason, the number of -180 degree crossings has to be counted at positive and negative frequencies.

The open-loop transfer matrix of the system under study is symmetric, as all the transfer matrices previously presented, such as the plant, filters, controller and the model of the digital implementation of the control. $[H_{ol}(s)]$ can be expressed as:

$$[H_{ol}(s)] = \begin{bmatrix} H_1(s) & H_2(s) \\ -H_2(s) & H_1(s) \end{bmatrix} \tag{2.85}$$

The eigenvalues, in this case, are simplified and have the following expression:

$$\lambda_{1,2}(s) = H_1(s) \pm jH_2(s) \tag{2.86}$$

To analyze the closed-loop stability from the open loop transfer matrix, these two eigenvalues will be represented separately. The representation has to be made at positive and negative frequencies, as $\lambda_{1,2}(s)$ contain complex coefficients.

2.3.5.2 Calculation of the open-loop transfer matrix

In Subsection 2.3.3 the Laplace block diagram representation of each element proved to be more complex and less intuitive to obtain the plant transfer matrix than the matrix representation of the components. For this reason, in this section, the matrix notation is going to be used to derive the open loop transfer matrix.

In Figure 2.26 the current control loop is represented, including all the elements previously described: the low-pass analog filter $[LPAF(s)]$, the model of the digital control implementation $[D_{conv}(s)]$, the plant from the converter voltage to the converter current $[G_{iv}(s)]$, the plant from the converter voltage to the capacitor branch voltage $[G_{vv}(s)]$ and the controller $[CONT(s)]$, which commonly is a PI controller.

By manipulating the block diagram, the inner loop transfer matrix can be calculated. It is given by:

$$V_{conv\ dq} = (I - [D_{conv}(s)][LPAF(s)][G_{vv}(s)])^{-1}\,[D_{conv}(s)]V_{cont\ dq}(s) \tag{2.87}$$

if this matrix is named $[G_{in}(s)]$, the open loop transfer matrix $[H_{ol}(s)]$, from $\varepsilon_{dq}(s)$ to $I_{conv\ dqf}(s)$ is given by:

$$I_{conv\ dqf}(s) = [LPAF(s)][G_{iv}(s)][G_{in}(s)][CONT(s)]\varepsilon_{dq}(s) \tag{2.88}$$

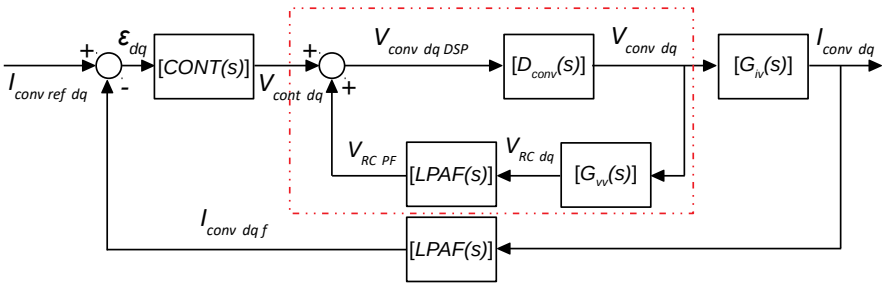


Figure 2.26: Converter current control diagram.

At this point, the closed loop stability can be analyzed from $[H_{ol}(s)]$:

$$[H_{ol}(s)] = [LPAF(s)][G_{iv}(s)][G_{in}(s)][CONT(s)] \tag{2.89}$$

$[H_{ol}(s)]$ retains the same symmetry than the rest of the elements previously defined, for this reason, the eigenvalues of this matrix are given by

$$\lambda_{1,2}(s) = H_1(s) \pm jH_2(s) \tag{2.90}$$

where $H_1(s)$ and $H_2(s)$ are respectively the diagonal and anti-diagonal terms.

2.3.5.3 Design of the controller

In the early developments of wind power, wind farms had a reduced power and were installed in developed countries, with strong grids. However, as wind power has been extended all over the world and the size of wind farms has grown, wind turbines are connected in many occasions to weak grids with extremely low SCRs. Some wind turbine manufacturers even demand the operation at SCRs equal to 1, meaning that the turbine rated power is equal to the short circuit power.

The first aspect that has to be considered before facing the design of the current control loop is the high variability of the plant that has to be controlled. This variability is caused by the variations in the grid inductance, which has an important impact in the system dynamics. These effects are analyzed in detail in Chapter 3 an Chapter 4. In this section three SCRs are considered for the design, 1, 15 and 100. In this way, we can analyze whether the power converter is stable or not, and with the desired dynamics for every grid condition. Through the design procedure, the main effects that the connection to weak grids have on the current control loop are outlined.

The control in the SRF is normally performed through a PI controller. However, to illustrate the effects of the grid inductance on the open-loop transfer matrix, the frequency response of the eigenvalues at positive and negative frequencies is represented in Figure 2.27 without the PI. From this figure, it can be clearly seen that the gain at low frequencies is strongly reduced in weak grids, meaning that the system becomes slower. The resonance of the grid side inductance and the capacitor voltage is moved towards lower frequencies, limiting the achievable controller bandwidth. At last, the LCL resonance frequency is also moved towards lower frequencies and its magnitude peak is increased.

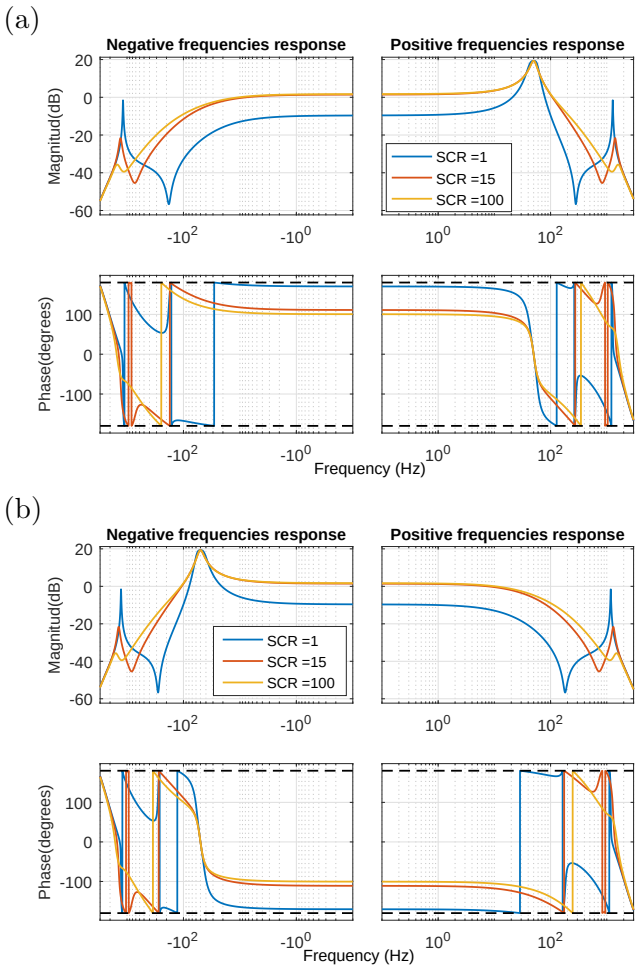


Figure 2.27: Frequency response of the eigenvalues of $[H_{ol}(s)]$ for three SCRs: 1, 15 and 100.

The frequency response of the eigenvalues of the open-loop transfer matrix determines the closed-loop stability. For this reason, the design of the controller is made from the Bode diagram of the two eigenvalues. As seen in Figure 2.27 the gain around 0 Hz is almost 0 dB. To achieve zero tracking error, the integrator of th PI controller is added, at this point the controller is simply:

$$[CONT(s)] = \begin{bmatrix} 1/s & 0 \\ 0 & 1/s \end{bmatrix} \tag{2.91}$$

When the integrator is included, the eigenvalues have an infinite magnitude at 0 Hz, as expected. Their frequency representation can be seen in Figure 2.28.

The open-loop transfer matrix has no unstable poles, and no -180 degree crossings with positive magnitude are visible in Figure 2.28. However, the closed-loop system is unstable, with two poles in the right-half plane (RHP) for every SCR. This instability is created by a -180 degree crossing that occurs at 0 Hz in both eigenvalues. If a different Bode plot is represented with a focus on 0 Hz, representing in the same graph positive and negative frequencies in Figure 2.29, those crossings can be seen.

In order to avoid this instability, an opposite crossing with -180 degree has to be introduced in the eigenvalues frequency response when the magnitude is positive. The current control bandwidth is set to 90 Hz for the lowest SCR, by adjusting the gain of the controller K_p, so the additional crossing must be produced within this bandwidth. If the zero of the PI is adjusted with T_n, to introduce at least a phase margin of 30 degrees at every gain crossover frequency of the eigenvalues, it can be seen that the required crossing to stabilize the closed-loop response can be obtained for the SCRs of 15 and a 100, but not for the weakest case under consideration, Figure 2.30. In this way, for weak grids, achieving the desired control bandwidth and phase margins while guaranteeing the system stability is not possible with a simple PI. Moreover, as the system is completely coupled, different crossover frequencies are obtained at positive and negative frequencies.

From Figure 2.30 it can be concluded that, to meet the goal of having a robust controller, able to operate at any grid, an additional phase of 40 degrees has to be introduced at 20 Hz in order to achieve the desired crossing that guarantees the stability for a SCR of 1. If this phase is added, the performance of the current controller is highly distorted for the strong grids considered, and consequently, it is not included.

To verify that the theory presented is able to predict the closed-loop

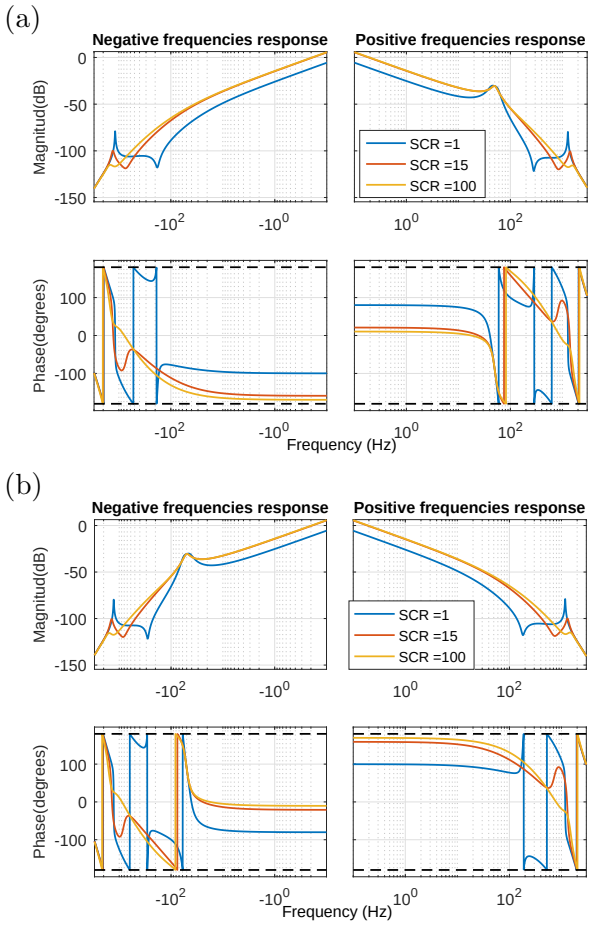


Figure 2.28: Frequency response of the eigenvalues of $[H_{ol}(s)]$, including the integrator, for three SCRs: 1, 15 and 100.

stability, in Figure 2.31 the zero-pole map is shown, with a zoom at the poles with the slowest dynamics. As expected, for a SCR of 15 and a 100, the system is stable, while for a weak grid, with a SCR of 1 it becomes unstable, with two RHP poles corresponding to each cross at the origin in $\lambda_1(s)$ and $\lambda_2(s)$.

In Chapter 3, a decoupling strategy is presented that allows the robust design of the controller to properly operate in different grid conditions.

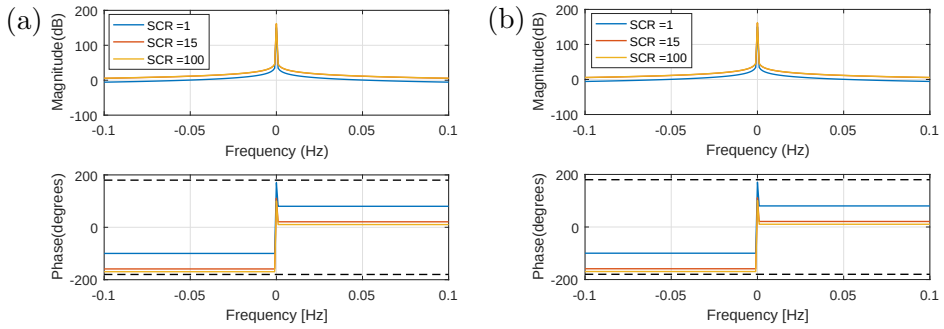


Figure 2.29: Frequency response of the eigenvalues of $[H_{ol}(s)]$, with a zoom at 0 Hz, including the integrator, for three SCRs: 1, 15 and 100.

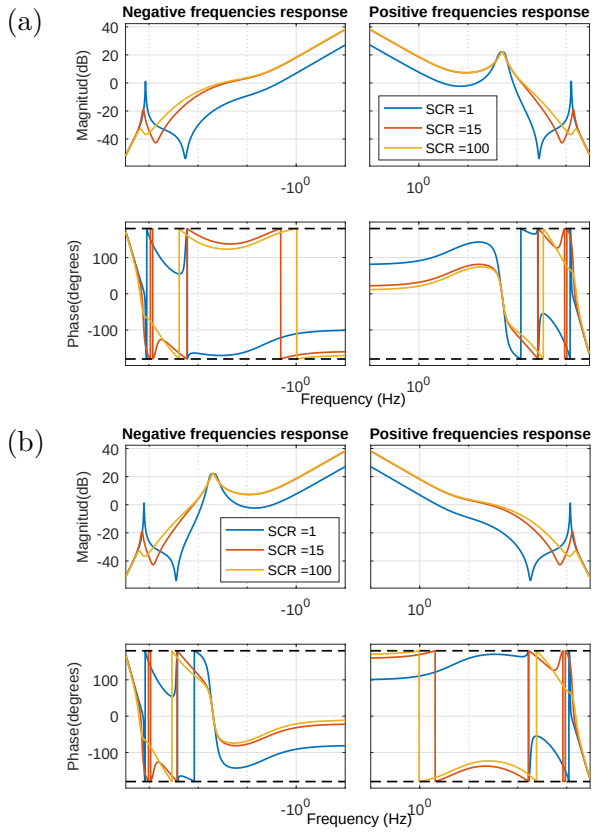


Figure 2.30: Frequency response of the eigenvalues of $[H_{ol}(s)]$, with the adjustment of the PI, for three SCRs: 1, 15 and 100.

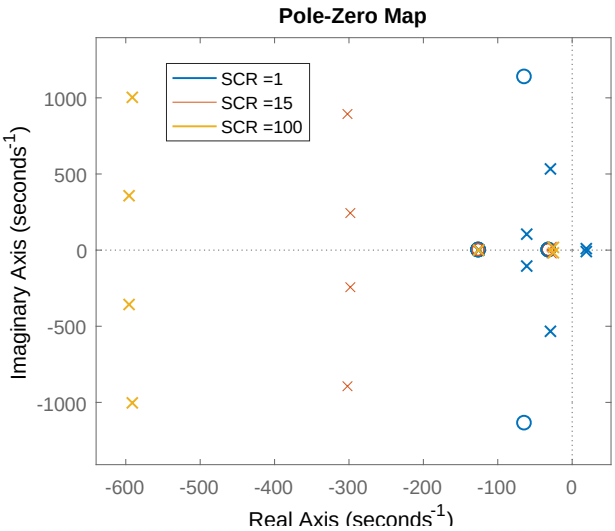


Figure 2.31: Current control closed-loop poles.

Chapter 3

MIMO-based decoupling strategy for grid-connected power converters

3.1 Motivation

The control in the synchronous reference frame of a power converter introduces cross-coupling terms in the *LCL* plant model, as well as in the filters and in the rest of the elements defined in the stationary reference frame. In practice, these cross-couplings imply that a change in the active power reference creates a variation in the reactive power, and vice-versa. The cross-couplings complicate the robust design of the controller, particularly if the power converter has to be connected to strong and weak grids, as it has been shown in Chapter 2. In high power conversion systems, the required high efficiency limits the sampling frequency, and consequently, the controller bandwidth. This circumstance increases the negative effects of the cross-couplings [BRI00, HOL04, SHE12]. For these reasons, in this chapter, a decoupling strategy is developed to improve the system response compared to the existing decoupling strategies, specially for low SCR.

3.2 State-of-the-art decoupling strategies

The state-of-the-art decoupling strategies have been widely used in the

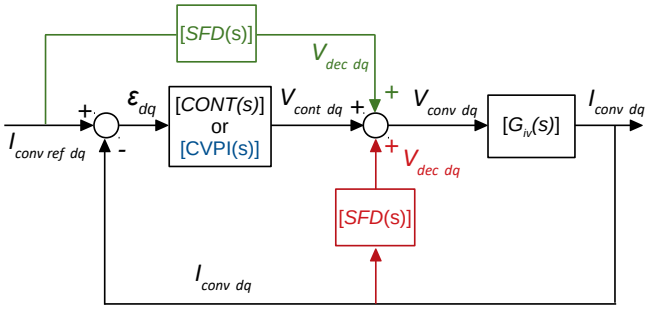


Figure 3.1: State of the art decoupling strategies.

literature, and can be classified depending on the system variable used. In Figure 3.1, the different decoupling strategies are represented for an ideal system with a plant $[G_{iv}(s)]$ and no delays. The first decoupling strategy uses the state variable measured, as depicted in red, to eliminate the plant cross-couplings, this technique receives the name of state-feedback decoupling (SFD) [BLA06, DAN09, YIM09, BAO13]. A different approach consists in using the error of the current controller. The main approach is the complex vector proportional-integrator decoupling (CVPID) [BRI00, YEP14b, SHI15], which substitutes the traditional controller by complex vector PI, represented in blue. Lastly, the current reference feed-forward (CRFF)uses directly the reference current [ZHO17], as represented in green in Figure 3.1.

To better understand the principles and limitations of the decoupling strategies, a purely inductive filter at the output of a grid-connected power converter is considered. This conversion structure is represented in Figure 3.2 (a), while in Figure 3.2 (b) the Laplace domain model is represented for the inductor.

The state feedback decoupling is the dominant approach in the literature. From the red terms in Figure 3.2 (b), a perfect decoupling, without additional sensors can be achieved, because this current is already measured. The decoupling is achieved by multiplying the currents by the matrix $[SFD(s)]$:

$$\begin{Bmatrix} V_{dec_d}(s) \\ V_{dec_q}(s) \end{Bmatrix} = \begin{bmatrix} 0 & -\omega_0 L \\ \omega_0 L & 0 \end{bmatrix} \begin{Bmatrix} I_{conv_{d_f}}(s) \\ I_{conv_{q_f}}(s) \end{Bmatrix} \tag{3.1}$$

where ω_0 is the frequency of the transformation to the SRF and L is the plant inductance. However, the real system is digitally controlled and the currents have to be acquired and filtered, obtaining a more complicated system as

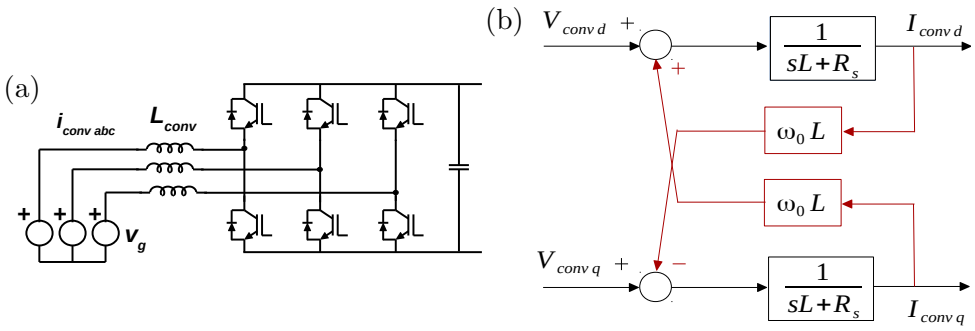


Figure 3.2: Grid-connected power converter with an inductive filter (a) and inductance model in SRF (b).

the one in Figure 3.3. The SFD effectiveness is strongly influenced by the existing delays in the feedback path, such as filters, computation and ZOH. Moreover, its performance is poorer when the converter is connected to weak grids. To avoid the limitations of the SFD introduced by the exiting delays in the control loop, [YIM09] proposed feeding back a one-step current prediction, improving the response and stability of the current control loop. However, the SFD, and consequently, the one-step current prediction SFD, have proved to be ineffective in dual-sequence current controllers, as the dual sequence terms cancel each other [YEP14a], a common control approach to deal with grid imbalances.

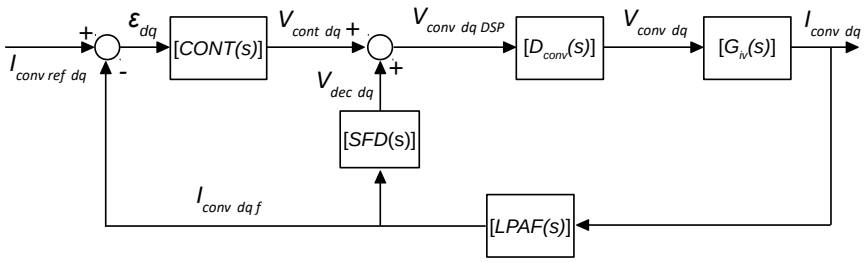


Figure 3.3: State feedback decoupling.

Alternatively, the complex vector proportional-integrator decoupling approach is based on the design of a complex PI that cancels the plant cross couplings [BRI00, BAH11, YEP14b, SHI15]. In Figure 3.4 the control diagram of the CVPI for a pure inductor is represented, where it can be seen

that the CVPID actuates on the error. The matrix $[CVPI(s)]$ is given by:

$$\begin{Bmatrix} V_{conv_{d_{DSP}}}(s) \\ V_{conv_{q_{DSP}}}(s) \end{Bmatrix} = \begin{bmatrix} K_p(1+\frac{R_s}{Ls}) & -\frac{K_p\omega_0}{s} \\ \frac{K_p\omega_0}{s} & K_p(1+\frac{R_s}{Ls}) \end{bmatrix} \begin{Bmatrix} \varepsilon_d(s) \\ \varepsilon_q(s) \end{Bmatrix} \tag{3.2}$$

where R_s is the inductor equivalent series resistor. This strategy has proven its effectiveness in dual-sequence current controllers [YEP14a] and is not so susceptible to the control delays and filters as the SFD. However, the parameters of the PI are set as a function of the plant parameters, imposing the design and the dynamics to the system [ZHO17]. With this strategy, the dynamics cannot be tuned independently of the decoupling strategy, as in the case of the SFD. Moreover, if a more complex control structure is required, in case that a simple PI cannot meet the requirements, this strategy has to be modified and becomes more complicated, depending on the controller implemented.

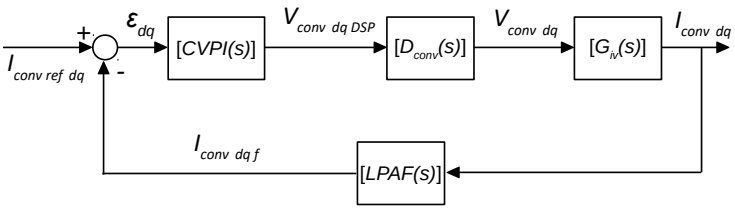


Figure 3.4: CVPID for an inductor.

Finally, the third decoupling strategy, the preprocessed current reference feed-forward (CRFF) [ZHO17] is implemented as shown in Figure 3.1 in green and Figure 3.5 for a non-ideal system. The inductor reference current is multiplied by a matrix to compensate the cross couplings, counteracting the system dynamics. The terms of the matrix include a compensation of the delay, approximating the term of the digital model implementation of the controller. Nevertheless, in this case, the system open-loop transfer matrix is not modified, and the robust design of the controller faces the same limitations seen at the end of Chapter 2.

To overcome the imitations of these strategies, a different decoupling strategy is presented in Section 3.3. The decoupling actions are calculated from the controller voltages, reducing the influence of the delays if compared with the SFD, and achieving independent tuning of the controller and the decoupler.

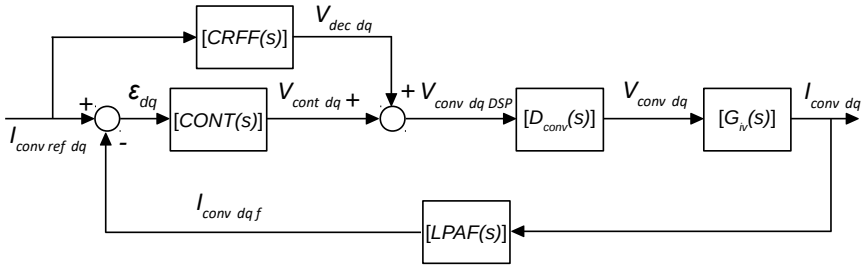


Figure 3.5: CRFF for an inductor.

3.3 Proposed decoupling strategy

In Figure 3.6 a simplified control diagram including the proposed decoupling control strategy is provided. For simplicity, this diagram does not include the filters and delays. The decoupling matrix $[CCD(s)]$ takes as inputs the controller voltages in the dq axis, compensating the known cross-coupling terms of the plant.

The working principle of the decoupling strategy can be derived for a generic plant model in the SRF that correlates the voltages imposed by the converter and the converter current, $[G_{iv}(s)]$, and has the symmetry already presented for the models developed in Chapter 2:

$$\begin{Bmatrix} I_{conv\ d}(s) \\ I_{conv\ q}(s) \end{Bmatrix} = \begin{bmatrix} G_1(s) & G_2(s) \\ -G_2(s) & G_1(s) \end{bmatrix} \begin{Bmatrix} V_{conv\ d}(s) \\ V_{conv\ q}(s) \end{Bmatrix} \tag{3.3}$$

A diagonal system can be obtained in Equation 3.3 if the CCD matrix in

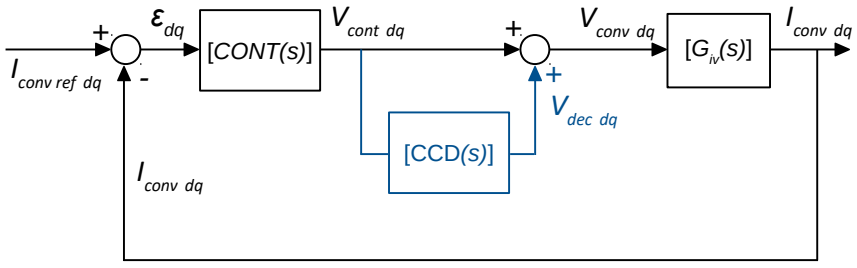


Figure 3.6: Derivation of the proposed decoupling strategy.

Figure 3.6 has the form:

$$[CCD(s)] = \begin{bmatrix} 0 & -\frac{G_2(s)}{G_1(s)} \\ \frac{G_2(s)}{G_1(s)} & 0 \end{bmatrix} \tag{3.4}$$

If the transfer matrix of the converter current, $I_{conv\ dq}(s)$, to the controller voltage, $V_{cont\ dq}(s)$, is obtained using a $[CCD(s)]$ matrix equal to Equation 3.4, the resulting diagonal system matrix is given by:

$$\begin{Bmatrix} I_{conv\ d}(s) \\ I_{conv\ q}(s) \end{Bmatrix} = \begin{bmatrix} \frac{G_1^2(s)+G_2^2(s)}{G_1(s)} & 0 \\ 0 & \frac{G_1^2(s)+G_2^2(s)}{G_1(s)} \end{bmatrix} \begin{Bmatrix} V_{cont\ d}(s) \\ V_{cont\ q}(s) \end{Bmatrix} \tag{3.5}$$

The proposed decoupling strategy can be comprehensively developed for a purely inductive filter and supposing a controller with no delays in Subsection 3.3.1. Once the cross controller decoupler (CCD) is derived for this simplified system, it is extended to an LCL filter in Subsection 3.3.2 considering the measurement filters and control delays.

3.3.1 Proposed decoupling strategy for an inductor

When the SRF model is obtained for an inductance, cross-coupling terms between both dq phases appear, as indicated in Figure 3.2.

The system dynamics have been already modeled and have the form and symmetry of Equation 3.3, where $G_1(s)$ and $G_2(s)$ are given by Equation 3.6 and Equation 3.7, respectively.

$$G_1(s) = \frac{L_c s + R_c}{(L_c s + R_c)^2 + (\omega_0 L_c)^2} \tag{3.6}$$

$$G_2(s) = \frac{\omega_0 L_c}{(L_c s + R_c)^2 + (\omega_0 L_c)^2} \tag{3.7}$$

L being the inductance value and R_s its series equivalent resistance. To achieve a decoupled system, or from the matrix point of view, a diagonal matrix in Equation 3.3, two cross-controller-decoupler transfer functions, $CCD_1(s)$ and $CCD_2(s)$ can be applied to the controller voltage $V_{cont\ dq}(s)$ as indicated in Figure 3.7 by the blue lines. These two terms must cancel the cross coupling effect.

As previously calculated, to achieve this cancellation $CCD_1(s)$ must be

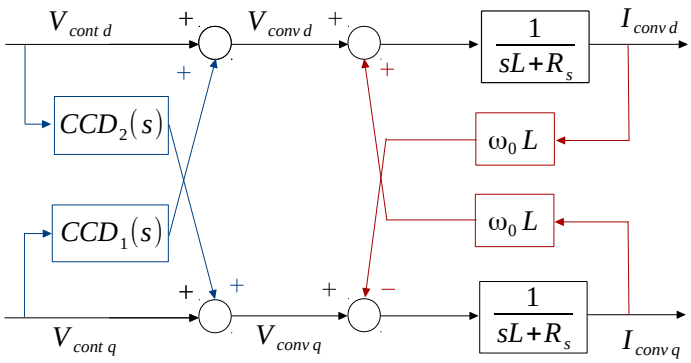


Figure 3.7: Inductance model with the CCD in continuous blue lines.

equal to:

$$CCD_1(s) = -\frac{G_2(s)}{G_1(s)} \tag{3.8}$$

while $CCD_2(s) = -CCD_1(s)$. $CCD_1(s)$ for an inductor is given by the simple expression in Equation 3.9.

$$CCD_1(s) = -\frac{\omega_0 L_e}{L_e s + R_e} \tag{3.9}$$

The matrix $[CCD(s)]$ can be defined for the cross-controller decoupler as:

$$[CCD(s)] = \begin{bmatrix} 0 & -\frac{\omega_0 L_e}{L_e s + R_e} \\ \frac{\omega_0 L_e}{L_e s + R_e} & 0 \end{bmatrix} \tag{3.10}$$

The decoupling term can be seen as a decoupled inductor, L_e with a series resistance R_e and a gain dependent on the inductance and the angular velocity of the SRF. If these parameters match the inductor ones, a perfect decoupling is achieved, as it is represented in Figure 3.8, where $G_2(s)$ is eliminated, and the frequency response of a decoupled inductor is obtained.

3.3.2 Extension of the proposed decoupling strategy for an LCL filter

The purely inductive filter is not commonly used in grid-connected power converters, as a bulky component is required to meet the grid codes. The LCL

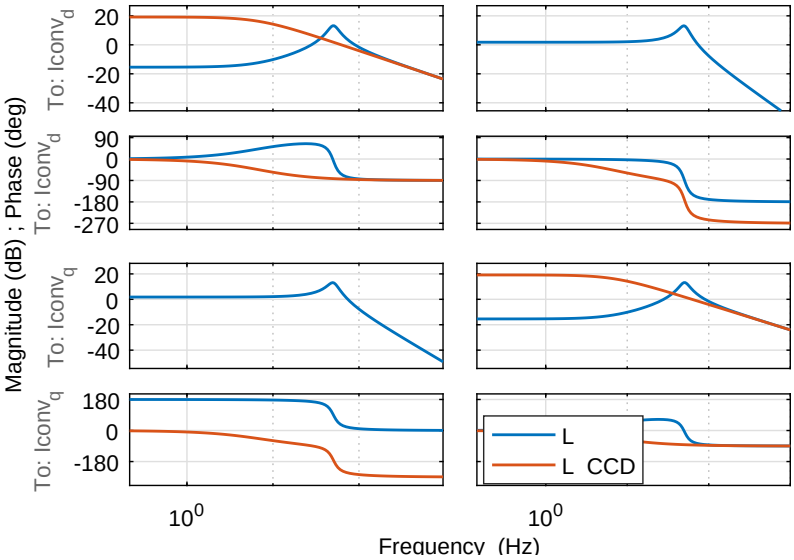


Figure 3.8: Bode plot of the inductance modeled in the SRF (blue) and decoupled with the CCD (red). The Bode plots in the first column correlate the converter currents in both axis with the voltage in the d axis, while the Bode plots in the second column the converter currents with the voltage in the q axis.

filter is the most extended solution, for this reason, the decoupling strategy is applied to this type of filters.

3.3.2.1 Direct extension of the decoupling strategy

The previously presented matrices for the decoupling strategy can be recalculated for the LCL filter, but as the plant complexity is increased, it requires more complicated expressions than the simple first order transfer functions obtained for the inductor.

The model of the LCL filter is reproduced in Figure 3.9, including the decoupling terms for an ideal system without delays. To better understand how the decoupling transfer functions are calculated, the system without them is considered. $[G_{iv}(s)]$ is the plant matrix, which models the dynamics of the plant between the converter voltage and current, already developed in Equation 2.54 and with the symmetry of Equation 3.3. This matrix has a diagonal term $G_{iv\ 1}(s)$ and anti-diagonal term $G_{iv\ 2}(s)$. A diagonal matrix could be obtained if the decoupling terms given in Equation 3.4 for the anti-diagonal terms, $CCD(s)$, of the matrix $[CCD(s)]$ are applied:

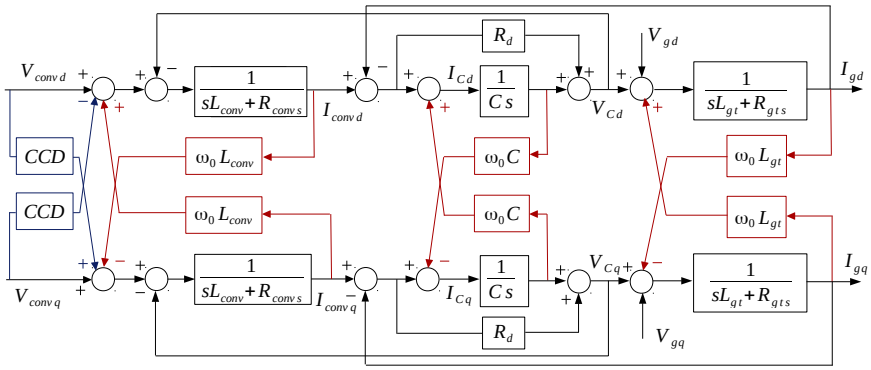


Figure 3.9: *LCL* model with te CCD in blue.

$$CCD(s) = \frac{G_{iv\ 2}(s)}{G_{iv\ 1}(s)} \tag{3.11}$$

As discussed in Subsection 2.3.3, both denominators of $G_{iv\ 1}(s)$ and $G_{iv\ 2}(s)$ have the same six order transfer functions that are canceled out when $CCD(s)$ is computed. However, the numerator of $G_{iv\ 2}(s)$ is a third order transfer function, while the one of $G_{iv\ 1}(s)$ is a fourth order transfer function. In this way, the complexity of $CCD(s)$ is highly increased compared to the purely inductive filter. Moreover, the coefficients depend on the parameters of the *LCL* filter and the equivalent series resistances of all the components, resulting in long expressions. The variability of the parameters, mainly caused by the high variability of the grid impedance, deteriorate the performance of the decoupling strategy if a precise estimation of the grid inductance is not available.

To improve this initial situation, the positive feed-back of the capacitor voltage is improved, designing the decoupling strategy for a simplified model.

3.3.2.2 Alternative based on the positive feedback of the capacitor voltage

The implementation of the proposed decoupling strategy for the *LCL* filter is based on an improved positive-feedback of the capacitor-voltage that reduces the variability of the plant within the current controller bandwidth for the different possible SCRs. By reducing this variability, the dynamics of a pure inductor are achieved at low frequencies and the CCD matrix can be implemented as in the case of a simple inductor.

Improvement of the positive-feedback of the capacitor voltage

The Bode plot of the LCL filter for the three different SCRs: 1, 15 and 100, is represented in Figure 3.10. Additionally, the converter inductance Bode plot. L_{conv}, has been also represented for comparison purposes. From this representation, it is clear that a great variability in the low frequency dynamics, within the current control loop bandwidth, is created by the changes in the grid impedance. Thus, the same inductance value cannot be emulated in the $[CCD(s)]$ for all the plants, as the decoupling achieved will suffer strong variations. The converter inductance is normally known and well characterized in high power converters. If the grid influence at low frequencies is reduced, the dynamics of the plant are dominated by the converter inductance in the current control loop bandwidth. As a consequence, a simple CCD could be derived to achieve the desired decoupling.

The positive-feedback of the capacitor-voltage helps to immunize the system face to grid inductance variations. Nevertheless, this voltage feed-forward can effectively cancel the variability in the control loop created by the unknown and variable grid impedance only if the delays in the control loop are eliminated or compensated [LI18]. With a perfect compensation of the delays, only the dynamics of the converter have to be controlled. However, this cannot always be achieved, as the transfer fucntion that has to be implemented depends on future samples of the capacitor voltage. The delays introduced by the measurement filters $[LPAF(s)]$, computation and ZOH, $[D_{conv}(s)]$, reduce the effectiveness of the positive feedback of the capacitor voltage. To alleviate these effects, the matrix $[PF(s)]$ is added in the voltage positive-feedback path, as shown in the diagram of Figure 3.11. From his figure, it is clear that the decoupling action combines the improved matrix for the positive-feedback of the capacitor-voltage $[PF(s)]$ and the

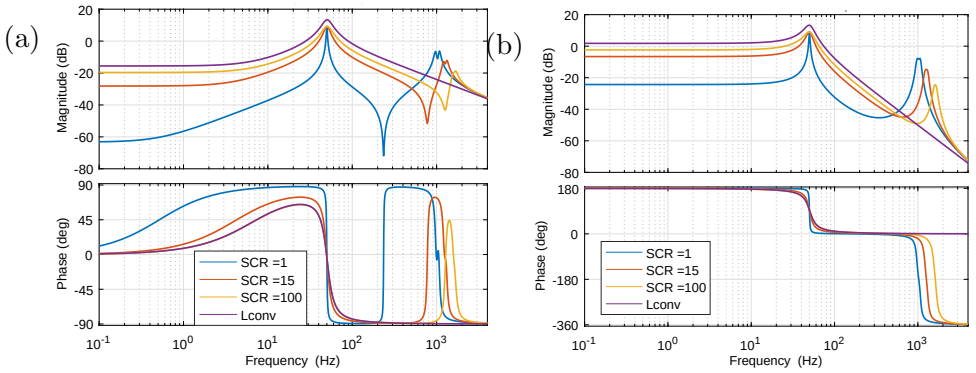


Figure 3.10: LCL variability for three SCRs: 1, 15 and 100.

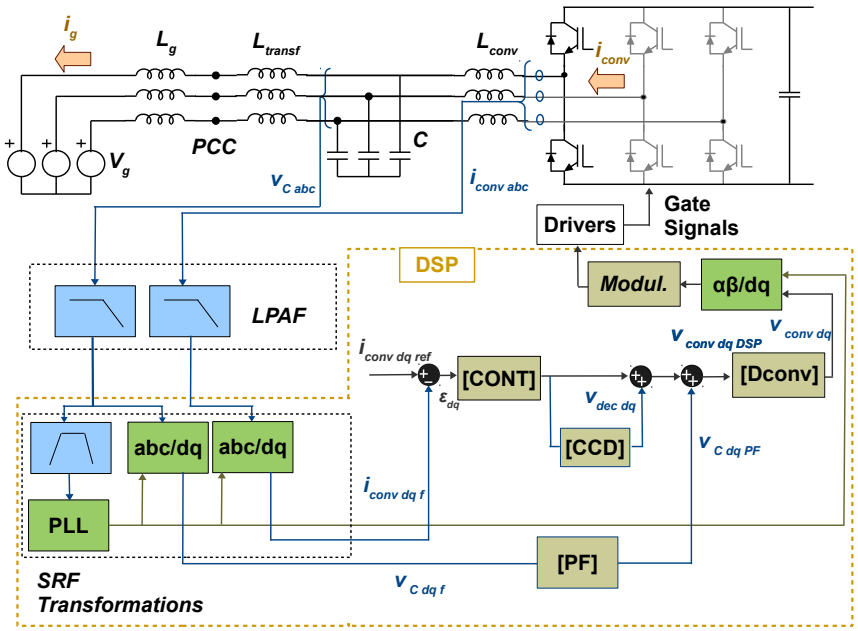


Figure 3.11: Diagram of the current control loop including the decoupling strategy.

cross-controller decoupler matrix $[CCD(s)]$.

If the current control loop depicted in Figure 3.11 is represented with the matrix notation in the Laplace domain, the diagram in Figure 3.12 is obtained. All the elements of this control loop diagram have been already introduced, except for the matrix $[G_{vv}(s)]$, a matrix that correlates the converter voltage with capacitor voltage that was calculated in Equation 2.58. From Figure 3.12 it is clear that the voltage feed-forward is affected by the product of $[LPAF(s)]$, $[PF(s)]$ and $[D_{conv}(s)]$. First, let us

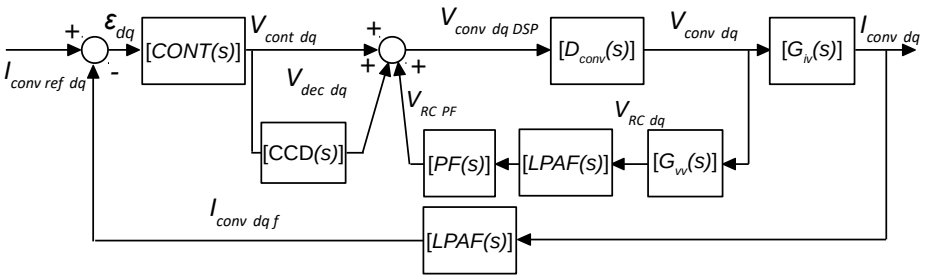


Figure 3.12: Matrix diagram of the current control loop including the decoupling strategy.

consider $[PF(s)]$ to be the identity matrix. In such case, the product of the three matrices can be represented by Equation 3.12 in terms of $A(s)$ and $B(s)$, where $A(s) = D_1(s)LPAF_1(s) - D_2(s)LPAF_2(s)$ and $B(s) = D_1(s)LPAF_2(s) + D_2(s)LPAF_1(s)$. This equation correlates the measured capacitor voltages in the SRF, $V_{C\ dqf}$, and the positive-feedback of the capacitor voltage, $V_{Cdq\ PF}$.

$$\begin{Bmatrix} V_{Cd\ PF}(s) \\ V_{Cq\ PF}(s) \end{Bmatrix} = \begin{bmatrix} A(s) & B(s) \\ -B(s) & A(s) \end{bmatrix} \begin{Bmatrix} V_{C\ d}(s) \\ V_{C\ q}(s) \end{Bmatrix} \tag{3.12}$$

Equation 3.12 reveals that the capacitor voltage positive feedback in the d axis, $V_{Cd\ PF}$, contains both measurements $V_{C\ df}$ and $V_{C\ qf}$. The same coupling is obtained in the q axis. In order to avoid that the voltage feed-forward introduces additional cross couplings, a compensation is required in $[PF(s)]$. By imposing that $V_{Cd\ PF}(s) = V_{C\ df}(s)$ and $V_{Cq\ PF}(s) = V_{C\ qf}(s)$ the compensation terms required to eliminate the effects of $[D_{conv}(s)]$ and $[LPAF(s)]$ are obtained, which are given in Equation 3.13.

$$[PF] = \begin{bmatrix} \frac{A(s)}{A(s)^2+B(s)^2} & -\frac{B(s)}{A(s)^2+B(s)^2} \\ \frac{B(s)}{A(s)^2+B(s)^2} & \frac{A(s)}{A(s)^2+B(s)^2} \end{bmatrix} \tag{3.13}$$

To gain an insight on the effectiveness of this improved capacitor voltage positive-feedback, the Bode plots of three different alternatives have been

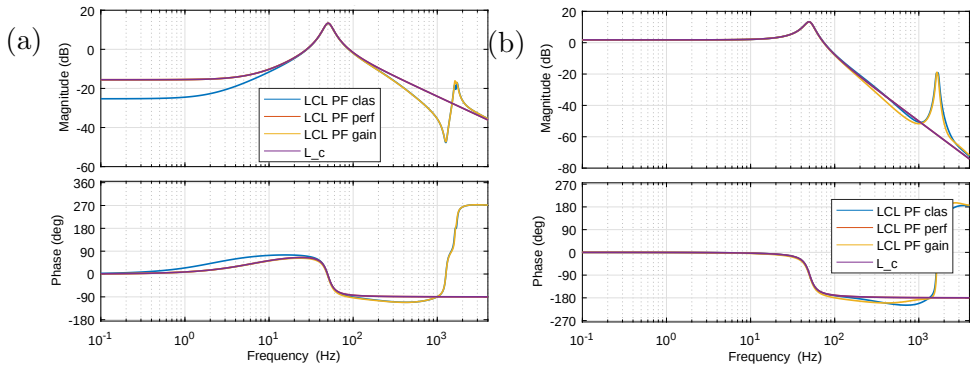


Figure 3.13: Comparison of the frequency response of the converter current $I_{conv\ dq}(s)$, with respect to the controller voltage $V_{cont\ dq}$, for different [PF] options: classical (blue), perfect (red) and gain approximation (yellow) and a pure inductance (purple). This representation has been made for an SCR of 100. A pure inductance, equal to the converter inductance, is also represented in purple

tested, modifying the matrix $[PF(s)]$. In Figure 3.13 the frequency response of the converter current $I_{conv\ dq}(s)$, with respect to the controller voltage $V_{cont\ dq}$, are plotted without including the matrix $[CCD(s)]$. The frequency response of these three alternatives is compared to the frequency response of the converter inductance in the same Bode plot. With the classical voltage feed-forward, which uses a unity matrix for $[PF(s)]$, the cross-couplings in $[LPAF(s)]$ and $[D_{conv}(s)]$ create a bad compensation at low frequencies, and the compensated system does not behave as a pure inductance equal to L_{conv}, blue curve labeled as *LCL PF clas.* If $[PF(s)]$ is equal to the matrix of Equation 3.13, the effects of $[LPAF(s)]$ and $[D_{conv}(s)]$ are completely canceled, and a pure inductance is obtained in the whole frequency range, up to the control Nyquist frequency (red curve: *LCL PF perf*). Unfortunately, this option is not feasible, as the resulting transfer function has a greater number of zeros than poles, depending on future samples. To overcome this limitation, an approximation of the matrix of Equation 3.13 is used. The desired inductive behavior can be achieved up to a frequency of 200 Hz by approximating Equation 3.13 to a gain, evaluating the transfer functions at 0 Hz. A good decoupling at low frequencies, as indicated in Figure 3.13 by the curves labeled *LCL PF gain*, can be obtained.

With the $[PF(s)]$ equal to a constant matrix, obtained by approximating Equation 3.13 at 0 Hz, the variability at low frequencies is highly reduced and the CCD can be implemented for a pure inductance equal to the converter inductance.

Transfer function for the decoupling term

Once the capacitor-voltage positive-feedback has been established, the cross-controller decoupling matrix can be included in the control loop, adjusted to decouple a pure inductance, equal to the converter inductance. The $[CCD(s)]$ matrix is given by:

$$[CCD(s)] = \begin{bmatrix} 0 & -\frac{\omega_0 L_{conv}}{L_{conv}s+R_{conv\ s}} \\ \frac{\omega_0 L_{conv}}{L_{conv}s+R_{conv\ s}} & 0 \end{bmatrix} \tag{3.14}$$

The transfer matrix correlating the converter current $I_{conv\ dq}(s)$ and the controller action $V_{cont\ dq}(s)$ are calculated, representing the diagonal and anti-diagonal terms of the resulting matrix in Figure 3.14, as the system is again symmetric.

The diagonal term in Figure 3.14 (a) has greater magnitude at low frequencies than the anti-diagonal term (b) by more than 16 dB for every possible SCR. This means that any voltage imposed by the converter in the

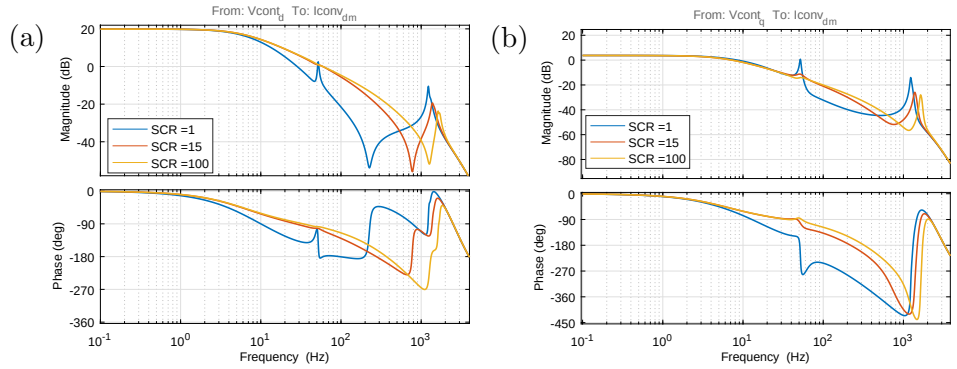


Figure 3.14: Bode plot of the converter current $I_{conv\ dq}(s)$ to the controller voltage $V_{cont\ dq}(s)$ including the CCD, for different SCR: 1, 15 and 100.

d axis has a dominant effect in the d axis current, in opposition to the initial case, without decoupling, where the crossed term was dominant. As discussed previously in the implementation of the matrix $[PF(s)]$, at higher frequencies the decoupling becomes less effective, specially in weak grids. This is due to the resonance frequency between the capacitor current and the grid inductance, which is moved towards lower frequencies as the grid impedance is increased. The improved capacitor-voltage positive-feedback is not able to cancel this resonance frequency, as the delays are not being compensated. Thus, the decoupling reduces its effectiveness, as the system is no longer an inductor at these frequencies for extremely low SCRs. At higher frequencies, around the LCL resonance frequency, the decoupling strategy is ineffective. However, the stability issues in this range of frequencies is treated in Chapter 4.

The design of the current control loop is made as in Subsection 2.3.5 from the eigenvalues frequency response, thus, it is useful to analyze the decoupling achieved from the eigenvalues perspective. For a system with the symmetry already presented:

$$[H_{ol}(s)] = \begin{bmatrix} H_1(s) & H_2(s) \\ -H_2(s) & H_1(s) \end{bmatrix} \tag{3.15}$$

Its eigenvalues are:

$$\lambda_{1,2}(s) = H_1(s) \pm jH_2(s) \tag{3.16}$$

If the system is decoupled, $H_2(s)$ is small compared to $H_1(s)$. Consequently, the complex part of the eigenvalue tends to be negligible and

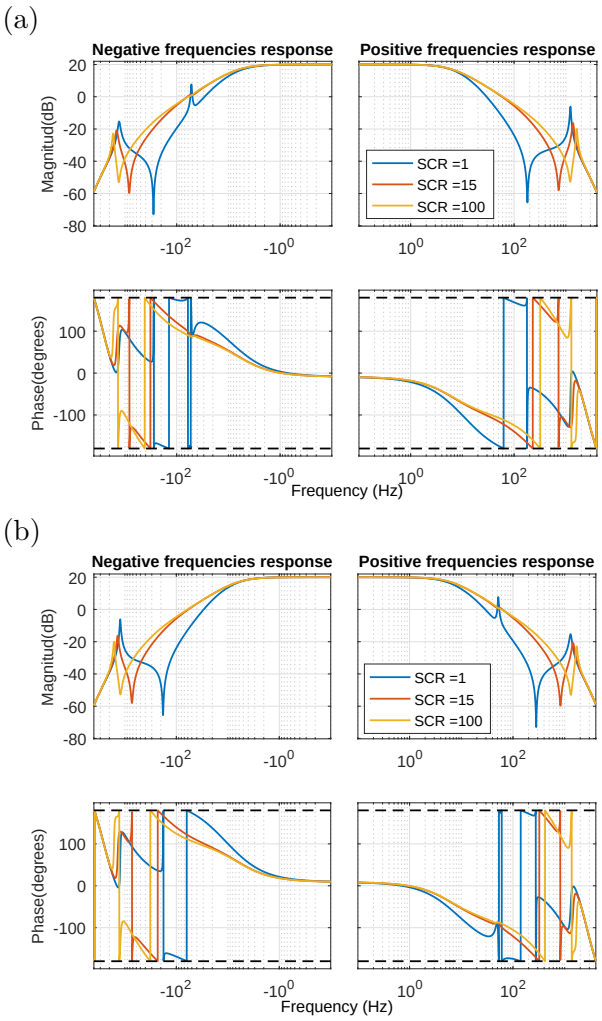


Figure 3.15: Bode plot of the eigenvalues of the open-loop transfer matrix from the converter current $I_{conv\ dq}(s)$ to the controller voltage $V_{cont\ dq}(s)$ including the CCD, for different SCR: 1, 15 and 100.

the Bode diagrams of $\lambda_{1,2}(s)$ are symmetric with respect to 0 Hz. If the eigenvalues of the open loop-transfer matrix of $I_{conv\ dqf}(s)$ to $\varepsilon_{dq}(s)$ are plotted in Figure 3.15, with $[CONT(s)]$ equal to a unitary matrix, this theory can be verified.

This analysis points out that a decoupled system has a symmetric frequency response with respect to 0 Hz, from the magnitude point of view, proving that a symmetric decoupled system has been achieved at low

frequencies, where the controller has to be adjusted. The analysis of the eigenvalues is continued in Section 3.5, but first, the decoupling achieved with the proposed strategy is compared to the performance of the state-feedback decoupling.

3.4 Comparison of the CCD with the SFD strategy

The SFD is the most extended decoupling strategy, for this reason, it is compared to the proposed one. With this purpose, the transfer matrix of the converter current to the controller voltage is studied, representing the diagonal term of the open loop transfer matrix ($I_{conv\ d}(s)/V_{cont\ d}(s)$) and the anti-diagonal term ($I_{conv\ d}(s)/V_{cont\ q}(s)$) in Figure 3.16 for two different SCRs: 1 and 15.

The proposed decoupling strategy provides a better decoupling between both axis than the conventional SFD, with lower variability at low frequencies when the grid inductance varies. Particularly advantageous are the results for weak grids (SCR=1), where the proposed strategy allows to properly decouple both axis by more than 15 dB, while with the state feedback decoupling (SFD), the anti-diagonal terms are dominant at some frequencies, e.g. 0.4 Hz, and the dynamics cannot be decoupled. This is true up to frequencies around the resonance frequency, greater frequencies than the current controller bandwidth.

To sum up, the proposed decoupling strategy is based on an improved capacitor voltage feed-forward in the SRF to eliminate the *LCL* plant

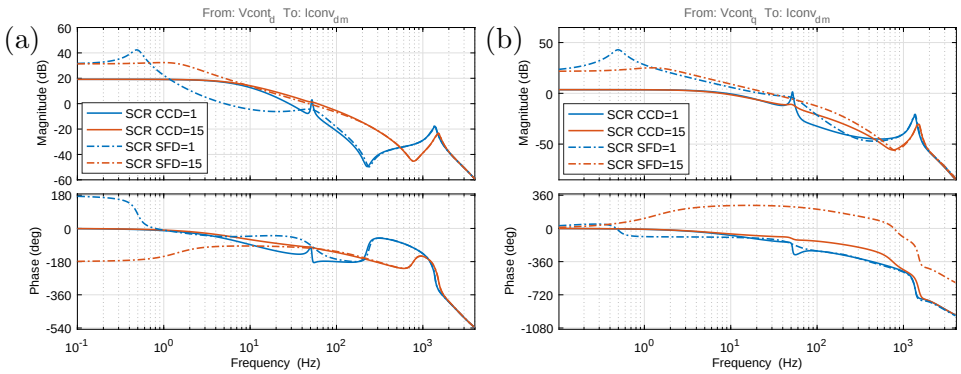


Figure 3.16: Comparison of the Bode plots for the SFD and the CCD, representing the converter current $I_{conv\ dq}(s)$ to the controller voltage $V_{cont\ dq}(s)$ for two different SCR: 1 and 15.

variability at low frequencies created by the unknown L_g. A decoupler, called CCD, is used to compensate the cross-coupling terms of the converter inductance, once the variability at low frequencies is eliminated.

With this decoupling strategy, the design of the controller becomes simpler, as shown in the next section.

3.5 Design of the controller

The introduction of the decoupling strategy modifies the plant, simplifying the controller design. As a first step, the reference tracking is discussed. As a second step, the rejection to grid disturbances is analyzed.

3.5.1 Reference tracking

To achieve the desired reference tracking dynamics, the same design procedure developed in Subsection 2.3.5 is followed here. First, the integrator of the PI is included to achieve zero tracking error. Later, the PI parameters are adjusted to achieve the desired cut-off frequency and phase margins. If the desired stability margins cannot be achieved, additional compensators would be introduced, such as lead-lag controllers.

If the integrator required to achieve the desired zero-tracking error is included, the Bode plot of the eigenvalues has infinite magnitude at 0 Hz, while the phase becomes +90 degrees at positive frequencies and -90 degrees at negative frequencies, Figure 3.17.

To analyze if there are -180 degree crossings with magnitudes greater than 0 dB at 0 Hz, as it happened in the system without decoupling, the positive and negative frequencies of the eigenvalues are represented in Figure 3.18 in the same plot, with a focus around 0 Hz. It can be concluded that there is not a crossing with -180 degree at the origin in neither eigenvalues. According to the Nyquist stability criteria, as there are no unstable poles in the open loop transfer matrix and no -180 degree crossings at 0 Hz, any additional -180 degree crossings should be avoided at magnitudes greater than 0 dB to attain a stable closed loop system.

If the current controller bandwidth is set at 120 Hz, with a desired phase margin of at least 30 degrees for every possible SCR, a simple PI is not sufficient. A PI controller will be able to avoid the first -180 degree crossing for the SCR of 1 and the ones occurring around 50 Hz for the SCRs equal to 15 and 100 in Figure 3.17, but not the one at 50 Hz for a SCR equal to 1. A

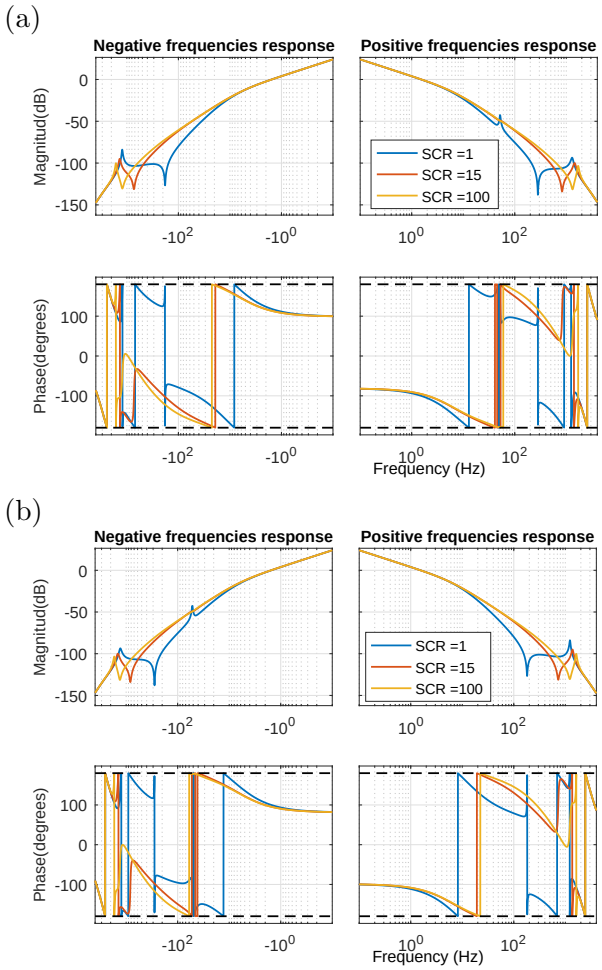


Figure 3.17: Bode plot of the eigenvalues of the open-loop transfer matrix from the converter current $I_{conv\ dq}(s)$ to the controller voltage $V_{cont\ dq}(s)$ including the CCD and the integrator, for different SCR: 1, 15 and 100.

lead-lag compensator is included with the PI controller, achieving a stable system for strong and weak grid conditions. The cut-off frequency is set at 120 Hz for the strong grid case, adjusting the phase to have at least 30 degrees of phase margin at every gain cross-over frequency. With these specifications, K_p has been adjusted to 0.78, T_n to 31 ms and the lead-lag compensator to introduce 30 degrees at 50 Hz, in order to avoid the -180 degree crossings for an SCR of 1. In Figure 3.19 the frequency response of the eigenvalues is shown, including the controller adjusted. As it is shown, no -180 degree crossing are obtained with positive magnitude, for this reason

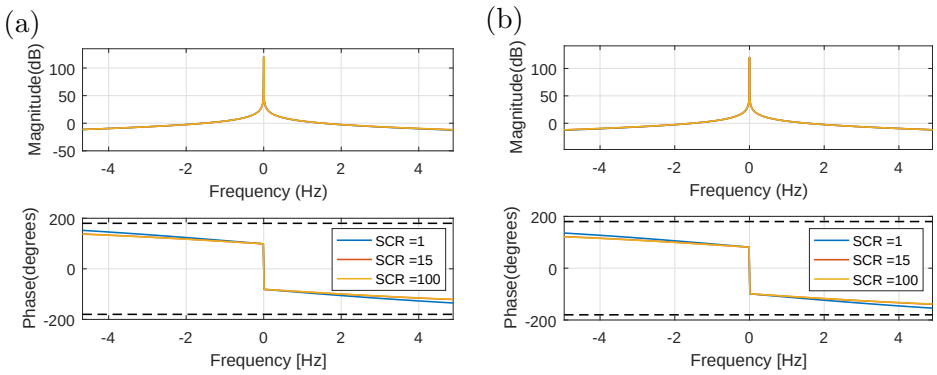


Figure 3.18: Bode plot of the eigenvalues of the open-loop transfer matrix from the converter current $I_{conv\ dq}(s)$ to the controller voltage $V_{cont\ dq}(s)$ including the CCD and the integrator with a focus on 0 Hz, for different SCR: 1, 15 and 100.

the closed loop-transfer matrix has no unstable poles.

With the proposed decoupling strategy, a robust controller has been adjusted for every possible grid impedance. However, in some real applications, it is known whether the grid is weak or strong, even though the exact value of the grid effective inductance might not be known. In these cases, the design of the controller should be performed for the actual possible range of grid impedances at the PCC, and not for the whole possible range of SCR, as it has been done in this section.

3.5.2 Rejection to grid disturbances

In grid-connected power converters, the rejection to grid disturbances is an important aspect that has to be studied. The grid can contain harmonics, that must be rejected in order to avoid the distortion of the current injected to the grid. Moreover, voltage dips, sags and over-voltages may cause high over-currents in the power converter.

The influence of the grid voltage on the converter current, is analyzed by means of the transfer matrix from the grid voltage, $V_{g\ dq}$, to the converter current, $I_{conv\ dq}$, obtained from Figure 3.20. In this control loop diagram the matrix $[G_{dist}]$ is the one calculated in Equation 2.60, correlating the converter current in the dq axis to the grid voltage in the same axis.

Depending on the design of the inductor and the materials used, the equivalent series resistance can have different values. A lower resistance will imply a lower damping and consequently worse rejection to grid

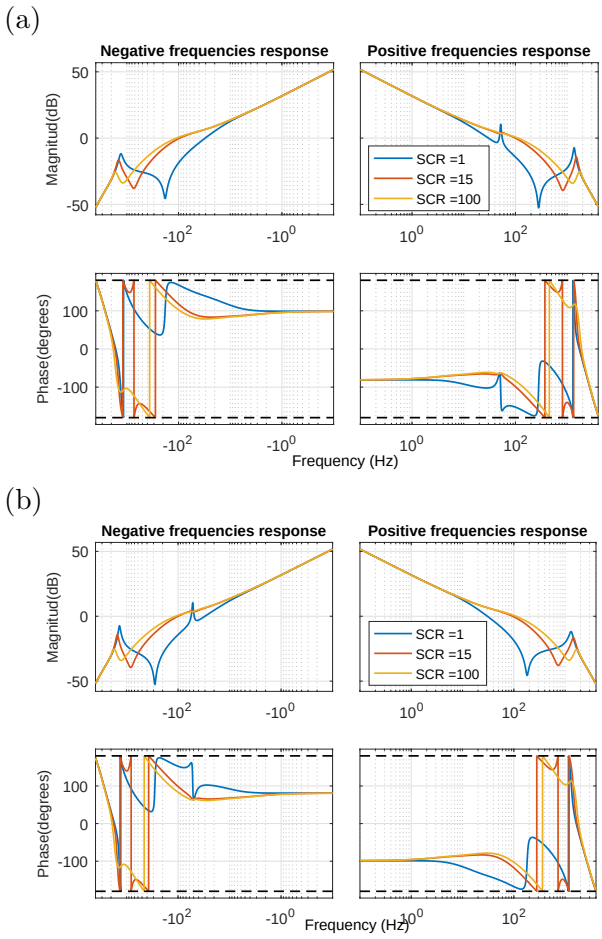


Figure 3.19: Bode plot of the eigenvalues of the open-loop transfer matrix from the converter current $I_{conv\ dq}(s)$ to the controller voltage $V_{cont\ dq}(s)$ including the CCD and the controller, for different SCR: 1, 15 and 100.

disturbances. For this reason, two different converter series resistors, $R_{conv\ s}$ in the rejection to grid disturbances, are tested. The passive damping of the system strongly influences the rejection to grid disturbances in the CCD decoupling strategy. To verify this behavior, the Bode plots of the closed-loop transfer matrix of the rejection to grid disturbances are plotted in Figure 3.21. To avoid the representation of three graphs in each Bode plot, only the SCR of 15 is considered to analyze the rejection to grid disturbances. Two Bode diagrams are shown, the diagonal term (a) and the anti-diagonal term (b), as the matrix has the same symmetry presented for the rest of the matrices. The first equivalent series resistor is 0.1 Ω, the real

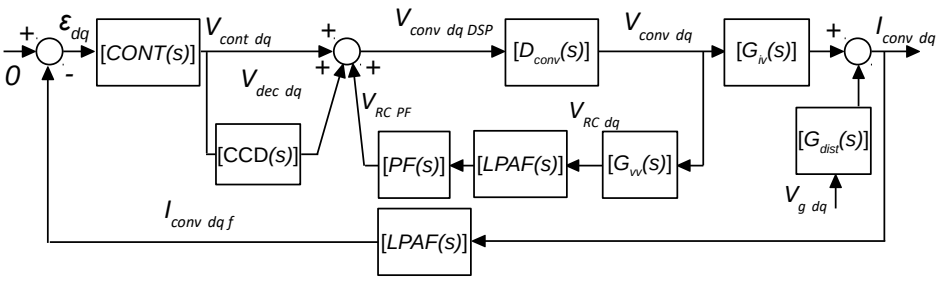


Figure 3.20: Matrix diagram of the current control loop including the decoupling strategy and the grid voltage as a disturbance.

resistor of the three-phase converter inductance of the power converter tested in the Renewable Energies laboratory at the UPNa. In this case, at least a 12 dB attenuation is achieved at any frequency, the lowest attenuation occurs at 50 Hz. If this equivalent series resistor is reduced by a factor of 10, and the CCD is adapted to emulate this series resistance, the rejection to grid disturbances is highly deteriorated. In Figure 3.21 it can be seen that in this case, an undesirable magnitude peak of 5 dB exists at 50 Hz.

The peak in the magnitude plot in Figure 3.21 is created by two complex poles with a low damping, which originate an important oscillation in the time domain step response. In Figure 3.22 (a) the effect that a step voltage in the d axis has on the converter current on the same axis is analyzed. If this response is compared to the one without the decoupling strategy in Figure 3.22 (b), it can be seen that the response is highly penalized by the CCD.

Low rejection to grid disturbances has also been reported for CVPI [HAR98, YEP14b]. The CVPI has a similar working principle that the

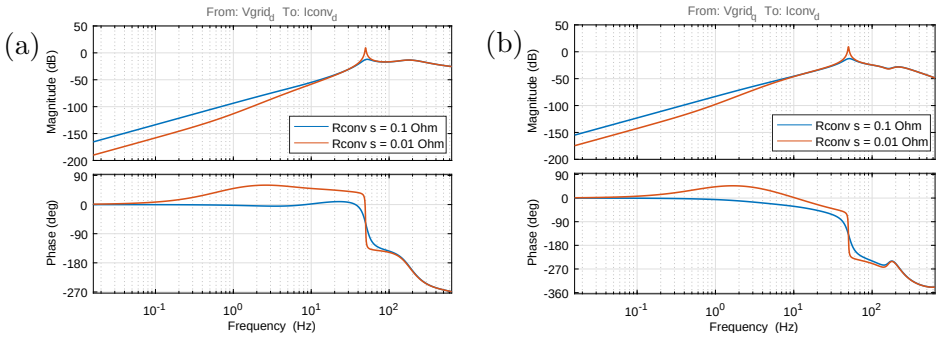


Figure 3.21: Bode plot of the diagonal and anti-diagonal terms of the rejection to grid disturbances transfer matrix for a SCR of 15 and two different $R_{conv\ s}$: 0.1 Ω and 0.01 Ω.

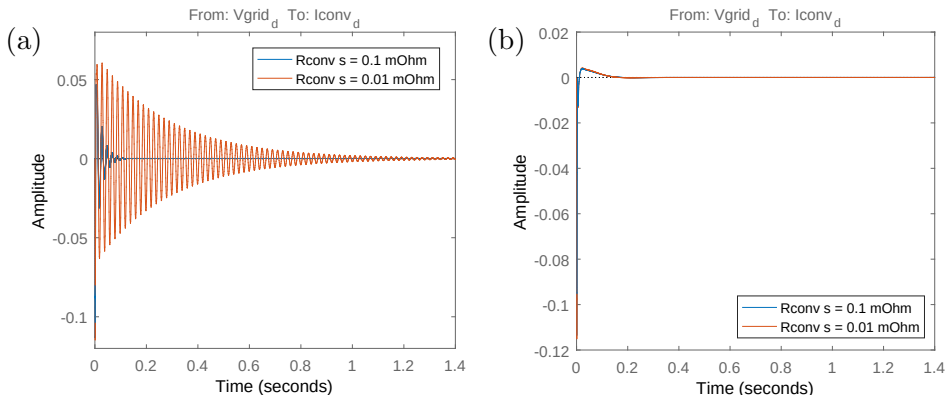


Figure 3.22: Step response of the converter current in the d axis to a step in the grid voltage in the d axis for an SCR of 15, and two different $R_{conv\ s}$: 0.1 Ω and 0.01 Ω. The response is compared for the system with the CCD (a) and without it (b).

proposed CCD, introducing a zero that cancels the plant cross-couplings. The main difference is that in the CVPI, the error is used to decouple both axis, and consequently, the PI controller has to be adjusted with the parameters required by the decoupling strategy [ZHO17], equal to the plant parameters. In contrast, the proposed CCD strategy is designed independently of the controller.

The rejection to grid disturbances can be improved for the proposed decoupling strategy with two different approaches, presented in the following subsections. The first one is a state-of-the-art solution that requires an additional inner loop, while the second one is inherent to the proposed decoupler, and depends on the emulated parameters.

3.5.2.1 Emulation of a virtual resistor

To improve the rejection to grid disturbances, a common approach when the CVPI decoupling strategy is used, is the emulation of a damping resistance in series with the converter inductor [HAR98, YEP14b], as indicated in Figure 3.23 by the red branch added.

In Figure 3.23 the matrix $[R_v]$ is a diagonal matrix whose terms are equal to the emulated virtual resistor R_{virt}. In the complex vector PI, the controller parameters are modified depending on the converter resistance. By doing this current negative feedback, the converter series resistance is modified through the control. For this reason, the parameters of $[CVPI(s)]$ have to be adapted taking into account the additional virtual resistor [ZHO17].

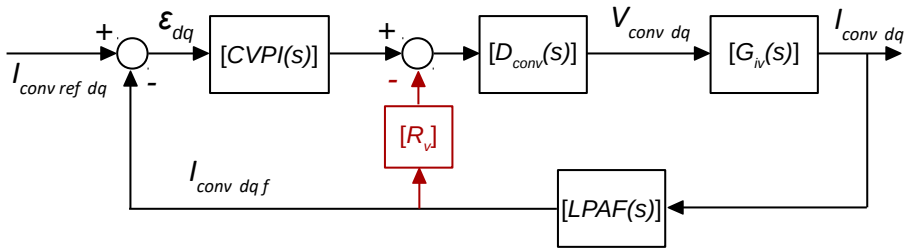


Figure 3.23: Matrix diagram of the current control loop with the CVPI decoupling strategy including the emulation of a virtual damping resistor.

This strategy can be directly applied to the system with the proposed decoupling strategy. In Figure 3.24 the current control loop, including the CCD and the emulation of the virtual resistor in series with the converter inductance (red path), is represented.

If $[R_v]$ is equal to:

$$[R_v] = \begin{bmatrix} R_{virt} & 0 \\ 0 & R_{virt} \end{bmatrix} \tag{3.17}$$

where R_{virt} is the emulated series resistance in series with the converter inductor. The matrix $[CCD(s)]$ has to be adapted to the new effective

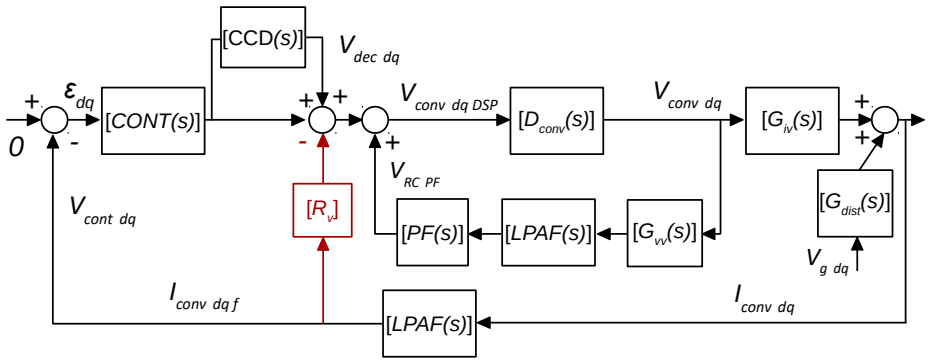


Figure 3.24: Matrix diagram of the current control lop including the CCD decoupling strategy and the emulation of a virtual damping resistor.

equivalent series resistor:

$$[CCD(s)] = \begin{bmatrix} 0 & -\frac{\omega_0 L_{conv}}{L_{conv}s+R_{conv\ s}+R_{virt}} \\ \frac{\omega_0 L_{conv}}{L_{conv}s+R_{conv\ s}+R_{virt}} & 0 \end{bmatrix} \tag{3.18}$$

With this new inner loop, and adapting the CCD for the new equivalent series resistor, the rejection to grid disturbances is analyzed once again in Figure 3.25. In this figure, only the case for the small physical series equivalent resistance of 0.01 Ω is represented. R_{virt} has been set to 0.5 Ω. In Figure 3.25 (a), the diagonal term of the grid disturbance rejection transfer matrix has been represented, while in Figure 3.25 (b) the effect that a step voltage in the d axis has on the converter current on the same axis is represented. Both graphs have been obtained for the equivalent series resistance of 0.01 Ω with and without the emulation of R_{virt}.

The emulation of the virtual impedance allows to improve the rejection to grid disturbances: the peak in the magnitude Bode plot in Figure 3.25 (a) is reduced while the time response is highly improved as it can be seen in Figure 3.25 (b), as a consequence of a greater damping of the complex poles at 50 Hz. The current created in the d axis by a step in the grid voltage in the same axis shows an initial peak that is rapidly driven to zero by the control loop.

To check the effect of the emulation of R_{virt} in the decoupling strategy, in

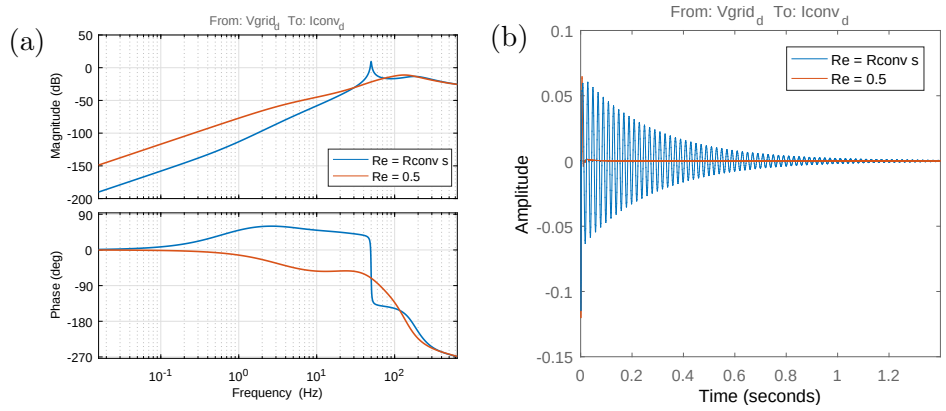


Figure 3.25: Bode plot of the diagonal terms of the rejection to grid disturbances transfer matrix (a) and step response of the current in d axis to a step voltage in the grid voltage in the d axis (b) for an SCR of 15 and an $R_{conv\ s}$ equal to 0.01 Ω. The inner loop with the emulation of a virtual resistor activated is plotted in the red curves, while it is deactivated in the blue curves.

Figure 3.26 the eigenvalues of the open loop transfer matrix, from $\varepsilon_{dq}(s)$ to $I_{conv\ dq}(s)$ are represented, for a $R_{conv\ s}$ equal to 0.01 Ω and an SCR of 15. In each Bode plot two cases are represented: with the emulation of a virtual resistor R_{virt} equal to 0.5 Ω and without this R_{virt}. In this representation, it can be seen that the symmetry around 0 Hz is maintained in the magnitude plot with the emulation of R_{virt}, as the CCD is adapted to take into account the emulated virtual resistance. Moreover, the stability margins are maintained with this emulation, as shown in Figure 3.26 (a) and (b).

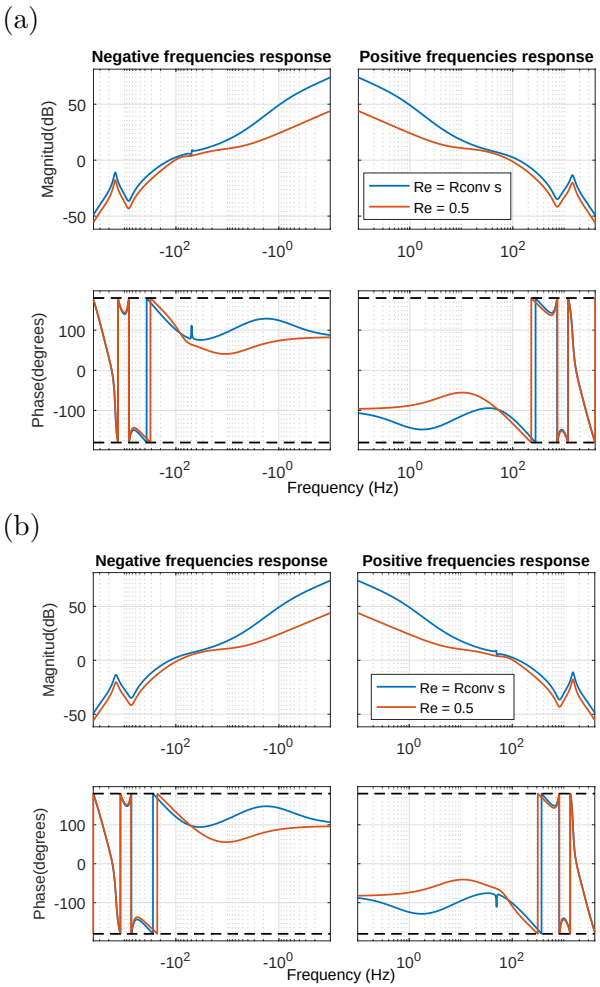


Figure 3.26: Bode plot of the eigenvalues of the open loop transfer matrix for an SCR of 15, with $R_{conv\ s}$ equal to 0.01 Ω and the emulation of a virtual resistor (red) and without this emulation (blue).

With this strategy, based on the emulation of a greater damping resistor

by means of an inner feedback loop, the symmetry around 0 Hz remains almost unaffected from the magnitude point of view, while the rejection to grid disturbances is highly improved. A different approach is presented in the next subsection, where an additional control loop is not required.

3.5.2.2 Improving the rejection to grid disturbances without additional inner loops

A simple way to improve the rejection to grid disturbances, without introducing an additional inner loop, is the emulation of a greater resistor in the CCD. By doing so, the converter inductance is not perfectly decoupled, and the open-loop transfer matrix will have a magnitude peak around 50 Hz (the real DC component), contributing to improve the rejection to grid disturbances. The anti-diagonal terms of the $[CCD(s)]$ are given by:

$$CCD(s) = \frac{\omega_0 L_e}{L_e s + R_{e\ s}} \tag{3.19}$$

If L_e and $R_{e\ s}$ match the converter inductance parameters, a perfect decoupling is achieved in the range of frequencies where the LCL behaves as pure inductor equal to he converter inductance. However, $R_{e\ s}$ can be chosen to emulate a greater value than the real converter inductance, improving the rejection to grid disturbances, but penalizing the decoupling.

The Bode plot of the diagonal term of the rejection to grid disturbances transfer matrix is represented in Figure 3.27 (a). The response to a step in the grid voltage can be seen in Figure 3.27 (b). Both graphs are represented for an SCR of 15 and a $R_{conv\ s}$ equal to 0.01 Ω. The blue curves correspond to an $R_{e\ s}$ in the CCD equal to the actual inductor series resistance. The red curves correspond to an $R_{e\ s}$ in the CCD equal to 0.5 Ω, as in the previous case where an inner loop was included to improve the rejection to grid disturbances.

From Figure 3.27 it is clear that the rejection to grid disturbances is highly increased if compared with the initial case. No magnitude peak exists at 50 Hz in the Bode plot, while in the step response, the effect of a step grid voltage on the converter current is rapidly attenuated. This response is similar to the one obtained in the previous subsection with the inner loop.

The effects that the adjustment of the CCD for a greater virtual resistor has on the decoupling achieved are also evaluated. With this purpose, the Bode plots of the eigenvalues are represented in Figure 3.28 for an inductor equivalent series resistance equal to 0.01 Ω and two different situations: an emulated resistor equal to the actual one (blue) and a series resistance equal

to 0.5 Ω (orange). It can be seen, that both eigenvalues are symmetric in magnitude around 0 Hz in both cases. Moreover, no crossings with -180 degrees occur at the origin, so the -180 degree crossings have to be avoided within the controller bandwidth. However, it should be noted that at 50 Hz the symmetry of the eigenvalues is broken when a greater series resistance is emulated, showing a magnitude peak at this frequency. Despite this peak, responsible of increasing the rejection to grid disturbances, the gain cross-over frequency is the same at positive and negative frequencies with identical phase margins.

Similarly to the previous case, in which a greater series resistance was emulated with an inner control loop, the rejection to changes in the grid voltage is drastically improved. However, with the approach presented in this subsection, the symmetry of the eigenvalues is broken at positive and negative frequencies, specially around 50 Hz (the real magnitude DC component). In this way, the decoupling between both axis is penalized with respect to the inner-loop approach.

To evaluate the effect of emulating in the CCD a different set of parameters than the actual ones, as proposed to improve the converter response in grid-connected applications, in Subsection 3.5.3 the evolution of the dominant poles as the emulated parameters are modified is studied.

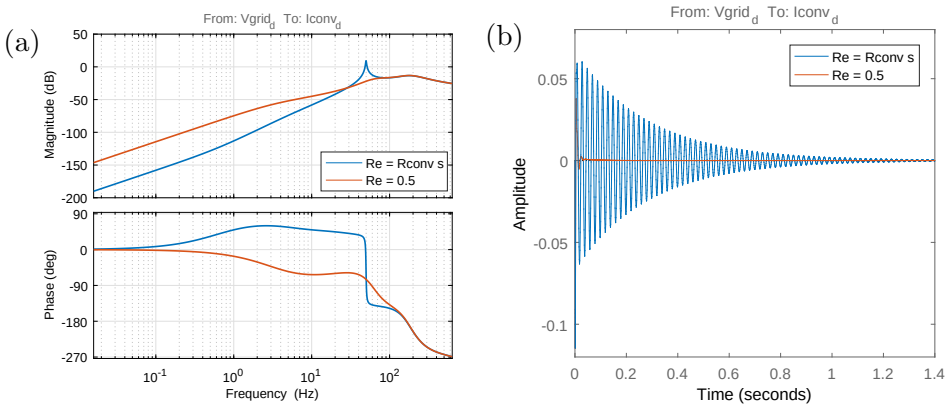


Figure 3.27: Bode plot of the diagonal terms of the rejection to grid disturbances transfer matrix (a) and step response of the current in d axis to a step voltage in the grid voltage in the d axis (b) for an SCR of 15, $R_{conv\ s}$ equal to 0.01 Ω with $R_{e\ s}$ in the CCD equal to $R_{conv\ s}$ and 0.5 Ω.

3.5.3 Robustness against model uncertainties

The decoupling strategy is based on the capacitor voltage positive-feedback and the cancellation of the cross-coupling terms of the resulting plant. For this reason, in this section, the robustness against variations in the real converter inductor parameters and the emulated ones is verified.

The filter components, more precisely the converter inductor, which is the one that determines the decoupling terms, have an inherent uncertainty. This

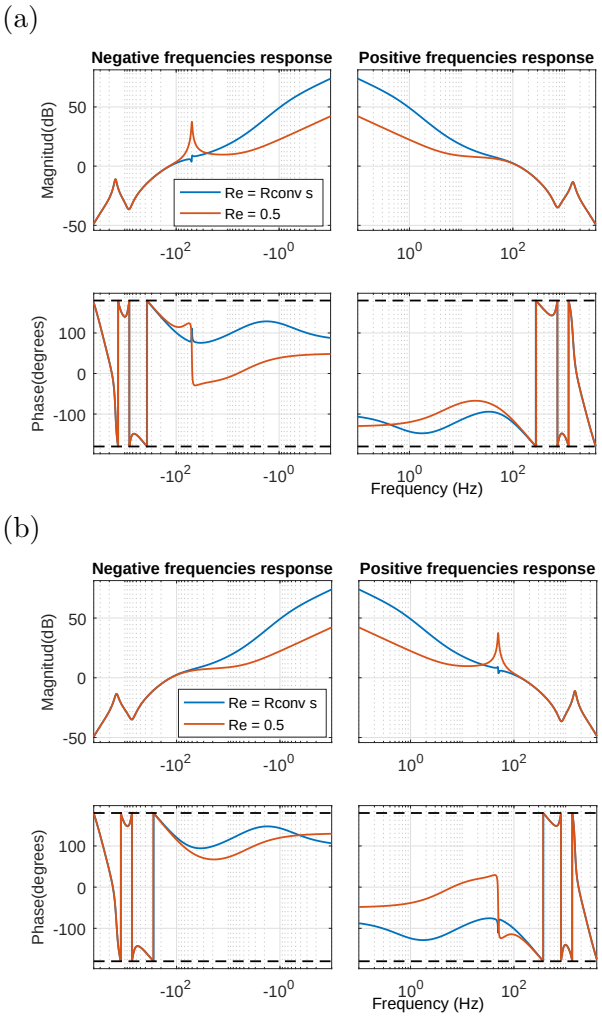


Figure 3.28: Bode plot of the eigenvalues of the open loop transfer matrix for an SCR of 15, $R_{conv\ s}$ equal to 0.01 Ω with $R_{e\ s}$ in the CCD equal to $R_{conv\ s}$ (blue) and 0.5 Ω (red).

uncertainty affects to both the converter inductance value and the equivalent series resistance. This uncertainty is never going to be greater than the ±60% variation considered in the converter inductance and the ±100% variation considered for the inductance series resistance. The closed-loop pole evolution when the emulated parameters does not match the real ones is plotted in Figure 3.29. For space reasons, in the figure $R_{conv\ s}$ is substituted by $R_{c\ s}$ and L_{conv} by L_c. The greater range of variation in $R_{c\ s}$ is justified because the resistance modeling the core losses is frequently unknown. In Figure 3.29 (a), the variation of the slowest poles of the system is represented as L_e is modified with respect to the converter real inductance. In Figure 3.29 (b) the effect on the slowest poles of a modification in the emulated series resistance $R_{e\ s}$, with respect to the real converter series resistance $R_{c\ s}$, is represented. In both cases, the lighter blue poles represent an increase in the emulated parameter with respect to the real one, while a decrease is represented in darker blue. It can be concluded that despite the great variations considered in the emulated parameters the system does not become unstable, however, the response of the slowest poles can be penalized, reducing its damping. This happens when L_e is greater than L_c and when R_e is lower than $R_{c\ s}$. Consequently, in general, it is better to overestimate $R_{c\ s}$ and underestimate L_c.

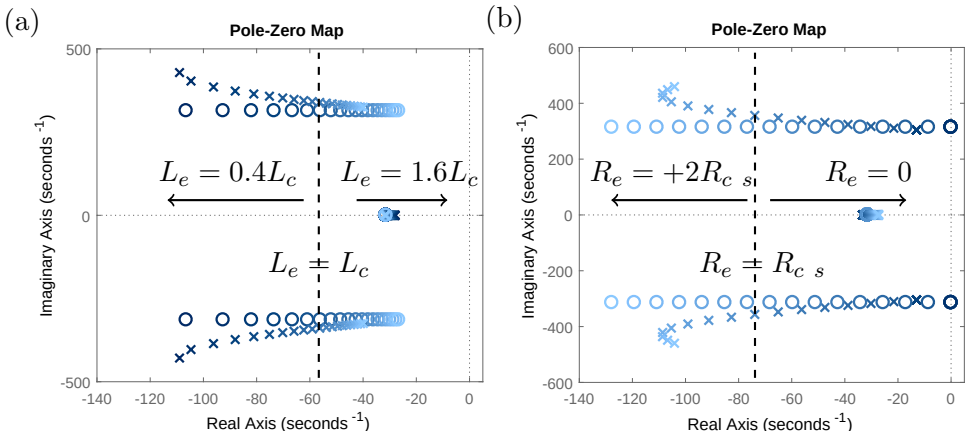


Figure 3.29: Closed-loop pole evolution when the emulated inductance does not match the real converter inductance (a) and when the emulated series resistance does not match the converter series resistance (b).

3.6 Validation of the proposed decoupling strategy – experimental results

The experimental set-up used to validate the proposed decoupling strategy is a 10 kW three-phase two-level power converter of the Renewable Energies Laboratory at the Public University of Navarre. Its parameters are the ones shown in Table 2.2, reproduced here or convenience. The swiching frequency is equal to 3900 Hz and the sampling frequency is equal to the switching frequency (symmetrical regular sampling [HOL03]). This power converter is shown in Figure 3.30 and is controlled by means of an Arduino Due. The DC-bus capacitors are connected to a DC source. The grid voltage is equal to 230 V at a frequency of 50 Hz.

Table 3.1: System parameters of a low power VSC.

Parameter	Symbol	Value
Converter inductance	L_{conv}	2.2 mH
Converter inductance series resistance	$R_{conv\ s}$	100 $m\Omega$
Grid side inductance	L_{gt}	1 mH
Grid side inductance series resistance	$R_{gt\ s}$	70 $m\Omega$
Filter capacitor	C	10 μF
Damping resistor	R_d	1Ω

In this section, the step response, as well as the robustness against plant uncertainties, are validated. Moreover, the proposed decoupling strategy is compared to the state-of-the-art SFD.

3.6.1 Step response

To validate the theoretical model developed to adjust and analyze the proposed decoupling strategy, the step response of this transfer matrix model is compared to the one obtained with a detailed simulation model and the one in the test bench.

The simulation results are performed using both the transfer matrix approach presented in the theoretical analysis, and a model developed using *Matlab Simscape Power Systems Library*. In the *Simscape Power* model, the code is programmed in a C function, and the output of the function are the gate signals to the converter model. The same code programmed in this model in C is the one used in the experimental set-up. This model includes the dead times and the switching patterns that are not modeled in the linear

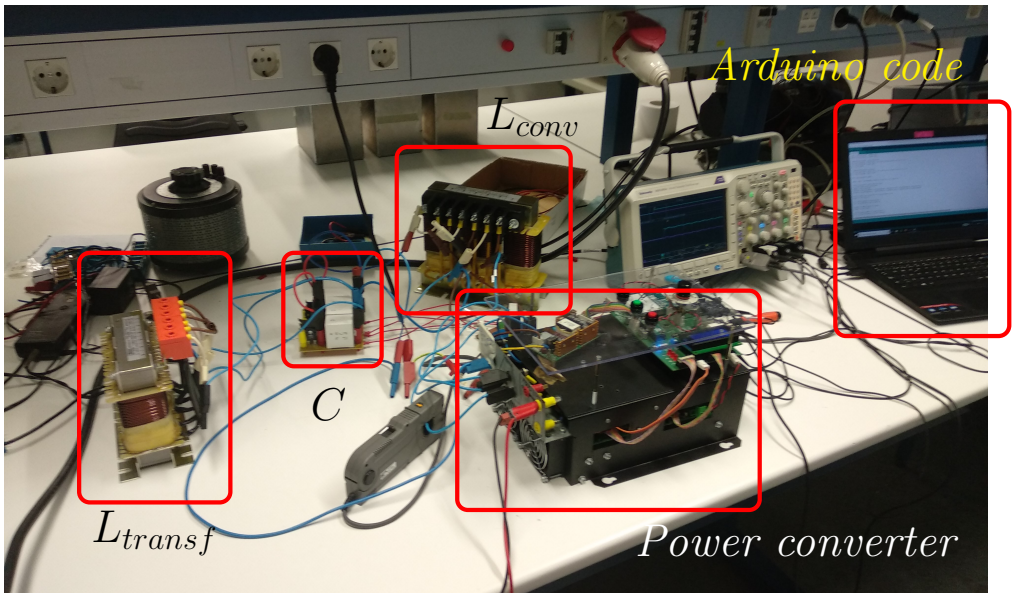


Figure 3.30: Experimental set-up used for the validation of the CCD.

transfer matrix approach used for the theoretical analysis.

A step of 16 A is introduced in the d axis, analyzing the response obtained in both the d and q axis. The diagonal and antidiagonal terms of $[PF(s)]$ are equal to 0.9896 and 0.1488, respectively. The CCD is set to emulate the actual converter inductance parameters. A simple PI control is used, adjusting K_p to 1.5 and T_n to 32 ms. The resulting phase margins, for the strong grid at which the power converter is connected, are high enough with a simple PI, so the lead-lag controller is not required. The transfer matrix linear model step response is plotted in Figure 3.31 (a), the *Matlab Simscape Power Systems* model step response is plotted in Figure 3.31 (b), and lastly, in Figure 3.31 (c), the step response of the experimental set-up is represented as captured by the oscilloscope.

The three graphs are represented in the same time-scale and it can be shown that there is a good agreement between the two models and the experimental set-up. The *Matlab Simscape Power Systems* model perfectly agrees with the experimental setup, while the transfer function model has some differences. The step response in Figure 3.31 (a) is slightly faster than (b) and (c). This is due to the nature of the Laplace domain modeling approach. As explained in Chapter 2, the Laplace domain modeling can be only applied to linear time invariant plants. In real power converters there are non-linear effects, such as the IGBTs commutations, dead times and minimum on times

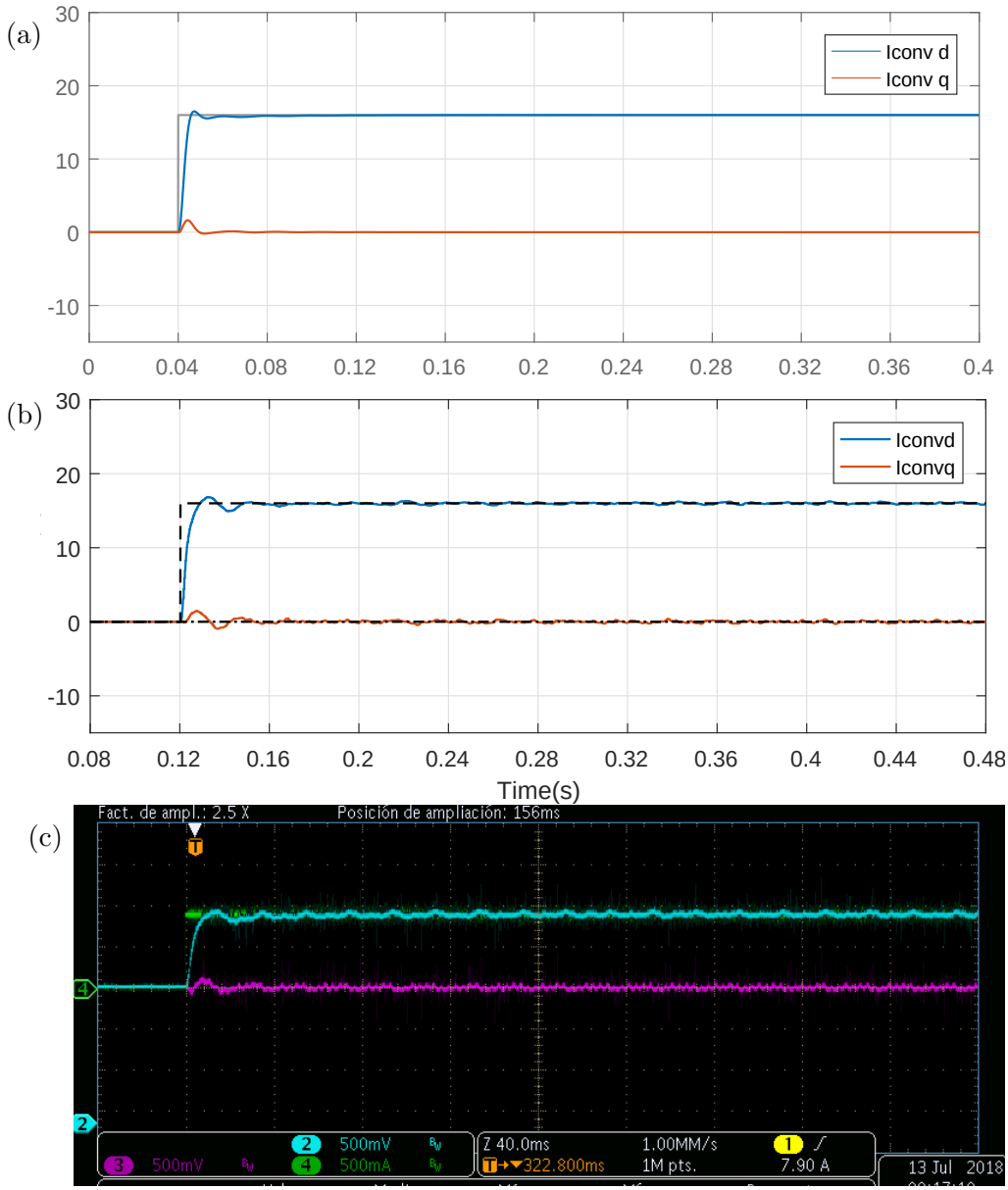


Figure 3.31: Comparison of the step response of the converter for the transfer function model (a), for the simulation model in *Matlab Simscape Power Systems* (b) and in the experimental set-up (9 A/div) (c).

that are modeled in the *Simscape Matlab* model but not in the Laplace domain. These differences in both models help to explain why the transfer

function approach has a slightly faster step response than the real power converter and the simulation model. The oscillations in Figure 3.31 (b) and (c) are created by the filtered switching harmonics of the power converter.

The real magnitude step response of the current is represented in Figure 3.32 for phase a, verifying the fast response of the controller, as well as the low current distortion.

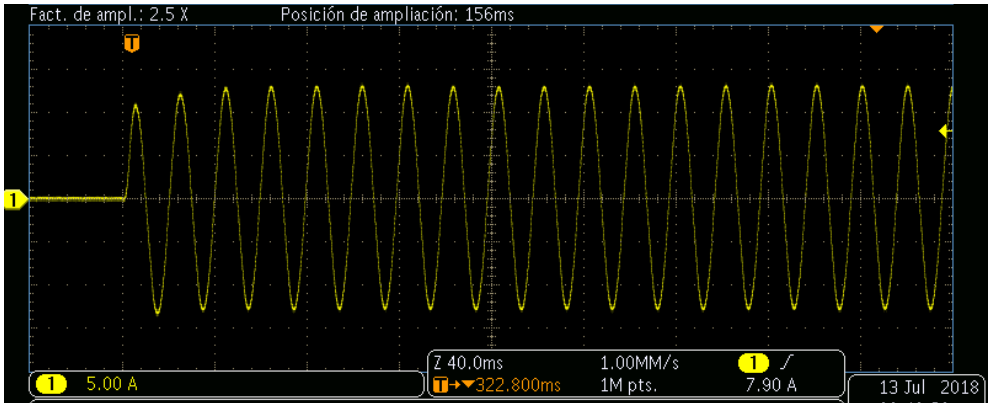


Figure 3.32: Real magnitude of the current in the experimental set-up when a step is introduced in the d axis.

3.6.2 Comparison with the SFD strategy

The decoupling achieved with the CCD is compared in this section with the dominant state-of-the-art decoupling strategy, the SFD, and with the system with no decoupling. The step responses obtained in the experimental set-up are represented in Figure 3.33.

It can be seen in Figure 3.33 (a), that without a decoupling strategy the step response is poor. A step in the current reference in the d axis, requires a step in the converter d axis voltage, which has a strong influence in both d and q components. The dynamic response becomes slow and is highly penalized. If the SFD is implemented, Figure 3.33 (b), the dynamic response is improved with respect to the case without decoupling, but due to the higher coupling between the axis, for the same PI parameters, the system is slower than with the CCD in Figure 3.33 (c). This can be justified from the analysis presented in Section 3.4. With the proposed decoupling strategy, a voltage imposed in the d axis, creates a current in the same axis that is greater than in the q axis by more than 15 dB, while with the SFD this difference is reduced to 9 dB.

3.6.3 Robustness against variations in the plant parameters

To validate the theoretical analysis performed in Subsection 3.5.3, in which the influence of a mismatch in the emulated parameters had on the dominant closed-loop poles was studied, in this subsection, the step response is analyzed

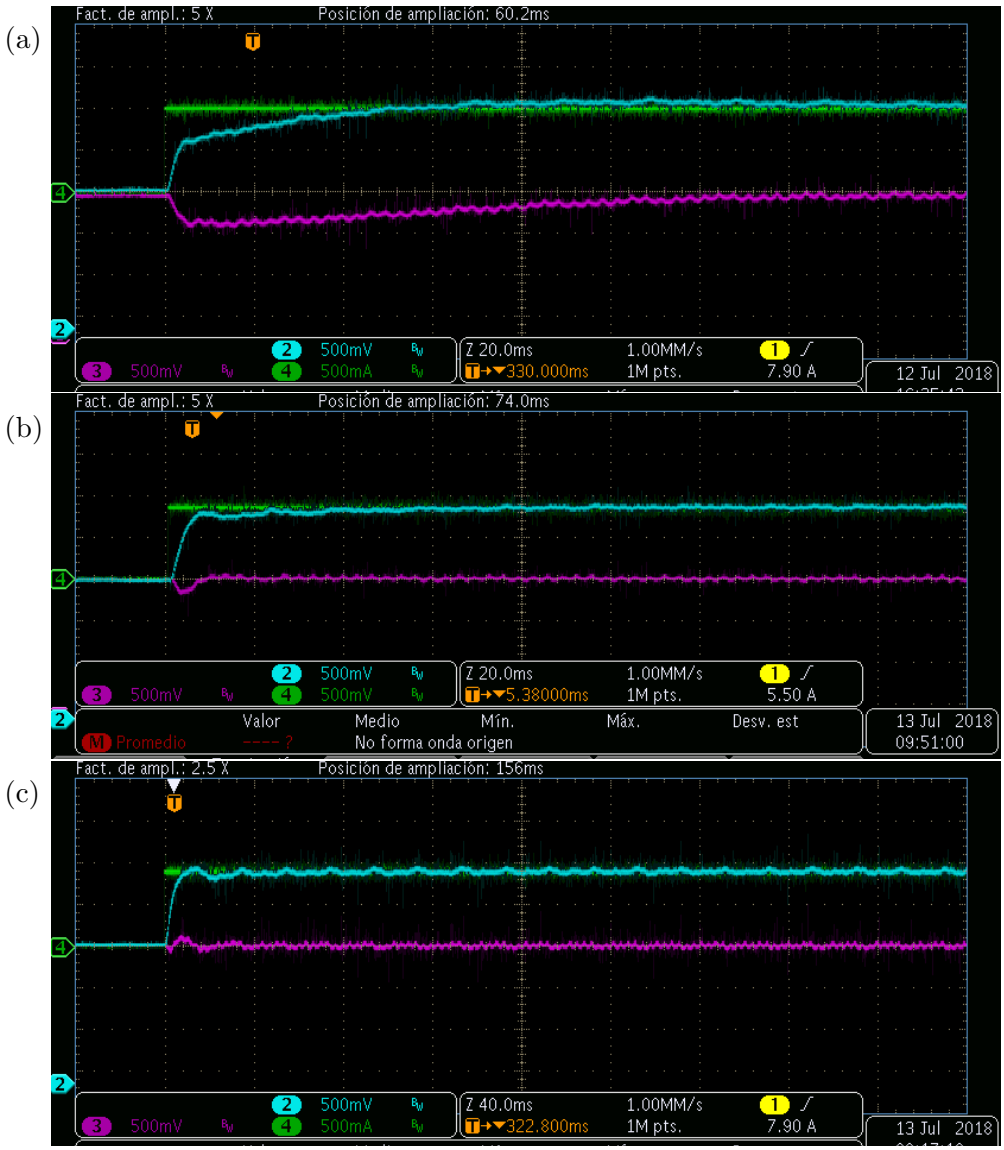


Figure 3.33: Comparison of the step response of the converter without decoupling (a), using the SFD (b) and using the CCD (c).

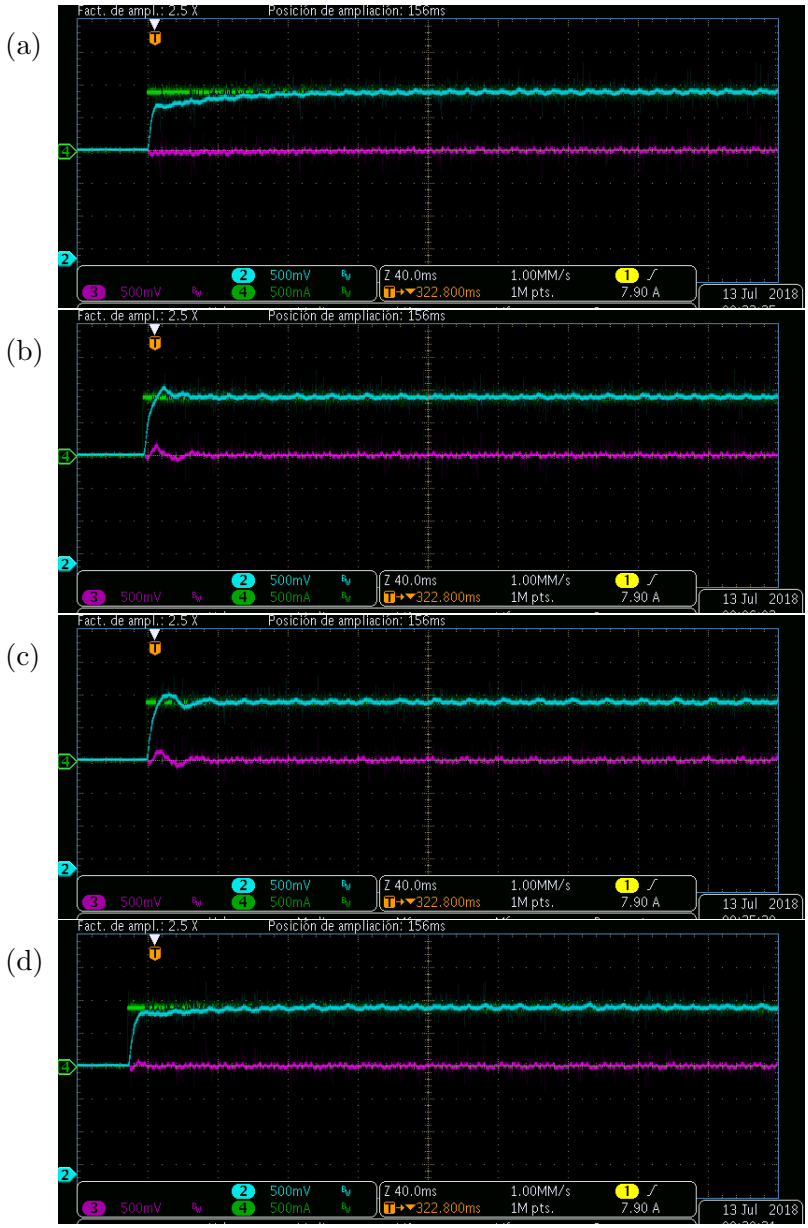


Figure 3.34: Robustness of the decoupling strategy against parameter uncertainty: $L_e = L_c$ and $R_e = 4R_{c\ s}$ (a), $L_e = L_c$ and $R_e = 0.2R_{c\ s}$ (b), $L_e = 1.5L_c$ and $R_e = R_{c\ s}$ (c) and $L_e = 0.5L_c$ and $R_e = R_{c\ s}$ (d).

for several deviations of the emulated parameters with respect to the actual ones. The effects of the mismatches on the damping of the dominant poles is

studied in this subsection through the step response.

In Figure 3.34 (a) and (b) the emulated R_e is modified to $4R_{c\ s}$ and $0.2R_{c\ s}$, respectively. The step response represented for a greater resistor, becomes slower, if compared with the previous one adjusted for the actual value, with no overshoot, as a consequence of a greater damping of the dominant poles. However, if the emulated resistor is reduced to $0.2R_{c\ s}$, a higher overshoot is obtained, as a result of the lower damping in te dominant poles. These results perfectly agree with the ones obtained in Figure 3.29 (b).

In Figure 3.34 (c) and (d) the emulated L_e is modified to $1.5L_c$ and $0.5L_c$ respectively, a 50% variation. Again, the step response agrees with the theoretical results in Figure 3.29 (a). A greater converter inductance value originates a greater overshoot, as a result of a lower damping. In contrast a lower inductance value reduces the overshoot and slows down the dynamic response.

3.6.4 Effects of the offsets in the measurements

To conclude the validation of the proposed decoupling strategy, a practical issue concerning the precision of the measurements, detected in the experimental set-up is discussed.

If the measurements contain a significant DC offset, that it is not compensated, the behavior of the converter current can be highly affected. If the emulated parameters are equal to the actual converter parameters, the rejection to these disturbances is poor, and the offset has a great impact on the current as shown in Figure 3.35 (a). This is caused because the DC offset is translated into a 50 Hz disturbance in *dq*. However, the rejection to disturbances, such as the offsets in the measurements, can be drastically improved if the value used for the resistance in the CCD block, $R_{e\ s}$, is set to a higher value than the actual one. In Figure 3.35 (b) the offsets have not been corrected, the only change made is the modification of $R_{e\ s}$, set to $3R_{conv\ s}$. With this modification the effects of the offsets on the converter current are eliminated, even though it becomes slightly slower.

3.7 Conclusion

In this chapter a novel decoupling structure based on an improved capacitor voltage positive feedback and a cross-controller decoupler has been presented for a *LCL* filter controlled in the SRF. The improved capacitor voltage positive-feedback reduces the plant variability at low frequencies, a

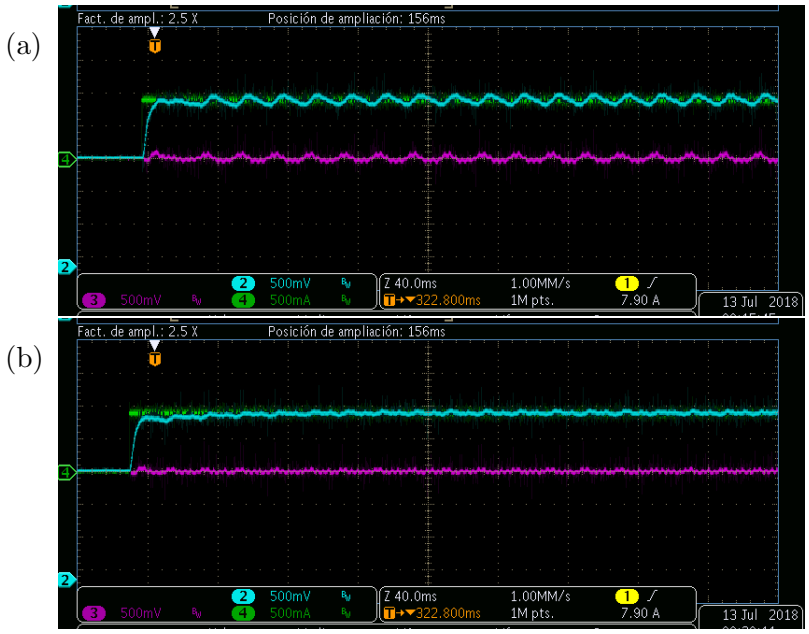


Figure 3.35: Effects that the offsets in the measurements have on the converter current when the $R_{e\ s}$ is equal to $R_{conv\ s}$ and when it is equal to $3R_{conv\ s}$.

variability that is mainly introduced by the variable grid inductance. Once this variability is eliminated, and the behavior of a pure inductance is obtained at low frequencies, a simple first order function, called cross-controller decoupler, CCD, is used to eliminate the cross-couplings. With this decoupling strategy, a greater independence of the response of both orthogonal axis is achieved, specially in weak grids, improving its dynamic response. Moreover, with the CCD strategy, a higher bandwidth with greater stability margins can be achieved with a simple controller, resulting in a better dynamic response if compared with the system without decoupling. The decoupling strategy developed is robust against variations in the emulated parameters. Enhanced rejection to grid disturbances can be provided by using an inner loop that emulates a greater inductance series resistor or without an additional inner loop, by implementing a greater resistor in the cross-controller decoupler than the actual inductor resistor. Experimental results validate the approach presented, showing an almost perfect agreement between the simulations and the results obtained in the experimental set-up. This agreement allows to validate also the detailed modeling approach presented in Chapter 2.

Chapter 4

Active damping of grid-connected power converters with an *LCL* filter

4.1 Motivation

The instability issues of grid connected power converters are not limited to low frequencies, as the ones analyzed in Chapters 2 and 3, within the current control loop bandwidth. As these power converters usually have an *LCL* filter at the output, instabilities at the resonance frequency may appear. This resonance frequency is normally located far from the current controller bandwidth, so there is nothing that this controller can do to stabilize the resonant poles. Moreover, as the power converters are connected to weak grids, the resonance frequency is moved towards lower frequencies, with a greater magnitude peak. This tendency, coupled with the high delays existing in high power converters, increase the instability problems. Traditionally, these instability issues have been tackled from a hardware perspective, adding a resistor in series with the filter capacitor to reduce the magnitude peak at the resonance frequency. However, a more interesting approach is the use of control strategies, called active damping strategies, that guarantee the system stability at the resonance frequency, without compromising the efficiency of the conversion structure. These strategies lose their effectiveness in the case of high power converters, where the lower sampling frequencies, and consequently, higher delays, complicate the implementation of the existing active damping strategies.

In the case analyzed in the two previous chapters, the converter under study is a low power converter whose sampling frequency is similar to the one in high power converters, so the same stability issues arise at low frequencies due to the delays in the control loop. Nevertheless, the passive components in this power converter, mainly the inductors, are not optimized to maximize the efficiency. Consequently, the capacitor series damping resistance and the equivalent series resistor of both inductors, were able to avoid stability problems at the LCL resonance frequency. However, in commercial high power converters as the ones used in WECS, the passive components are optimized to reduce the power losses, increasing the efficiency of the overall conversion structure, but highly reducing the passive damping at the LCL resonance frequency.

A power converter with the same control structure as analyzed in Chapter 2 is studied in this chapter, and represented for convenience in Figure 4.1. The parameters of the power converter are summarized in Table 4.1, corresponding to the GSC of a back-to-back structure used in WECS and developed by the company Ingeteam Power Technologies. The eigenvalues of the open-loop transfer matrix $[H_{ol}(s)]$, correlating the error, $\varepsilon_{dq}(s)$, to the converter current, $I_{conv\ dqf}(s)$, can be calculated as already done in Chapter 2 and are plotted in Figure 4.2 for three SCRs: 1, 15 and 100. From this figure it is clear, that at the resonance frequency, all the -180 degree crossings for every SCR occur when the magnitude is already below 0 dB, so no unstable closed-loop poles

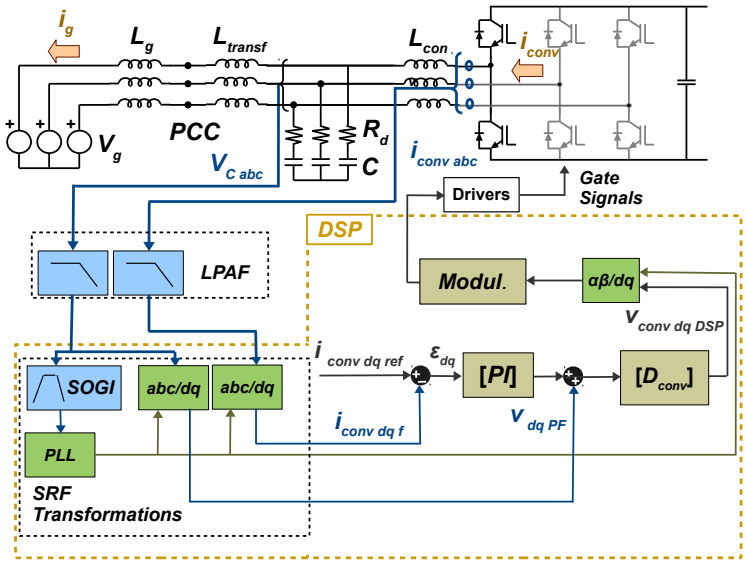


Figure 4.1: Schematic of the converter control loop.

Table 4.1: System parameters for the 500 kW power converter analyzed.

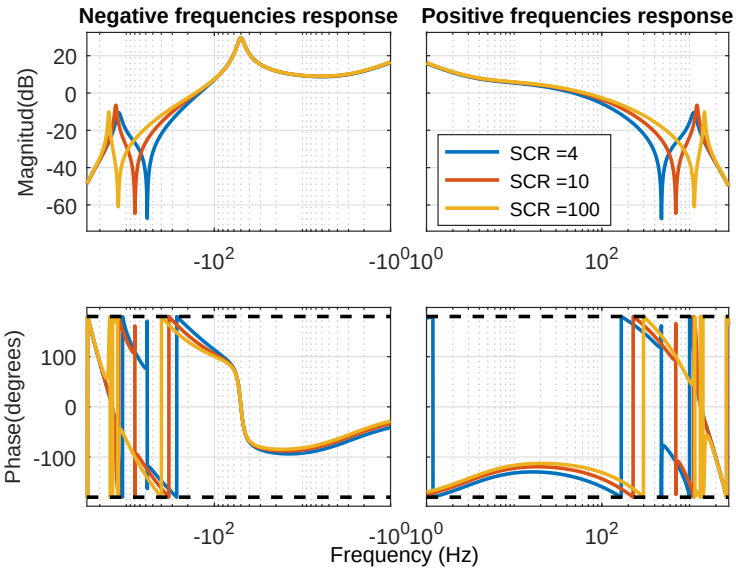
Parameter	Symbol	Value
Grid voltage	V_g	690 V
Rated power	S_{rated}	500 kVA
Sampling-switching frequency	$F_{s_{DSP}}$-F_{sw}	5.6 kHz-2.8 kHz
Converter inductance	L_{conv}	400 μH
Converter inductance series resistance	$R_{conv\ s}$	10 $m\Omega$
Transformer leakage inductance	$L_{transf\ s}$	150 μH
Transformer equivalent series resistance	$R_{transf\ s}$	8 $m\Omega$
Filter capacitor	C	100 μF
Damping resistor	R_d	0 Ω
Short circuit ratio	SCR	1-300

should be expected unless the open-loop transfer matrix also has unstable poles. This is verified in Figure 4.3, where four unstable poles can be seen for the strongest case under consideration. These four unstable poles are translated into the closed-loop, so the system is unstable for the strongest grid under consideration, while in the weakest cases it will be stable.

This result can be shocking at first sight, however, it can be explained from the analysis of the capacitor-voltage positive-feedback. As the short-circuit-ratio is decreased, the grid inductance becomes greater, and the LCL resonance frequency moves towards lower frequencies. At lower frequencies the capacitor-voltage positive-feedback has a damping effect in the resonant poles, stabilizing the control loop. As the grid becomes stronger, the resonance frequency is moved towards higher frequencies, where the capacitor-voltage positive-feedback has the opposite effect. Instead of damping the LCL resonant poles, it tends to destabilize the system, introducing four unstable poles in the open-loop transfer matrix. This is caused by the influence of the delays in the feedback path. The filters, computational delay and ZOH modify the phase in the feedback path, creating a negative feedback at high frequencies that tend to destabilize the resonant poles in strong grids. With this voltage positive-feedback there is nothing that can be done from the control perspective to solve the stability issues, as the active damping strategies are not useful under these circumstances.

To avoid the negative effect of the capacitor-voltage positive-feedback a low pass digital filter is included in this path, as represented in Figure 4.4. This low-pass filter has a cut-off frequency of 100 Hz, in order to attenuate the resonant components in the feedback path. The matrix $[LPDF(s)]$ is a diagonal matrix, whose terms are equal and denoted by $LPDF(s)$. $LPDF(s)$

(a)



(b)

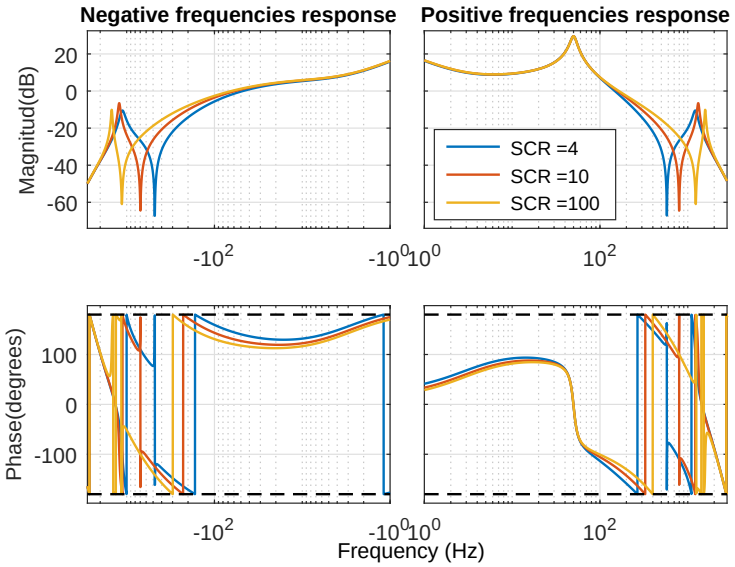


Figure 4.2: Frequency response of the eigenvalues of $[H_{ol}(s)]$ for three SCRs: 1, 15 and 100.

is a first-order low-pass digital filter applied to the magnitudes in the *dq* axis. The system is modeled in the Laplace domain, so its equivalent continuous transfer function is equal to the continuous transfer function already defined

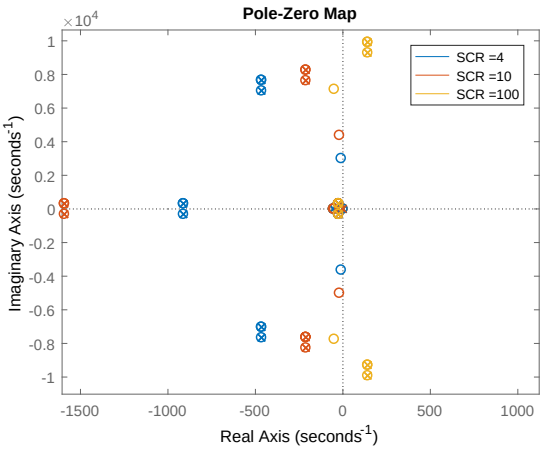


Figure 4.3: Open-loop poles of the current control loop.

for the low-pass analog filter.

The stability is analyzed again for the system presented in Figure 4.4. For this current control loop, the transfer matrix model represented in Figure 4.5 can be obtained.

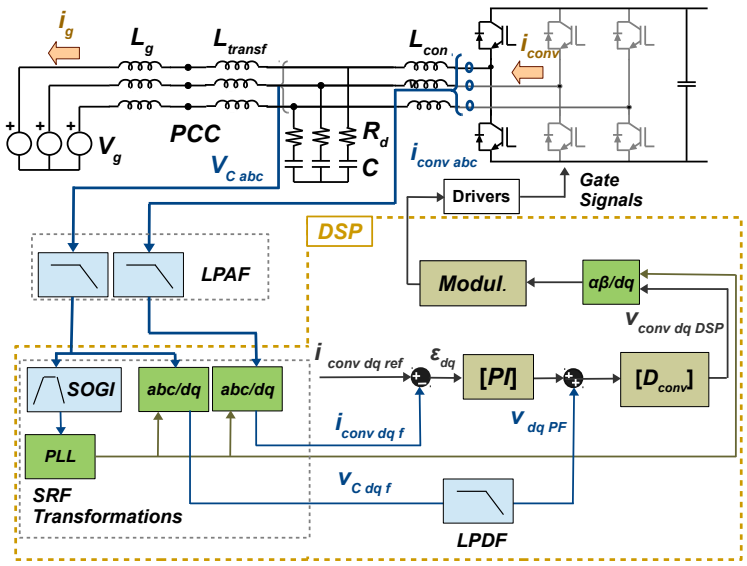


Figure 4.4: Schematic of the converter control loop including the low-pass digital filter in the capacitor positive-feedback.

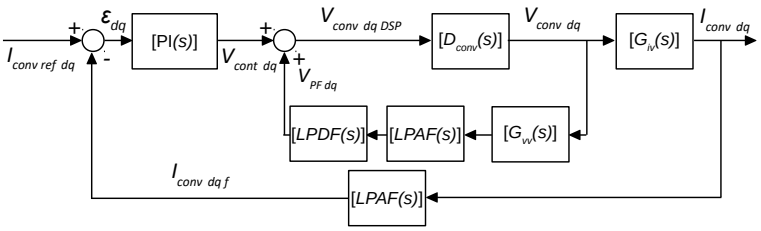


Figure 4.5: Matrix representation in the Laplace domain of the converter current control loop including the low-pass digital filter in the capacitor positive-feedback.

The eigenvalues of the open-loop transfer matrix, $[H_{ol}(s)]$, from $\varepsilon_{dq}(s)$ to $I_{conv\ dqf}(s)$, are calculated by operating with the matrix representation of the current control loop of Figure 4.5. In this case, an important magnitude peak at the resonance frequency is obtained, as the capacitor-voltage positive-feedback does not have an influence on the resonant poles. It can be seen in Figure 4.6 (a) and (b) that around the resonance frequency, four -180 degree-crossings occur for every SCR when the magnitude is positive, meaning that the closed loop transfer function will have four unstable poles for these SCRs. This can be verified when the closed loop poles of the converter current control are represented in Figure 4.7, where the four -180 degree-crossings are translated into four unstable poles at the same frequency than the crossings.

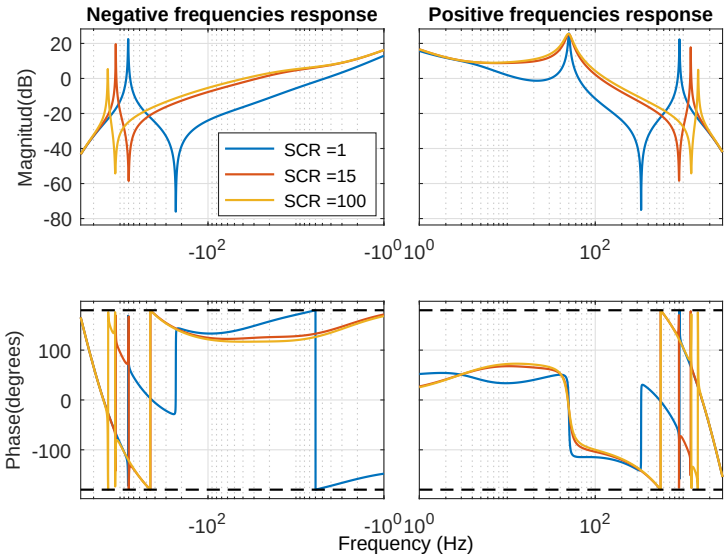
In Figures 4.2 and 4.6 it can be seen that the variation in the effective grid inductance greatly modify the output filter resonance frequency. To include any possibility in the stability analysis made in this chapter of the thesis, these variations are bounded by the ideal limits of SCR given by 0, obtaining the lowest resonance frequency (F_{r_l} in Equation 4.1) and ∞, obtaining the highest resonance frequency (F_{r_h} in Equation 4.2).

$$F_{r_l} = \frac{1}{2\pi}\sqrt{\frac{1}{C_f L_{conv}}} \tag{4.1}$$

$$F_{r_h} = \frac{1}{2\pi}\sqrt{\frac{L_{trans} + L_{conv}}{C_f L_{conv} L_{transf}}} \tag{4.2}$$

A SCR equal to ∞ means that the converter is connected to an ideal grid, without an impedance, while a SCR of 0 means that the grid has an infinite impedance. Currently, in many wind farms demand a stable operation within SCRs of ∞ and less than 1. In this chapter, a wider variation than the current requirements are applied, anticipating future restrictions.

(a)



(b)

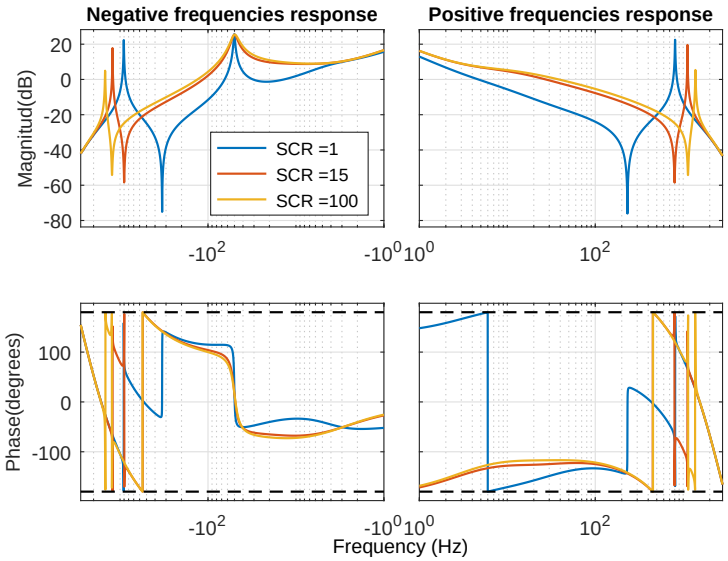


Figure 4.6: Frequency response of the eigenvalues of $[H_{ol}(s)]$ for three SCRs: 1, 15 and 100.

In a real application, the parasitic resistances of the inductors, which tend to increase with frequency, capacitors and semiconductors will help to stabilize the system for the strongest SCR values. However, for the rest of the cases, an active damping method has to be introduced to avoid using additional

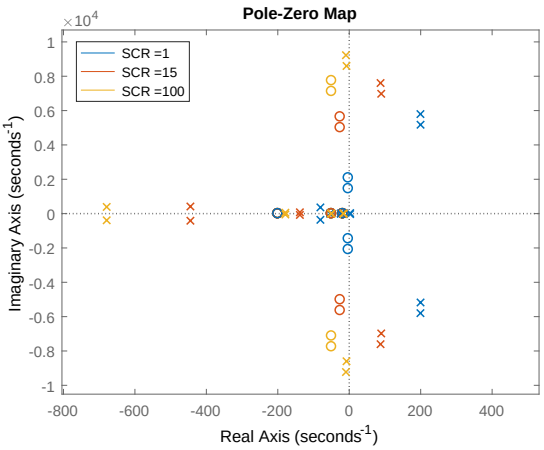


Figure 4.7: Closed loop poles of the current control.

resistors and consequently increasing the power losses.

4.2 State-of-the-art active damping techniques

To avoid the stability problems at the *LCL* resonance frequency, there are several passive damping approaches, consisting in the addition of damping resistors that increase the converter power losses. Even though some damping topologies present reduced power losses [BER16b], they introduce additional passive components and the filter complexity grows.

Alternatively, the active damping (AD) approaches have been widely explored in the literature, as they can stabilize the system without increasing its power losses. The capacitor voltage positive-feedback can effectively damp the filter resonant poles, but it becomes ineffective as the *LCL* resonance frequency approaches the converter control Nyquist frequency [LI18]. This circumstance occurs in high power converters, as shown in Section 4.1, where the switching frequency, and accordingly the sampling frequency, is limited to reduce the power losses, and the resonance frequency is increased to lower the filter size, a different AD strategy is required. A notch filter, inserted in the current control loop and tuned at the resonance frequency, could damp the resonance [DAN11], but it requires an estimation of the effective grid inductance, as it can change depending on the grid at which the VSC is connected and the power injected at the PCC [AGO11, AKH18]. Alternatively, a lead-lag controller can be tuned in the current control loop

to avoid -180 degree crossings [DAN11] that can lead to instability. However, when the resonance frequency approaches the converter control Nyquist frequency, it is unable to introduce enough phase lead. A suitable option to overcome this limitation is the introduction of additional delays and low-pass filters [WAN16], which are able to stabilize the resonant poles. Nevertheless, they provide a poor damping at the resonant poles, compromising the grid current harmonic content and, therefore, the fulfillment of the grid codes. The capacitor current proportional feedback is one of the preferred solutions, equivalent to the implementation of a virtual resistor in parallel with the filter capacitor [DAN10, PAR14, PAN14, WAN15, SAÏ18]. The main drawback is that it requires additional sensors as this current is not normally measured in a grid-connected VSC. An alternative is using the capacitor voltage, already measured for synchronization purposes, computing its derivative to estimate the capacitor current and performing an active damping strategy equivalent to the previous one [LIS02, XIN16, PEÑ14].

Both, the capacitor current feedback and the capacitor voltage derivative AD strategies, are based on the emulation of a virtual damping resistor. However, this virtual resistance becomes a virtual impedance by the effects of the control delays [PAN14, WAN15]. The real part of the emulated virtual impedance varies with frequency and it can become negative, leading to instability if the resonance frequency is located in the negative region. This issue has been reported in the literature: in [PAR14] the stability region where the capacitor current AD can effectively damp the resonance is limited to $\omega_s/6$, ω_s being the sampling frequency. The stability region calculated imposes constraints on the *LCL* filter design: the *LCL* resonance has to be lower than $\omega_s/6$. This restriction compromises the achievement of an optimised filter in order to meet the grid codes at the lowest price. In [PAN14] they identified the same stability limits, suggesting that the resonance frequency should be limited to be lower than $\omega_s/6$, where the emulated virtual resistance is positive, so that the AD can stabilize the resonant poles. Alternatively, they proposed reducing the computation delay to widen the stability interval. At last, [WAN15] proposed an *RC* virtual damper that modifies the stability region, changing the feedback sign in order to operate at the region where the emulated virtual resistor is negative. In this case the resonance frequency is restricted to a wider interval limited by $\omega_s/5$ and $\omega_s/2$.

The stability regions provided in the literature do not have to meet the *LCL* resonance frequency limits of a real filter design. In the commercial high power converter presented in Section 4.1, the converter side inductance is around 0.1 p.u., the filter capacitor is 0.03 p.u., while the grid side inductance

is formed by the transformer leakage inductance, 0.05 p.u., and the effective grid inductance, which is unknown and would modify the filter resonance frequency. The resonance frequency, for the values provided in Table 4.1, is bounded within $0.15\omega_s$ and $0.27\omega_s$, as the grid inductance varies from an SCR at the PCC of 1 to 300. This interval of possible resonance frequencies does not fall within the stability regions identified by the previous papers, as it is represented in Figure 4.8.

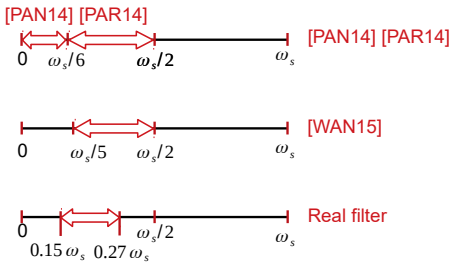


Figure 4.8: AD stability intervals provided in the literature and LCL resonance frequency variation of a real power converter.

4.3 Proposed active damping strategy

To solve the issues presented in Section 4.2, a different approach is presented in this section. Instead of designing the LCL filter to locate the resonance frequency where the AD is able to stabilize the resonant poles, the AD stability region is modified and adapted to be robust and stable within the entire range of frequencies where the LCL resonant poles can be located for a given power converter design. With this purpose, the delay in the AD path is modified after an analysis of the existing delays in the control loop, considering the filters applied to the measurements. These filters are neglected in the literature, even though they strongly affect the AD stability region and must be introduced to avoid noise amplification by the derivative action. Analytical expressions are provided for the adjustment of the delay, which are valid for both the capacitor current proportional feedback and the capacitor voltage derivative AD (CVDAD), as it is particular case of the other technique. This chapter is focused on the latest strategy, but at the end of the chapter, the theory presented is extended to the capacitor current active damping.

The proposed adjustment of the AD strategy requires an appropriate implementation of the derivative. However, in high power converters, the

LCL resonance frequency can fall close the control Nyquist frequency. In these cases, the digital implementation of the derivative is not possible without a magnitude or phase distortion. For this reason, a study of the techniques to compute the derivative is developed, proving that the multisampled derivative is the most convenient option for the proposed active damping strategy.

In this section, as a first step, analytical expressions are developed to describe the AD strategy. The second step leads to the analysis of the implementation of the derivative, and finally, a systematic procedure is proposed to select the parameter of the active damping.

4.3.1 General description of the active damping strategy

In Figure 4.9 the SRF plant model and control loop, including the proposed AD, are represented. The AD feedback branch, depicted in green, includes two term; $[Der(s)]$ and $[H_{AD}(s)]$. $[Der(s)]$ is the derivative action proposed in the literature, given by:

$$[Der(s)] = k_{AD} \begin{bmatrix} s & 0 \\ 0 & s \end{bmatrix} \tag{4.3}$$

where k_{AD} is a constant. $[H_{AD}(s)]$ is a new block proposed in this thesis whose main purpose is adapting the delay in the AD path to avoid stability problems caused by the variations in the sign of the damping action, within all the range of frequencies where the *LCL* resonance frequency can be located. Without $[H_{AD}(s)]$, the damping based on the derivative could even tend to destabilize the system. $[H_{AD}(s)]$ is a diagonal matrix whose diagonal terms are denoted by $H_{AD}(s)$.

To tune the transfer function $H_{AD}(s)$ and the gain k_{AD}, the interaction between the active damping branch and the rest of system has to be studied. The transfer matrix diagram represented in Figure 4.9 can be decomposed into blocks, as shown in Figure 4.10. In this block diagram, the series resistances of the passive components have not been taken into account, because they increase the model complexity and they are not required for the analysis performed in the following.

From Figure 4.10 it is clear that the AD action is affected in the direct path by $D_{conv1}(s)$ and $LPAF_1(s)$ and in the cross path by $D_{conv2}(s)$ and $LPAF_2(s)$. It must be reminded that $D_{conv1}(s)$ and $D_{conv2}(s)$ stand for the diagonal and anti-diagonal terms of $[D_{conv}(s)]$, while $LPAF_1(s)$ and $LPAF_2(s)$ are those corresponding to $[LPAF(s)]$. Adjusting $H_{AD}(s)$ to guarantee the damping

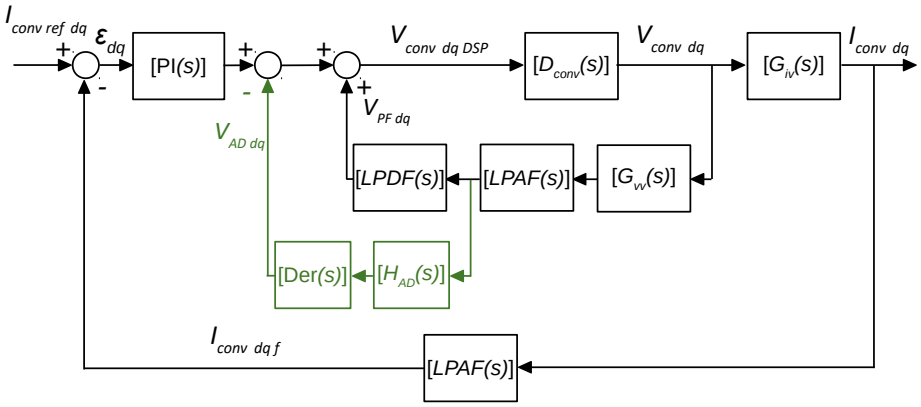


Figure 4.9: Matrix representation of the current control loop including the CVDAD.

action considering the complete model is unnecessary complex, for this reason, some simplifications are made. $D_{conv1}(s)$ always has a magnitude greater than $D_{conv2}(s)$ and $LPAF_1(s)$ is also greater than $LPAF_2(s)$, in this case 14 and 100 times greater respectively within the interval of possible resonance frequencies,

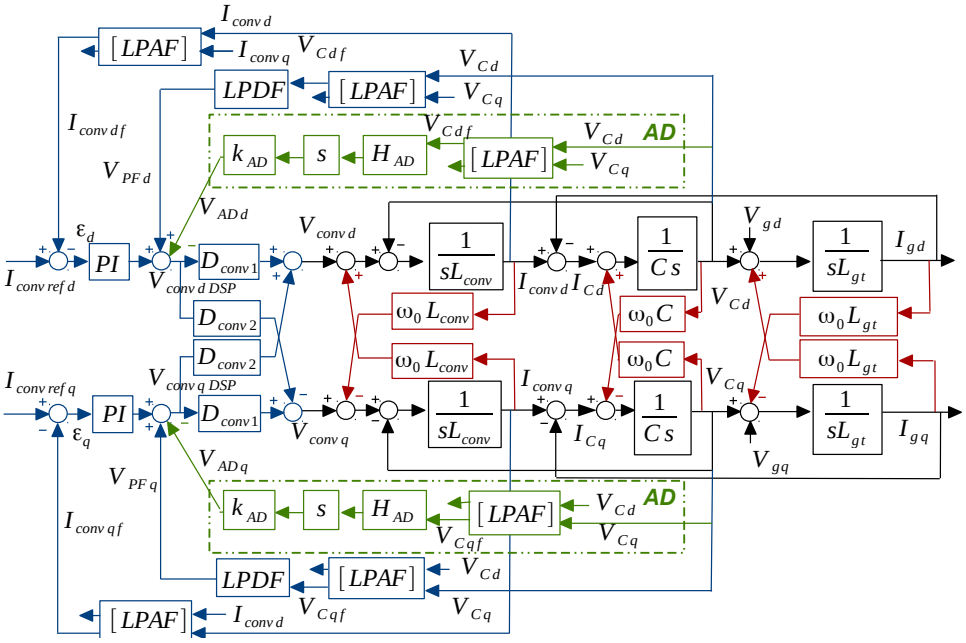


Figure 4.10: Block diagram representation of the current control loop including the CVDAD.

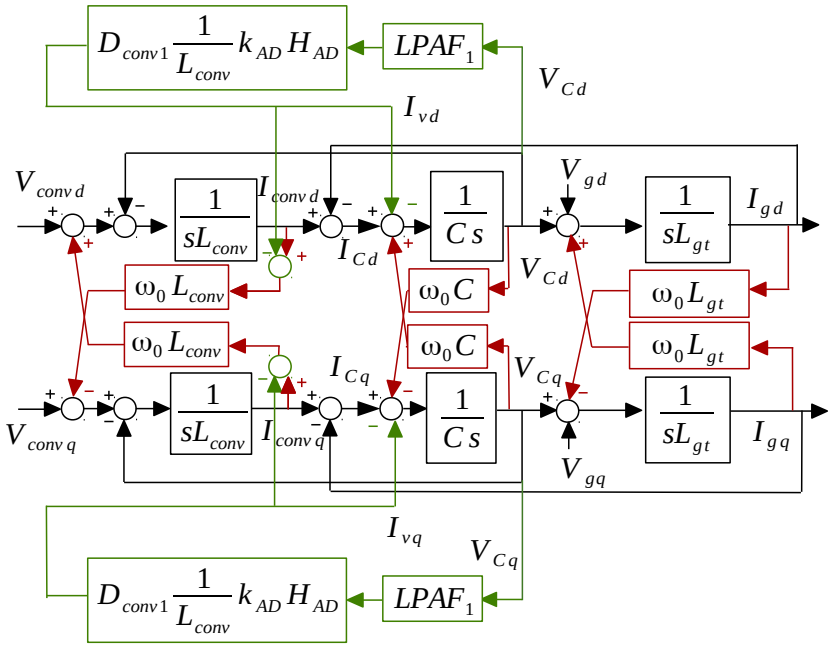


Figure 4.11: Simplified block diagram representation of the CVDAD strategy.

so they can be neglected for the adjustment. By neglecting the cross terms for the AD tuning, the AD control loop diagram can be rearranged as shown in Figure 4.11, where only the plant and the AD loop are shown for clarity. With these simplifications it is clear that the AD feedback is the same in d and q axis, so only the d axis is studied in the tuning procedure. A virtual impedance can be defined as the ratio of the capacitor voltage in one axis and the virtual current in the same axis. This impedance is given by:

$$Z_{AD}(s) = \frac{V_{Cd}(s)}{I_{vd}(s)} \approx \frac{L_{conv}}{H_{AD}(s)D_{conv1}(s)k_{AD}LPAF_1(s)} \tag{4.4}$$

Which can be redefined as:

$$Z_{AD}(s) \approx \frac{R_{da_v}}{H_{AD}(s)D_{conv1}(s)LPAF_1(s)} \tag{4.5}$$

where the ratio L_{conv}/k_{AD} has been defined as R_{da_v}, a damping virtual resistor.

Equation 4.5 includes the components generally found in the classical AD strategies: a virtual impedance dependent on D_{conv1} and $LPAF_1$. It is known that the real part of this classical emulated virtual impedance,

$Re(Z_{AD}(s))$, or equivalently, its resistive component, changes its value and sign as a function of frequency. A change in the sign of $Re(Z_{AD}(s))$, within the location of the poles at the resonance frequency, causes instability [PAR14, PAN14, WAN15]. But the proposed additional term $H_{AD}(s)$ in the AD path, will be designed to modify the delay and guarantee no changes in the sign of $Re(Z_{AD}(s))$ within the range of possible resonance frequencies. Nevertheless, before addressing this key aspect, a detailed analysis of the derivative term is required within the entire range of possible LCL filter resonance frequencies. The implementation of the derivative in the digital controller becomes complex taking into account the low switching frequencies and the high sampling times of high power converters.

4.3.2 Digital implementation of the derivative

The digital implementation of the derivative in the DSP is not possible without a significant magnitude or phase distortion close to the control Nyquist frequency [XIN16]. The distortion of the derivative depends on its implementation and the sampling time. Both aspects are discussed in this section.

Equation 4.6 contains the backward Euler discrete implementation of the derivative.

$$Der(z) = \frac{1 - z^{-1}}{T_s} \tag{4.6}$$

where T_s stands for the sampling time. If this derivative is implemented in the DSP ($T_s = T_{s_{DSP}}$), which is executed twice per switching period, it loses up to 90 degrees as it approaches the control Nyquist frequency, as shown in Figure 4.12. For the specific power converter under consideration, within the limits for the LCL filter resonance frequency (F_{r_l},F_{r_h}), represented by the vertical dashed lines in Figure 4.12. With this derivative, the phase at the maximum resonance frequency is equal to 35 degrees, far from the ideal 90 degrees.

Recently, more accurate derivatives have been presented for the capacitor voltage active damping, in order to extend the applicability of this active damping approach [XIN16, PAN17]. In [PAN17] two differentiators are proposed with the same derivative characteristics as the non-ideal generalized integrator presented in [XIN16], so the two proposals presented in [PAN17] are discussed here, due to their simple expressions and their direct discrete nature. The first proposal is a first order differentiator, given

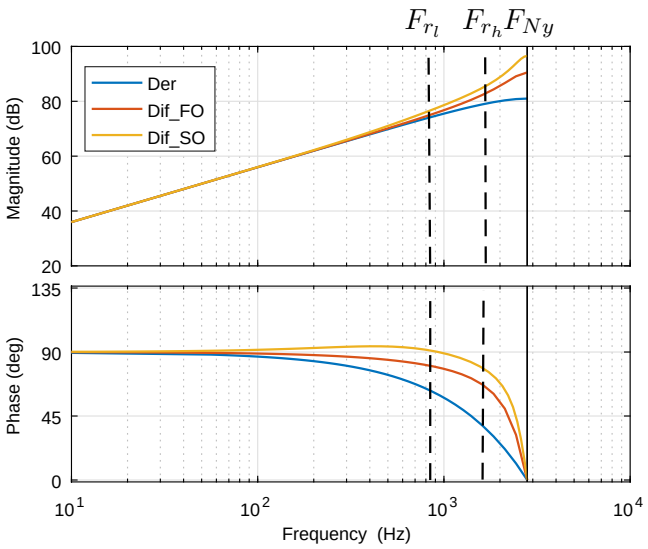


Figure 4.12: Comparison of the frequency response of the backward Euler derivative and the first- and second-order differentiators proposed in [PAN17] when they are implemented in the DSP.

by Equation 4.7.

$$Dif_{FO}(z) = \frac{1+m}{T_{s_{DSP}}} \frac{1-z^{-1}}{1+mz^{-1}} \tag{4.7}$$

where m is a constant that can vary between 0 and 1. The second proposal is a second order differentiator, given by Equation 4.8

$$Dif_{SO}(z) = \frac{2}{T_{s_{DSP}}} \frac{(k+1)(2-z^{-1})(1-z^{-1})}{2(k+1)+z^{-1}-z^{-2}} \tag{4.8}$$

where k is a constant that can vary between 0 and infinity. The parameters m and k modify the frequency response of the derivative close to the control Nyquist frequency. For the representation made in Figure 4.12, m has been chosen to be 0.5 and k has been chosen to be 1, trying to find a compromise between phase flatness within F_{r_l} and F_{r_h}, while keeping the magnitude peak at the control Nyquist frequency at a reduced value.

From Figure 4.12 it can be concluded that for the *LCL* filter parameters under consideration, the derivatives proposed in [XIN16, PAN17] can perform an accurate derivative within the limits of the *LCL* resonance frequency. However, in both cases, the error in the phase grows rapidly

towards the control Nyquist frequency, F_{Ny}. In some high power conversion systems, such as in parallel interleaved power converters, used in high power wind turbines above 4 MW where the LCL resonance frequency is designed to attenuate higher-order harmonics than the first switching harmonic family, the resonance frequency is moved towards the control Nyquist frequency, and these differentiators could not be used.

To solve this limitation, the use of a multisampled derivative is proposed. The implementation can be made on an external device, such as a field programmable array (FPGA), or in the same DSP by making use of interrupts. In many applications, the DSP is already complemented by an FPGA sampling the measurements at a greater speed for filtering purposes [BUE09]. This is a common approach in high power converters, where the control sampling frequency is limited as a result of the reduced switching frequency. To explain how the multisampled approach can be easily implemented, in Figure 4.13 the sample instants of the DSP, k, and the FPGA, r, are represented. The FPGA only performs the difference between two consecutive samples. At instant k the DSP samples the difference between the FPGA samples r and *r-1*, which is used for the control calculations.

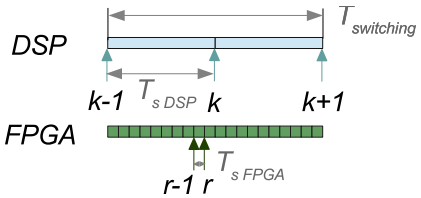


Figure 4.13: Time diagram illustrating a possible implementation of the multisampled derivative in a FPGA.

The multisampled derivative is implemented using Equation 4.6, with a high enough ratio of the DSP to the FPGA sampling times, the derivative has almost no phase distortion within the limits of the LCL resonance frequency. This is shown in Figure 4.14, where the frequency response of the multisampled backward Euler derivative is plotted for three multisampling ratios, mr, of the FPGA sampling frequency to the DSP sampling frequency. If the FPGA runs 4 times faster than the DSP, an accurate derivative is obtained within F_{r_l} and F_{r_h}, but at the control Nyquist frequency it loses 24 degrees. If the the multisampling ratio is equal to 10, less than 6 degrees would be lost at the the highest resonance frequency, F_{R_h}. If the FPGA runs only 4 times faster than the DSP, at the maximum resonance frequency 14 degrees would be lost. If mr is reduced to a minimum of 2, a higher deformation is obtained in the phase of the derivative and 30 degrees would be lost at F_{R_h}. For a mr equal

to 2, the FPGA Nyquist frequency is denoted in Figure 4.14 as $F_{Ny\ mr2}$.

4.3.3 Procedure for the systematic design of H_{AD}

The design of the transfer function applied in the AD path, $H_{AD}(s)$, is a key aspect to achieve a robust AD. This transfer function, as shown in Equation 4.9, includes two terms. The first term is a band pass filter, $BPF(s)$, designed to avoid noise amplification and reduce the AD action to the one required for damping purposes. The second term is an adjustable delay, $DAD(s)$, included to achieve the desired robustness in the AD strategy long the entire range of possible resonance frequencies.

$$H_{AD}(s) = BPF(s)DAD(s) \tag{4.9}$$

The design of $H_{AD}(s)$ is made in two steps:

- *Step 1: Design of the bandpass filter.*

$BPF(s)$ should be able to attenuate both the switching frequency harmonics and the fundamental component (DC in dq), to avoid noise amplification and to reduce the applied AD action. However, it should not affect the AD action inside the range of possible resonance frequencies (from F_{r_l} to F_{r_h}), where the AD is required. As a general rule to achieve these goals, the lower stop-band is set at half the lowest LCL resonance frequency, $F_{r_l}/2$, and the highest stop-band is set at $(F_{r_h} + F_{sw})/2$, F_{sw} being the switching frequency. Once both stop-bands have been set, the filter order has to be defined. For the power stage studied in this works, a second-order filter is used. If a greater attenuation were required, the order of the filter could be increased.

- *Step 2: Adjustment of the delay.*

If a change in the sign of the emulated virtual resistance occurs within the range of possible LCL resonance frequencies, the system will be unstable for some SCR, as the AD will generate a destabilizing action. In Figure 4.15 the real part of $Z_{AD}(s)$ is plotted against frequency for a R_{da_v} equal to 1 and three different AD techniques, to illustrate this problem. The CVDAD with the classical derivative, including the $BPF(s)$ and the $LPAF_1(s)$, is able to stabilize the resonant poles for weak grids (lowest resonant frequencies), but it will be unstable if it is connected to strong grids. If the multisampled

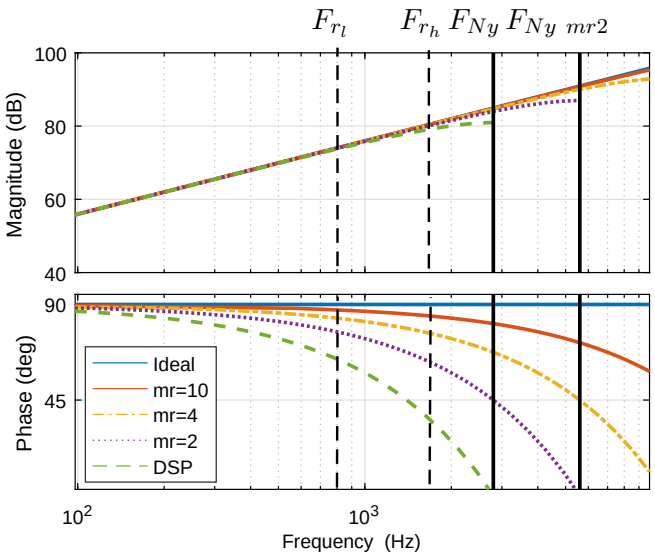


Figure 4.14: Comparison of the frequency response of the ideal derivative with the backward Euler derivative implemented in the DSP and in an FPGA running 10, 4 and 2 times faster than the DSP.

derivative is used, the delay in the feedback path is reduced and the AD is able to stabilize the system for strong grids, but not in the weakest cases. However, these changes in the sign of $Re(Z_{AD}(s))$ inside the range of possible resonance frequencies (from F_{r_l} to F_{r_h}) can be avoided by modifying the phase, adding an additional delay in the AD feedback path, $DAD(s)$. $DAD(s)$ is calculated to achieve at the central resonance frequency, $F_{r_c} = (F_{r_l} + F_{r_h})/2$, a pure virtual resistance. As shown in Figure 4.15, using the multisampled derivative and the proposed additional delay, $DAD(s)$, the AD will be able to stabilize the system in the whole range of resonance frequencies, shifting the changes in the sign of $Re(Z_{AD}(s))$ outside the range of possible resonance frequencies to achieve the desired robustness. A negative virtual resistor is emulated, so the AD feedback path sign has to be positive.

As a first step to adjust $DAD(s)$, the phase of $Z_{AD}(s)$, $\varphi(Z_{AD}(s))$, has to be characterized and it is given by:

$$\begin{aligned}\varphi(Z_{AD}(s)) = &- \varphi(D_{conv1}(s)) - \varphi(LPAF_1(s)) - \varphi(BPF(s)) - \\ &- \varphi(DAD(s))\end{aligned} \tag{4.10}$$

The additional delay, expressed as the number of sample times, y, required to achieve a purely resistive impedance at the central resonance

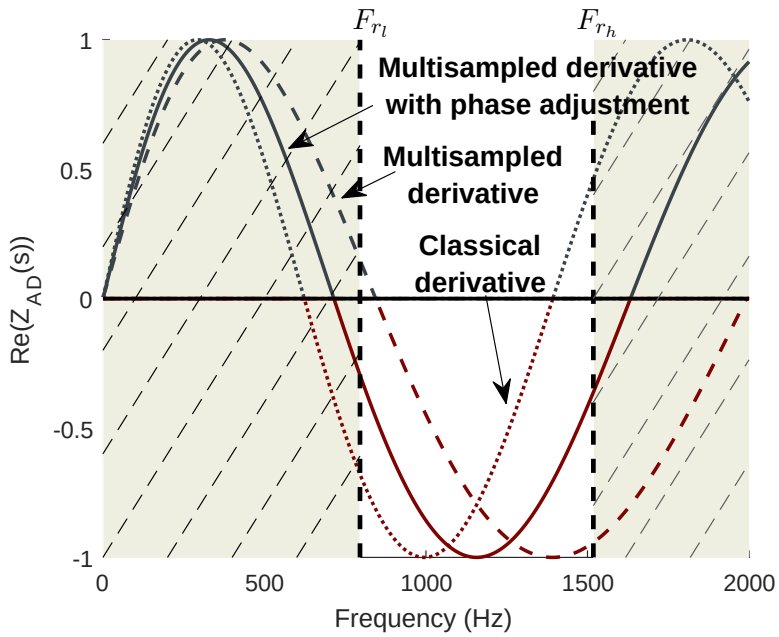


Figure 4.15: Variation of the virtual impedance real part with frequency for the multisampled derivative, the classical derivative and the proposed approach: the multisampled derivative with phase adjustment.

frequency, can be calculated by imposing that, at the central resonance frequency Equation 4.10 has to be equal to π. This equation can be analytically solved to calculate y, obtaining Equation 4.11.

$$y = \frac{1}{\omega_{r_c} T_{s_{DSP}}} \left(\sum_{i=0}^{n_{zb}} atan\left(\frac{\omega_{r_c}}{z_{BPF_i}}\right) - \sum_{i=0}^{n_{pb}} atan\left(\frac{\omega_{r_c}}{p_{BPF_i}}\right) + \right.$$
$$\left. + \sum_{i=0}^{n_{zl}} atan\left(\frac{\omega_{r_c}}{z_{LPAF1_i}}\right) - \sum_{i=0}^{n_{pl}} atan\left(\frac{\omega_{r_c}}{p_{LPAF1_i}}\right) + \pi \right) - 1.5 \qquad (4.11)$$

where n_{zb} and n_{zb} are the number of zeros, z_{BPF_i}, and poles, p_{BPF_i}, of $BPF(s)$ respectively. 1.5 stands for the delay of $D_{conv1}(s)$, and $T_{s_{DSP}}$ is the DSP sampling time. Lastly, n_{zl} is the number of zeros, z_{LPAF1_i}, and n_{pl} is the number of poles, p_{LPAF1_i}, of $LPAF_1$. If a first-order low-pass analog filter is considered, when it is expressed in the SRF, $LPAF_1(s)$ has one zero and two poles.

This delay of y sample times has to be programmed in the DSP, where an integer delay can be easily implemented as z^{-y}. However, in general, y will be

a real number. In this general case, it is decomposed into its integer part, y_i, and its fractional part, y_f, which can be implemented in the DSP by means of a linear interpolation [LAA96], as shown in Equation 4.12.

$$DAD(z) = \left((1 - y_f) + y_f z^{-1}\right) z^{-y_i} \tag{4.12}$$

It can be seen in Figure 4.15, represented for a mr equal to 10, that at the highest resonance frequency the real part of the emulated virtual impedance is equal to 0.4, meaning that there is a margin of 25 degrees before the emulated virtual resistance becomes negative. If this margin becomes small, the damping at the LCL resonant poles is highly reduced, and the system can even become unstable as the virtual resistance turns negative. In this way, the multisampling ratio (mr) of the FPGA to the DSP is a key aspect. As indicated in Figure 4.14, if mr is equal to 4, 8 additional degrees are lost with respect to mr equal to 10, and there is only a margin of 17 degrees until the system becomes unstable. If mr is decreased to 2, 24 additional degrees are lost, reamining only 1 degree until the virtual resistance becomes negative. The damping provided is almost negligible and hence, an important ripple could be expected at the LCL resonant poles for high SCRs. For this reason, the ratio of the multisampled derivative is such an important aspect.

In this approach, the delay has been adjusted for the widest possible range of resonance frequencies. Nevertheless, the delay can be adjusted to optimize the damping action at the LCL resonance frequency, in those applications in which the SCR at the PCC is known, by evaluating Equation 4.11 at the expected resonance frequency. In this way, a pure virtual resistor would be emulated at the resonance frequency, providing optimal damping at the resonant poles. Once the delay of the AD path has been properly adjusted, the selection of the emulated virtual resistor, R_{da_v}, would determine the amplitude of the AD action.

The proper adjustment of the delay guarantees that the phase of the emulated virtual impedance has enough margin before its resistive component changes its sign for any SCR greater than 1. As a result, the emulated virtual resistance does not need to be modified for the different grid impedances.

4.3.4 Selection of the emulated virtual resistor

The last step to tune the CVDAD is the selection of the virtual resistor gain, R_{da_v}, defined as the ratio between L_{conv} and k_{AD} in Equation 4.5. An initial

estimation for R_{da_v} can be found from the expression for the damping of an LC filter with a resistor in parallel with the filter capacitor, Equation 4.13, as this is the equivalent system emulated with the AD strategy. This R_{da_v} would provide the desired damping, ξ, when a pure virtual resistance is emulated, however, by the effects of the delays, this can only be precisely achieved at the central frequency for which the delay has been adjusted.

$$R_{da_v} = \frac{Z_{Cf}}{2\xi} \tag{4.13}$$

where Z_{Cf} is the impedance of the capacitor branch at the central resonance frequency. By calculating the required R_{da_v} to achieve a damping of 0.25 at the central resonance frequency, where Equation 4.13 is valid, a value of 2.75 Ω is obtained. In Fig. 4.16 the evolution of the resonant poles is plotted for several virtual resistors and an SCR of 10, corresponding to the SCR of the grid at which the experimental set-up is connected. This short circuit ratio brings the LCL resonance frequency close to the central resonance frequency, F_{r_c}, so an excellent daming can be expected with the proposed damping strategy. It is observed that the proposed AD is able to stabilize the resonant poles for different virtual resistors, showing robustness faced to variations in this parameter. The greatest damping is achieved for an R_{da_v} close to the initial estimate of 2.75 Ω.

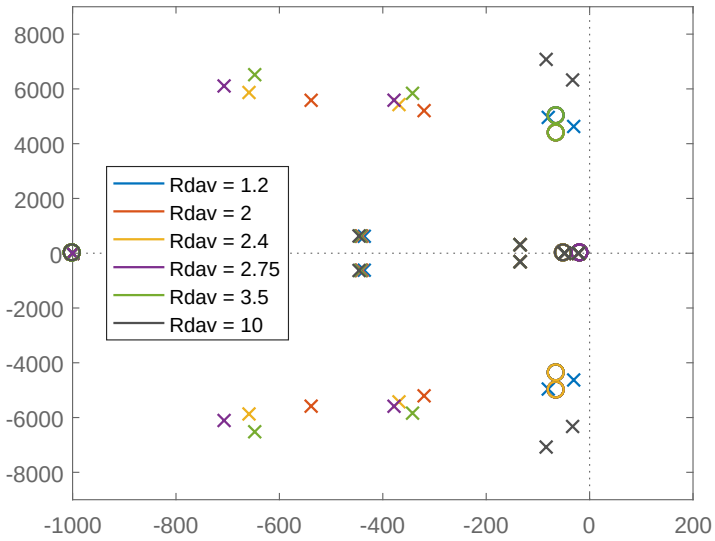


Figure 4.16: Pole placement of the resonant poles for SCR = 10 and different virtual resistors.

4.3.5 Noise rejection analysis

It is common in power converters, to sample all the measured variables synchronously, either with symmetrical sampling (once per switching frequency), or with asymmetrical sampling (twice per switching frequency). In this way, aliasing and noise problems are minimized. In the power converter analyzed in this work, all the measurements are sampled asymmetrically, a common approach in high power converters, because the switching frequency is low, except for the capacitor voltage measurement used in the CVDAD strategy, for which a multisampled derivative is used.

The main source of noise in the measurement of the capacitor voltage is the switching of the power converter. Consequently, the most representative harmonics in the measurement are expected to be located at the switching frequency and its sidebands and all the multiples of the switching frequency and their sidebands. If the multisampled derivative is implemented in an FPGA, the measurement of the capacitor voltage filtered by the LPAF is sampled by the FPGA, and the derivative performed. This derivative will be sampled by the DSP, and the high frequency noise will be translated into low frequency alias at a frequency given by Equation 4.14.

$$F_{alias} = |F_{s_{DSP}} - F_{real}| \tag{4.14}$$

where F_{alias} is the low frequency alias of the real harmonic, with a frequency F_{real}, and where $F_{s_{DSP}}$ is the DSP sampling frequency. The sidebands of the first switching harmonic family appear at ±100 Hz, ±200 Hz... with the asymmetrical update of the switching orders. When sampled by the DSP, these harmonics are seen as alias with a frequency close to the switching frequency and are attenuated by the band-pass filter. The second switching harmonic family sidebands appear at ±50 Hz, ±250 Hz... and are seen by the DSP as alias with a low frequency, which are also attenuated by the bandpass filter previously adjusted. All the switching harmonic families are similarly attenuated and none of the aliases fall within the AD region. If in a given application, the alias of the switching family falls within the AD region, an anti-aliasing filter could be implemented in the FPGA. The experimental set-up, in which the CVDAD strategy is tested, will demonstrate that there are no noise problems that compromise the performance and stability of the CVDAD.

4.4 Simulation Results

In the experimental set-up the grid inductance cannot be modified. For this reason, simulations are performed using *Matlab Simscape Power Systems* in order to validate the proposed AD strategy with delay adjustment. The parameters of the simulation model are the same ones provided in Table 4.1.

According to Figure 4.15, the multisampled derivative without phase adjustment (M) is able to stabilise the resonant poles for high SCRs (high resonance frequencies), while the classical implementation of the derivative (C) will be able to damp the resonance in weak grids (low resonance frequencies). Only the proposed CVDAD strategy that combines the multisampled derivative with the delay adjustment (M+D) is able to stabilise the converter for any SCR.

To verify this behaviour two simulations are performed, in which the AD is switched from the multisampled derivative with phase adjustment, to the classical derivative and later to the multisampled derivative without phase adjustment. Two different SCRs are simulated to verify the stability regions obtained in Figure 4.15: an SCR of 1.5, corresponding to an *LCL* resonance frequency of 860 Hz and an SCR of 70, corresponding to a resonance frequency of 1400 Hz.

If an SCR of 1.5 is considered, both the multisampled with delay adjustment and the classical AD strategy can effectively damp the resonance, as shown in Figure 4.17. In contrast, the multisampled strategy without phase adjustment leads the system to instability, and a component at the resonance frequency rapidly grows. As expected from Figure 4.15, with the multisampled approach and an SCR of 1.5, the sign of the emulated virtual resistor changes and a destabilizing action is applied. In contrast, in a strong grid with an SCR of 70, both multisampled strategies, with and without phase adjustment, can damp the system. However, with the classical derivative the system is unstable as the sign of the emulated virtual resistance has changed, confirming again the results in Figure 4.15. In this way, the proposed AD is the only strategy able to stabilize the system for any grid considered.

The reduction of the multsampling ratio, *mr*, introduces a phase displacement that cannot be ignored for high SCRs. In Section 3.3 this issue was analyzed based on the theoretical phase displacement obtained in Section 3.2. To validate this theoretical analysis, a simulation has been performed for a SCR of 300, transiently modifying *mr* from 10 to 4 and later to 2, the same *mr* that have been theoretically analyzed. With the original *mr* of 10, the system is perfectly stable obtaining a negligible component at

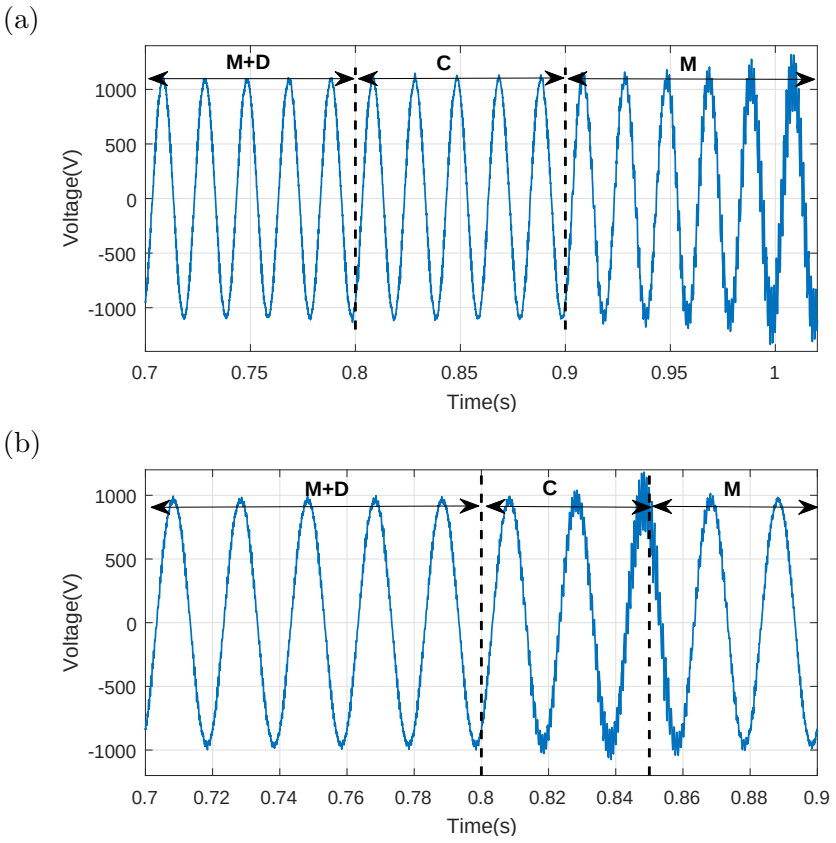


Figure 4.17: Capacitor line voltage evolution for the three AD strategies and two SCRs: 1.5 (a) and 70 (b).

the *LCL* resonance frequency, as shown in Figure 4.18. If *mr* is reduced to 4, the system becomes closer to instability, as the margin in the emulated virtual resistance is reduced to 17 degrees. The damping of the resonant poles is diminished and an harmonic component at this frequency appears. With a multisampling ratio of only 2, the margin in the phase of the emulated virtual resistor is only 1 degree and the system is on the verge of instability. An unacceptable harmonic component at the *LCL* resonant poles frequency is obtained, even though the system is still stable.

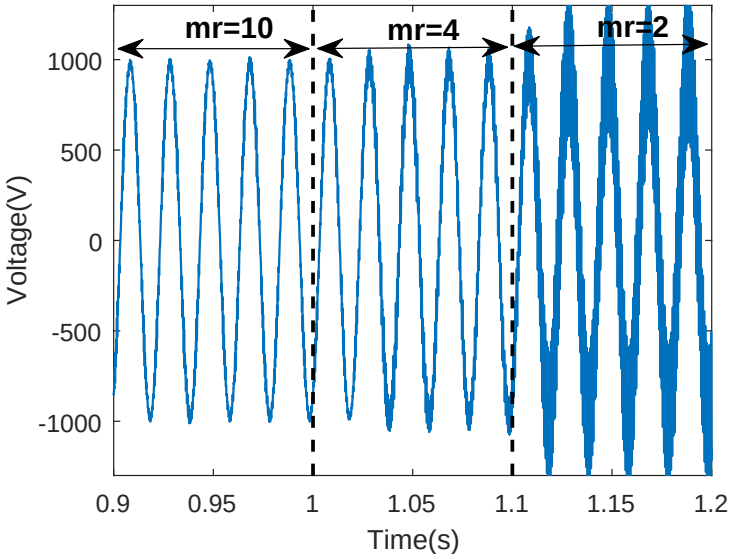


Figure 4.18: Capacitor line voltage for a SCR of 300 and three different ratios (mr) of the FPGA sampling time to the DSP sampling time.

4.5 Experimental Results

4.5.1 Description of the experimental set-up

The validity of the approach is tested on the 500 kW back-to-back power converter shown in Figure 4.19, designed for a DFIG wind turbine. Only the grid side converter is used, because the purpose of the test is to validate the robust active damping strategy presented.

The system parameters are detailed in Table 4.1, and it is connected to a grid with an SCR of 10. The DC bus voltage is 1100 V, and the passive resistors, normally used to damp the filter resonance are bypassed. The DSP sampling frequency is set to 5.6 kHz with a converter switching frequency of 2.8 kHz (asymmetrical sampling). An FPGA is used for filtering purposes, running 10 times faster than the DSP and synchronized with it. The AD strategy is implemented following the steps in Section 4.3. The derivative is implemented in the FPGA and passed to the DSP, where the bandpass digital filter and the adjustment of the delay are applied, emulating a resistor of 2.75 Ω.

Figure 4.19: Equipment used validate the AD strategy.

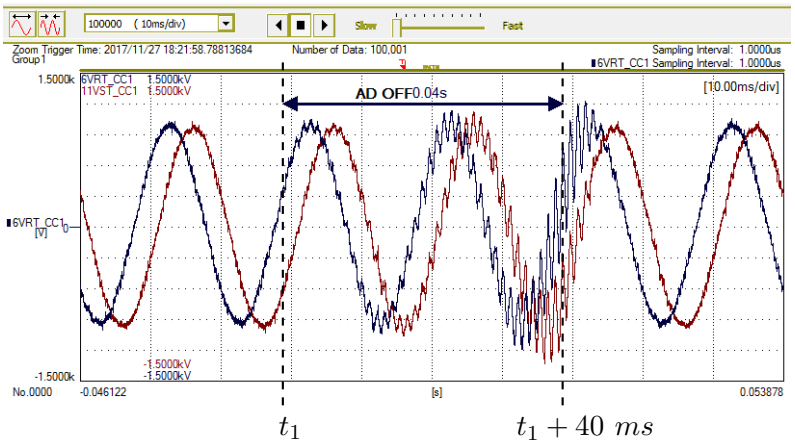
4.5.2 Validation of the stability analysis

According to the stability analysis already conducted in Section 4.1 and Section 4.3, the system without AD is unstable, while if the proposed AD is included it would become stable.

This behavior is validated in the experimental set-up by transiently disabling the AD action. In Figure 4.20 the capacitor line voltages and the converter side current are shown as registered by the Yokogawa DL850E. Initially, the proposed AD is activated and the system is stable, but as soon as it is deactivated at instant t_1, the system becomes unstable and a component at the LCL resonance frequency grows exponentially, verifying the behavior predicted. When the AD is activated again after 40 ms, it becomes stable and is able to recover quickly from instability.

The current waveform is distorted, due to the low current injected by the power converter, less than a 5%. With this low fundamental current, the low frequency harmonics, mainly introduced by the dead times, and the high frequency harmonics created by the switching of the power converter have a strong influence in the waveform. Nevertheless, even under such a distorted situation, the AD is able to damp the resonance

(a)



(b)

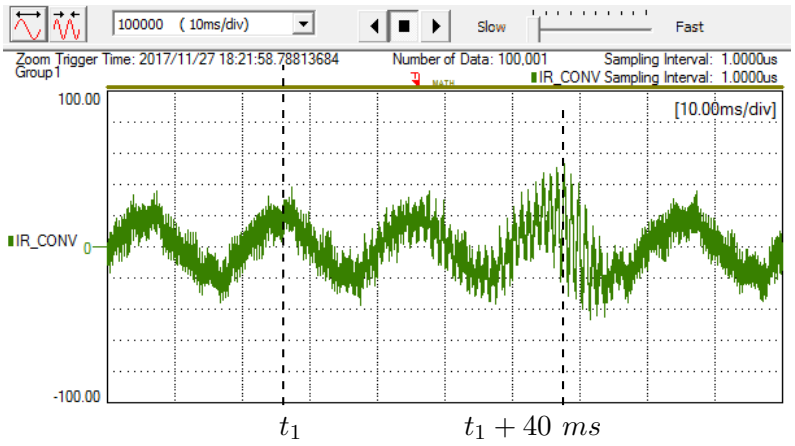


Figure 4.20: Capacitor line voltage (a) and converter side current (b) evolution when the AD strategy is deactivated for 40 ms.

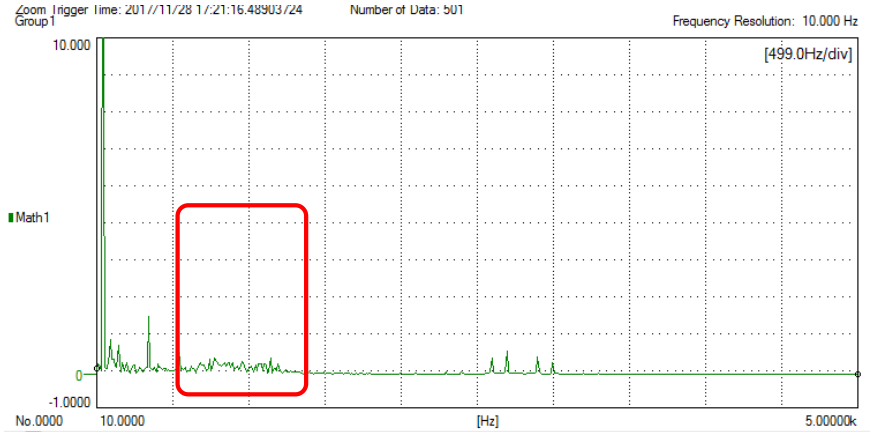
4.5.3 Sensitivity analysis to the virtual impedance adjustment

The accurate model of the power converter and control in the SRF developed in Chapter 2, with the detailed analysis and adjustment of the delay performed in Section 4.3, allow to precisely adjust the CVDAD to guarantee the stability of the power converter at the *LCL* resonance frequency, for different grid inductances. The optimal adjustment of both, the emulated virtual resistor and the delay, is demonstrated by deviating these values from the optimal ones and verifying the CVDAD performance.

4.5.3.1 Variations in the emulated virtual resistor

With the phase of the emulated virtual impedance properly adjusted at the central resonance frequency, the gain of the emulated virtual impedance is modified. In Figure 4.16 the evolution of the resonant poles is plotted for several emulated virtual resistors. From this figure, it can be concluded that the greatest damping in the resonant poles is obtained for a virtual resistor close to 2.75 Ω. It can also be seen that for the lowest and highest resistor values, 1.2 and 10 Ω, the system is stable, but the resonant poles are poorly damped and they are close to instability. According to the stability analysis,

(a)



(b)

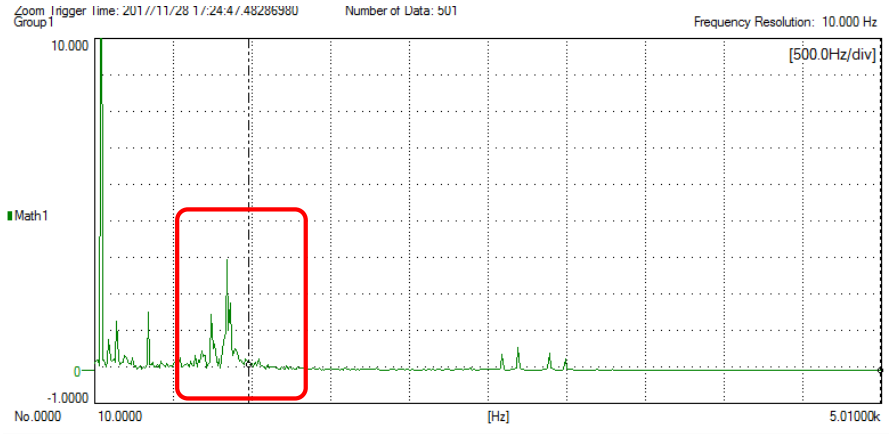


Figure 4.21: Grid current harmonic content with the AD strategy emulating a virtual resistor of 2.75 Ω (a) and a virtual resistor of 10 Ω (b).

the performance of the CVDAD should be highly deteriorated if these two virtual resistors are emulated. In this section, this behavior is verified.

The grid current harmonic content with the AD strategy activated is shown in Figure 4.21. It can be seen that, when a virtual resistor equal to 2.75 Ω is emulated, no significant harmonics at the *LCL* resonance frequency appear, meaning that the resonant poles are properly damped, as shown in Figure 4.21 (a). Moreover, it can be seen that the grid current has low amplitude harmonics, proving that the AD strategy is robust against noise and aliasing. Nevertheless, if a virtual resistance of 10 Ω is emulated, the resonant poles have a poor damping, and consequently significant harmonics at the *LCL* resonance frequency appear in the grid current, as demonstrated in Figure 4.21 (b). These results perfectly agree with the zero pole map shown in Figure 4.16.

To further analyze the effects of the AD in the converter variables, the capacitor line voltage is plotted in Figure 4.22 for the same virtual resistors as in Figure 4.21. With the optimal virtual resistor emulated, the capacitor line voltage does not present a component at the resonance frequency and the waveform is clean. In contrast, if a virtual resistor of 10 Ω is emulated, the voltage waveform is distorted, with an important component at the resonance frequency. If the emulated virtual resistor is equal to 1.2 Ω, and the resulting current harmonic content plotted in Figure 4.23, similar results are obtained than with the virtual resistor equal to 10 Ω. The system is close to instability and the current harmonic content is distorted at the *LCL* resonance frequency.

In this way it can be concluded that the detailed modeling approach allows to precisely adjust the emulated virtual resistor of the AD strategy.

4.5.3.2 Variations in the adjustment of the delay

The same sensitivity analysis can be performed for the delay adjusted in the CVDAD feedback path. If the delay is deviated from the one adjusted in Section 4.3, the performance is deteriorated and the system, as expected, can even become unstable.

This behavior can be seen in Figure 4.24 (a) and (b), where the delay is adjusted to introduce a deviation of -60 μs to the optimal delay calculated according to Equation 4.11. The resonance frequency of the *LCL* filter, considering the grid inductance of the experimental set-up, is 1 kHz. At this resonance frequency, the emulated virtual impedance, with the delay optimally tuned, is almost a virtual resistor, as shown in Figure 4.24 (a). However, if the delay is deviated from the optimal value, by -60 μs, the

emulated resistance is reduced, and some damping is lost. The lower damping at the resonant poles has a direct effect in the grid current harmonic content, Figure 4.24 (b), where harmonics at the LCL resonance frequency appear. If a greater deviation is introduced, these harmonics are increased, and eventually, the system would become unstable.

It can be concluded that the existing delays have been properly modeled and the proposed adjustment of the delay correctly derived, as the results in the experimental set-up, support the theoretical analysis.

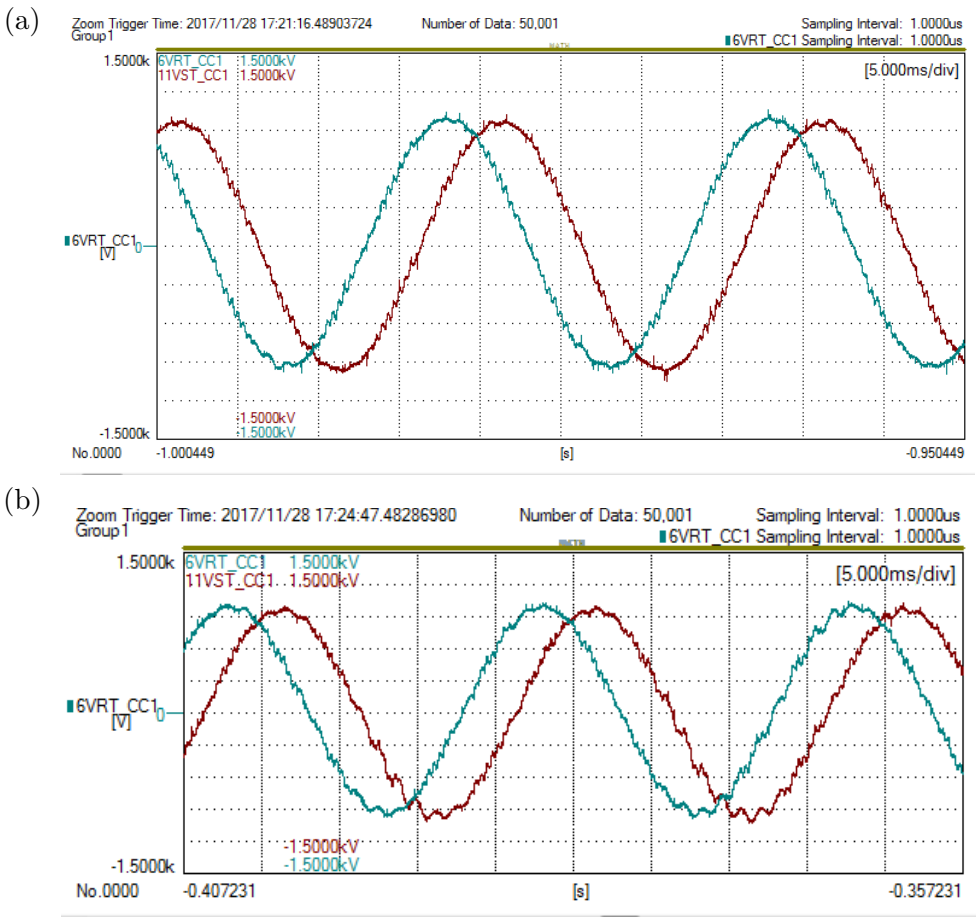


Figure 4.22: Capacitor line voltage waveforms with the AD strategy emulating a virtual resistor of 2.75 Ω (a) and a virtual resistor of 10 Ω (b).

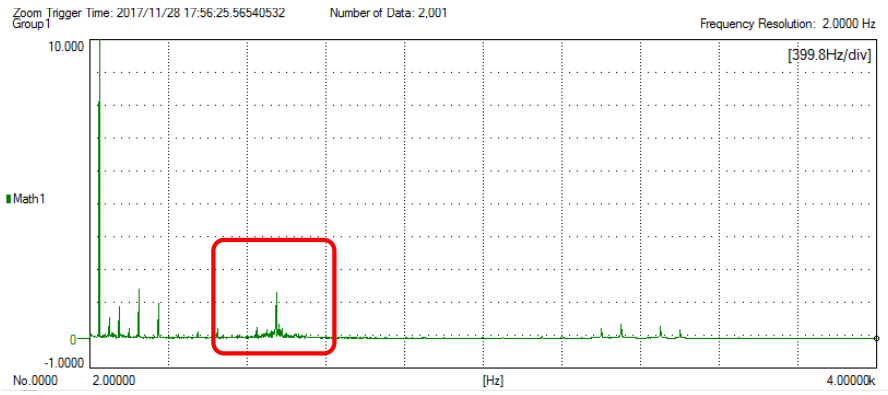


Figure 4.23: Grid current harmonic content with the AD strategy emulating a virtual resistor of 1.2 Ω.

4.6 Application of the adjustment of the delay to the capacitor current AD strategy

The capacitor current proportional feedback is one of the most extended AD solutions (CCAD), [DAN10, PAR14, PAN14, WAN15, SAÏ18] even though additional sensors are required. This strategy is equivalent to the CVDAD. The capacitor current is given by:

$$I_{C\ dq}(s) = \begin{bmatrix} Cs & -C\omega_0 \\ C\omega_0 & Cs \end{bmatrix} V_{C\ dq}(s) \tag{4.15}$$

so it already includes the derivative term of the capacitor voltage. The block diagram in Figure 4.10 can be reorganized to include the previous expression obtaining the CCAD implementation in Figure 4.25, where $k_{AD\ C}$ is the constant used to adjust the AD action.

The block diagram presented in Figure 4.25 is analogous to the one presented for the CVDAD, so both strategies can be adjusted following the same design procedure for H_{AD} proposed in Subsection 4.3.3 with $k_{AD\ C}$ equal to:

$$k_{AD\ C} = \frac{k_{AD}}{C} \tag{4.16}$$

The capacitor-current AD does not require a derivative, so a multisampled approach is not needed. However, it does need two current sensors in the capacitor branches. In the power converter used in the experimental set-up, these current sensors have been included in order to be able to test this AD strategy. Replicating the design procedure developed for the CVDAD, which

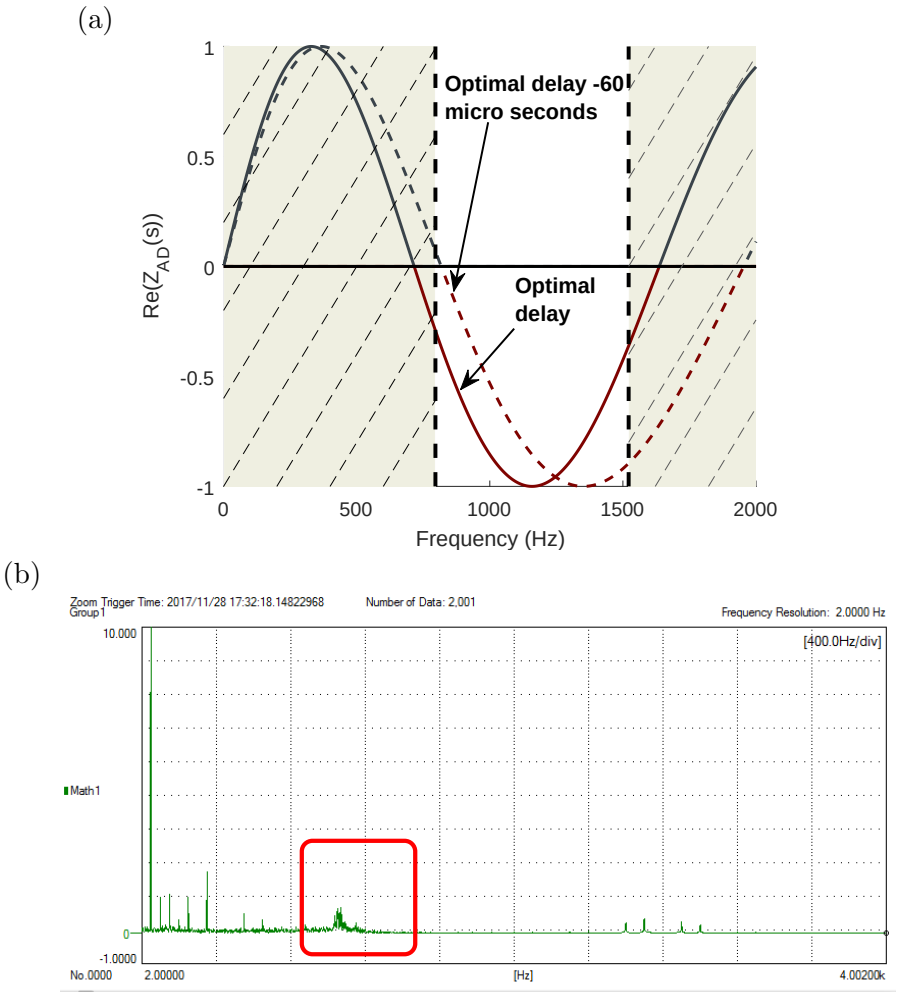


Figure 4.24: Effect of the delays on the resistive component of the virtual impedance (a) and grid current harmonic content (b) with the AD strategy introducing an additional delay in the AD feedback path equal to the optimal -60 μs.

has been already validated, this strategy is adjusted, and the experimental results represented in Figure 4.26. In Figure 4.26 (a) the capacitor line voltages are represented, while in Figure 4.26 (b) the grid current harmonic content can be seen. It can be seen that the current control loop is stable, as for the CVDAD, with similar performance if compared with Figure 4.21 (a).

4.7 Efficiency improvement

The AD strategy presented in this thesis allows to eliminate the damping resistors, normally included in series with the filter capacitor in order to damp the poles at the *LCL* resonance frequency. In this way, the losses in this component can be avoided, consequently increasing the overall converter efficiency.

To determine the efficiency improvement when the damping resistor is eliminated, simulations for the power converter under study are performed without the AD strategy. The *LCL* resonant poles are stabilize with a passive damping resistor in series with the filter capacitor. Several SCR are simulated, calculating in each case the required damping resistor to provide a damping of 0.05 at the resonant poles. This damping is low, but sufficient to avoid oscillations and poor harmonic content. The harmonics introduced by the power converter are small in this range of frequencies, so a greater damping is not required. The power losses in this component, obtained from the simulations, are summarized in Table 4.2.

In this table, the grid SCR at which the power converter is connected in each simulation and the required resistor to damp the resonant poles can

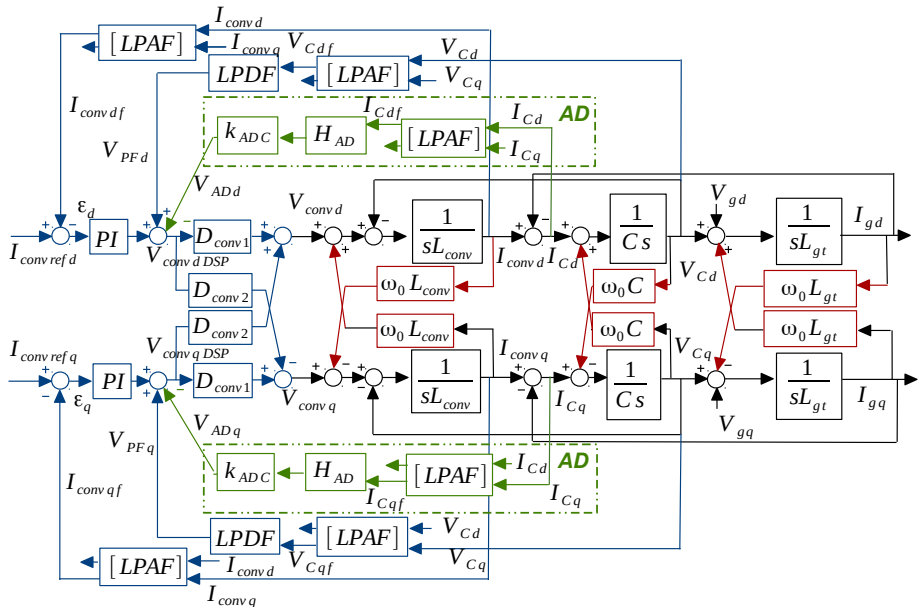
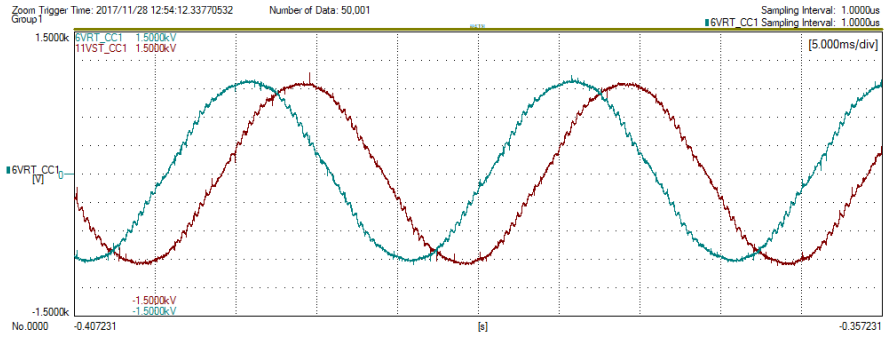


Figure 4.25: Block diagram representation of the current control loop including the CCAD.

(a)



(b)

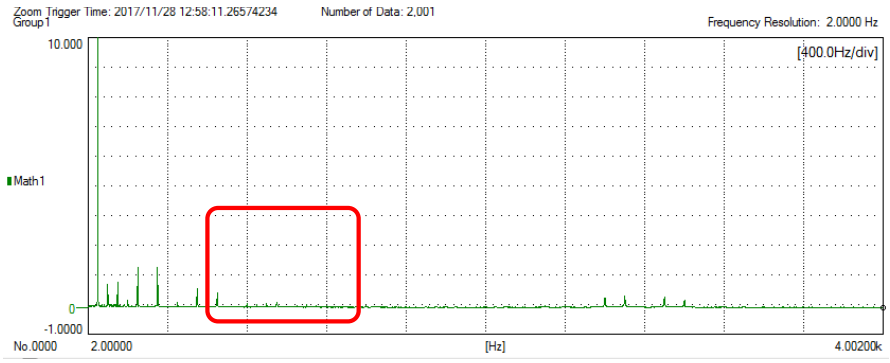


Figure 4.26: Performance of the capacitor-current AD: capacitor line voltages (a) and grid current harmonic content (b).

Table 4.2: Power losses in the *LCL* damping resistor for different SCRs.

SCR	R_d required (Ω)	Power losses (W)	Efficiency gain (%)
1	0.45	1200	0.24
2.5	0.4	1050	0.21
5	0.3	840	0.17
10	0.25	630	0.13
20	0.2	530	0.11
40	0.15	420	0.08
80	0.13	380	0.08
160	0.12	365	0.07

be found, along with the total power losses in steady state in the damping resistors and its percentage, normalized with respect to the power converter rated power. This last column is labeled as efficiency gain because it represents the improvement in the efficiency that can be obtained for the power converter under study if the damping resistors are eliminated. Even though the efficiency

gain is not impressive, it comes at no cost, just by modifying the DSP control.

4.8 Conclusion

In this chapter a robust active damping strategy based on the capacitor voltage derivative is proposed. With the approach presented, the AD stability region is adapted to the optimized design of a given LCL filter and all the possible PCCs where the converter can be connected, instead of imposing additional constraints on the LCL design procedure. This goal is achieved by means of an adjustable delay, presenting a systematic procedure to tune this delay in the active damping feedback path by means of an analytical expression that requires reduced information on the control loop. The design procedure and the analytical expression provided to adjust the delay are also applicable to the capacitor current proportional feedback active damping. To overcome the limitations of the derivative close to the control Nyquist frequency, a multisampled derivative is implemented, offering greater robustness against variations in the resonance frequency, as a result of a lower delay. The detailed model developed for the LCL filter and the converter current control loop allows to precisely adjust the active damping strategy. The solution proposed is costless, does not increase the power losses, and is based on the measurements available in grid-connected power converters and the existing digital systems to implement the multisampled derivative. It allows to eliminate the passive resistors, simplifying the filter and gaining up to a 0.24% in the efficiency. The performance and robustness of the proposed AD have been tested through experimental and simulation results.

Chapter 5

Discontinuous PWM for the efficiency improvement of the back-to-back conversion stage

5.1 Motivation

The AC to AC conversion required in WECS has been successfully implemented with the back-to-back conversion structure. This structure was presented in Chapter 2 and reproduced for convenience in Figure 5.1 It is formed by two two-level three-phase power converters, denoted by MSC and GSC along this thesis. The modulation implemented in GSC and MSC influences characteristics as important in a power converter as the grid code compliance, in terms of grid current harmonic content, the power conversion efficiency and the common-mode (CM) and phase-to-ground (PG) voltages imposed to the electrical generator. CM and PG voltages have to be limited in WECS in order to avoid premature failures in bearings and winding insulation [ALE12]. The importance of the modulation on these characteristics motivates the analysis performed in this chapter. The implementation of new PWM techniques in B2B power converters is proposed, which improves the system efficiency without penalizing the other characteristics.

The theoretical background required to analyze the influence of the modulation in terms of harmonic content, efficiency and common-mode and phase-to-ground voltages is determined before the development of the proposed modulation strategies. An analysis of the state-of-the-art modulations for two-level three-phase power converters is also included.

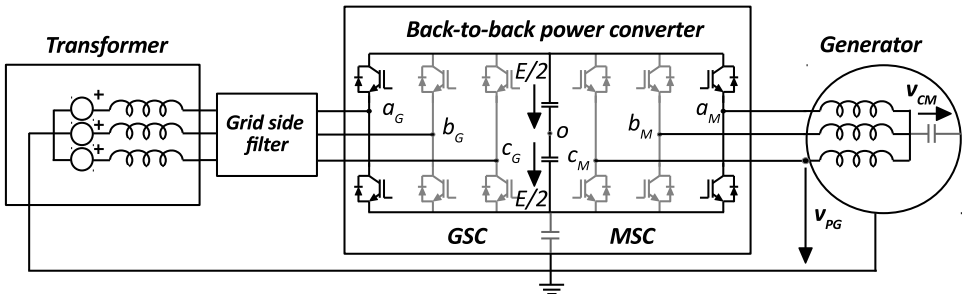


Figure 5.1: Typical B2B structure used in WECS and electrical drives.

5.2 Theoretical approach to analyze the influence of the modulation on the B2B performance

5.2.1 Modulation of a VSC

Before analyzing the influence of the modulation of GSC and MSC on the performance of the B2B conversion structures, the modulation of a single VSC is presented, to later extend it to the B2B power converter.

The voltage imposed in any converter leg, with respect to the DC-bus mid point, can be given by the product of the switching function F and half of the DC-bus voltage:

$$v_{G_a} = F_{G_a}\frac{E}{2} \tag{5.1}$$

where the subindex G stands for the grid side converter and a for the phase. Similarly, the voltages in phases b and c can be given by the product of the two switching functions, F_{G_b} and F_{G_c}, and half of the DC-bus voltage.

As the switching function can have two values, -1 and 1, for a three-phase two-level VSC there are eight possible switching states. In Section 2.2 the dependency of the common-mode and differential-mode voltages on the switching states of each leg have been calculated, which are given by:

$$v_{cm_o} = \frac{E}{6}(F_{G_a} + F_{G_b} + F_{G_c}) \tag{5.2}$$

$$v_{dm_{Ga}} = \frac{E}{6}(2F_{G_a} - F_{G_b} - F_{G_c}) \tag{5.3}$$

$$v_{dm_{Gb}} = \frac{E}{6}(2F_{G_b} - F_{G_a} - F_{G_c}) \tag{5.4}$$

$$v_{dm_{Gc}} = \frac{E}{6}(2F_{G_c} - F_{G_a} - F_{G_b}) \tag{5.5}$$

The eight possible switching states of a three-phase two-level VSC are summarized in Table 5.1, along with the differential phase voltages and common-mode voltages. In this table, in the last column, a vector number ($v_0 - v_7$) is assigned to each of the eight possible switching states of the VSC.

Table 5.1: Possible switching states of a tree-phase two-level VSC.

F_{G_a}	F_{G_b}	F_{G_c}	$v_{dm_{Ga}}$	$v_{dm_{Gb}}$	$v_{dm_{Gc}}$	v_{cm_o}	Vector
-1	-1	-1	0	0	0	-E/2	v_0
-1	-1	1	-E/3	-E/3	2E/3	-E/6	v_5
-1	1	-1	-E/3	2E/3	-E/3	-E/6	v_3
-1	1	1	-2E/3	E/3	E/3	E/6	v_4
1	-1	-1	2E/3	-E/3	-E/3	-E/6	v_1
1	-1	1	E/3	-2E/3	E/3	E/6	v_6
1	1	-1	E/3	E/3	-2E/3	E/6	v_2
1	1	1	0	0	0	E/2	v_7

The vectors in Table 5.1 can be classified as zero vectors: v_0 and v_7 and differential vectors: $v_1 - v_6$. The positive zero vector has a common mode of +E/2, while the negative zero vector has a common mode of -E/2. The differential vectors can be classified depending on their common-mode voltage: the odd vectors (v_1, v_3 and v_5) have a common mode of -E/6, while the even vectors (v_2, v_4 and v_6) have a common mode of E/6.

These vectors can be projected in the $\alpha\beta$ reference frame by means of the Clarke transformation, given in Equation 2.15, obtaining the well-known space vector hexagon of a two level three-phase power converter, represented in Figure 5.2. The vectors with a negative common-mode voltage have been represented in red, while the ones with positive common-mode are represented in blue. The hexagon is divided by these vectors into six subsectors.

To determine the value of the switching function of each VSC leg, and consequently, the differential mode and common-mode voltages, there are two main approaches: scalar modulation and space vector modulation. In the scalar modulation, the reference voltage generated in the *dq* axis is transformed to the three-phase voltages by means of the inverse [T] matrix, obtained in Equation 2.21. From the intersection of these voltages with a carrier wave, the switching states are determined. In contrast, in the space vector pulse width

modulation (SVPWM) [VAN88], the vectors that have to be applied in each switching period are calculated, along with their duty cycles, directly from the reference vector expressed in the $\alpha\beta$ coordinate system. The SVPWM is suitable for digitally controlled power converters, as it provides a more intuitive approach to program and modify the modulation, if it is required. In this thesis, the space vector implementation of the modulation is studied.

The combination of the possible switching states to synthesize the average voltages calculated by the controller loop, create the existing different modulation strategies. The conventional approach to modulate the desired reference vector is using the two adjacent differential vectors, which define the boundaries of the sector in which the reference vector is located, during the required time. By using this strategy, the error with the reference vector is minimized, which reduces the current ripple. The rest of the switching period is distributed between other vectors that do not contribute to the net differential voltage but allow to obtain the desired magnitude of the average voltage. The vector used during the exceeding time of the switching period distinguishes the modulations among them, as it will be explained in Section 5.3, where the state-of-the-art modulations are discussed. If the two adjacent vectors are used to synthesize the reference voltage, their duty cycles are calculated by means of the two following equations:

$$d_C = \frac{\sqrt{3}}{2} m sin(N\pi/3 - \delta) \tag{5.6}$$

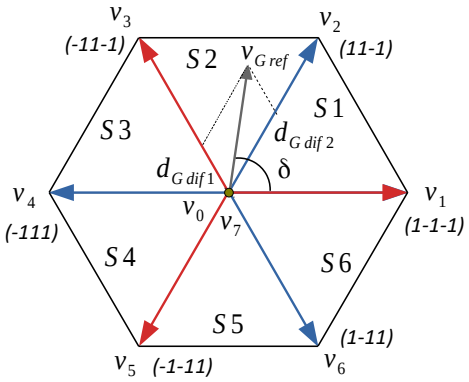


Figure 5.2: Space vector diagram with the eight possible switching states of a two-level three-phase power converter and the representation of the reference vectors of the grid side converter, v_{Gref}.

$$d_A = \frac{\sqrt{3}}{2} m sin(\delta - (N-1)\pi/3) \tag{5.7}$$

where d_C is the closest differential vector to $v_{G_{ref}}$ in the clockwise direction, while d_A is the closest one in the anticlockwise direction. m is the modulation index, defined as the ratio of the voltage reference vector and E/2, which is restricted to vary within the linear region, from 0 to $2\sqrt{3}/3$. Lastly, N is the sector where the reference vector is located and δ is the angle of the reference vector.

The most extended modulation is the classical SVPWM7, described here to introduce the implementation of the space vector modulations. It uses the two adjacent vectors to reproduce the reference vector, while the rest of the switching period is divided equally between both zero vectors. The vectors are always applied in a sequence that guarantees that only one converter leg is switched in any vector transition. Each switching period starts with the negative zero vector, v_0, followed by the first differential vector, v_{dif1}, the adjacent red vector to v_{ref} in Figure 5.2. v_{dif1} is followed by v_{dif2}, the adjacent blue vector, and finally, the positive zero vector, v_7:

$$v_0 \rightarrow v_{dif1} \rightarrow v_{dif2} \rightarrow v_7 \rightarrow v_{dif2} \rightarrow v_{dif1} \rightarrow v_0$$

The duty cycle of each vector is denoted by d: d_{z0} is the duty cycle of v_0, d_{dif1} is the duty cycle of v_{dif1} and d_{dif2} the one of v_{dif2}. d_{dif1} and d_{dif2} are calculated according to Equation 5.6 and Equation 5.7. The application instants of these vectors can be obtained from the comparison of three auxiliary duty cycles: low (d_L), medium (d_M), and high (d_M), with a triangular carrier wave, as shown in Figure 5.3. The auxiliary d_L, d_M and d_H are computed according to Equations 5.8 to 5.10.

$$d_L = d_{z0} \tag{5.8}$$

$$d_M = d_{z0} + d_{dif1} \tag{5.9}$$

$$d_H = d_{z0} + d_{dif1} + d_{dif2} \tag{5.10}$$

where d_{z0} is obtained for the classical SVPWM7 as:

$$d_{z0} = \frac{1 - d_{dif1} - d_{dif2}}{2} \tag{5.11}$$

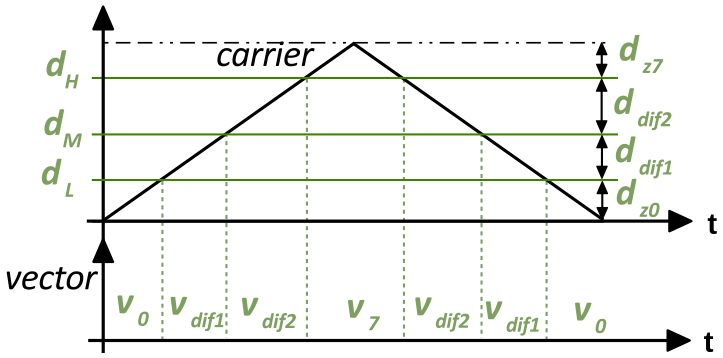


Figure 5.3: Space vector implementation of the modulation.

As a consequence, d_{z7} is equal to d_{z0}.

In this way, the modulations of both GSC and MSC of the back-to-back power converter can be implemented straightforward. The modulation of GSC will strongly influence the grid code compliance, while the efficiency and the CM and PG voltages are determined by the modulation of both power converters. Before introducing the state-of-the-art modulations, the impact of the modulation on each characteristic is covered in the following.

5.2.2 Influence of the modulation on the grid code compliance

The grid codes [BDE08, IEE08] impose limitations on the grid current harmonic content. The harmonics in the grid current are affected by the *LCL* filter used at the output of GSC, but also by the modulation implemented. The influence of the modulation on the grid current harmonic content can be analyzed from the the common-mode and differential-mode model of the B2B power converter. This model is shown in Figure 5.4, including the *LCL* filter in GSC and the *dv/dt* filter in MSC.

Under balanced circumstances, the generator voltages add up to zero, and, by definition, the differential voltages of MSC as well. If the impedances are also balanced all the elements from O'_M to N_m do not contribute to the current circulating in the grid side converter. The common-mode voltage sources, $v_{G\ cm}$ and $v_{M\ cm}$, do not contribute to the differential current in GSC. They only contribute to the common-mode current, which is small, as it has to circulate through parasitic capacitances. In addition, this current is derived to the ground through the earthing connection of the low voltage side neutral point. In this way, only the difference between the differential voltages imposed by the converter and the grid voltage, contribute to the grid current harmonic

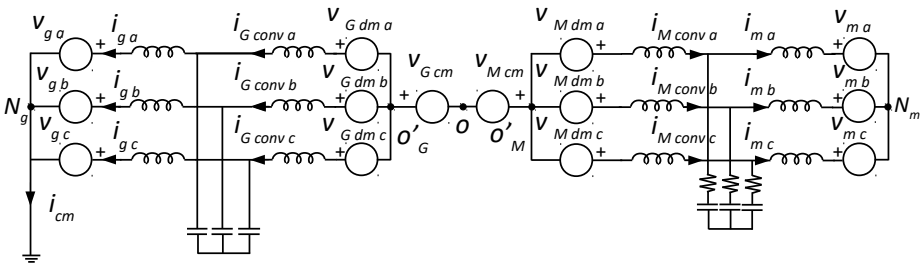


Figure 5.4: Common-mode and differential-mode decomposition of the B2B conversion structure.

content.

If the differential voltage harmonics introduced by the grid side converter are minimized, the required filter to meet the grid codes can be reduced. It is worth to note that the distribution of the zero vector also affects the grid current harmonic content. When a zero vector is modulated, $V_{G\ dm\ abc}$ is set to zero, but the grid still imposes a voltage on the filter components, contributing to the ripple of the grid current. When in Section 5.3 the state-of-the-art modulations are presented, the differential voltage harmonic content would be compared for the different modulation strategies.

5.2.3 Influence of the modulation on the efficiency

The switching sequence is normally selected so that only a leg of the VSC converter switches at any vector transition in the SVPWM7. With this modulation, the B2B structure has 12 commutations per switching period.

Other modulations increase the efficiency by reducing the number of vectors used in each switching period, eliminating one of the zero vectors or using only differential vectors. The modulations that use only one of the zero vectors are called discontinuous space vector pulse-width modulations (DSVPWM). This name comes from the discontinuous nature of the resulting modulating waves when a single zero vetor is used. In this cases, the total number of commutations per switching period are reduced. The existing alternatives to increase the efficiency in a power converter through the modification of the modulation are presented in Section 5.3.

5.2.4 Influence of the modulation on the CM voltage

From Figure 5.4, it can be deduced that if the filter impedances are balanced, the voltage between N_m and N_g depends only on the common-mode voltage sources $v_{G\ cm}$ and $v_{M\ cm}$. By definition, the differential voltages add-up to zero, so the common-mode mode can be simplified to the one given by Figure 5.5.

In this model $L_{G\ conv\ l}$ is the grid side converter leakage inductance and $L_{M\ conv\ l}$ is the machine side converter leakage inductance, if three-phase coupled inductors are used in both cases. L_m is the inductance offered by the machine. The common-mode voltage, v_{CM} in Figure 5.5, is given by the difference of the common-mode voltages of GSC and MSC, Equation 5.12, as the transformer secondary neutral point is connected to ground [IEE07].

$$v_{CM} = \frac{(v_{M_{ao}} + v_{M_{bo}} + v_{M_{co}})}{3} - \frac{(v_{G_{ao}} + v_{G_{bo}} + v_{G_{co}})}{3} \tag{5.12}$$

This equation can be rewritten in terms of the switching functions; F_{M_a}, F_{M_b} and F_{M_c} for MSC and F_{G_a}, F_{G_b} and F_{G_c} for GSC. By expressing the phase voltages in Equation 5.12, in terms of the switching functions, Equation 5.13 is obtained.

$$v_{CM} = \frac{E}{6}\Big((F_{M_a} + F_{M_b} + F_{M_c}) - (F_{G_a} + F_{G_a} + F_{G_c})\Big) \tag{5.13}$$

In this way, when opposite zero vectors coexist in GSC and MSC, v_{CM} reaches ±E, which are the worst possible cases. The second highest voltages occur when a zero vector matches a differential vector with opposite sign common-mode voltage; in this case v_{CM} would be equal to ±2E/3. When two differential vectors, with opposite common-mode coexist, v_{CM} is equal to ±E/3, while it becomes 0 when two vectors with the same common-mode are modulated simultaneously.

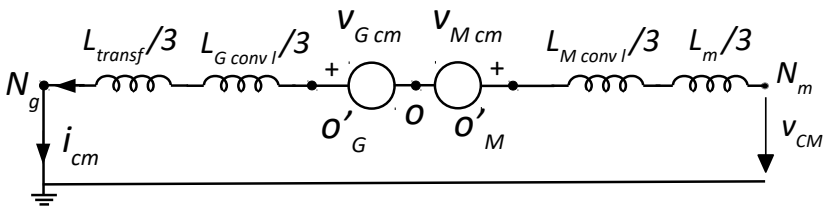


Figure 5.5: Common-mode model of the B2B conversion structure.

Limiting the common-mode voltages is specially important in doubly-fed induction generators (DFIG). In this systems, the common-mode voltage imposed by the power converter rises the shaft voltage with respect to ground [ERD96, CHE96]. This shaft is not directly connected to ground, but the bearings and their lubrication oil form a capacitive path. If the shaft voltage becomes greater than the oil dielectric breakdown voltage, currents will flow through the bearings. This currents deteriorate the bearings, becoming the major cause of failure in DFIG turbines [ALE12]. In full converter topologies used in WECS, there are also capacitive couplings, but as the power converter is connected to the stator, the common-mode voltage is distributed between the parasitic capacitance between the stator and rotor, which is smaller than the one between the rotor, the bearings and the case, and consequently, the first one withstands the majority of the common-mode voltage.

5.2.5 Influence of the modulation on the PG voltages

The phase-to-ground voltage in the generator terminals, can also be obtained from Figure 5.4. By simplifying the grid-side differential voltage sources that do not contribute to the generator phase-to-ground voltages, Figure 5.6 is obtained.

The phase-to-ground voltage in the generator phase i, v_{PG_i}, depends on the common-mode voltage introduced by GSC and the sum of the common-mode voltage in MSC plus the differential voltage in each phase. By definition, $v_{M\ cm} + v_{M\ dm\ a}$ is equal to $v_{M_{ao}}$ and similarly in the other two phases. Consequently, the phase-to-ground voltages in phase i, are given, in

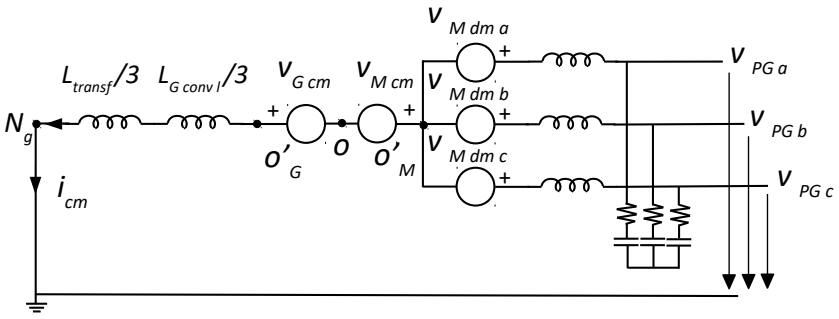


Figure 5.6: Phase-to-ground voltages in the generator terminals.

steady state, by Equation 5.14.

$$v_{PG_i} = v_{i_{Mo}} - \frac{(v_{G_{ao}} + v_{G_{bo}} + v_{G_{co}})}{3} \tag{5.14}$$

If this equation is rewritten in terms of the switching functions, it can be expressed as in Equation 5.15.

$$v_{PG_i} = \frac{E}{2}\left(F_{M_i} - \frac{(F_{G_a} + F_{G_b} + F_{G_c})}{3}\right) \tag{5.15}$$

The PG voltage in phase i, v_{PG_i}, is equal to ±E when a zero vector of GSC coexist with a voltage in the converter leg i of MSC with opposite sign. It is equal to ±2E/3 when the leg voltage in MSC coexist with a differential vector of opposite common-mode in GSC. It is ±E/3 if the leg voltage in MSC matches a differential vector in GSC with the same common-mode sign. And finally, v_{PG_i} is 0 when the leg voltage i in MSC matches a zero vector with the same CM sign.

In both, full-converter and DFIG topologies, the phase-to-ground voltages have to be limited to avoid premature failures in the winding insulation. The first coils of the winding have to withstand greater voltage levels, originated by the transmission of the electromagnetic wave through the cable after each commutation of the power converter. If the maximum step in the phase-to-ground voltage is reduced, the maximum peak voltage is also reduced.

5.3 State-of-the-art modulation strategies

Once the influence of the modulation on the grid code compliance, the efficiency, the common-mode voltage and the phase-to-ground voltages have been characterized, an analysis of the state-of-the-art modulation strategies is performed in this section. The impact of each modulation on these characteristics is highlighted throughout this section.

As mentioned previously, the most extended modulation technique for a two-level three-phase power converter is the SVPWM7 [VAN88]. This modulation presents the best characteristics from the differential voltage harmonics point of view [HAV99], having 6 commutations per switching period. If the SVPWM7 is used on both GSC and MSC with synchronized switching carriers, the CM voltages, v_{CM}, and PG voltages, v_{PG}, are limited to ±2E/3 [BRO96], as long as the modulation index in GSC is greater than in MSC. v_{CM} can be further reduced to ±E/3, without introducing

additional commutations, by modifying the duration of the zero vectors of MSC depending on the switching orders of GSC. This modulation is referenced as SVPWM7-CMVR [LEE01]. A further reduction can be made with the approach presented in [VID17], in which v_{CM} is totally canceled. Nevertheless, in this modulation strategy the symmetry of the switching period is broken to force the switching events of GSC and MSC to happen at specific instants, affecting the grid differential voltage harmonic content, and consequently, the filter design. In both modulations [LEE01, VID17], the power losses are equal to the case with SVPWM7 in GSC and MSC.

To improve the common mode of each VSC, several modulations have been proposed: active zero SVPWM (AZSVPWM), remote state SVPWM (RSSVPWM) and near state SVPWM (NSSVPWM). These modulations are based on the sole utilization of differential vectors, so if they are applied to the B2B power converter, v_{CM} will be bounded by ±E/3. AZSVPWM uses 4 differential vectors to synthesize the reference, the two adjacent ones, as the SVPWM7, and two opposite differential vectors during the rest of the sampling period [LAI04b]. This modulation also has 6 commutations per switching period. The CM peak voltage is reduced for a single VSC, but it still oscillates between ±E/6. To achieve a constant CM voltage, the RSSVPWM was proposed, a modulation that uses only one set of vectors to modulate v_{ref}, either the ones with negative common-mode (v_1, v_3 and v_5 in red, Figure 5.2) or the ones with a positive common-mode (v_2, v_4 and v_6 in blue). This modulation presents higher losses than SVPWM7, as it has 8 commutations per switching period, with an important reduction of the DC-link voltage utilization [CAC99, CAV10]. At last, NSSVPWM uses three adjacent differential vectors to produce v_{ref} [UN09] (v_1, v_2 and v_3 for the example in Figure 5.2 for $v_{G\,ref}$), with four commutations per switching period. As a drawback, this modulation cannot be used for low modulation indexes. In this sense, the NSSVPWM is complementary to the RSSVPWM. AZSVPWM, RSSVPWM and NSSVPWM all present a significantly higher harmonic content in the output differential voltage than SVPWM7 [HAV09], so they are not an appropriate solution for GSC, as a bulkier filter would be required in order to meet the grid codes. RSSVPWM and NSSVPWM cannot be applied to MSC, due to the wide range of variations of the modulation index. AZSVPWM does not present limitations in the modulation index, but it has the same number of commutations than SVPWM7, so it does not present any advantage for B2B power converters compared to [LEE01, VID17].

In this context, the use of discontinuous space vector PWM (DSVPWM) does not inherently bring an improvement of the CM in a VSC with respect

to the SVPWM7. These modulations are similar to the SVPWM7 but they only use a zero vector in each switching period. The main purpose of considering the use DSVPWM is increasing the power converter efficiency. In such sense, several modulations have been proposed. All of them use the two adjacent differential vectors, but just a zero vector, requiring only four commutations per switching period. The degree of freedom offered by the zero vector is used by some authors to minimize the power losses. In this sense DSVPWM0 [KOL91], DSVPWM1 [DEP77], DSVPWM2 [OGA90], and GDSVPWM [HAV98], avoid any switching in the converter leg with the highest current. With these strategies, the switching losses can be reduced to a half of the SVPWM7 switching losses, but the differential voltage harmonic content is increased [HAV99]. In [KOL91] DSVPWM3 is proposed, based on the utilization of the zero vector to find a compromise between reduced power losses and improved differential voltage harmonic content. The application of DSVPWMs is an appealing option for B2B power converters, as they offer important reductions in the switching losses, without strongly compromising the grid code compliance. However, if DSVPWMs are used in MSC and GSC, the peaks of v_{CM} and v_{PG} reach $\pm$E, as it is demonstrated in Section II, a 50% greater than with SVPWM7.

A comparison of the total harmonic distortion of the modulations presented in this section is performed in [HAV99] as a function of the modulation index. To represent the total harmonic distortion, a function, HDF, called harmonic distortion factor is computed, which is a measure of the ripple current for each PWM method. The results obtained in this article are plotted in Figure 5.7.

From this figure, it can be concluded that SVPWM7 and DSVPWM are greatly superior, in terms of grid current quality, than the presented AZSVPWM, RSSVPWM and NSSVPWM. For this reason, they are more suitable for grid-connected applications. The different scale factor in the HDF between SVPWM7, DSVPWM and the rest of the modulations, does not allow to compare the grid current quality between SVPWM7 and DSVPWMs. However, in [HAV98] the comparison between the different DSVPWMs and SVPWM7 is made. This comparison reveals that DSVPWMs, at high modulation indexes have similar performance than the SVPWM7, and can even become better if the switching frequency is increased for the DSVPWMs to compensate the reduction in the power losses.

DSVPWM allow to effectively increase the efficiency of the power converter without compromising the grid-code compliance in terms of grid current harmonic distortion. However, it increases the common-mode and phase-to-ground voltages in B2B conversion structures. If these two

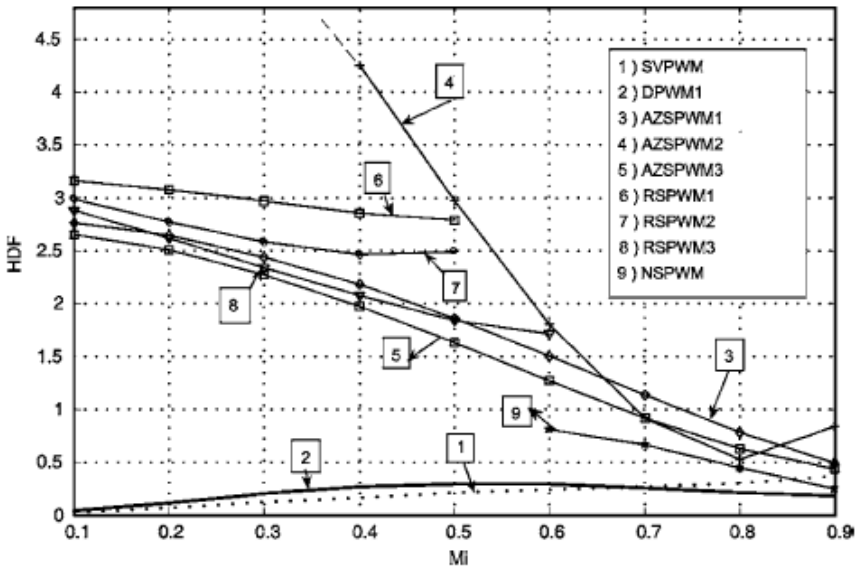


Figure 5.7: Comparison of the HDF for different modulation indexes [HAV99].

limitations are solved, without increasing the grid current harmonic content, the use of DSVPWM in B2B power converter can become a really interesting option. In this chapter, in Subsection 5.4.2, two DSVPWM strategies are presented for the B2B structure in order to reduce both the CM and PG voltages, retaining a low distortion in the grid current harmonic content. Both strategies are based on the synchronization of the switching orders of GSC and MSC. With the first strategy both v_{CM} and v_{PG} are limited to $\pm$2E/3, retaining the efficiency of DSVPWMs. With the second strategy, v_{CM} is limited to $\pm$E/3, introducing additional commutations. Achieving in both cases, a greater efficiency than with SVPWM7.

5.4 Proposed DSVPWM for back-to-back power converters

5.4.1 Common-mode and phase-to-ground voltages for the conventional DSVPWM

In this section, the worst cases in v_{CM} and v_{PG_i} are analyzed when the state of the art DSVPWMs are applied to a B2B conversion structure. According to the implementation of the space-vector modulation, discussed in Subsec-

tion 5.2.1, if d_L is equal to zero or d_H is equal to 1, v_0 or v_7, respectively, are eliminated from the sequence. In this way the DSVPWMs are implemented.

With DSVPWM the worst possible case in v_{CM} and v_{PG_i} occurs when the reference vector of GSC, v_{Gref}, and the reference vector of MSC, v_{Mref}, have largely different modulus and both power converters use different zero vectors. To show this, let us suppose that the reference vectors are in the positions showed in Figure 5.8. v_{Mref}, is in the first sector (S1), while v_{Gref}, is located in the second sector (S2), having v_{Gref} a greater module than v_{Mref}. Regardless of the discontinuous modulation implemented, MSC is going to use a different zero vector than GSC at some instants of the switching period. The situation described fo the reference vectors has been represented in Figure 5.9 (a) with the corresponding switching states of GSC and MSC and the resulting values of v_{CM} and v_{PG_a}. In this figure, MSC is using the positive zero vector, while GSC is using the negative zero vector. If the zero duty cycles are sufficiently large according to Equation 5.13, as in the case depicted, v_{CM} is equal to E. According to Equation 5.15, v_{PG_a} is also equal to E, because the negative zero vector in GSC, with a CM of -E/2, meets a leg voltage of E/2 in the phase a of MSC.

This higher CM and PG voltages, if compared with SVPWM7 or SVPWM7-CMVR, can lead to premature failures in bearings and insulation [KAU00]. As it has been proved, if MSC and GSC are modulated independently, v_{CM} and v_{PG} would reach ±E, so coordinated modulations for B2B

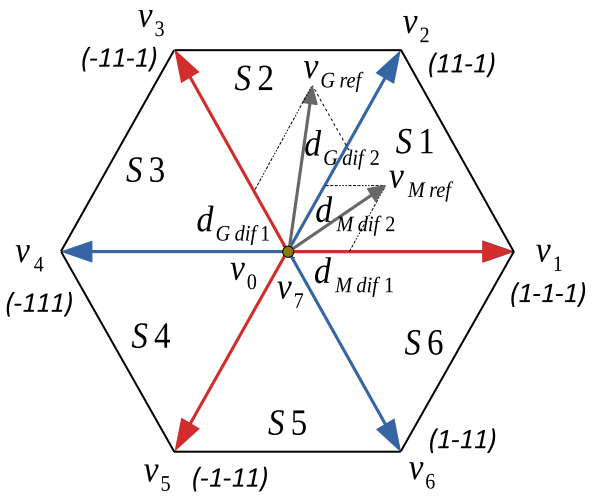


Figure 5.8: Space vector diagram with the eight possible switching states of a two-level three-phase power converter and the representation of the reference vectors of the machine and grid side converters; v_{Mref} and v_{Gref}.

structures are required. These modulations are presented in the next subsection, and developed to resemble te characteristics of the SVPWM7.

5.4.2 Proposed DSVPWM strategy

To improve the phase-to-ground and common-mode voltages of DSVPWM for B2B VSC, the modulation of MSC is modified, depending on the vectors used in GSC and their duty cycles, keeping the modulation in GSC unaltered. The discontinuous modulation to be used in GSC will be discussed in Subsection 5.4.3. Two modulations for MSC, synchronized with GSC, are proposed. In the first proposal, referred as DSVPWM-CMVR1, the worst case in both, v_{CM} and v_{PG}, is reduced to $\pm$2E/3 without introducing additional commutations. In the second proposal, DSVPWM-CMVR2, v_{CM} is further reduced to $\pm$E/3, but in this case additional commutations are required only in certain switching periods.

5.4.2.1 DSVPWM-CMVR1: limiting v_{CM} and v_{PG} to $\pm$2E/3

It has been identified in the previous section that v_{CM} reaches a peak of $\pm$E whenever MSC and GSC use at the same instant opposite zero vectors, as shown in Figure 5.9 (a). Besides, v_{PG} always reaches $\pm$E if the zero vector of GSC is not matched by the same zero vector in MSC. Taking into account both premises, v_{CM} and v_{PG} can be simultaneously reduced to $\pm$2E/3 by introducing in MSC the same zero vector than in GSC. As both power converters use the same carrier frequency, v_{PG} will never reach $\pm$E as long as the modulation index in MSC is lower than in GSC. This condition is also a requirement for the SVPWM7. The zero vector used by MSC is determined by Equation 5.16. If the lowest duty cycle of GSC, d_{GL} is greater than 0, meaning that GSC is using v_0, MSC is forced to use the same vector: $d_{Mz0} = d_{Mz}$. Otherwise, MSC uses v_7, the same zero vector than GSC.

$$d_{Mz0} = \begin{cases} d_{Mz} & \text{if } d_{GL} > 0 \\ 0, & \text{otherwise} \end{cases} \tag{5.16}$$

This condition will be checked every sampling period, and the duty cycles of MSC (d_{ML}, d_{MM}, d_{MH}) calculated accordingly. In Figure 5.9 (b), represented for the same reference vectors as in case (a), MSC is forced to use the same zero vector than GSC, by imposing in every sampling period Equation 5.16. With this strategy, the peaks of v_{CM} and v_{PG} are effectively reduced to $\pm$2E/3. Moreover, no additional commutations are introduced, so

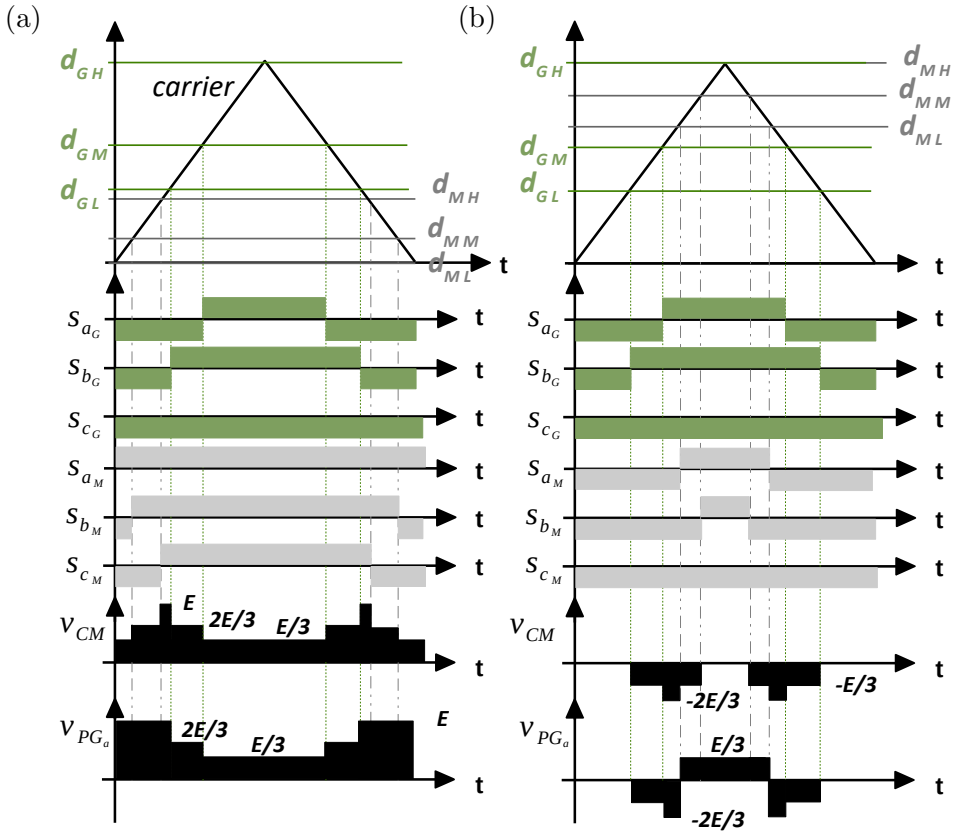


Figure 5.9: CM and PG voltages depending on the switching states of GSC (with v_{ref} in S2) and MSC (with v_{ref} in S1) and different modulation strategies: DSVPWM (a) and DSVPWM forcing MSC to use the same zero vector than MSC (DSVPWM-CMVR1) (b).

the whole B2B structure presents 8 commutations per switching period instead of 12 with SVPWM7, achieving a great reduction of the switching losses. As a drawback, the modulation in MSC cannot be optimized as in GSC to minimize the switching losses, by using the GDSVPWM, or to minimize the differential voltage harmonic content, by using DSVPWM3.

5.4.2.2 DSVPWM-CMVR2: limiting v_{CM} to ±E/3

With the modulation presented in the previous subsection, called DSVPWM-CMVR1 the same peak in v_{CM} and v_{PG} is achieved than with SVPWM7, while reducing the power losses. Nevertheless, with the SVPWM7-CMVR the peak

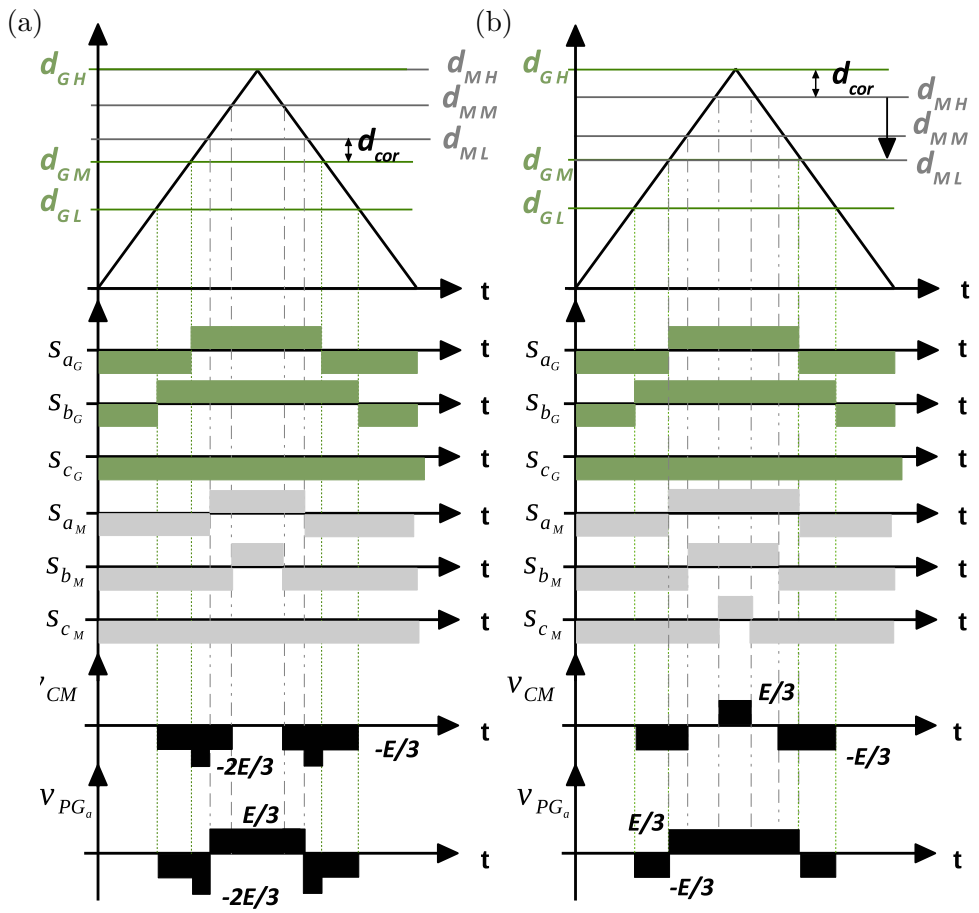


Figure 5.10: CM and PG voltages depending on the switching states of GSC (with v_{ref} in S2) and MSC (with v_{ref} in S1) and different modulation strategies: DSVPWM forcing MSC to use the same zero vector than MSC (DSVPWM-CMVR1) (a) and DSVPWM in GSC and SVPWM7 in MSC, whenever it is required, displacing the zero vector to reduce the common-mode voltage to $\pm E/3$ (DSVPWM-CMVR2) (b).

of v_{CM} is reduced to ±E/3. To achieve the same voltage levels, a modification to the DSVPWM-CMVR1, denoted as DSVPWM-CMVR2, is proposed in the following.

In Figure 5.9 (b) the common-mode voltage, once GSC and MSC apply the same zero vector, reaches its maximum of ±2E/3 only when a zero vector coincides with a differential vector in the other converter that has a common-mode with opposite sign. If Figure 5.9 (b) is carefully examined, it can be concluded that this occurs when d_{ML} is greater than d_{GM}. Similarly, this

situation also occurs when d_{MH} is lower than d_{GM}. In both cases, v_{CM} reaches $\pm$2E/3 because the time duration of the zero vector in MSC is greater than the sum of the durations of the zero and adjacent differential vector in GSC.

To avoid these situations, in a similar way as the SVPWM7-CMVR, the three duty cycles in MSC can be modified by d_{cor}, which only affects to the distribution of the zero vectors and not to the differential ones. In the case represented in Figure 5.9 (b), d_{cor} is set equal to the difference between d_{ML} and d_{GM}. With d_{ML} reduced by d_{cor}, meaning that the application time of v_0 in MSC is decreased, the -2E/3 peak in the common-mode voltage is avoided. The other zero vector, v_7 in this case, has to be increased to avoid a modification in the modulated average magnitude of the generated voltage compared to the reference vector. As a consequence, two additional commutations are introduced in this particular switching period. Whenever the modulation has to be corrected in MSC to avoid the $\pm$2E/3, MSC has 6 commutations per switching period, resulting in 10 in the whole B2B structure. However, this correction is only applied when the conditions in Equation 5.17 and Equation 5.18 are satisfied. For comparison, DSVPWM-CMVR1 has 8 commutation per switching period, while SVPWM7-CMVR has 12 commutations in every switching period.

$$\begin{aligned} if(d_{ML} > d_{GM}) &\rightarrow d_{cor} = d_{ML} - d_{GM} \\ &\rightarrow d_{Mz0} = d_{Mz} - d_{cor} \end{aligned} \tag{5.17}$$

$$\begin{aligned} if(d_{MH} < d_{GM}) &\rightarrow d_{cor} = d_{GM} - d_{MH} \\ &\rightarrow d_{Mz0} = d_{cor} \end{aligned} \tag{5.18}$$

Once the conditions and the required corrections specified in Equation 5.17 and Equation 5.18 are applied, the duty cycles are recalculated with the expressions in Equations 5.8, 5.9 and 5.10. In Figure 5.9 (c) the proposed modifications have been applied, showing that the peak of v_{CM} is reduced to $\pm$E/3. The number of times in which the correction has to be used is different depending on the DSVPWM used in GSC, as it is analyzed in the next subsection. For the particular situation represented in Figure 5.9 (c), v_{PG} is also confined within $\pm$E/3, however, along the fundamental period, it will reach $\pm$2E/3, so both v_{CM} and v_{PG} are equal than with SVPWM7-CMVR.

5.4.3 Switching losses of the proposed modulation strategies

The main motivation for using DSVPWM in B2B power converters is the improvement of the efficiency. It has been established in the previous section, that the proposed modulations effectively limit v_{PG} and v_{CM}. Moreover, as GSC has a modulation index close to unity, DSVPWM present a reduced THD. However, the proposed modulations for B2B structures, present some differences with those applied to a single power converter and for this reason, an analysis of the switching losses is performed.

The switching power losses of SVPWM7, or equivalently of the SVPWM7-CMVR, are compared with those of the proposed DSVPWM-CMVR1 and DSVPWM-CMVR2. Two different DSVPWM are tested for GSC: GDSVPWM, used to minimize the switching losses, and DSVPWM3, used to minimize the impact on the grid harmonic content. The space-vector implementation of GDSVPWM and DSVPWM3 is represented in Figure 5.11. Each sector is divided into two sub-sectors (I and II), this division determines the transition between the utilization of the positive and the negative zero vector. The DSVPWM-CMVR1 does not introduce additional commutations, however, with the DSVPWM-CMVR2 the modulation in MSC is modified if the conditions in Equation 5.17 and Equation 5.18 are satisfied. As a consequence, every time one of these conditions are met, two additional commutations per switching period are introduced. Nevertheless, depending on the modulation used in GSC, the modulation in MSC has to be modified a different number of times to keep v_{CM} within ±E/3. To visualize this, in Figure 5.12 the duty cycles of the

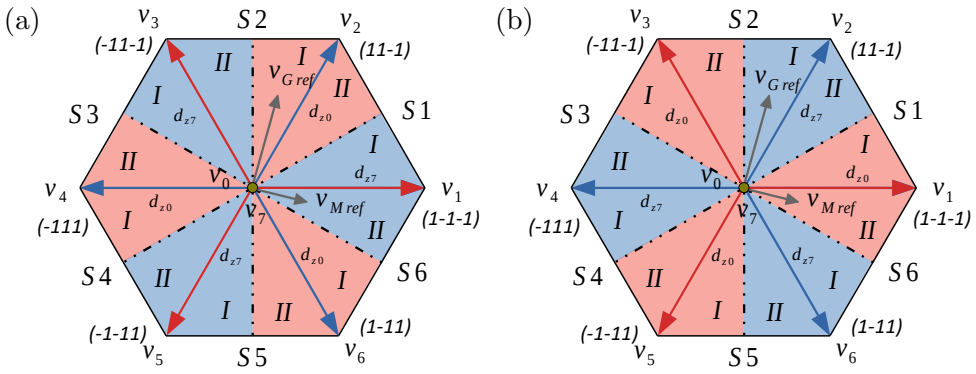


Figure 5.11: Implementation of the GDSVPWM with unity power factor (a) and DSVPWM3 (b).

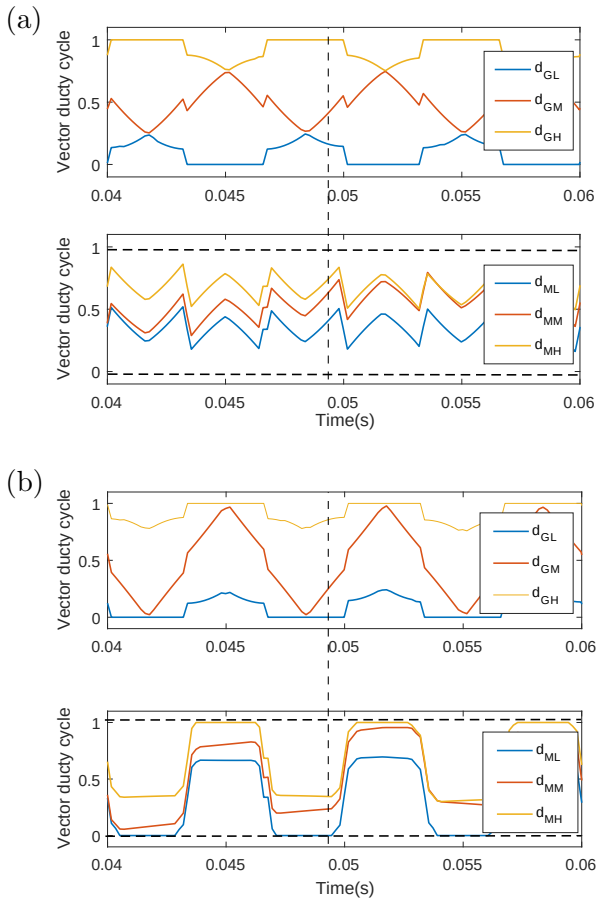


Figure 5.12: Duty cycles of GSC and MSC with the modulation DSVPWM-CMVR2 using in GSC GDSVPWM (a) and DSVPWM3 (b).

vectors of GSC and MSC are represented, along a fundamental period, for the modulation DSVPWM-CMVR2 and the two different modulations in GSC previously indicated. In Figure 5.12 (a), GSC uses the GDSVPWM, in Figure 5.12 (b), it uses the DSVPWM3. The duty cycles represented in Figure 5.12 correspond to a modulation index in GSC of 1 and a frequency of 50 Hz, while in MSC the modulation index is 0.4 and the frequency is 11 Hz. In Figure 5.12 (a) and (b), every time that in the low graph, where the duty cycles of MSC are represented, d_{ML} is different than 0 and, simultaneously, d_{MH} is different than 1, the corrections described in Equation 5.17 and Equation 5.18 are being applied. In Figure 5.12 (a) it can be seen that MSC is using the correction in every sampling period, applying

both zero vectors, to avoid common-voltages of ±2E/3, while in Figure 5.12 (b) the correction is used in just a few sampling periods.

To better understand this difference in the number of corrections required, let us consider the situation represented in Figure 5.11 (a) and (b), with $v_{G_{ref}}$ in S2-I and $v_{M_{ref}}$ in S6-II. This instant is marked with the vertical dashed line in Figure 5.12. With the GDSVPWM in GSC, Figure 5.12 (a), the zero vector v_0 is used. At the same time, in order to avoid ±E peaks in both v_{CM} and v_{PG}, MSC is forced to apply the same zero vector v_0. As the modulation index in MSC is lower than in GSC, d_{ML} would be greater than d_{GM}, given that d_{Gdif1}, the duty cycle of v_3, is small, Figure 5.11 (a). The correction in MSC has to be applied in every sampling period, forcing the B2B VSC to commute 10 times in every switching period. In contrast, with the modulation DSVPWM3 in GSC, few corrections are required. As it can be seen in Figure 5.11 (b), the zero vector v_7 is used in the same instant considered. MSC is also forced to use v_7, but as the duty cycle d_{Gdif1} is small, it hardly occurs that d_{MH} is lower than d_{GM}. In this way, the switching power losses depend on the modulation used, but also on the modulation index in MSC.

To gain an overall idea of the switching losses, the mean switching power losses are computed for a 500 kW B2B power converter using *Matlab Simpower Systems*, for five different modulations:

- SVPWM7-CMVR: taken as the reference power losses
- GSC with GDSVPWM and MSC with both DSVPWM-CMVR1 and DSVPWM-CMVR2.
- GSC with DSVPWM3 and MSC with both DSVPWM-CMVR1 and DSVPWM-CMVR2.

As GSC is connected to the grid, it has an almost constant modulation index, close to 1. In contrast, the MSC modulation index varies, from 0.2 to 1.1 in the analysis performed. The power is increased with the modulation index. In this way, the behavior of a generator in a DFIG wind turbine is replicated. As the wind speed is higher, the generator rotates faster, generating more power and increasing its voltage. The switching losses are represented, against different modulation indexes in MSC in Figure 5.13, normalized with respect to the losses obtained with the SVPWM7-CMVR. At low modulation indexes the utilization of CMVR2 increases the power losses with respect to CMVR1, because the duty cycle of the zero vector in MSC is large and the corrections described in Equation 5.17 and Equation 5.18 have to be applied. However, with GDSVPWM the switching

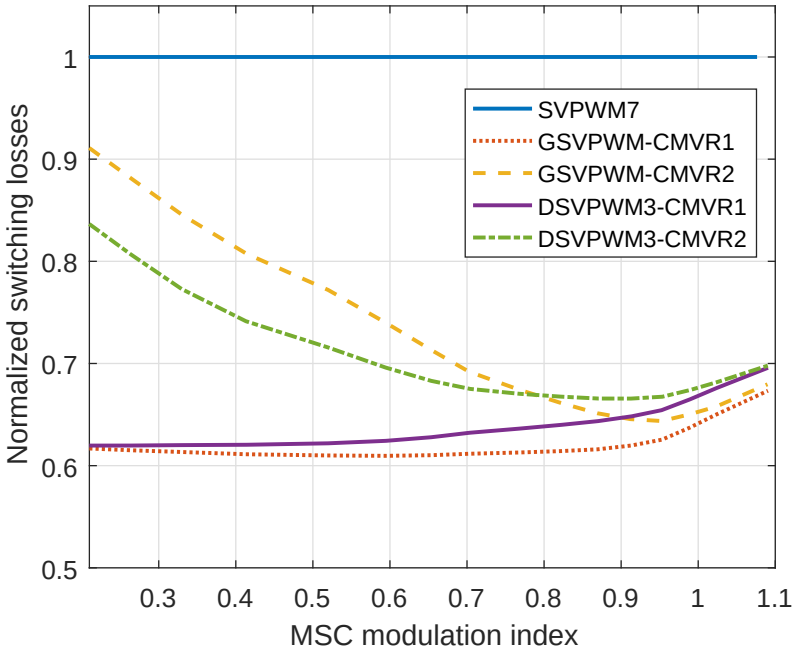


Figure 5.13: Normalized switching losses for different modulations: GSC with GDSVPWM and CMVR1 in MSC (GDSVPWM-CMVR1), GSC with GDSVPWM and CMVR2 in MSC (GDSVPWM-CMVR2), GSC with DSVPWM3 and CMVR1 in MSC (DSVPWM3-CMVR1) and at last GSC with DSVPWM3 and CMVR2 in MSC (DSVPWM3-CMVR2).

power losses are greater than with DSVPWM3 despite the minimization of the switching losses in GSC, this is because additional compensations have to be applied in MSC. At higher modulation indexes, the duty cycle of the zero vector in MSC is reduced, and less compensations are required with the CMVR2, becoming GDSVPWM superior to DSVPWM3 in terms of losses. DSVPWM3 has a better harmonic content than GDSVPWM, in this way, the utilization of DSVPWM3 in GSC, with either CMVR1 and CMVR2, is preferable to the utilization of GDSVPWM in GSC. With the application of CMVR1, the differences between DSVPWM3 and GDSVPWM in terms of power losses, are small, as only GSC can minimize the power losses.

Once the switching losses reduction has been analyzed the efficiency gain, a figure of merit for any power conversion structure, is evaluated for the proposed modulation. To calculate the efficiency gain, the difference between the power losses of the SVPWM7 and those of the proposed modulation strategies is calculated, normalizing this result to the converter rated power. In Figure 5.14 the efficiency gains for the different modulations are represented as a function of the modulation index in MSC. According to the

simulation results, the maximum efficiency gain with DSVPWM3-CMVR1 is 0.51%, while with GDSVPWM-CMVR1 is 0.44%. If the common-mode voltage is limited to ±E/3, the maximum efficiency gain is 0.39% for DSVPWM3-CMVR2 and 0.42% for GDSVPWM-CMVR2.

As a result, it can be concluded that both, DSVPWM3-CMVR1 and DSVPWM3-CMVR2 allow to significantly reduce the power losses, with respect to SVPWM7-CMVR, with the same phase-to-ground and common-mode voltages that SVPWM7 and SVPWM7-CMVR, respectively.

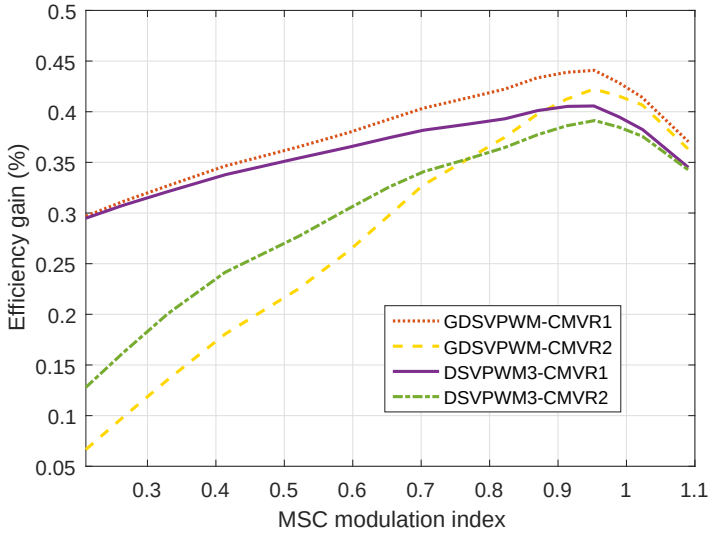


Figure 5.14: Efficiency gain with the proposed DSVPWMs for B2B converters.

5.5 Experimental Results

The two modulations presented in this chapter have been developed to reduce the CM and PG voltages in B2B structures with DSVPWM. Both of them have been validated in the experimental set-up of Figure 5.15; a 500 kW B2B power converter designed for a DFIG wind turbine, with a switching frequency of 2.8 kHz and a DC-bus voltage equal to 1150 V. This is also the same power converter used to validate the active damping strategy presented in Chapter 4. The important aspect of the converter to validate the proposed modulation strategies is the voltage imposed by the power converter, and not the filter parameters, for this reason the filter component values are not detailed. If the reader is interested, they can be found in Table 4.1.

Three different DSVPWM modulations are compared; the use of DSVPWM3 in both GSC and MSC, and the use of DSVPWM3-CMVR1 and DSVPWM3-CMVR2. The three modulations are compared in terms of common-mode voltage, phase to ground voltages and also the differential voltage in MSC. The machine side modulation index is 0.3 with a fundamental frequency of 30 Hz, while in GSC the modulation index is 0.8 with a fundamental frequency of 50 Hz. In all the cases tested, both GSC and MSC use the same carrier wave. The results obtained are showed in Figure 5.16. Initially, in Figure 5.16 (a) GSC and MSC modulate their reference vector independently, using both the DSVPWM3. As expected, and theoretically showed in Figure 5.9, both v_{CM} and v_{PG} reach maximum peaks of ±E (1150 V). These peaks are limited to ±2E/3 (766 V) when the DSVPWM3-CMVR1 is applied, Figure 5.16 (b). When both power converters are forced to use the same zero vector, the spikes of ±E are eliminated. A further reduction is obtained in the common-mode when DSVPWM3-CMVR2 is used, Figure 5.16 (c). By displacing the zero vectors in MSC when it is required, the CM voltage is confined within ±E/3 (383 V), while the PG voltage is still limited to ±2E/3. The phase differential voltage harmonic content in MSC is affected with the DSVPWM3-CMVR1 and the DSVPWM3-CMVR2. With both modulations, the first switching harmonic family amplitude is reduced, but the harmonic content is expanded to a wider range of frequencies. The harmonic content in MSC is not a critical aspect, as long as no important low frequency harmonics are introduced that may cause torque oscillations. This is not the case for the proposed

Figure 5.15: Test bench used for the validation of the proposed modulation strategies.

modulations, so the modulations are valid for their use in MSC.

The DSVPWM3 is the preferred modulation to be used with CMVR2, because it has a better harmonic content than GDSVPWM, with a greater efficiency at low modulation indexes of MSC, due to the lower number of corrections required. In both, DSVPWM3-CMVR1 and DSVPWM3-CMVR2, the modulation of GSC remains unaltered, so the grid current harmonic content is not modified. In Figure 5.18 (a) the grid current is represented when the DSVPWM3 is used in the grid-side converter, with its harmonic analysis in Figure 5.18 (b). In Figure 5.19, only the grid current harmonic content is represented for the SVPWM7, as in the temporal current waveform no differences can be found by simple inspection. As

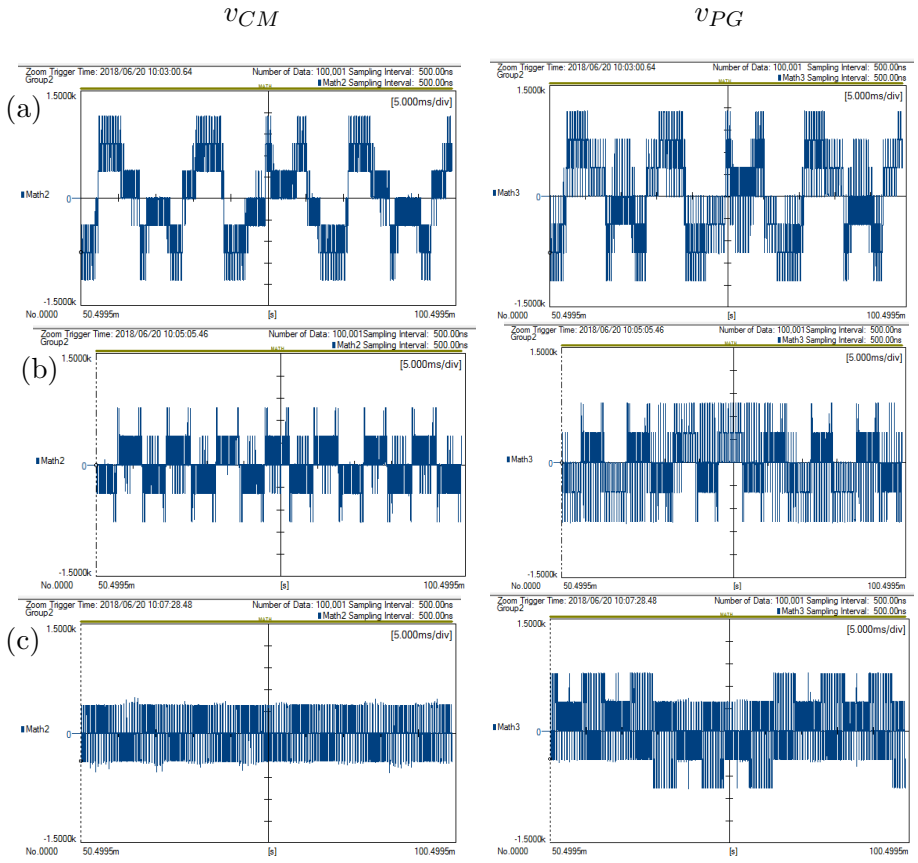


Figure 5.16: Comparison of the common-mode and phase-to-ground voltages normalized with respect to the DC-bus voltage for: DSVPWM3 in GSC and MSC (a), DSVPWM3-CMVR1 (b) and DSVPWM3-CMVR2 (c).

expected, with the DSVPWM3 in GSC at high modulation indexes the grid current quality is very similar to the SVPWM7 [HAV99]. The main problems for the fulfillment of the grid codes are normally found around the switching frequency, where the limits imposed by the BDEW become more strict. In this range of frequencies, the grid code compliance is not compromised with the use of DSVPWM3 in GSC, as the amplitude of the harmonics at these frequencies are very similar in both cases.

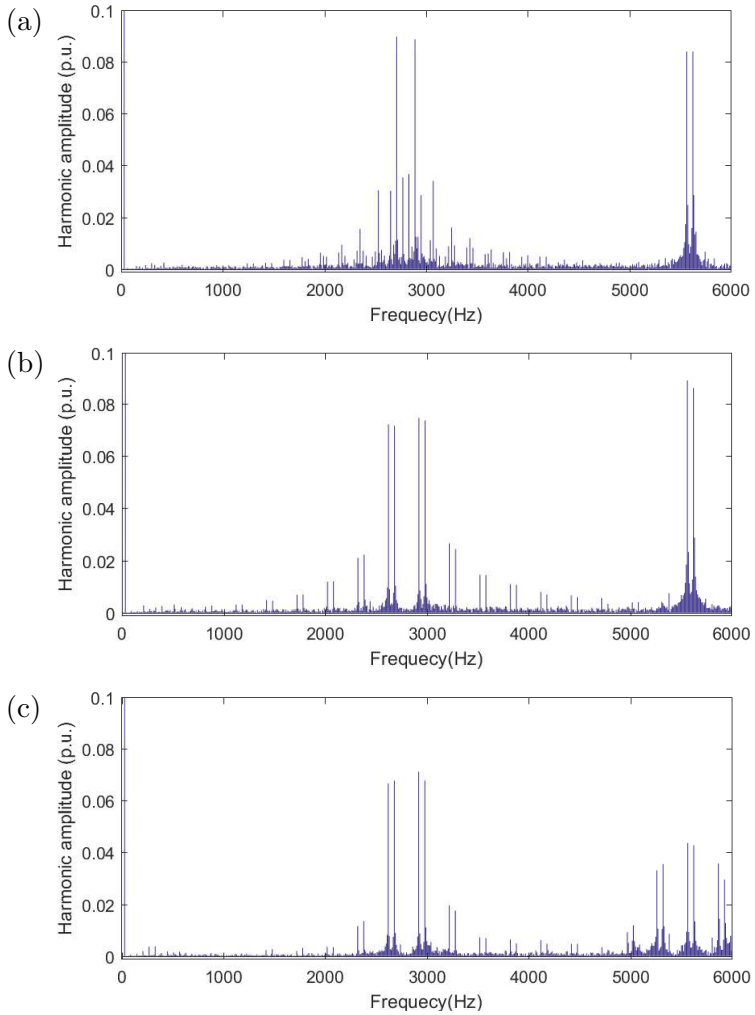
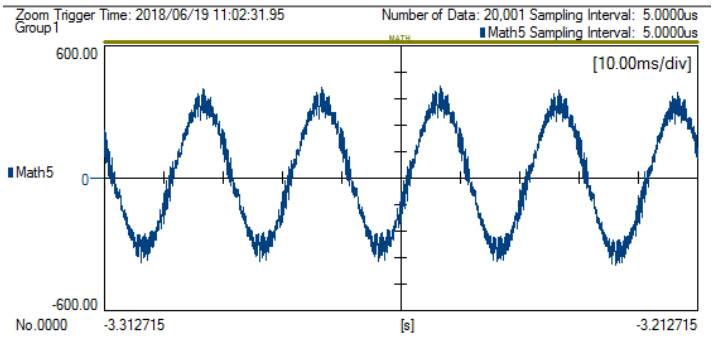


Figure 5.17: Comparison of the phase differential voltage harmonic content in MSC for: DSVPWM3 in GSC and MSC (a), DSVPWM3-CMVR1 (b) and DSVPWM3-CMVR2 (c).

(a)



(b)

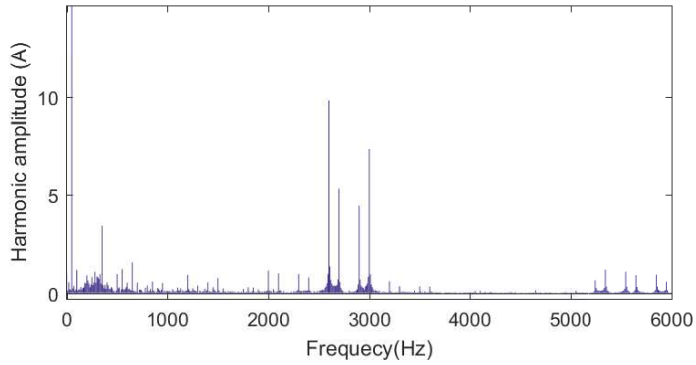


Figure 5.18: Grid current waveform (a) and harmonic content (b) for the DSVPWM3.

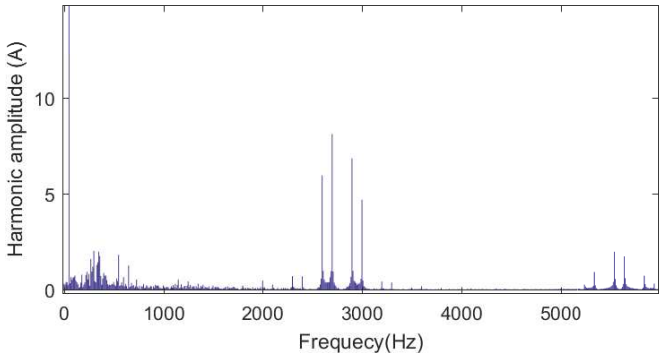


Figure 5.19: Grid current harmonic content for the SVPWM7.

5.6 Conclusion

Discontinuous space vector modulations are an interesting approach for back-to-back power converters used in WECS. In grid-connected applications, the modulation index is high, and consequently, DSVPWMs present a reduced harmonic content, similar to the SVPWM7. It has been shown that if GSC and MSC are modulated independently, the common-mode and phase-to-ground voltages reach the whole DC-bus voltage. To solve this issue, a modulation is proposed for back-to-back power converters that simultaneously allow to reduce the common-mode and phase-to-ground voltages to ±2E/3. These are the same voltage levels that if the classical SVPWM7 is used in B2B power converters with synchronized carriers in GSC and MSC, a common solution in B2B power converters. However, with the proposed modulation DSVPWM-CMVR1, the number of commutations per switching period is reduced from 12 to 8. This modulation forces MSC to use the same zero vector than GSC. To further reduce the common-mode voltage to ±E/3, another modulation is proposed, DSVPWM-CMVR2 that also forces MSC to use the same zero vector that in GSC, but additionally uses both zero vectors in MSC in some sampling times to avoid the peaks of ±2E/3. For this modulation, only in that particular switching periods the number of commutations is increased to 10. The number of corrections depends on the modulation used in GSC and the modulation index in MSC. This modulation achieves the best efficiency and differential voltage when it is combined in GSC with the DSVPWM3. These modulations can reduce the switching power losses by more than a 30% for modulation indexes higher than 0.6 in MSC, achieving efficiency gains of 0.44%. Experimental results validate the reduction of common-mode and phase-to-ground voltages with the proposed modulations. It is also shown that the quality of the grid and machine side differential voltages are not compromised.

Chapter 6

Parallelization of B2B conversion structures for high-power offshore wind turbines

6.1 Motivation

The European offshore wind market is dominated by four main players that account for 96% of the cumulative installed power, as it has been seen in Chapter 1. The most important manufacturer is Siemens-Gamesa, with 64.5% of the cumulative installed power, followed by MHI Vestas, 18.7%, and Senvion, 7.7% [EUR18]. By taking a look at the wind turbine portfolio for the offshore segment of these manufacturers, a general idea of the market trends can be gained, in order to set the requirements for the power conversion structure for offshore WECS.

Table Table 6.1 summarizes the commercial wind turbines offered by the main manufacturers. It can be seen that the rated power of the wind turbines is steadily increasing and the permanent magnet generator (PMG) at low voltage is the dominant trend. Both Siemens-Gamesa and MHI Vestas have wind turbines with similar rated powers and generator topologies, while Senvion uses a doubly-fed induction generator (DFIG) with a reduced turbine rated power.

The same trend, high-power with a low-voltage generator, can be found in other manufacturers such as GE Renewable Energy, who recently announced

Table 6.1: Offshore wind turbine portfolio of the main manufacturers.

Manufacturer	Wind turbine	Rated power (MW)	Generator	Voltage (V)
Siemens-Gamesa	SWT-6.0-154	6	PMG	690
	SWT-7-154	7	PMG	690
	SG 8.0-167 DD	8	PMG	690
MHI Vestas	V117-4.2 MW	4.2	PMG	690
	V164-8.0	8	PMG	690
	V164-9.5	9.5	PMG	690
Senvion	6.XM	6.1-6.3	DFIG	690 (rotor)

the release of Haliade-X: a 12 MW Wind turbine, using a PMG generator with direct-drive technology and an output voltage of 900 V.

These high-power low-voltage wind turbines with PMG generators require a power converter that is able to transform the whole power generated. Consequently, the power converter has to be able to work with high current levels, which reach 7000 A per phase for an 8 MW power converter. Currently, commercial IGBTs can handle maximum currents of 3600 A in DC, such as the FZ3600R17HP4 model made by Infineon. In practice, the maximum current is limited to half of the DC value, as the switching increases the power losses. To reach the desired 7000 A, four modules in parallel would be required. However, it is hard to guarantee an homogeneous distribution of the current among the four parallel IGBTs. Alternatively, several power conversion stages could be coupled in parallel to increase the current handling capabilities, controlling the output current of each of these stages. These power conversion stages could be designed as a single power converter, achieving some benefits in terms of power density. For these reasons, in order to reach the desired power ratings for offshore wind turbines, the parallelization of several low voltage B2B conversion units is the most suitable option.

The size is a crucial aspect in the design of a wind turbine, due to materials cost, greater loads and stress and limiting factors in its transport such as roads, trucks, bridges... For this reason, a high power density is an important feature for the power converter. Moreover, in offshore wind turbines redundancy is an important characteristic: in this systems, the maintenance is programmed in time intervals of 6 to 12 months, requiring boats for many tasks and resulting in a high cost. The parallelization of power converters allows to achieve designs with a high power density [AND07] and redundancy, that allows to still operate the system, at a reduced power, decreasing the downtime time [BIR07]. The use of parallel power converters is aligned with the tendency of generators with

multiple three-phase stator windings in 8 MW and higher rated power wind turbines. Even though a greater power density could be achieved with mid and high voltage solutions [CHI13], wind turbine makers are still reluctant to their utilization as they have not been technologically fully tested in wind applications [YAR15].

Additionally, the correct operation of modular converters connected in parallel allows to increase the system efficiency of a wind turbine. At low wind speeds only the required number of power converters will be connected. In this way, the power converters are able to operate during the maximum time at their point of maximum efficiency. However, finding the optimal operation of several parallel power converters, from the efficiency point of view, is not trivial, not even for the case of two power converters [VOG14].

Two main options can be considered to parallelize power converters. The first option is focused in the increase of the power density, designing the parallel power conversion stage as a single power converter. The conversion stage designed in this ay is called **single-block**. In this approach, several aspects of the conversion structure can be optimized, such as the output converter filter, achieving a higher power density. The second option is focused in achieving a high redundancy. It consists in designing a smaller modular and independent power converter that can be parallelized as many times as required to reach the power ratings of offshore wind turbines. Redundancy and optimization by designing the parallel power conversion stage as a single power converter, cannot be achieved at the same time. If an optimized single-block based on parallel conversion structures is designed for the whole rated power, the single-block has to be disconnected in case of failure, as it might not operate properly or comply with the imposed requirements. In this way, there is a trade-off between design integration and redundancy. In this chapter the issues of parallelization of B2B structures are discussed with goal of finding a compromise between the optimization of the single-block and modularity. There are several requirements that have to be taken into account when the solution for the single-block is developed:

- High power density
- High efficiency
- Optimal relation cost/MW
- Grid code compliance
- Reducing the downtime time

- Stability and fast dynamic response

- Scalable

6.2 State of the art of the parallel connection of power converters

The parallel connection of power converters is a straightforward approach to increase the power rating of a power conversion stage without a complete redesign of the converter itself. There are two main ways of connecting in parallel several power converters: direct coupling and inductive coupling. The latest can be divided into isolated coupling, and non isolated coupling.

Each of these alternatives present some benefits and inconvenients in terms of power density and redundancy. In the following, the coupling of the power converters is analyzed in terms of their performance in these two aspects. The state of the art of the parallel connection of power converters is discussed for only two power converters in parallel for simplicity. The conclusions for two power converters are expandable to N power converters in parallel.

6.2.1 Direct coupling

The direct connection of power converters is represented in Figure 6.1. This connection forces both of them to switch each leg at the same time instants. As indicated in Figure 6.1 if both power converters, in a given instant, do not have the same switching state in a given phase (phase c in the case depicted), the DC-buses will be short-circuited, independently of their connection. Only when both power converters use the zero vectors with independent DC-buses, can they apply different zero vectors. In case the DC-buses are coupled, both converters have to switch at the same instants, even during the zero vectors.

As the semiconductors and drivers are not exactly identical, both power converters might not switch exactly at the same time instants, and thus, small inductances are required to limit the circulating currents. These inductors avoid the short-circuit of the DC-buses that will occur otherwise due to these small differences in the switching instants and improve the current sharing between both power converters.

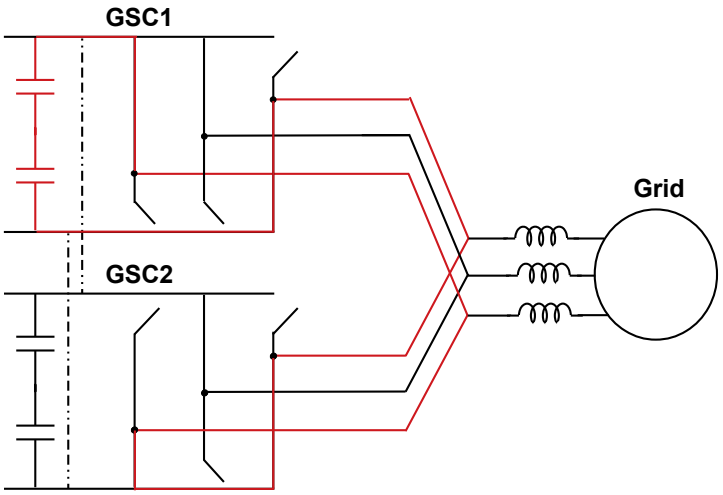


Figure 6.1: Direct coupling of two power converters.

6.2.2 Inductive coupling

6.2.2.1 Isolated coupling

In the isolated coupling, the electrical isolation can be achieved in both the grid and the machine. In the grid side converters, the connection is made through an isolation transformer [SHA11, KRI15, JAF17], as shown in Figure 6.2. In the machine side converter by connecting each power converter to different stator windings in multi-stator machines [KHA08, SHA15, PRI15, ZOR18].

In these conversion structures, there is not an electrical connection between both power converters, however, they are magnetically coupled, as they share the same magnetic core in the transformer. With the appropriate modulation strategies, the differential harmonic content at the output could be reduced, while the homopolar current components cannot circulate, as they do not magnetize the transformer's magnetic core and they could only flow through parasitic capacitances. In Figure 6.3 the common-mode and differential mode of this coupling option has been represented to illustrate this idea, representing in red the recirculated current. The definitions presented in Chapter 2 have been used. Similarly to the common-mode components, the switching harmonics phase shifted in both power converter by 180 degrees do not magnetize the magnetic core.

If the DC-buses are connected, both power converters are still isolated and they would not be circulating currents among GSC1 and GSC2. In this case

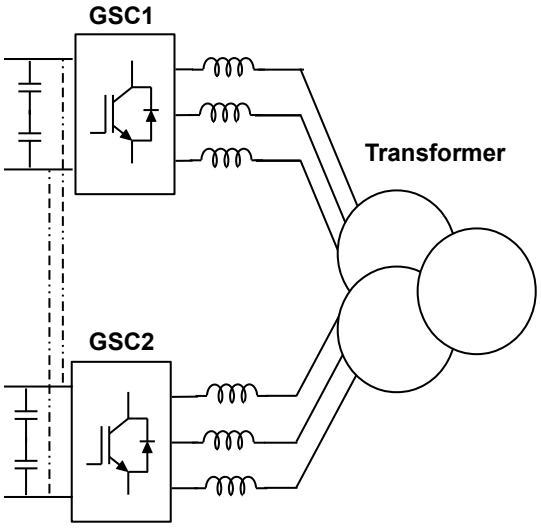


Figure 6.2: Isolated coupling of two power converters.

the switching harmonics will flow through the same DC-bus and its harmonic

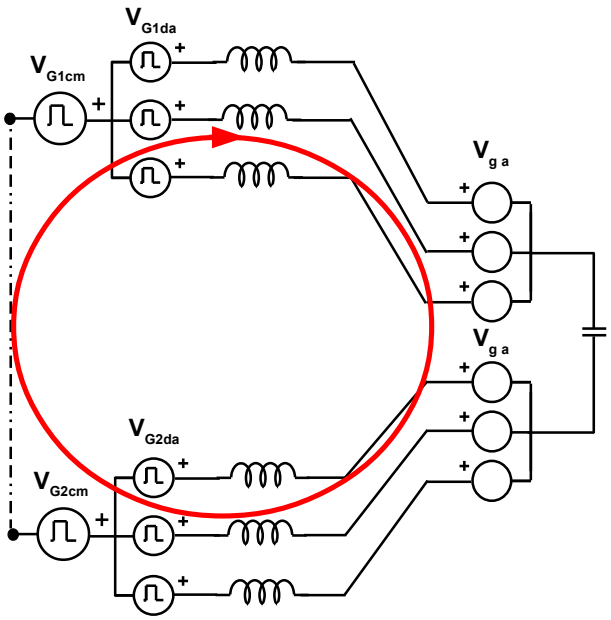


Figure 6.3: Common-mode and differential mode currents in the isolated coupling of two power converters.

content will change.

6.2.2.2 Non-isolated coupling

The non-isolated inductive coupling is represented in Figure 6.4. In this alternative, the power converters are directly coupled through inductors. These inductors allow the different modulation of both converters, granting the optimization of the output filtering stage, as harmonic cancellations can be achieved in the output current. The main difference with respect to the isolated coupling, is that in this coupling, a circulating current occurs between the power converters when they are modulated differently.

6.2.2.3 Optimization of the inductive coupling

As mentioned, with the inductive coupling of power converters, both converters do not have to switch at the same time instants and some enhanced modulation techniques can be implemented between the power converters, which can be used to reduce the output filter size. Additionally, the converter output inductances can be partially or totally integrated in the same magnetic core, reducing the total output filter size. Both aspects are briefly discussed in the next paragraphs.

Modulation techniques for harmonic content reduction

Several modulation strategies have been proposed in the literature to

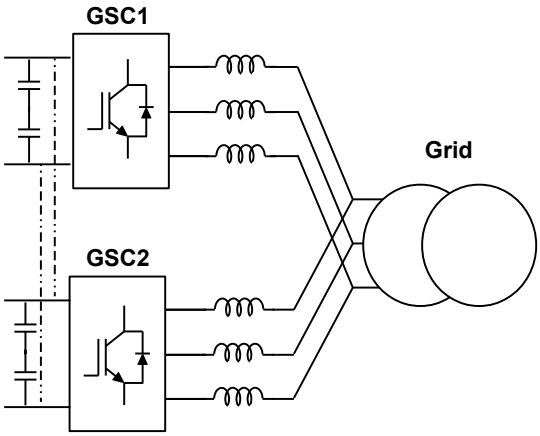


Figure 6.4: Inductive coupling of two power converters.

improve the output harmonic content of parallel power converters. An approach is the modulation of the N paralleled power converters as a multilevel converter. [QUA17] presented the three-level modulation approach for two two-level power converters. In this case, both power converters have to be controlled as a single converter, meaning that different control actions cannot be provided by each of them. Another approach is the implementation of selective harmonic elimination (SHE) in parallel power converters [KON16]. This technique, inherently complicated to optimize, becomes more complicated for N parallel B2B power converters, as these converters have additional restrictions, such as common-mode and phase-to-ground voltages at the generator terminals and efficiency that highly complicate the optimization procedure. Nevertheless, between all the advanced modulation strategies for parallel power converters, interleaving is the most extended one. This technique can be easily extended to several B2B parallel power converters, in which the machine-side modulation has to be synchronized with the grid-side modulation to improve the common-mode and phase-to-ground voltages, as demonstrated in Chapter 5. This approach is the one followed in this work, and for this reason, it is explained in greater detail in the following.

The first application of interleaving to three-phase VSC dates back to the late 80s for uninterruptable power supplies (UPS) and AC motor drives [HOL88, HAS87, KAW88]. However, nowadays, it still attires attention from many researchers working on different aspects of this modulation approach. Interleaving is based in phase shifting the carrier waves of the power converters coupled in parallel in order to reduce the output voltage harmonic content or minimize the impact of the switching harmonics in different converter components. As indicated in Figure 6.5, the carrier waves of two power converters can be displaced by an angle δ. In this way, the harmonics at the switching frequency are also phase-shifted by the same angle. If δ is selected to be 180 degrees, the harmonics at the switching frequency are phase shifted by the same angle. For two parallel power converters, it means that the harmonics at the switching frequency not contribute to the grid current component. In contrast, these harmonics would create cross-currents between both power converters. The same happens for all the odd switching harmonic families. The harmonics around the second switching harmonic family are displaced by 360 degree, so they are in phase and contribute to the grid current harmonic content. The same happens for all the even switching harmonic families.

To show the effects of interleaving a simulation is performed for two parallel power converter with a switching frequency of 1950 Hz and asymmetrical

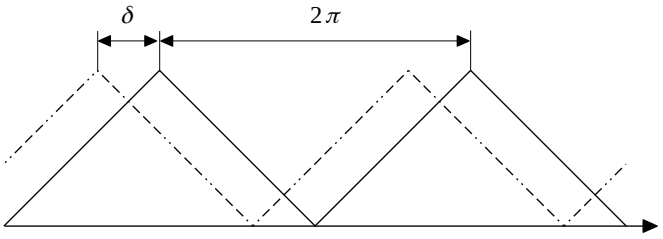


Figure 6.5: Application of interleaving.

sampling, due to the lower harmonic content of updating the modulation twice per switching period [HOL01]. The interleaving angle is 180 degrees and the resulting voltage harmonic content is plotted in Figure 6.6. In both power converters the modulation index is 1. In the same graph, the phase voltage with respect to the midpoint DC-bus is plotted, $V_{G1_{a0}}$, with the mean of the two phase voltages of phase a, denoted by V_{Gn_a} and equal to $(V_{G1_{d_{a0}}} + V_{G2_{d_{a0}}})/2$, and the difference between both phase voltages, $(V_{G1_{a0}} - V_{G2_{a0}})$. All the voltages are normalized with respect to the DC-bus mid point voltage. The modulation used is the SVPWM7.

By analyzing the voltages harmonic content represented in Figure 6.6 it can be verified the previous analysis. With an interleaving angle of 180 degrees, the normal voltage does not contain harmonics at the switching frequency, equal to 1950 Hz, and the first harmonics that have to be filtered by the output LCL filter are the second switching harmonic family. The first switching harmonic family creates a cross-voltage, and consequently, a cross-current that has to

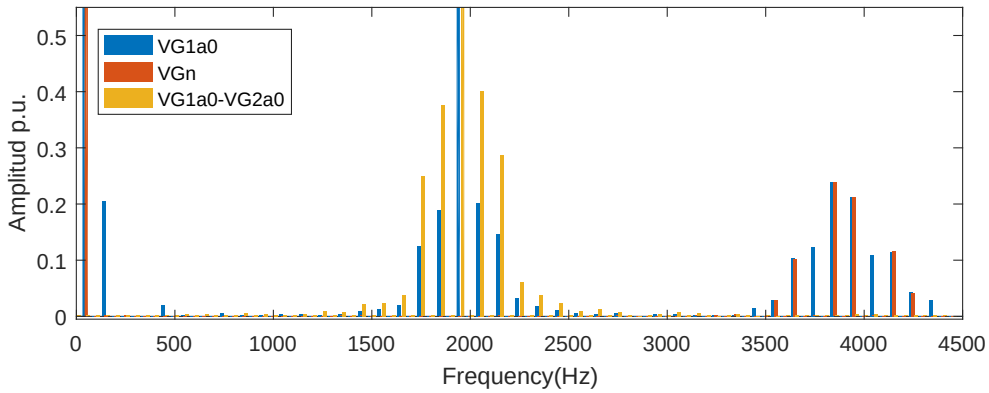


Figure 6.6: Harmonic content of the phase voltage, the normal voltage and the difference between both phase voltages.

be limited by the inductive coupling.

To minimize the size of the output filter, if N power converters are connected in parallel and the carrier waves are phase shifted by $360/N$ degrees, the first *N-1* harmonic families are recirculated between the power converters and have no effect on the output grid current. In this case the first group of harmonics that has to be attenuated by the output filter is the N^{th} multiple of the switching harmonic family.

Normally, the control of the power converters coupled in paralleled is performed in the same digital system, however, in some applications, the parallel power converters may be controlled independently without communication between them. The implementation of interleaving in these systems is studied in [PER97]. From the system stability point of view, as only the second harmonic family is filtered, the resonance frequency of the LCL output filter could move towards the Nyquist frequency. This circumstance should be take into account in the implementation of the active damping strategy.

The application of interleaving to parallel power converters also brings benefits to other passive components, no only to the reduction of the output filter. In [ZHA11a] the effect of interleaving on the DC-link ripple reduction is studied for two parallel power converters sharing the same DC-link. It is found that for an interleaving angle of $\pi/2$ the DC-ripple is minimized with the SVPWM7 modulation for high power factor applications, as the one studied in this work. In contrast, for the DSVPWM the DC-ripple is minimized for an interleaving angle of π in high power factor applications.

But interleaving not only influences the grid current harmonic content and the DC-link, it also conditions the design of the inductors used to limit the circulating currents between the two converters [ZHA10a]. A common approach to limit the circulating current with a reduced inductor is the use of interphase transformers (IPTs), also referred in the literature as intercell transformers.

Interphase transformers

Interphase transformers are coupled inductors that can offer a greater impedance to the circulating current harmonics than to the output current. Therefore they allow the obtention of an appropriate dynamic response and a reduction of the required filter size and cost, as each current component can be limited by the required inductance [FOR09]. There are several alternatives when it comes to choosing the appropriate IPT: single-phase inductors, three-phase inductors with additional core legs in order to limit the common-mode, and integrated inductors that offer different paths to the

circulating currents than to the output grid currents. Several IPTs have been proposed [FOR07, LAK13, LAK14, BHI11, LAB08, HED16, GOH15a, GOH16, OHN18, KNI08, GHO08], the most interesting alternatives for the single-block power converter are modeled in Subsection 6.6.2.

As an example, the simplest IPT to couple two power converters in parallel is represented in Figure 6.7. This single-phase IPT couples both power converters offering different impedances to the circulating currents that are phase shifted than to the current components that are in phase. If the currents I_{G1_a} and I_{G2_a} are in phase and equal in magnitude, the fluxes created by both components cancel each other, and the core is not magnetized. The only inductance seen by the current under these circumstances is the leakage inductance. This is the inductance provided to

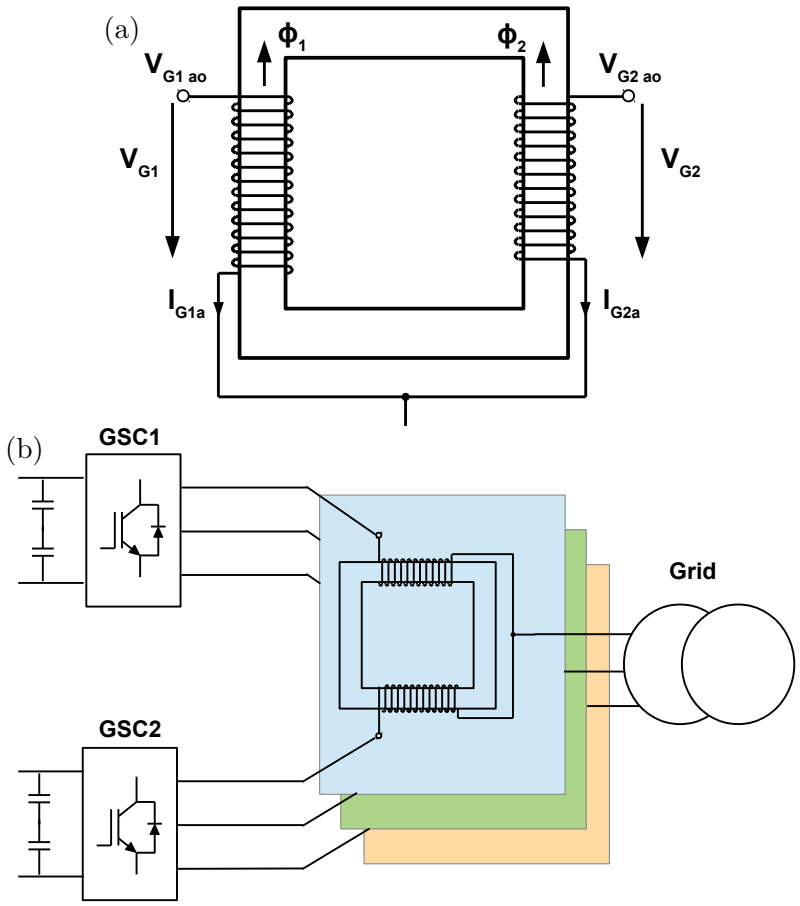


Figure 6.7: Single-phase IPT.

the output filter. However, if the currents are phase shifted by a 180 degrees, the magnetic flux is reinforced. As a consequence, this component is used to limit the circulating currents. The same working principle

Reduction of the size of the IPT

To reduce the size and losses in the IPT, several modifications on the modulation strategies have been proposed. [COU11] analyzed the influence of SVPWM7 and discontinuous modulations on the flux created in the IPT. They proposed a modulation that combines some of the state-of-the-art DSVPWM and a new proposal, in which the modulation used depends on the modulation index. [GOH15c] modified the discontinuous modulation vector sequence to reduce the flux, and consequently the size, of the IPT. By doing so, additional commutations are introduced, having 6 commutations per switching period in each VSC and partially losing the benefits of the implementation of DSVPWMs in terms of efficiency. [ZHA12] presented also a modification of the DSVPWM in order to reduce the circulating current and reduce the IPT, based on a modification of the modulation if the reference vectors of both power converters are located in different sub-sectors. [XIN99a] proposed a method to control the low frequency oscillations that may appear in parallel interleaved power converters when the transition between subsectors in the two power converters occur at different time instants.

6.3 Modeling B2B power converters in parallel

The model to analyze the coupling of B2B conversion structures in parallel is obtained from the extension of the models obtained in Chapter 2 for a single B2B power converter. In this section, a detailed description of the modeling procedures is provided to enhance the understanding of the modulation and control strategies proposed in this chapter.

The analysis and modeling approach developed in this section is performed for a system with non-isolated couplings, as the isolated coupling is similar to having different power converters. In the parallel connection of power converters, the converters might not switch at the same time instants, so circulating currents will appear between them. In fact, this is always the case when interleaving is applied. The circulating current has to be limited by the inductive coupling of the parallel power converters. To better understand the voltages driving the circulating currents between the power converters and how the passive components are affected by them, the

equivalent circuits of each current component in the parallel back-to-back conversion structure is analyzed in this section. First of all, the equivalent circuits are described for two back-to-back power converters connected in parallel and they are later extended to the general case of N parallel power converters.

6.3.1 Analysis of the currents in the power converter

To derive the equivalent circuits and clarify the study, the converter output current is divided into two components [ZHA10b, JUA14]:

- Normal current
- Cross-current

The normal current in phase i of a particular power converter is defined, for the connection of two power converters, as half of the current delivered to the grid or to the machine, Equation 6.1. The nomenclature used for this current is $I_{Gx_{n_i}}$, where G stands for the grid side converter, x for the power converter number connected in parallel, n refers to the normal current and at last, i stands for the phase: a, b or c. In the case of the machine side converter, the subindex M will be used. The difference between the output current of each power converter and the normal current in a given phase is called cross-current, $I_{Gc_{y-z_i}}$. Where c indicates that it is the cross-current and y and z represent that the cross-current occurs between the converters y and z, with a positive sign form the first one to the second one. The cross current and the normal current are represented in Figure 6.8 for the grid-side converter, a representation that is extensible to the machine-side converter.

The cross-current $I_{Gc_{1-2_a}}$ can be considered as the part of the current in phase a of GSC1, that instead of flowing towards the grid, flows through phase a of GSC2. This current, defined positive when circulating from GSC1 to GSC2, has the same magnitude but opposite sign when it is defined from the perspective of GSC2. The normal and the cross-currents are defined by the following equations:

$$I_{Gx_{n_i}} = \frac{I_{g_i}}{2} = \frac{I_{G1_i} + I_{G2_i}}{2} \tag{6.1}$$

$$I_{Gc_{1-2_i}} = \frac{I_{G1_i} - I_{G2_i}}{2} \tag{6.2}$$

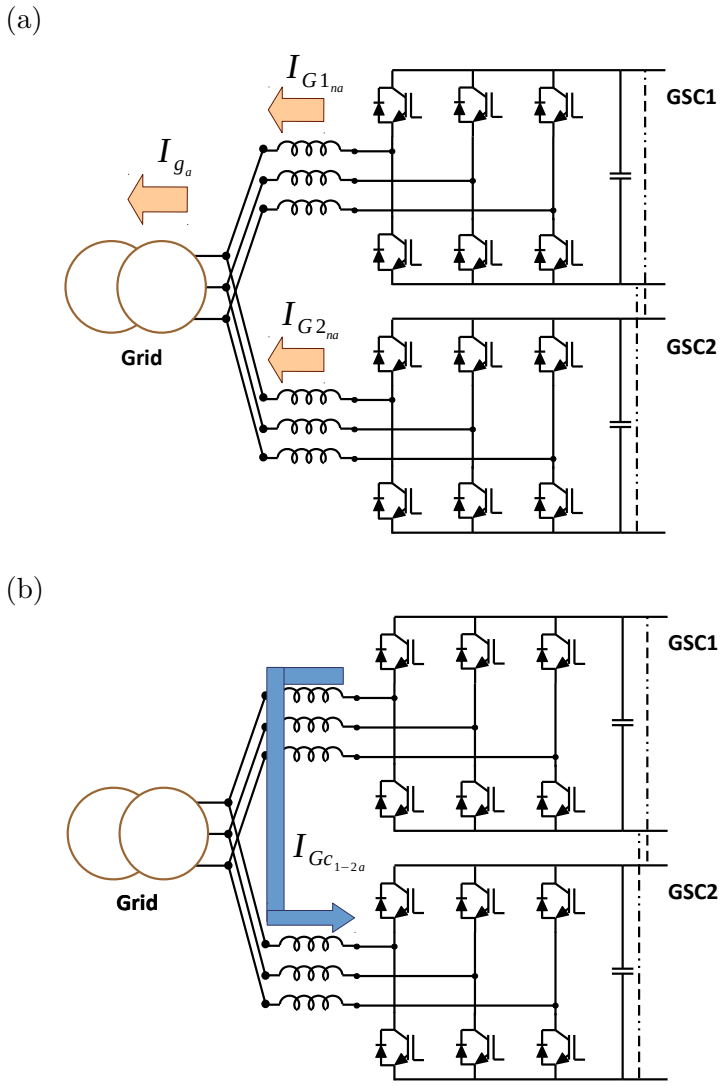


Figure 6.8: Normal current (a) and cross-current (b).

$$I_{Gc_{2-1_i}} = -I_{Gc_{2-1_i}} = \frac{I_{G2_i} - I_{G1_i}}{2} \tag{6.3}$$

where I_{G1_i} is the total current in phase i of each power converter and I_{g_i} is the total current injected to the grid in phase i.

The cross-current can be decomposed at the same time in homopolar cross-current, $I_{ch_{1-2}}$, and differential cross-current $I_{Gcd_{1-2_a}}$. For this reason, two

voltages are defined: the homopolar voltage, V_{Gx_h}, and differential voltage, $V_{Gx_{d_i}}$, that for the converter GSC1 are given by:

$$V_{G1_h} = \frac{V_{G1_{ao}} + V_{G1_{bo}} + V_{G1_{co}}}{3} \tag{6.4}$$

$$V_{G1_{d_i}} = V_{G1_{io}} - V_{G1_h} \tag{6.5}$$

with i equal to a, b or c. It can be seen that the homopolar voltage is also the converter common-mode voltage source previously defined in Chapter 2. In the following it is referred as homopolar voltage, as it is done in the literature, because it has an impact on the circulating currents, in contrast with the overall common-mode voltage, which causes the grid ground currents. The differential voltages are equal to the ones defined in Chapter 2. Moreover, by definition:

$$V_{G1_{d_a}} + V_{G1_{d_b}} + V_{G1_{d_c}} = 0 \tag{6.6}$$

If Equation 6.2 is applied at every phase, the total cross-current of each phase is obtained. Knowing that, by definition, the homopolar cross-current is equally shared between the three phases, it can be calculated by adding the three cross-currents:

$$I_{ch_{1-2}} = I_{Gc_{1-2_a}} + I_{Gc_{1-2_b}} + I_{Gc_{1-2_c}} \tag{6.7}$$

And consequently, the differential cross-current is determined by:

$$I_{Gcd_{1-2_i}} = I_{Gc_{1-2_i}} - \frac{I_{ch_{1-2}}}{3} \tag{6.8}$$

$I_{ch_{1-2}}$ should not be mistaken with the grid common-mode current, which flows through the ground. $I_{ch_{1-2}}$ is the component of the cross-current, that flows between both power converters and is equal in the three phases. This current is represented by the red arrow in Figure 6.9.

It can be demonstrated that the homopolar cross-current of GSC is equal in magnitude to the one in MSC but with an opposite sign [JUA14]. If there are only two B2B conversion structures connected in parallel without connecting their DC-buses, the homopolar cross-current is equal for the four power converters and is dependent on the homopolar voltage introduced by the four power converters. Otherwise, if the DC-buses are connected, the homopolar cross-current will flow in GSC through both converters and the

DC-bus, driven by the GSC homopolar voltages, and similarly will occur in MSC. In contrast, the normal current and the differential cross-current in the grid side, depend only on the voltage imposed by the GSCs. The same can be stated about the machine normal current and differential cross-current.

To sum-up, the current between two power converters connected in parallel can be divided into three components:

- Normal current: the current component that flows towards the grid or the machine, created by the differential voltages that are in phase.
- Differential cross-current: the current component recirculated between the converters that share the same side, GSC or MSC, adding up to zero. This current in driven by the differential cross-voltages that are not in phase.
- Homopolar cross-current: the current component recirculated between the four power converters, or two if the buses are linked, driven by the homopolar voltage.

These current components are represented in Figure 6.9, the homopolar cross-current is represented in red, the differential cross-current in green and, lastly, the normal current is represented in yellow.

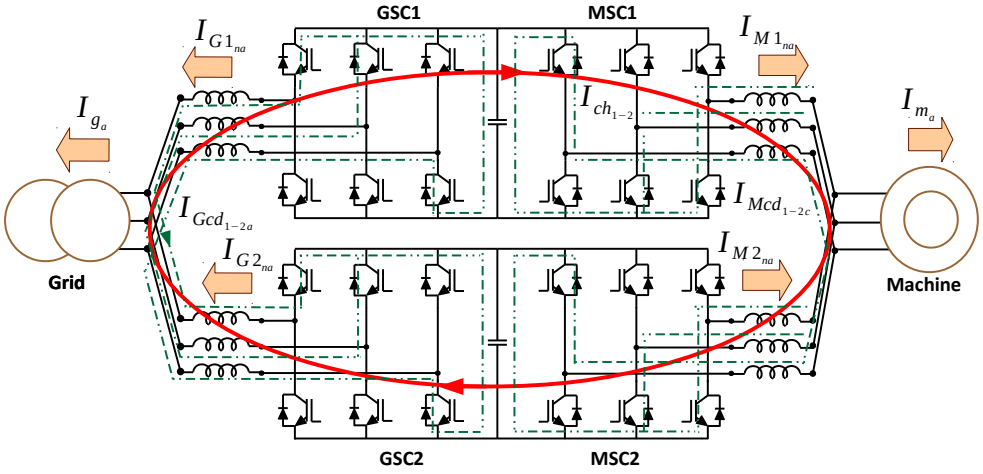


Figure 6.9: Representation of the currents in two parallel power converters.

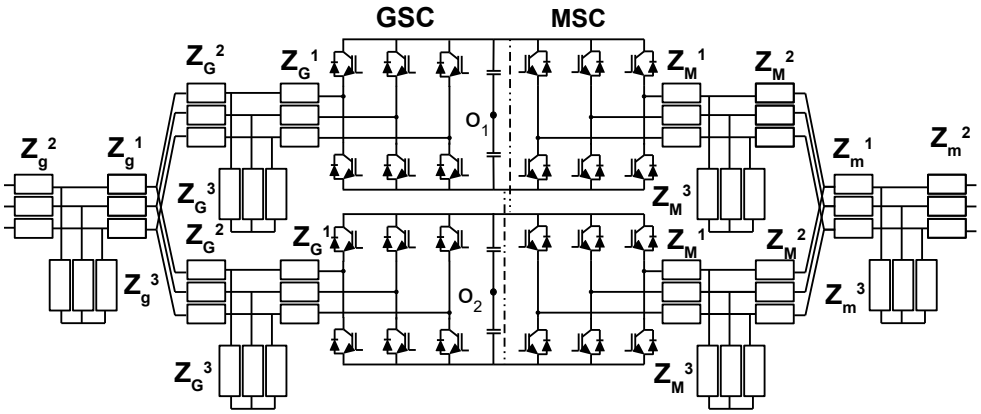


Figure 6.10: System to be modeled.

6.3.2 Obtention of the equivalent circuits

Once the current has been decomposed in its different terms, the models for each component can be obtained. For the B2B power converter typically used in WECS and modeled in Chapter 2, the output impedances in GSC are the LCL components and their parasitic resistances. In MSC the filter dv/dt is found, which is formed by an inductor and the RC branch. However, in general, there can alternative output filters, which are definitely going to affect the interaction between the power converters. For this reason, following the approach in [JUA14], a general model is developed in this thesis considering a set of series and parallel resistances at the output of MSC and GSC, as shown in Figure 6.10. From the general models developed in this section, the effect of the specific filtering solutions can be easily obtained.

The models developed in this section are only valid if the impedances are balanced and equal in both power converters. Otherwise, the normal voltage components would affect both the normal and cross-currents and the same would happen with the cross-voltages. In the following, for the derivation of the models, the superposition principle is applied to understand the origin of each current component. By decomposing the system in terms of the homopolar and differential voltages, Figure 6.10 can be represented as in Figure 6.11. Where V_{Gx_h} is defined according to Equation 6.4 and $V_{Gx_{d_i}}$ according to Equation 6.5. These models will be the starting point for the following analysis.

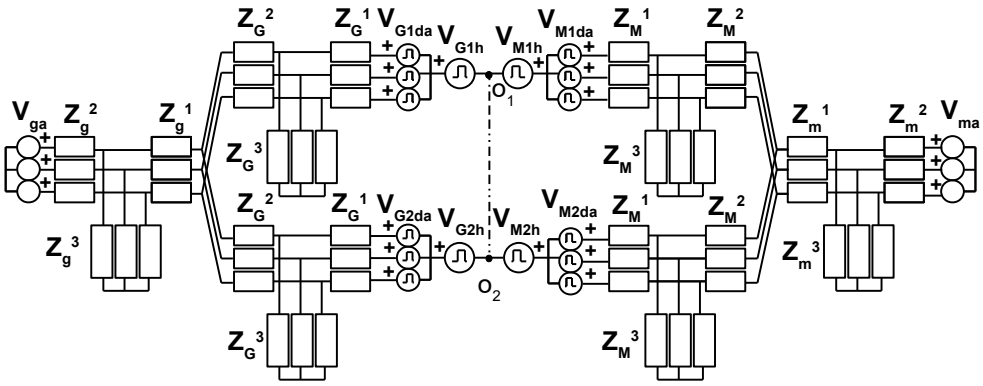


Figure 6.11: Representation of the system in terms of the homopolar and differential voltages.

6.3.2.1 Homopolar cross-current component model

By definition, the homopolar current is the current recirculated between both power converters that is equal in the three phases. For this reason, the machine and the grid do not affect this component. Moreover, the parallel impedances have an isolated neutral point, so no homopolar currents can flow through them. Taking into account these facts, the homopolar cross-current component is given by the model represented in Figure 6.12.

Considering that all the impedances are balanced, the differential voltages cannot create an homopolar cross-current, so the homopolar and differential circuits are decoupled. In such a way, the model in Figure 6.12 can be further simplified to the one represented in Figure 6.13. The homopolar cross-current is driven by the homopolar voltage sources and limited by the third part of the

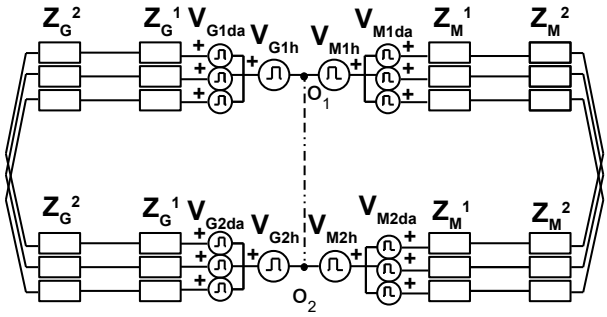


Figure 6.12: Model for the homopolar cross-current component.

series impedances. If the impedances are independent inductors, the effective inductance offered by each of the impedances in Figure 6.13 would be a third of the inductance in each phase. If the impedances are three-phase inductors the current will be limited by a third of the inductor leakage inductance.

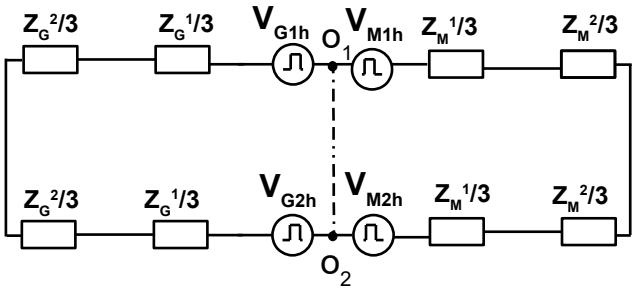


Figure 6.13: Model for the homopolar cross-current component.

It can also be clearly seen that if the DC-buses are independent, the homopolar cross-current is the same in the four power converters, while if the DC-bus is shared for both power converters, the homopolar current has two paths, one through GSC and the DC-link and another one through MSC and the DC-link.

6.3.2.2 Equivalent circuit for the differential cross-current component

The homopolar voltages do not influence the normal current component and the differential cross-current as long as the impedances are balanced. If the homopolar voltage sources are eliminated from the equivalent circuit in Figure 6.11, independent systems are obtained in GSC and MSC. As all the impedances are balanced, and the voltage sources are all differential voltage sources, the neutral point voltage is the same for all the impedances, and the neutral points can be connected as indicated in Figure 6.14 by the dashed lines. GSC and MSC have the same differential mode circuit, so they can be studied independently. For this reason, in the following, the scope is focused in GSC, as it can be directly extended to MSC. The single phase equivalent circuit of phase i of GSC is shown in Figure 6.15, where i can be equal to *a, b* or *c*.

The differential voltages can be decomposed into two different voltage sources, one of them driving the differential cross-current, defined as the

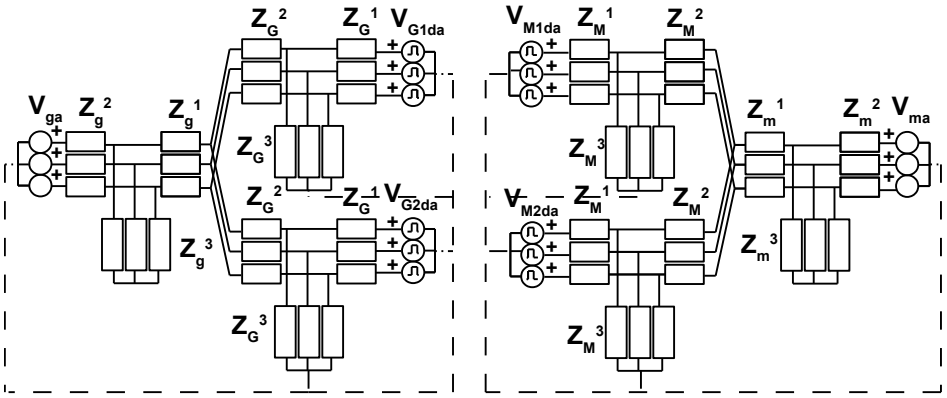


Figure 6.14: Differential mode circuit.

difference of the differential voltages of GSC1 and GSC2:

$$V_{Gcd_i} = V_{G1_{d_i}} - V_{G2_{d_i}} \tag{6.9}$$

and a normal voltage source, driving the normal current. This voltage source is defined as

$$V_{Gn_i} = \frac{V_{G1_{d_i}} + V_{G2_{d_i}}}{2} \tag{6.10}$$

If only the differential cross-current is studied, as the normal voltage does

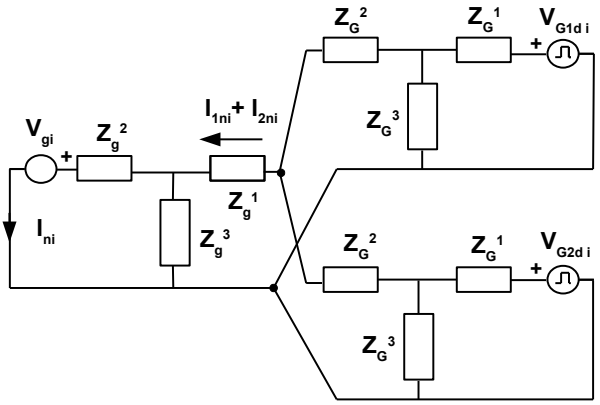


Figure 6.15: Single phase differential mode circuit.

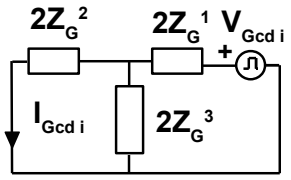


Figure 6.16: Differential cross-current circuit.

not create a recirculation, the system can be simplified as shown in Figure 6.16.

6.3.2.3 Equivalent circuit for the normal current component

Similarly, if only the normal current component is analyzed from the converter perspective, the system can be simplified to the one shown in Figure 6.17 (a), as V_{Gcd_i} does not make any contribution. The grid impedances are multiplied by

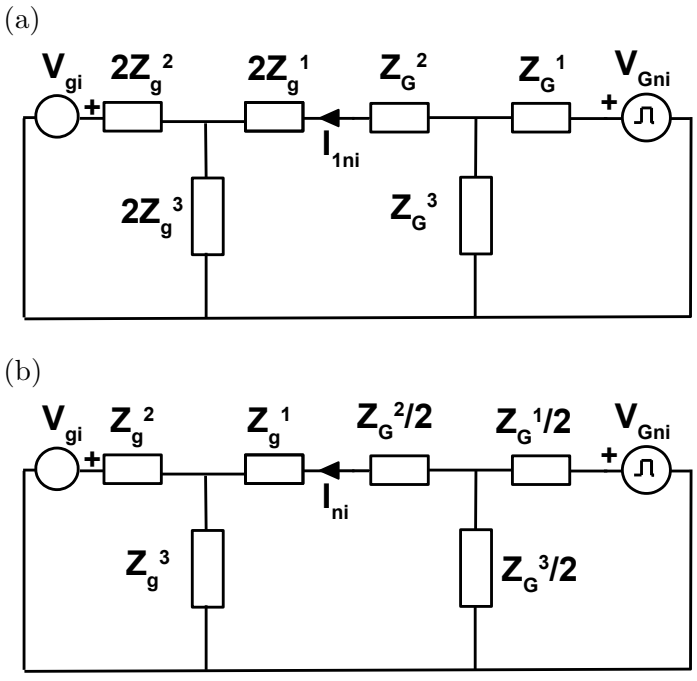


Figure 6.17: Normal current circuit: from the converter perspective (a) and from the grid perspective (b).

two, because the current normal component creates a voltage drop across these impedances that is in phase for GSC1 and GSC2, consequently, the converter sees greater grid impedances. In contrast, from the grid side perspective, the converter impedances are divided by two, as represented in Figure 6.17 (b).

In this way, it is clear that the number of converters in parallel strongly influences the system stability and the control adjustment, as it is modifying the system dynamics.

6.3.3 Extension of the equivalent circuits to *N* B2B paralleled power converters

The equivalent circuits developed allow to study the interactions between two power converters. However, in general, a greater number of B2B units can be parallelized to achieve the desired power ratings. Fortunately, the models can be easily extended to the general case where a number N of B2B power converters are connected in parallel. In the following, the generalization is made.

In Figure 6.18 the interaction between N B2B paralleled power converters is represented, where only the currents between 1-2 and 1-N have been represented for simplicity.

The normal and cross-current components are defined according to the following expressions:

$$I_{G1_{ni}} = I_{G2_{ni}} = I_{GN_{ni}} = \frac{I_g}{N} = \frac{I_{G1_i} + I_{G2_i} + ... + I_{GN_i}}{N} \tag{6.11}$$

$$I_{Gc_{1-2_i}} = -I_{Gc_{2-1_i}} = \frac{I_{G1_i} - I_{G2_i}}{2} \tag{6.12}$$

or

$$I_{Gc_{1-N_i}} = -I_{Gc_{N-1_i}} = \frac{I_{G1_i} - I_{GN_i}}{2} \tag{6.13}$$

If the cross-current is decomposed in its homopolar cross component and differential cross component, as in Figure 6.18, the following definitions are required:

$$I_{ch_{1-N}} = I_{Gc_{1-N_a}} + I_{Gc_{1-N_b}} + I_{Gc_{1-N_c}} \tag{6.14}$$

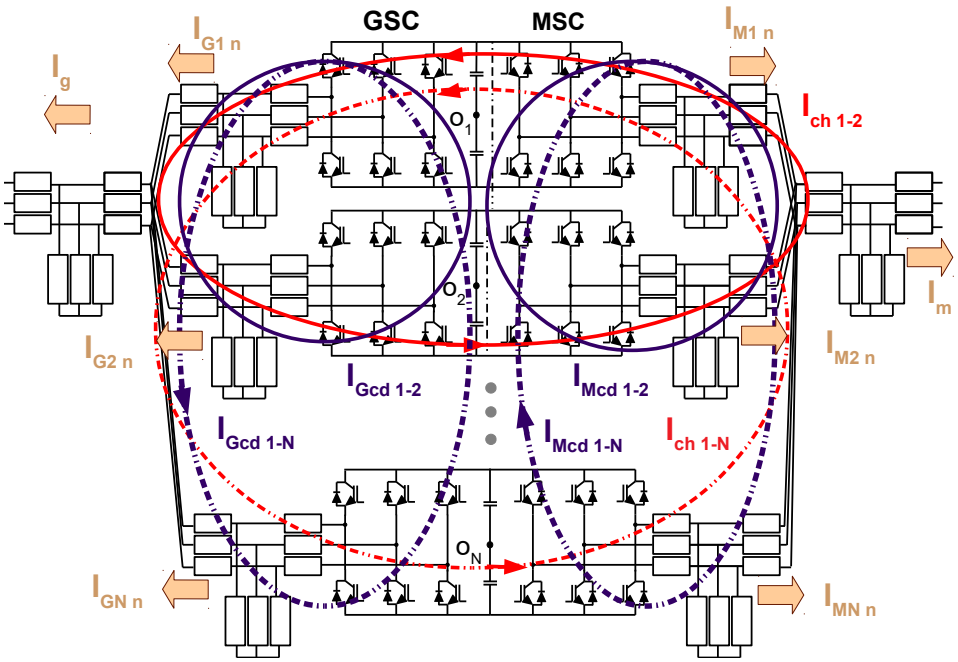


Figure 6.18: Interaction between N parallel B2B converters.

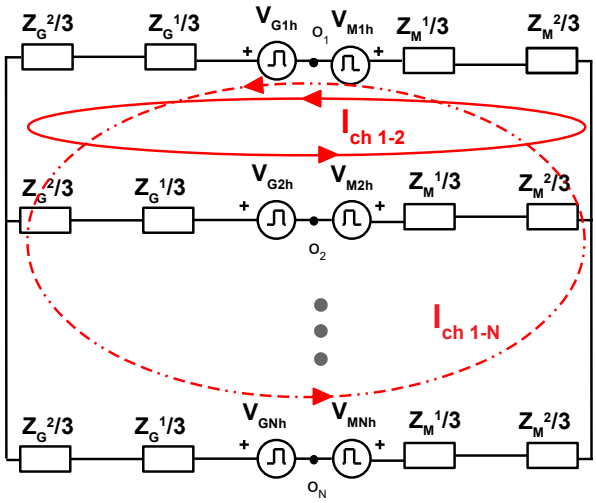


Figure 6.19: Homopolar cross-current equivalent circuit.

$$I_{Gcd_{1-N_i}} = I_{Gc_{1-N_i}} - \frac{I_{ch_{1-N}}}{3} \tag{6.15}$$

And from these definitions, the previous models can be extended for the general case of N paralleled power converters. In Figure 6.19 the homopolar cross-current equivalent circuit is represented with the circulating currents between the B2B conversion structures 1-2 and 1-N. It can be seen that this model is the extension of the model derived for two B2B converters, adding the additional homopolar circuits in parallel.

The differential cross-current circuit between the first and the N^{th} B2B conversion structure is given by Figure 6.20. It can be seen that the components in this circuit are exactly the same that in the case with two B2B conversion lines, as the differential cross-current between two power converters is only affected by the difference of the differential voltages of those power converters and the impedances in this path, which are the same for all the power converters.

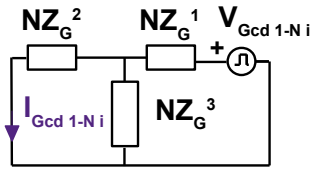


Figure 6.20: Differential cross-current equivalent circuit.

Lastly, the normal current component is given by the circuit represented in Figure 6.21. It can be seen that the grid impedances are multiplied by the number of power converters connected in parallel. The connection of parallel power converters increases the grid impedance, decreasing the SCR accordingly.

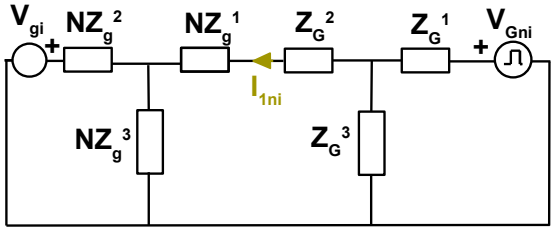


Figure 6.21: Normal current equivalent circuit.

The equivalent circuits developed in this section are the base for the

analysis presented throughout the chapter. In Section 6.4 they are used to define the single-block topology. The same circuits are used to study the influence of the modulation on the performance of the power converter in Section 6.5. In Section 6.6 to design the passive components, and lastly in Section 6.8 to derive the model for the control of the power converter.

6.4 Definition of the single-block conversion structure topology

One of the main goals set in this chapter is the development of the single-block power converter. As a first step, in this section, the most suitable topology is defined. Initially, the single-block rated power is established, and later, the type of coupling between the power converters is defined.

With commercially available IGBTs, very reliable B2B structures around 2 MW can be obtained. A straightforward option is coupling these power converters in parallel. In this configuration, the scalable single-block would be formed by a single B2B power converter. This option provides a high redundancy, an interesting option in high power systems, specially in offshore wind turbines. To achieve this redundancy, breaking and protection devices should be added between the single-blocks to disconnect the damaged converters if a failure occurs. This option provides redundancy and the required rated power to meet the wind turbine requirements, however, this option does not allow to increase the power density.

To increase the power density another option is integrating the design of all the required power converters in parallel to meet the wind turbine power requirements. In this case the single-block power converter is equal to the required rated power, the power density can be optimized, reducing the output filter with appropriate modulation strategies, but no redundancy can be achieved.

To achieve a compromise between these two alternatives, an interesting option is the selection of a single-block power converter with a rated power of 4 MW, based on two two-level three-phase B2B conversion structures. Only two lines are parallelized to minimize the number of IGBTs, consequently minimizing the possibility of failure. This single-block is optimized and replicated as many times as required to meet the requirements of current wind turbines. By instance, for 8 MW WECS two single-blocks are required and, in case of failure, the wind turbine can still be operated at half power. In this way, the use of a single-block power converter with rated

of 4 MW is aligned with current wind turbines of 8 to 12 MW.

Once the single-block has been established as two 2 MW power converter in parallel, the coupling between them has to be defined. The direct coupling of the B2B power converters, in both GSC and MSC, is a straightforward solution to increase the rated power of both power converters. Nevertheless, as both GSC B2B structures are then forced to switch at the same time instants, no additional benefits can be gained from this coupling, as the grid side output filter cannot be reduced to meet the grid codes. The isolated coupling, requires a transformer with different secondary windings, becoming bulkier. Moreover, in many cases, the power converter manufacturer is not the same one that designs the wind turbine, so he does not decide the transformer to be used in it. For these reasons, the non-isolated inductive coupling becomes the most interesting option to be explored in GSC. Moreover, the grid-side filter can be reduced taking into account the use of interleaving and IPTs. The direct coupling in MSC is the most interesting option, as there is not an harmonic code to fulfill in this side and the machine inductance is sufficient to limit the current harmonics. In MSC the only required filter is the *dv/dt* filter, used to protect the insulation of the machine winding. In this way, the coupling in GSC is inductive and direct in MSC.

The selected topology is represented in Figure 6.22, were it can be seen that the possibility of using a single DC-bus is marked by the dashed lines. In MSC three-phase inductors are depicted, reducing the required magnetic material, while in GSC independent inductors are represented. In GSC three-phase inductors cannot be used, because the homopolar circulating current when interleaving is applied will be only limited by converter leakage inductance. The optimized implementation of the output inductance is considered in Section 6.6.

Finally, to determine if the single block DC-buses should be connected or independent, the equivalent circuits presented in Section 6.3 are used. Supposing that the DC-buses are connected and that MSC is directly coupled, using the three-phase small inductors required by the *dv/dt* filter and represented in Figure 6.22, the equivalent circuit for the homopolar cross-current is obtained and given by Figure 6.23. In this figure $L_{Mconv\ l}$ stands for the leakage inductance of the three-phase inductor, as the homopolar cross-current does not magnetize the core of the three-phase inductor. Even though, in the direct coupling, both MSC power converters are forced to switch at the same instant, the component mismatches in the IGBTs and drivers can force them to switch at different time instants. Let us consider for a moment that MSC1 and MSC2 are using one of the differential vectors with a negative homopolar voltage. At a given instant of time they

are both forced to switch to the positive homopolar voltage vector, but MSC2 makes the transition 1 μs later than MSC1. The voltage across the sum of the two leakage inductances is:

$$v_L = V_{M1_h} - V_{M2_h} = E/6 - (-E/6) = E/3 \tag{6.16}$$

This voltage will generate a significant current spike. For instance, for the *dv/dt* filter of the converter studied in Chapter 4 and Chapter 5, with an inductance of 7 μH and considering the leakage inductance around 10% of the inductor magnetic inductance, $L_{Mconv\ l}$ is 0.7 μH. In this way, considering that the DC-buses are connected, the homopolar cross-current in MSC is given by:

$$i_{Mch} = \frac{v_L}{2L_{Mconv\ l}}\Delta t = 273\ A \tag{6.17}$$

This large circulating current generated in 1 μs could be highly reduced by simply modifying the topology. By making both DC-buses independent the homopolar current-component is also limited by the inductances in GSC, which offer a greater inductance, effectively limiting the homopolar circulating current. From the homopolar circulating current point of view, independent DC-buses are a cost-effective solution, as otherwise an additional core might be added in MSC. Moreover, from the maintenance point of view it is also a more appealing option. If two independent DC-buses are used, in case of failure, only on of them has to be replaced, with a lower capacitance than if a unique DC-bus is implemented.

The MSC differential cross-current is independent of GSC, so the small differences in the switching instants of MSC1 and MSC2, are only limited by

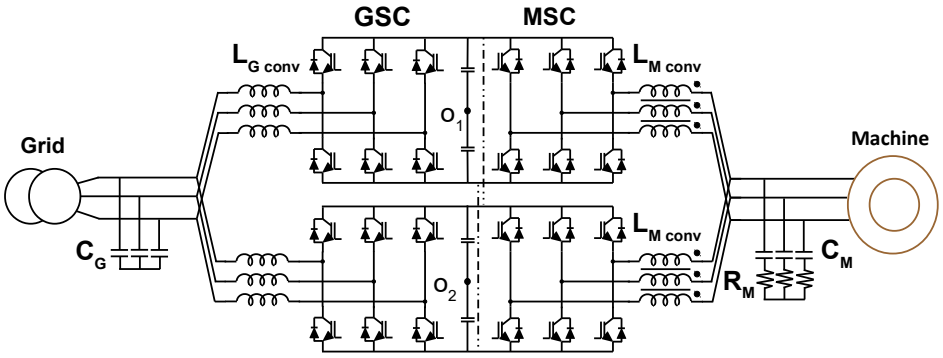


Figure 6.22: Topology of the single-block power converter.

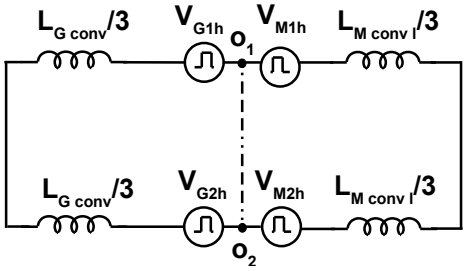


Figure 6.23: Single-block equivalent circuit for the homopolar cross-current.

the three-phase inductors in MSC. However, in this case, as it is a differential current, it magnetizes the three-phase inductor. In this way, if for the same time duration as before, 1 μs, the converters apply different voltages in a given phase, the voltage difference across de inductor is $2E/3$, but the current is limited by two times L_{Mconv}. The circulating current is limited to 53 A, an acceptable current level compared to the rated current.

To sum-up, the selected topology for the single-block power converter is represented in Figure 6.24. It is based on two B2B power converters directly coupled in MSC and with an inductive coupling in GSC. The DC-buses of both B2B power converters are independent.

In the next sections, the most suitable modulation strategy and control strategies for the single-block conversion structure are analyzed. Once the desired modulation has been determined, its influence on the design of the passive components is faced in Section 6.6.

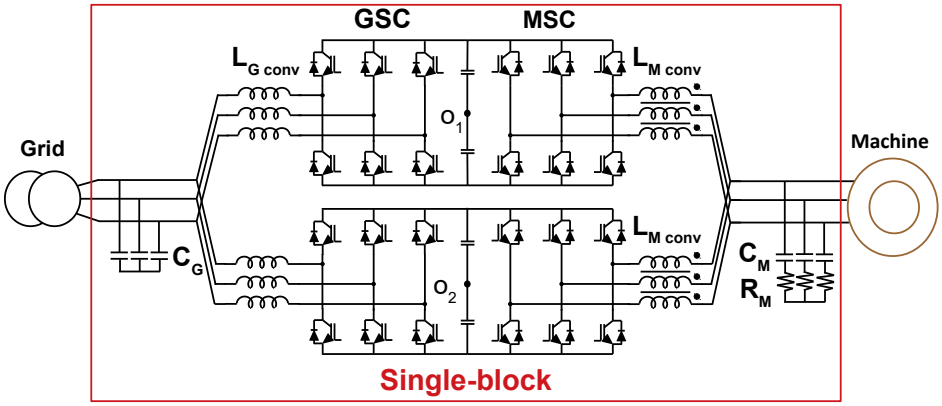


Figure 6.24: Selected topology for the single-block power converter.

6.5 Modulation techniques to increase the efficiency for the single-block conversion structure

In this section, the influence of the modulation on the key aspects of the power converter, such as efficiency, grid-code compliance, phase-to-ground and common-mode voltages, DC-bus rms current and its effect on the inductive coupling are analyzed in detail.

6.5.1 Efficiency

The efficiency of the single-block power converter is one of the most important aspects. However, the improvement of the efficiency must not introduce limitations to the grid-code compliance, the phase-to-ground and common-mode voltages, as well as higher size and cost in other passive components such as the inductive coupling between the GSCs.

From the efficiency point of view, DSVPWMs offer important benefits compared to the use of SVPWM7. With DSVPWM3 the commutations per converter and switching period are reduced from 6, with SVPWM7, to 4, meaning that the switching power losses can be reduced by a 33%. With the GDSVPWM an additional benefit can be obtained: as the converter leg with the maximum current is not switched, an additional reduction in the switching power losses is obtained reaching up to a 50% reduction [HAV98]. The implementation of both modulations can be seen in Figure 6.25, where the blue areas indicate the region where the positive zero vector, v_7, has to be applied and the red areas where the negative zero vector, v_0 is used.

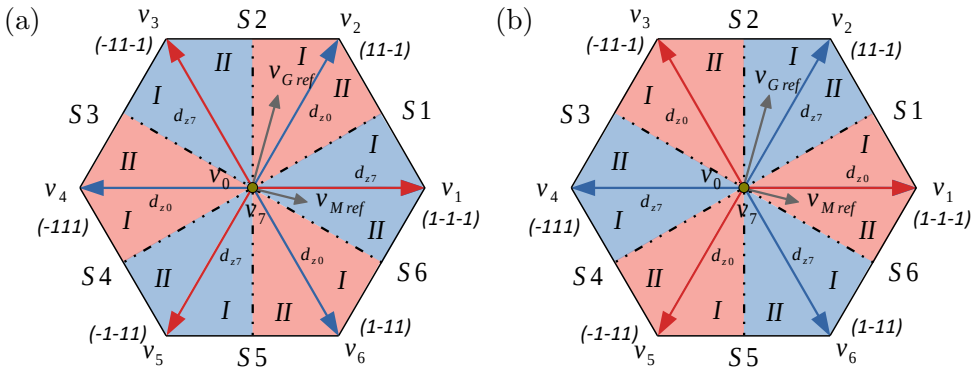


Figure 6.25: Implementation of the GDSVPWM with unity power factor (a) and DSVPWM3 (b).

In Chapter 5 the benefits of these modulations on the B2B conversion structure, with the proposed modifications, were demonstrated. In the following, the performance of these modulations in the single-block conversion structure is evaluated to determine the most suitable modulation. The three modulations: SVPWM7, DSVPWM3 and GDSVPWM are going to be evaluated. As the reduction of the power losses with these modulations have been already demonstrated in the existing literature, in the next section, the influence of the modulation index and the angle of interleaving on the differential-mode voltages that determine the grid-current harmonic content are analyzed.

6.5.2 Differential-mode voltages in the grid-side converter

The grid codes impose limitations on the grid current harmonic content. The injected harmonic content is determined by the differential voltage introduced by the power converter and the converter output filter.

In order to properly compare the different modulation strategies for parallel power converters and decide the best interleaving angle for each modulation, a figure of merit is required. An inductor is normally at the output of the converter, in order to control the current. In this way, the voltage harmonics with a greater frequency have a lower weight in the output current harmonic content. Traditionally, the total harmonic distortion, or THD, has been used to evaluate the output voltage quality, which is given by [HOL03]:

$$THD = \sqrt{\left(\frac{2V_0}{V1}\right)^2 + \sum_{n=2,3,\ldots}^{\infty}\left(\frac{V_n}{V_1}\right)^2} \tag{6.18}$$

where V_0 is the DC-value, V_1 is the amplitude of the fundamental value and V_n the amplitude of the nth harmonic. However, the THD is not an effective indicator to compare different modulations, as it only takes into account the value of each harmonic. In this way, different waves with similar harmonic magnitudes located at completely different frequencies, can have similar THD values [HOL03]. A different indicator that also takes into account the frequency of each harmonic is the weighted total harmonic distortion, WTHD. It is a more adequate figure of merit because higher order harmonics will have a lower contribution to the total WTHD.

The formula for the WTHD, considering that no DC-component is introduced by the modulation, something that can be guaranteed through

the control strategy, is given by:

$$WTHD = \frac{\sqrt{\sum_{n=2}^{\infty} \left(\frac{V_n}{n}\right)^2}}{V_1} \tag{6.19}$$

This figure of merit is computed for each modulation strategy, making a swept to different modulation indexes and interleaving angles. It is calculated for the normal voltage, as it is the one that has an impact on the grid-code compliance. The 3-D plot obtained from the representation of the WTHD against the interleaving angle, δ, and the modulation index, m, can be found in Figure 6.26 for the SVPWM7. In this figure it can be verified that with the SVPWM7 and high modulation indexes, an interleaving angle of 180 degrees minimizes the WTHD. However, at lower modulation indexes, the optimal interleaving angle is obtained for a δ equal to 105 degrees. These results agree with the ones presented in [PRA14].

If the weighted total harmonic distortion is calculated for the GDSVPWM, and represented in a 3-D plot as in the case of the SVPWM7, Figure 6.27 is obtained. As expected, with the GDSVPWM at low modulation indexes, the performance of the modulation becomes poorer. As the modulation index is increased, the distortion is reduced, being minimal with an interleaving angle of 180 degrees. With a high modulation index and an angle δ equal to 180 degrees, this modulation strategy becomes competitive with the SVPWM7 for two parallel interleaved power converters.

The same procedure is performed for the DSVPWM3, which proved in Chapter 5 to be an interesting option for B2B power converters, plotting the results in Figure 6.28. An interleaving angle of 180 degrees provides the lowest WTHD for the whole possible range of modulation indexes. As in the previous case, where the GDSVPWM was used, at low modulation indexes the WTHD is highly increased.

The determination of the most suitable modulation in terms of the total weighted distortion is not obvious from Figures 6.26-6.28. For this reason, the contour lines at a modulation index of 1.1 are represented in Figure 6.29. When the contour lines are visualized in the same plot, representing the WTHD as a function of the interleaving angle for a constant modulation index, an insight can be gained to the benefits of each modulation. In the case of two parallel interleaved power converters, the GDSVPWM provides, with an interleaving angle of 180 degree, the lowest WTHD for a modulation index of 1.1. This is a really interesting option, because this modulation is the one with the lowest switching losses.

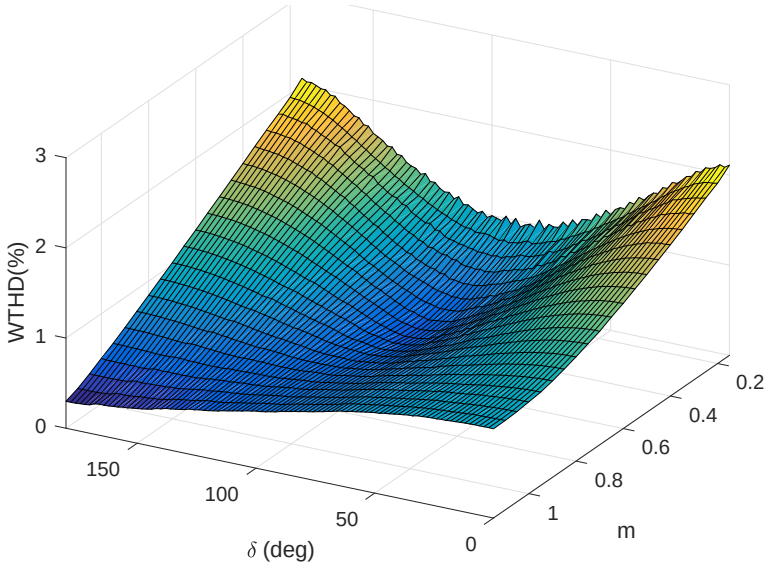


Figure 6.26: WTHD for the SVPWM7 as a function of the interleaving angle and the modulation index.

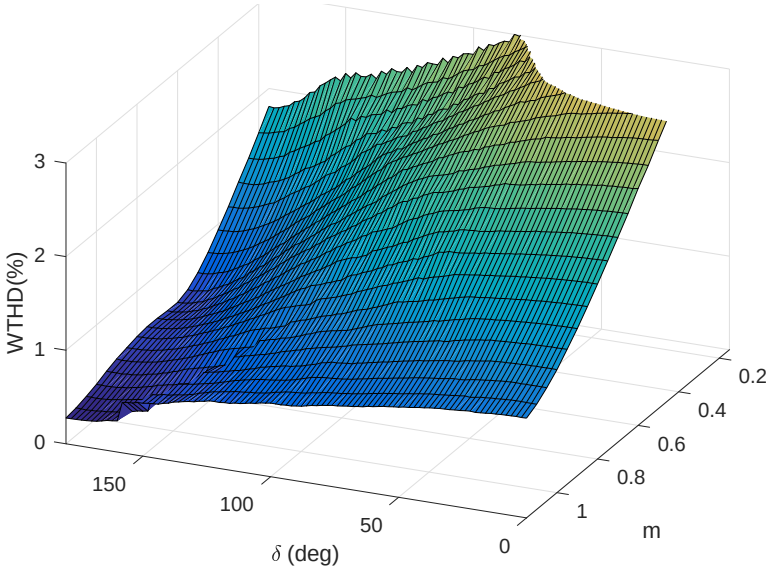


Figure 6.27: WTHD for the GDSVPWM as a function of the interleaving angle and the modulation index.

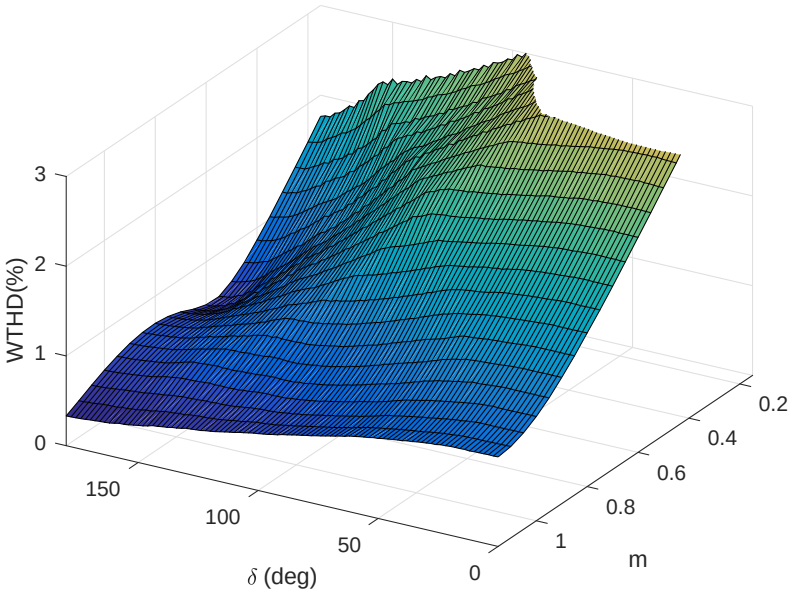


Figure 6.28: WTHD for the DSVPWM3 as a function of the interleaving angle and the modulation index.

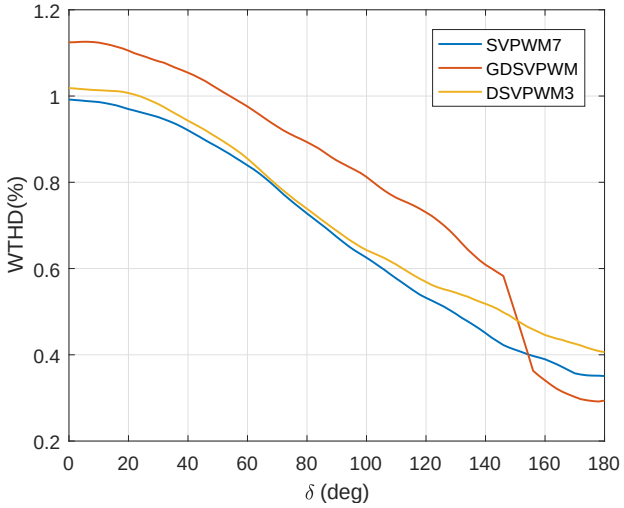


Figure 6.29: Comparison of the WTHD as a function of the interleaving angle for a modulation index of 1.1.

Grid-connected power converters work with modulation indexes that do not suffer strong variations and are usually between 1 and 1.15. For this reason, the GDSVPWM seems the best option for the system under study. If this modulation is used in the four power converters (considering GSC and MSC), the switching losses will be reduced by a 50%.

To select this modulation for the four power converters that form the single-block conversion structure, it does not have to be superior only in terms of the grid-code compliance and efficiency. This superiority has to be accompanied by an adequate performance in terms of the phase-to-ground and common-mode voltages, DC-bus current ripple and it cannot imply a bulkier IPT that cancels the benefits of the reduced *LCL* output filter. In the following, these aspects are analyzed.

6.5.3 Common-mode and phase-to-ground voltages

The common-mode and phase-to-ground voltages have been studied in Chapter 5 for a single back-to-back power converter. In this case, the system is formed by two parallel power converters, applying interleaving between both GSC power converters, while MSC1 and MSC2 are simultaneously switched. Consequently, the model and worst case situations in both the common-mode and the phase-to-ground voltages vary and have to be redefined in this section.

The common-mode voltage model can be derived from the homopolar cross-current model derived in Figure 6.13. If in this model the ground connection and the inductance offered by the transformer to the ground current is drawn, the representation in Figure 6.30 is obtained. L_{transf} is the transformer leakage inductance, $L_{G\ conv\ h}$ is the inductance offered to the homopolar component by the inductive coupling of GSC. Lastly, $L_{M\ conv\ l}$ is the leakage inductance of the *dv/dt* filter of MSC.

As the common-mode current flows through parasitic capacitances, the resonance between these small capacitances and the inductances create high frequency transients. Once this transients have been attenuated, the common-mode voltage in steady-state is given by the difference between the homopolar voltages of MSC and GSC:

$$V_{CM} = \frac{(V_{M1_h} + V_{M2_h}) - (V_{G1_h} + V_{G2_h})}{2} \tag{6.20}$$

In MSC both power converters use synchronous switching, so the common-

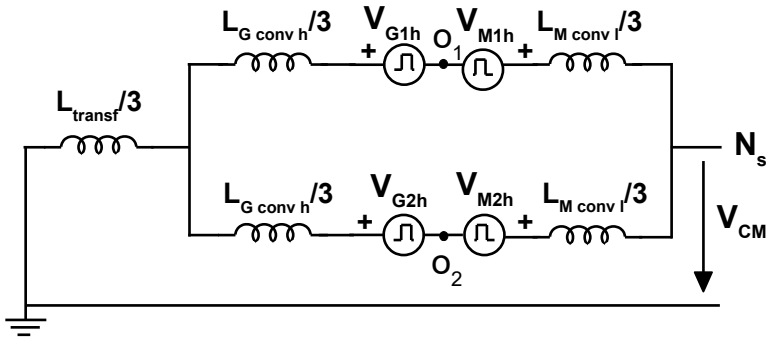


Figure 6.30: Common-mode model.

mode voltage can be rewritten as:

$$V_{CM} = V_{M1_h} - \frac{V_{G1_h} + V_{G2_h}}{2} \tag{6.21}$$

The model for the phase-to-ground voltage in phase i is represented in Figure 6.31. It should be noted that V_{M1_i} are the phase voltages of MSC.

In this way, in steady state, the phase-to-ground voltage depends on the homopolar voltage in GSC and the voltage imposed in phase i by MSC:

$$V_{PG:i} = \frac{(V_{M1_i} + V_{M2_i}) - (V_{G1_h} + V_{G2_h})}{2} \tag{6.22}$$

Knowing that MSC1 and MSC2 always switch at the same time instants,

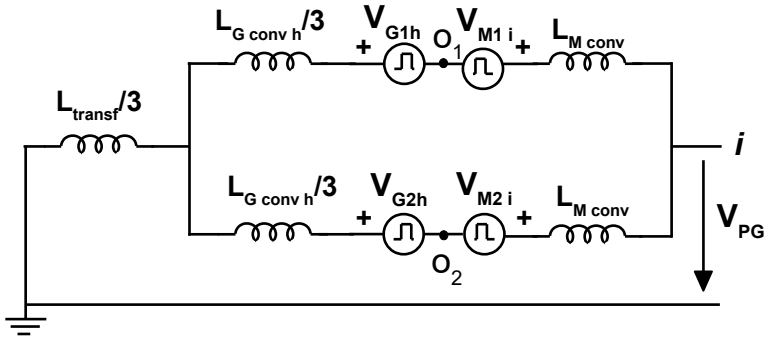


Figure 6.31: Phase-to-ground model.

this equation can be rewritten as:

$$V_{PG_i} = V_{M1_i} - \frac{V_{G1_h} + V_{G2_h}}{2} \tag{6.23}$$

Once the models have been derived, the influence that the modulation used, in both GSC and MSC, has on V_{CM} and V_{PG_i} is analyzed. In the following it is going to be demonstrated that the use of SVPWM7 offers a slightly reduced common-mode and phase-to-ground voltages. The performance of this modulation in the single-block power converter is compared to the one of the GDSVPWM, as it is the one with the best efficiency and differential harmonic content for two paralleled interleave power converters. The DSVPWM3 has been discarded, as the normal voltage has a greater harmonic content than the GDSVPWM with greater losses. Nevertheless this modulation has the same performance in terms of CM and PG voltages than the GDSVPWM.

6.5.3.1 SVPWM7

If the SVPWM7 is used in the four power converters, the worst case in the phase-to-ground and common-mode voltages for the parallel power converters are equal to the ones with a single B2B conversion structure.

As shown in Figure 6.32, the opposite zero vectors always coexist in GSC1 and GSC2, as a result of the application of interleaving. When this occurs, the common-mode voltage is equal to:

$$V_{CM} = V_{M1_h} \tag{6.24}$$

So when GSC uses the zero vector, the worst possible case in the common-mode voltage is ±E/2, which happens when MSC is using a zero vector. However, this is not the worst case for the common-mode voltage. The highest voltage peak is obtained when the same differential vector coexist in GSC1 and GSC2 with a zero vector, with opposite homopolar voltage in MSC. Under these circumstances, the common-mode voltage is equal to:

$$V_{CM\ wc} = V_{M1_h} - \frac{V_{G1_h} + V_{G2_h}}{2} = \pm\frac{2E}{3} \tag{6.25}$$

For the phase-to-ground voltage, a similar reasoning procedure can be followed in order to derive the worst case. When the zero vectors are applied

in GSC, they cancel each other, so the phase to ground voltage is given by:

$$V_{PG_i} = V_{M1_i} = \pm\frac{E}{2} \tag{6.26}$$

However, a higher phase-to-ground voltage, which is obtained whenever the same differential vector coexist in GSC1 and GSC2 with an opposite leg voltage in MSC.

$$V_{PG\ wc_i} = V_{M1_i} - \frac{V_{G1_h} + V_{G2_h}}{2} = \pm\frac{2E}{3} \tag{6.27}$$

In this way, in parallel interleaved power converters, the peaks in V_{CM} and V_{PG} are $\pm 2E/3$, the same values than for a single B2B power converter. For full-converter topologies, the study of the implementation of modulations to reduce the common-mode peak to $\pm E/3$ is not a key aspect. As shown in Table 6.1, most offshore wind turbines use a PMG generator. This means that the power converter is connected to the stator and the common-mode voltage is divided among the capacitance between the stator and the rotor and the capacitance of the rotor to ground through the bearing. The capacitance between the stator and the rotor is smaller and consequently it offers a greater impedance and withstand the majority of the common-mode voltage. For this reason, in full-converter applications bearing currents are not as problematic as in DFIG wind turbines. For this reason, CMVR techniques are not explored for SVPWM7 in parallel power converters.

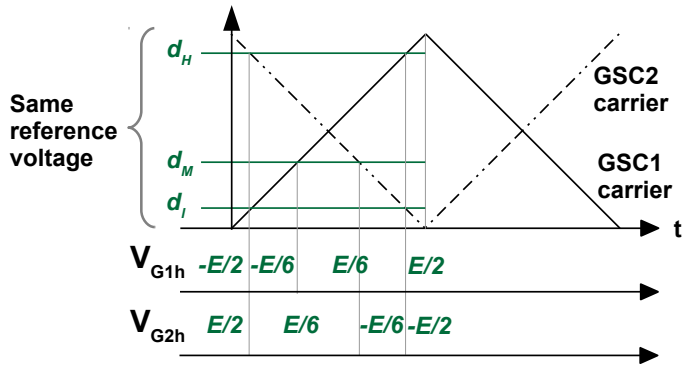


Figure 6.32: Homopolar voltages with interleaving and SVPWM7 in GSC.

6.5.3.2 DSVPWM

Even though the preferred modulation for parallel interleaved power converters is the GDSVPWM, the analysis performed will be also valid for the DSVPWM3. For this reason, it is performed in a general approach valid for any DSVPWM. As represented in Figure 6.33, with DSVPWM and interleaving, in GSC both zero vectors do not match and consequently, a zero vector of GSC2 matches a differential vector of GSC1, and vice-versa. Whenever GSC1 uses the zero vector and GSC2 a differential vector with the same homopolar voltage, the highest peak in V_{CM} can be obtained if MSC is using the opposite zero vector. Under these circumstances:

$$V_{CM\ wc} = V_{M1_h} - \frac{V_{G1_h} + V_{G2_h}}{2} = -\frac{E}{2} - \left(\frac{E/2 + E/6}{2}\right) = -\frac{5E}{6} \tag{6.28}$$

Similarly, the peak of $+5E/6$ is obtained. So in general, V_{CM} oscillates with peaks equal to $\pm$5E/6, a 16% higher that with SVPWM7. Under the same situation in GSC, a zero vector in one of the converters with a differential vector that has the same sign in the common mode in the other converter, creates the worst case in the phase-to-ground voltage:

$$V_{PG\ wc_i} = V_{M1_i} - \frac{V_{G1_h} + V_{G2_h}}{2} = \pm\frac{5E}{6} \tag{6.29}$$

Both V_{CM} and V_{PG} are increased by a 16% if compared to the SVPWM7. Again, the higher CM voltages are not critical, but higher PG voltages might not be allowed by the wind generator manufacturer, to prevent early insulation failures. In these cases, with DSVPWM the phase-to-ground voltages can be reduced if an inductive coupling is also used in MSC and both power converters

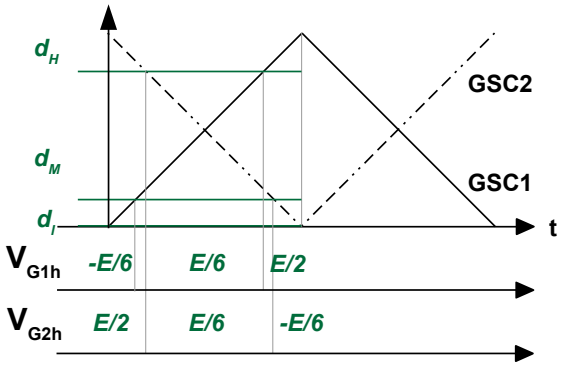


Figure 6.33: Homopolar voltages with interleaving and DSVPWM in GSC.

can be modulated independently. In this way, as proposed in Chapter 5, MSC1 can be forced to use the same zero vector than GSC1 and MSC2 to use the same one than GSC2, keeping the benefits of the DSVPWMs.

The common-mode voltage fo DSVPWM could be reduced, using the modulations in MSC that do not use the zero vectors, something that is analyzed in the following subsection.

Nevertheless, as a conclusion, the 16% increase in the CM and PG voltages is not considered critical, so the GDSVPWM is still the preferred modulation for the single-block power converter due to the high improvement in the efficiency.

6.5.3.3 Reduction of the common-mode voltage for DSVPWMs

A reduction in the common-mode voltage can be achieved when DSVPWMs are used in GSC, by modifying the modulation in MSC. If instead of using DSVPWM in MSC as well as in GSC, one the modulations which does not use the zero vectors is implemented, the worst case in V_{CM} can be avoided. These modulations are active zero SVPWM (AZSVPWM), remote state SVPWM (RSSVPWM) and near state SVPWM (NSSVPWM). Both RSSVPWM and NSSVPWM have restrictions in the modulation index, so they are not applicable to MSC, where the modulation index can vary from 0 to 1.15. For this reason, AZSVPWM [LAI04b, LAI04a] is the preferred option to be used in MSC if a voltage reduction in V_{CM} is required.

In this modulation, instead of using the zero vectors at the beginning and at the end of every sampling period, two opposite zero vectors are used during the same time, so their differential voltage net contribution is zero. As an example, in Figure 6.34 the implementation of the AZSVPWM is shown when the reference is located in the first sector. In this case the vector sequence is given by:

$$v_6 \rightarrow v_1 \rightarrow v_2 \rightarrow v_3 \rightarrow v_2 \rightarrow v_1 \rightarrow v_6 \tag{6.30}$$

where v_6 and v_3 are used during the same amount of time to avoid any contribution to the reference vector $v_{M\ ref}$. It can be seen that only one converter leg switches at any transition, so the switching power losses are equal to the ones in SVPWM7.

In the rest of the sectors, the vector sequences are also defined in a similar way, so that only one branch switches at any time, they are given for a half of the switching period by:

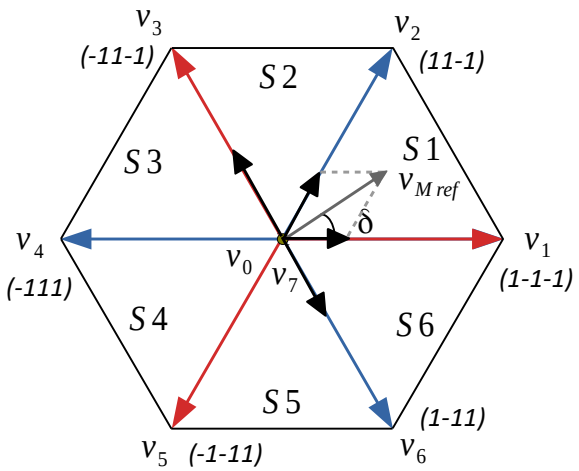


Figure 6.34: Space vector implementation of AZSVPWM.

$$S2 : v_4 \rightarrow v_3 \rightarrow v_2 \rightarrow v_1$$

$$S3 : v_2 \rightarrow v_3 \rightarrow v_4 \rightarrow v_5$$

$$S4 : v_6 \rightarrow v_5 \rightarrow v_4 \rightarrow v_3$$

$$S5 : v_4 \rightarrow v_5 \rightarrow v_6 \rightarrow v_1$$

$$S6 : v_2 \rightarrow v_1 \rightarrow v_6 \rightarrow v_5$$

In this way, if the common-mode voltage is represented for the sequence used in the AZSVPWM, it can be seen that the homopolar voltages oscillates between ±E/6 for a single power converter, Figure 6.35.

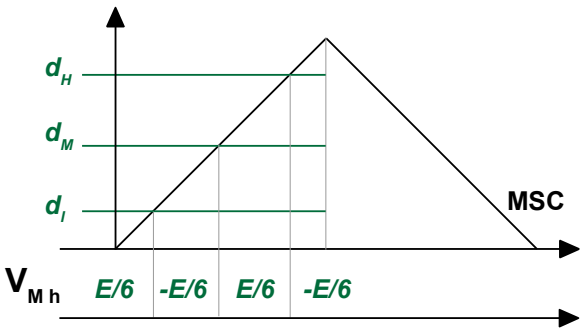


Figure 6.35: Homopolar voltage with AZSVPWM.

The worst case in the common-mode voltage with DSVPWM in GSC1 and GSC2 combined with interleaving, and AZSVPWM in MSC with synchronous switching, occurs when GSC1 uses the zero vector and GSC2 a differential vector with opposite common-mode. In this case, if this homopolar voltage in GSC matches a differential vector in MSC, the peak voltage is given by:

$$V_{CM\ wc} = V_{M1_h} - \frac{V_{G1_h} + V_{G2_h}}{2} = -\frac{E}{6} - \left(\frac{E/2 + E/6}{2}\right) = -\frac{E}{2} \qquad (6.31)$$

With this modulations, the maximum peak-to-peak in the common-mode voltage is bounded by ±E/2. This is a reduction of E/3 if compared to the use of GDSVPWM. As a drawback, the power losses are increased for two reasons: the leg with the highest current is forced to switch and two additional commutations are added every sampling in each MSC if compared with the GDSVPWM. Moreover, in MSC the current harmonic content is increased with the AZSVPM [HAV09]. So the application of this technique is only justified if the common-mode voltage is a key aspect in a given wind turbine.

If the performance of this alternative, GDSVPWM in GSC and AZSVPWM in MSC, is compared to the use of SVPWM7, the common-mode voltage is also reduced: from ±2E/3 with SVPWM7 to ±E/2, a reduction of E/6. However, the proposed alternative is not able to reduce the phase-to-ground voltage, which is kept at ±5E/6, greater than with SVPWM7. The same will occur with the RSSVPWM and the NSSVPWM. In this way, increasing the power losses to reduce the common-mode voltages while keeping the phase-to-ground voltages at the same level is not justified.

6.5.3.4 Validation through simulation of the common-mode and phase-to-ground voltages

To validate the calculations performed and the proposed alternative to reduce the common-mode voltage for the single-block power converter with interleaving and GDSVPWWM in GSC, simulations of the overall conversion stage are performed in Matlab. In these simulations, the performance of the power converter in terms of common-mode voltage, phase-to-ground voltage and harmonic quality in MSC is performed for the three alternatives studied:

- SVPWM7 with interleaving in GSC and synchronous switching in MSC.
- GDSVPWM with interleaving in GSC and synchronous switching in MSC.

- GDSVPWM with interleaving in GSC and AZSVPWM with synchronous switching in MSC.

The simulation results are presented in Figure 6.36. In Figure 6.36 (a) the common-mode and phase-to-ground voltages are represented for the SVPWM7 in both GSC and MSC. It can be seen that the maximum peak in both is bounded by ±2E/3. If the GDSVPWM is used in the whole single-block power converter structure, the peaks are increased, bounded by ±5E/6 as represented in Figure 6.36 (b). To reduce the common-mode peaks, the AZSVPWM is implemented in MSC, keeping in GSC the

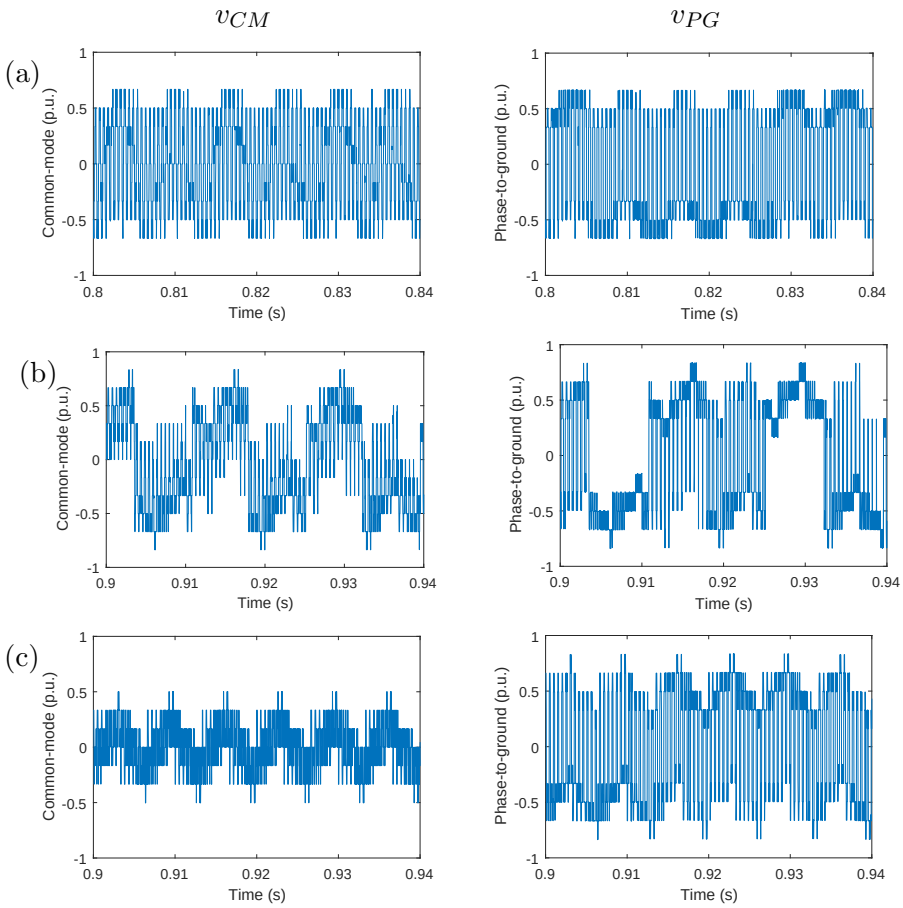


Figure 6.36: Comparison of the common-mode and phase-to-ground voltages normalized with respect to the DC-bus voltage for: SVPWM7 in both GSC and MSC (a), GDSVPWM in both GSC and MSC (b) and GDSVPWM is GSC and AZSVPWM in MSC (c).

GDSVPWM with interleaving. As it is shown in Figure 6.36 (c), the peaks in the common-mode are reduced to ±E/2. However, as already studied theoretically, the phase-to-ground voltage remains with the same maximum peaks. These simulations confirm the results obtained in the theoretical analysis, validating the proposed approach to reduce the common-mode voltage.

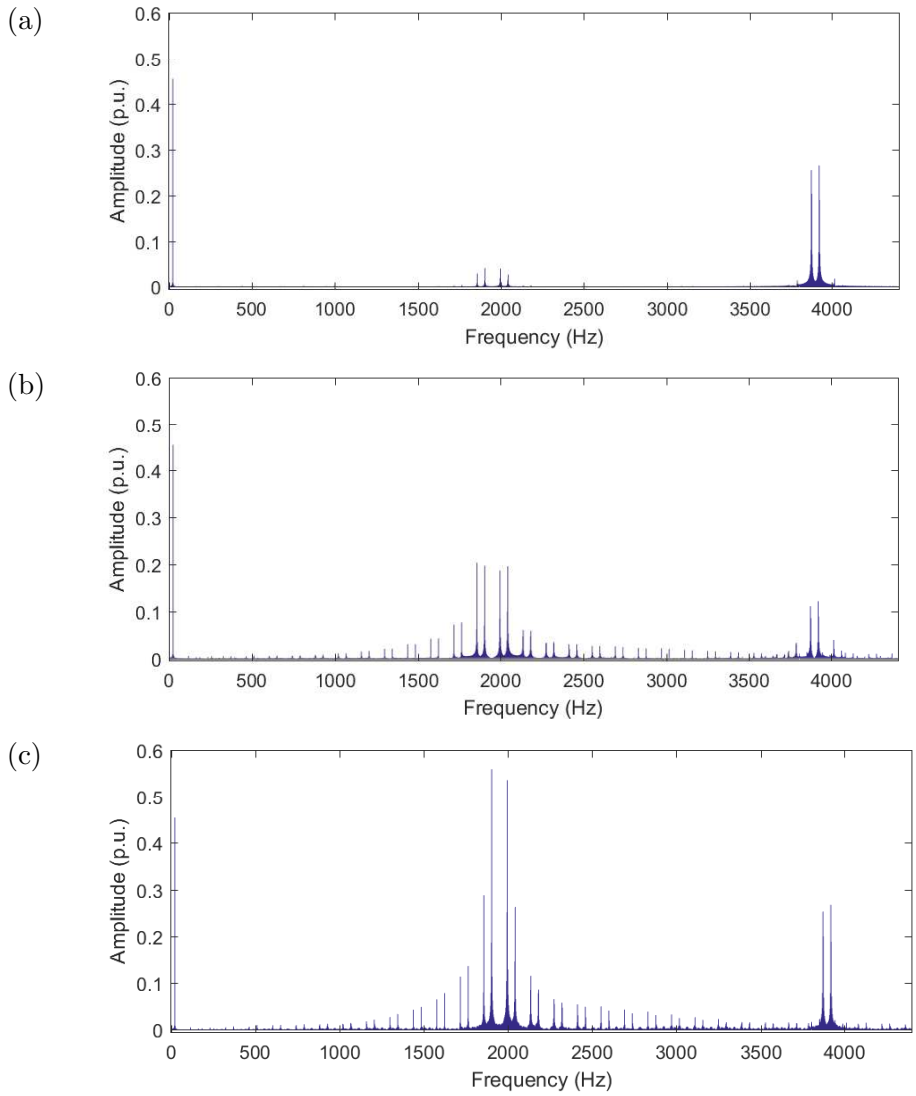


Figure 6.37: MSC differential voltage normalized with respect to the DC-bus voltage for: SVPWM7 (a), GDSVPWM (b) and AZSVPWM (c).

To conclude this study, the differential voltage in MSC is analyzed, to evaluate the increase in the harmonic content in MSC caused by the use AZSVPWM and GDSVPWM with synchronous switching if compared with the SVPWM7. The harmonic content is represented in Figure 6.37 for a modulation index of 0.4. With the AZSVPWM a significantly greater harmonic content is obtained. Again, the use of AZSVPWM, and any other of the modulations that do not use a zero vector, damages the differential harmonic content in MSC, another inconvenient to add up to the grater losses than the DSVPWMs while they present the same PG peaks. As a conclusion, the GDSVPWM with interleaving in GSC and synchronous switching in MSC is used.

6.5.4 DC-bus current ripple

The effect of the modulation used in the DC-bus current ripple is performed by simulating the system for the SVPWM7 and GDSVPWM with the application of interleaving in GSC and without its application. The simulations are performed at rated power, when the DC-current is maximum. The rms value of the DC-current ripple is calculated by summing the harmonic rms value for the first 200 harmonics:

$$I_{DC\ rms} = \sqrt{\sum_{n=1}^{200} I_{n\ rms}^2} \tag{6.32}$$

The calculated harmonic content is normalized with respect to the single-block rated current.

The DC-ripple is calculated for the four cases under consideration and represented in Figure 6.38. As it can be seen at a glance in Figure 6.38, the modulation SVPWM7 creates less ripple in the DC-bus than the GDSVPWM. However, the implementation of interleaving with an angle of 180 degrees in GSC offers the possibility of reducing the differences between both modulations. With an interleaving angle of 180 degrees in GSC, the modulation GDSVPWM presents a normalized current rms value of 21.4%, while the SVPWM7 offers a 17%.

6.5.5 Influence on the inductive coupling of GSC

The GDSVPWM presents some benefits when combined with interleaving from the normal voltage component point of view. However, in this section, the

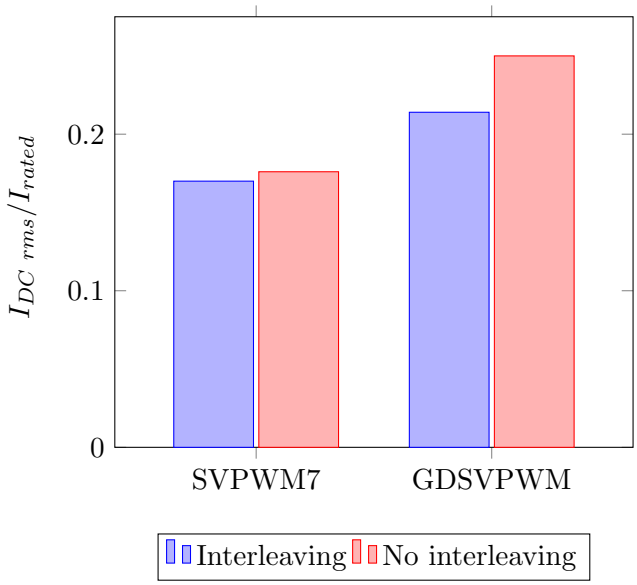


Figure 6.38: DC-bus current ripple comparison for SVPWM7 and GDSVPWM with and without interleaving in GSC.

influence of the modulation on the inductive element used to couple both power converters is studied. The main goal is to verify whether a greater inductance value is required by the GDSVPWM, compared to the SVPWM7, resulting in a bulkier inductor.

According to the analysis performed in Subsection 6.3.1 the inductive coupling between the power converters in GSC is responsible of limiting the cross-current between the power converters. It must filter the harmonics created by the difference of the homopolar voltages, V_{G_h}, and the differential cross-voltages, V_{Gcd_i}, introduced by both GSCs across the inductive coupling as a result of the application of interleaving. These components are defined as:

$$V_{G_h} = V_{G1_h} - V_{G2_h} \tag{6.33}$$

$$V_{Gcd_i} = V_{G1d_i} - V_{G2d_i} \tag{6.34}$$

Due to the synchronous switching in MSC, its homopolar voltages do not appear in Equation 6.33.

In grid-connected power converters the modulation index does not vary significantly. It normally has a value close to 1.1 and for this reason, the IPT

is designed to limit the cross-current that is created by the cross voltages introduced at this modulation index. This design approach is also used in [GOH16]. The harmonic content of the homopolar voltage and the differential cross-voltage is represented in Figure 6.39 and Figure 6.40 for the GDSVPWM and SVPWM7 with a modulation index of 1.1 and a swittching frequency of 1950 Hz. The SVPWM7 has a greater harmonic content in the homopolar cross-voltage than the GDSVPWM. Nevertheless, the GDSVPWM has a greater differential cross-voltage harmonic content.

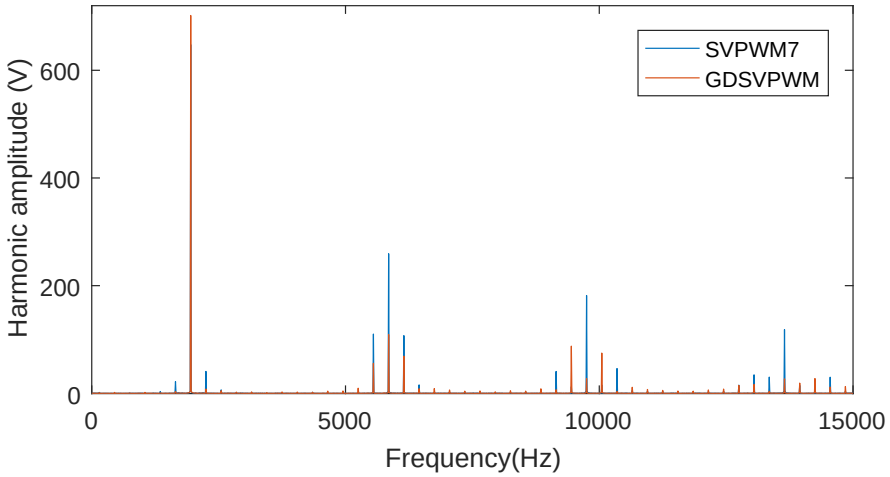


Figure 6.39: Homopolar cross-voltage with GDSVPWM and SVPWM7.

The inductive coupling is not designed to limit each individual harmonic component, as in the case of the output LCL filter, it is designed to reduce the peak of the cross-current. The worst case for the design of the inductive coupling is when each power converter applies only two different vectors during half of the sampling period. This occurs, for example, when the modulation index is 1.15 (at the end of the linear modulation region) every 60 degrees, at the bisector of each sector of the modulation hexagon. In this case, the voltage across the inductive coupling in one of the phases is equal to the whole DC-bus voltage, E, during this half of the sampling period, T_{samp}. If the maximum peak in the cross-current, Δi_{Gc}, is restricted to be 0.4 p.u. peak-to-peak, the required cross-inductance, L_{cross} can be calculated:

$$L_{cross} = \frac{ET_{samp}}{2\Delta i_{Gc}} = \frac{E}{F_{sw}\Delta i_{Gc}} \tag{6.35}$$

Considering a switching frequency equal to 1950Z Hz, the required inductor is 737 μH. The required inductance is too high to use independent inductors

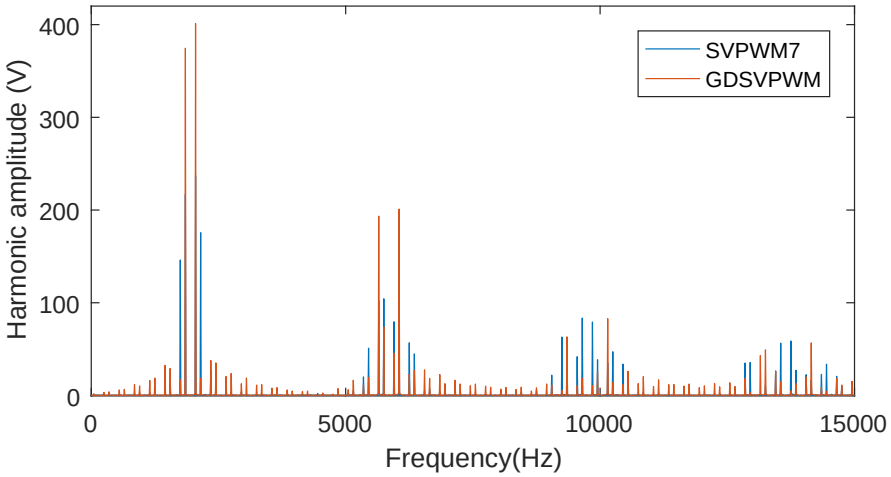


Figure 6.40: Differential cross-voltage with GDSVPWM and SVPWM7.

or three-phase four-limb inductors to limit the circulating current. With these options the fundamental component will also magnetize the inductor and a really bulky inductor would be required. For this reason, the use of interphase-transformers (IPT) is a preferred solution. The discussion on suitable IPTs for the single-block power converter is discussed in Subsection 6.6.2.

6.5.6 Proposed implementation of DSVPWMs

To conclude this subsection, in which the influence of the modulation on the topology and passive components is analyzed, the implementation of DSVPWM in parallel interleaved power converters is discussed. Up to this moment, DSVPWMs have been used for the sinle-block power converter, supposing that it is properly programmed. This implementation is not trivial and some papers have been focused on this issue [XIN99b, ZHA11b]. If no considerations are taken when these modulations are programmed, unexpectedly high cross-homopolar current components may appear. The previously performed analysis, has revealed that the GDSVPWM is the most interesting option for the singe-block. The implementation of this modulation is performed as indicated in this subsection, an approach that is valid for any other DSVPWM.

One of the main practical problems with DSVPWM is that, depending on the required reference vectors in GSC1 and GSC2, different zero vector might be applied in both power converters, as represented in Figure 6.41.

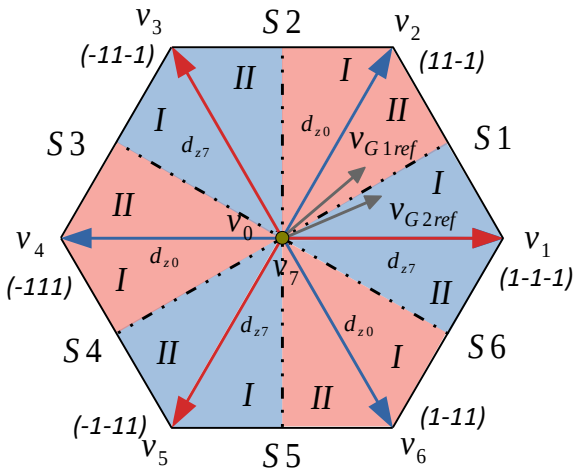


Figure 6.41: Reference voltages of GSC1 and GSC2.

Under this circumstance, an homopolar low frequency component appears between both power converters. This homopolar current will either saturate the inductive coupling between both GSC power converters, if it is not taken into account in the design stage, or will force to over-dimension the inter-phase transformer that can be used for the inductive coupling. To solve this issue, [XIN99b] proposed a modulation that does not uses the zero vectors. A different solution is provided in [ZHA11b]. In this paper they modified the switching orders whenever GSC1 and GSC2 are applying different zero vectors. The modification is made in one of the power converters, using both zero vectors whenever different zero vectors coexist. In this way, two additional switching orders are introduced, increasing the power losses. The implementation of this strategy is represented in Figure 6.42 and Figure 6.43. In Figure 6.42 the initial situation is represented, when GSC1 and GSC2 change the zero vector at different time instants, during each sampling period the zero vectors of GSC1 and GSC2 are different and a net homopolar voltage component is introduced that drives an homopolar circulating current. As represented in Figure 6.43, when this transition occurs, GSC1 uses both zero vectors. Avoiding the coexistence of both opposite zero vectors.

In this thesis a different implementation is proposed. Instead of adding additional commutations to the DSVPWM, a master slave implementation of the DSVPWM is proposed that requires no additional commutations while it still avoids the coincidence of different zero vectors in GSC1 and GSC2. To achieve these goals, each power converter calculates its reference vector

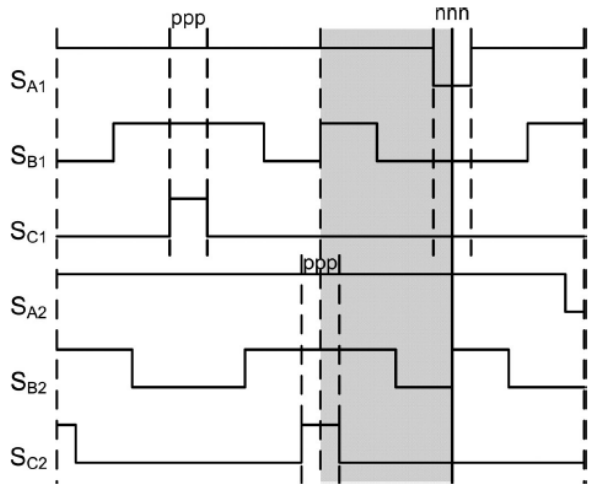


Figure 6.42: Switching orders of GSC1 and GSC2 when the reference vectors change the zero vector at different time instants [ZHA11b].

and the duty cycles during which each vector has to be applied: both adjacent differential vectors and the zero vector. However, only GSC1 determines which zero vector should be used in each sampling period, so GSC1 is the Master in this strategy. This zero vector is also used in GSC2, the Slave in this implementation. In this way, when the transition occurs at different time instant in both power converters, the application of the same zero vectors

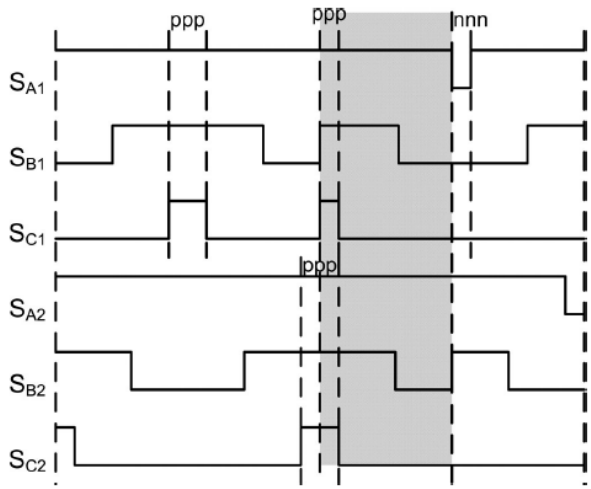


Figure 6.43: Switching orders of GSC1 and GSC2 when the reference vectors change the zero vector at different time instants and the correction in [ZHA11b] is used.

in both GSC1 and GSC2 is guaranteed for every sampling period without additional switching losses. This implementation is represented in Figure 6.44 for the situation represented in Figure 6.41, where the reference vector of GSC1 changes earlier than GSC2. GSC1 starts to use the zero negative vector before then GSC2. However, the second converter is forced to make the transition at the same sampling interval with the master-slave implementation, so according to the representation in Figure 6.44 no homopolar current offsets are created.

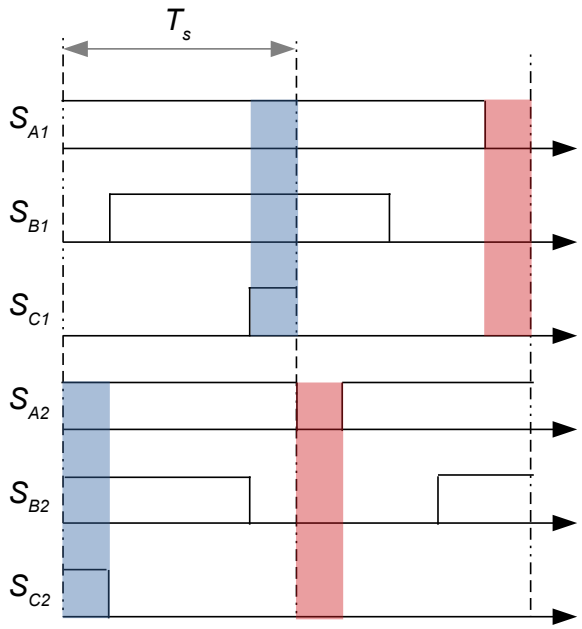


Figure 6.44: Switching orders of GSC1 and GSC2 when the reference vectors change the zero vector at different time instants and proposed master-slave implementation is used.

6.6 Design of the passive components

6.6.1 Design of the output *LCL* filter

In this section, a systematic design procedure for the output filter is presented and applied to the single-block power converter. The design procedure of the output filter is made into three steps:

- Step 1: Determination of the filter design inputs: normal voltage harmonic content and grid-code current limits.

In the first step the harmonic content of the normal voltage is calculated for the modulation used in the single-block power converter. The normal voltage is the one driving the normal current, the current flowing to the grid, for this reason, characterizing this voltage is an important aspect. The normal voltage harmonics vary with the modulation index. However, under normal operation, the grid-connected power converter is operated at modulation indexes between 1 and 1.15. In this way, the harmonic content of the normal voltage in this range of frequencies will be analyzed to determine the worst case for the design.

The second input are the limits imposed to the injected grid current harmonic content. The grid-codes normally impose limitations on the individual harmonics and the interharmonics. The specific limits depend on the grid code and the grid at which the power converter is connected.

- Step 2: Calculation of the admittance limit and selection of the filter topology.

  By computing for each harmonic the coefficient between the limit imposed by the selected grid code and the normal voltage, the maximum limit of the output filter admittance can be obtained. With the admittance limit as a function of frequency, a proper filtering topology can be selected. The most common one is the LCL filter, followed by the trap filter.

- Step 3: Selection of the filter components.

  In this step the filter components are selected. This selection is made taking into account the converter maximum ripple, the reactive energy consumption and the energy density of the different components. For the classical LCL filter, this step will be divided into two parts, the selection of filter capacitor and the selection of the converter inductor, as the grid inductance is provided by the transformer leakage inductance and the grid inductance. Once those filter components are selected in this step, the compliance with the calculated maximum admittance limit has to be verified iteratively by adjusting the output converter inductance.

As an example, the design procedure is applied for the single-block with an LCL output filter in this section.

Step 1 The design procedure is initiated with the characterization of the normal output voltage for the GDSVPWM, previously defined as:

$$V_{Gn_i} = \frac{V_{G1_{d_i}} + V_{G2_{d_i}}}{2} \tag{6.36}$$

The harmonic content of this normal voltage is computed for several modulation indexes in the normal range of modulation indexes of grid-connected power converters: from 1 to 1.15. In Figure 6.45 the normal voltage harmonic content for a switching frequency of 1950 Hz, the 39^{th} harmonic multiple of the fundamental frequency component, and an interleaving angle of 180 degrees is shown.

There are differences between the harmonic content of the modulation indexes, even though in Figure 6.45 cannot be fully visualized. For this reason, in Figure 6.46 a zoom is made at the second switching harmonic family. It can be concluded from this plot that the voltage harmonics highly depend on the modulation index. The first sidebands are greater as the modulation index is decreased. In contrast, the next sidebands increase with the modulation index. For this reason, the virtual normal voltage harmonic content is generated and used for the filter design procedure, taking for each harmonic the highest voltage harmonic within the modulation indexes range from 1-1.15. In Figure 6.47 the virtual normal voltage harmonic content is represented, this is the voltage that will be used for the calculation of the

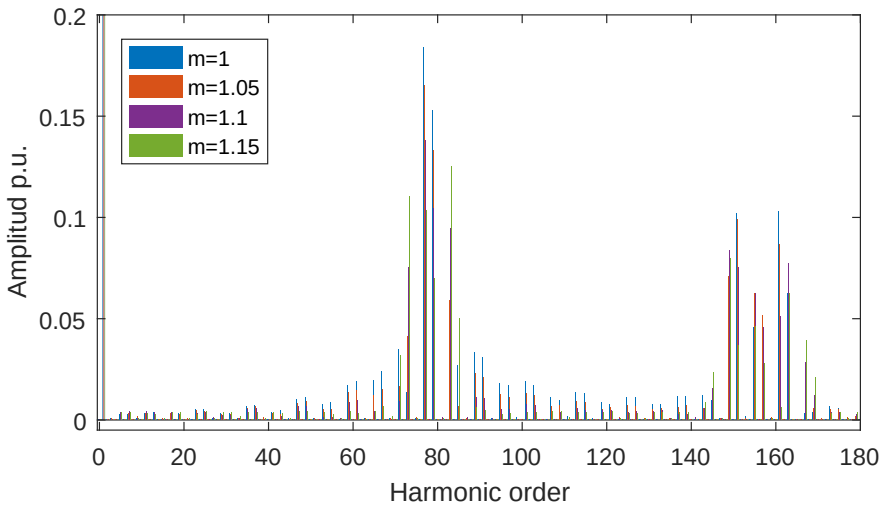


Figure 6.45: GDSVPWM normal voltage for different modulation indexes.

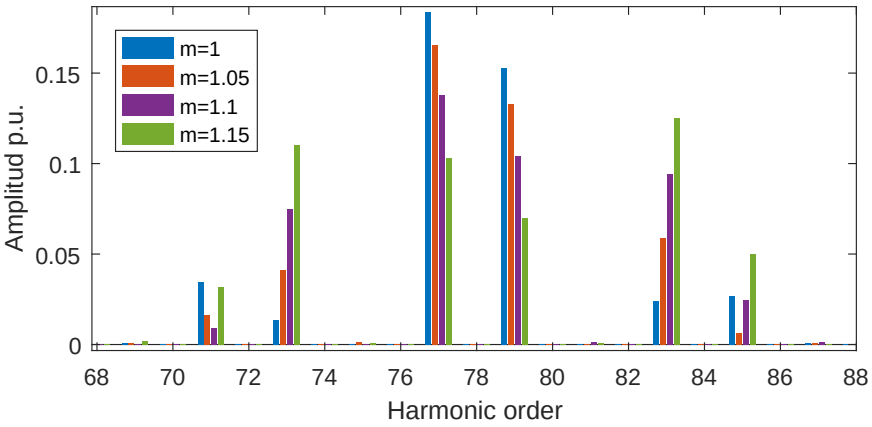


Figure 6.46: GDSVPWM normal voltage for different modulation indexes with a zoom at the second switching harmonic family.

admittance limit in *Step 2*.

Once the harmonic content of the modulation to be used in GSC is determined, the harmonic limits imposed by the grid codes are computed and passed as the second input for the design procedure. The grid-code selected for the design procedure is the German one, developed by the BDEW [BDE08]. The limits imposed to the currents by this grid-code vary depending on the apparent power of the WECS and the SCR at the PCC. This standard imposes restrictions up to 9 kHz for WECS connected to 10 kV grids. As indicated by Table 6.2, special limits are provided for the

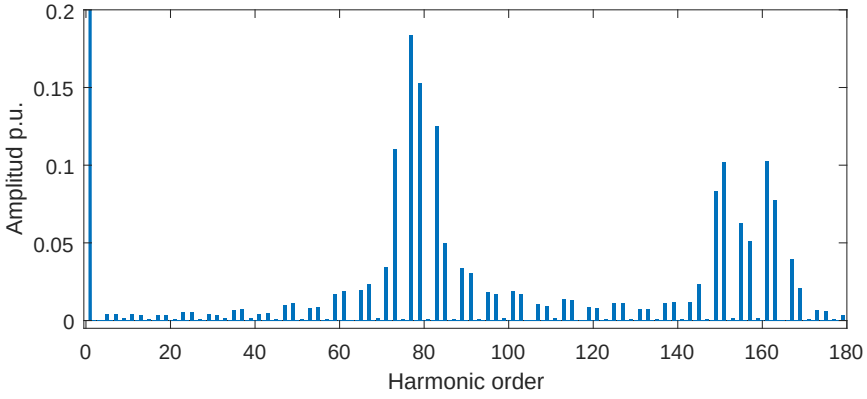


Figure 6.47: Virtual normal voltage harmonic content for the GDSPWM.

odd harmonic multiples of the grid fundamental frequency below the 25^{th} multiple. Additionally, the limits imposed to the higher harmonics, between 40 and 180, are for the integral and non-integral harmonics grouped within a range of 200 Hz according to EN 61000-4-7. To calculate the limits for the single-block power converter, $I_{lim\ BDEW}$, the harmonic limits provided in the table, $i_{lim\ BDEW}$, have to be transformed to the low-voltage side (690 V) and multiplied by the SCR and the apparent rated power of 4 MW, S_r.

$$I_{lim\ BDEW} = i_{lim\ BDEW} \frac{10000}{690} S_r SCR \tag{6.37}$$

Table 6.2: BDEW current harmonic limits for renewable energy systems connected to the 10 kV network.

Harmonic order h	Current injection limit (A/MVA)
5	0.058
7	0.082
11	0.052
13	0.038
17	0.022
19	0.018
23	0.012
25	0.010
Even-ordered h<40	$0.06/h$
Odd-ordered 25<h<40	$0.01 \text{x} 25/h$
40<h<180	$0.18/h$

The limits imposed by the BDEW are computed and represented in Figure 6.48. The WECS rated power is 4 MVA for the calculation, and the secondary grid voltage 690 V. In this way, if the single-block power converter meets the BDEW, when several units are parallelized to increase the converter power, the grid-code compliance will be guaranteed. As an example, the current limits are calculated for three different SCRs: 1, 10 and 100.

Step 2 In this step the maximum allowable filter admittance is calculated for every SCR. It is given by:

$$Y_{lim} = (1 - s.c.) \frac{I_{lim\ BDEW}}{V_{VHC\ n}} \tag{6.38}$$

where $I_{lim\ BDEW}$ are the current limits and $V_{VHC\ n}$ are the virtual harmonics at every frequency, both calculated in *Step 1.* Lastly, *s.c.* is a security coefficient, selected to be 0.05 for the design procedure.

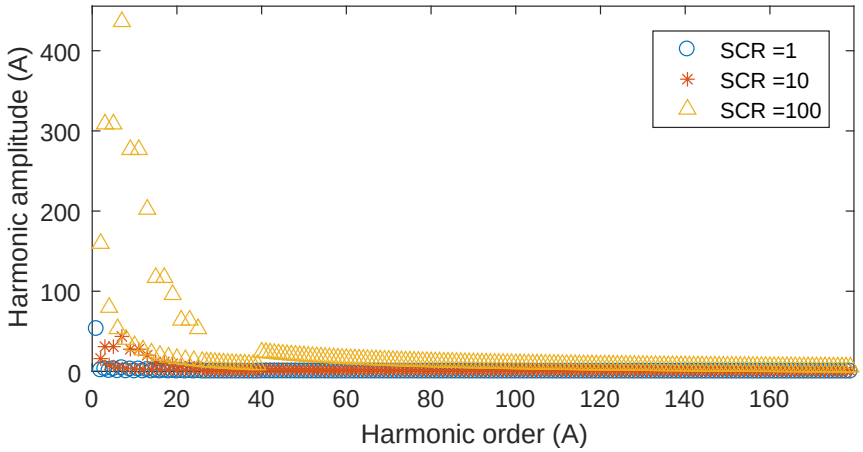


Figure 6.48: BDEW grid current harmonic limits for different SCR, the currents have been transformed to the low voltage side of the transformer.

In Figure 6.49, the admittance limits are shown for a SCR equal to 1. It can be seen in this figure, that around the switching frequency, selected to be at the 39^{th} harmonic of the grid fundamental frequency, as the application of interleaving cancels these harmonics, the filter allowable admittance is high. However, at twice and four times the switching frequency the admittance is highly reduced.

In order to comply with the admittance limit profile, an LCL filter is used at the output of the converter. This LCL filter is an appropriate solution to achieve the required attenuation represented in Figure 6.49.

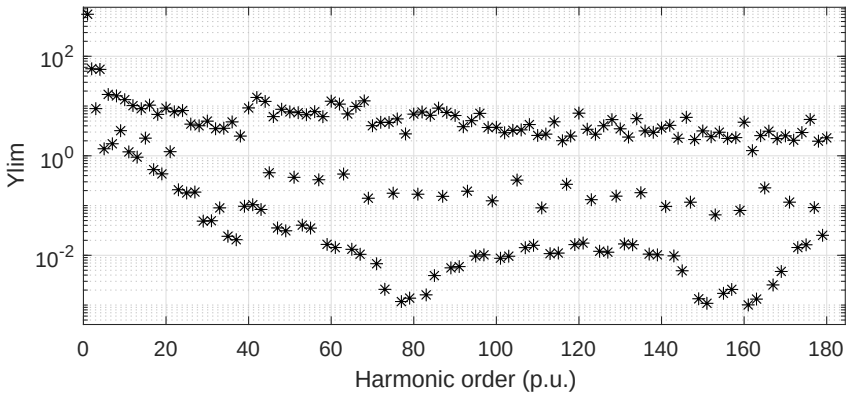


Figure 6.49: Admittance limits for a SCR of 1.

Step 3 The third step for the design of the power converter is the selection of the filter components.

The *LCL* filter is formed by the grid-side inductance, which is the sum of the transformer leakage inductance and the grid inductance. The grid inductance depends on the PCC and can suffer strong variations. The transformer leakage inductance can vary depending on the transformer used, for a 4 MW step-up transformer from 690 V to 10 kV, it is around 0.06 p.u. [SIE13]. In this way, to define the *LCL* output filter, only the capacitor filter, C_G, and the converter side normal inductance, L_{Gconv}, have to be defined. It should be noted that the grid code compliance only sets requirements on the output converter inductance not on the inductance that limits the cross-current components between power converters. In this way, this step can be divided into two steps:

- Step 3.1: Selection of the capacitor
- Step 3.2: Selection of the converter side normal inductance

Step 3.1

Capacitors have a grater energy density than inductors, as shown in Figure 6.50. For this reason, selecting a greater capacitor value may allow to reduce the required converter normal inductance, achieving a more compact design. Nevertheless, the filter capacitors are subjected to the grid voltage, and consequently, they have a reactive power consumption. This reactive power should be limited, because as this power grows, the greater the reactive current becomes, and thus, the losses. The reactive power consumption is limited for the capacitor branches to 0.05 p.u. for the maximum grid voltage of 1.1 p.u. [GOH15b].

As an initial guess, the filter capacitor value C_G is selected to be a 0.035 p.u.:

$$C_G = 0.035 C_b \approx 900nF \tag{6.39}$$

Step 3.2

In this step, after the selection of capacitance, the converter inductance value is calculated to meet the maximum admittance requirement obtained in *Step 2*. The inductance value computed in this step must also guarantee that the maximum switch current ripple does not exceed the desired limit imposed. The maximum peak-to-peak switching ripple is a function of the

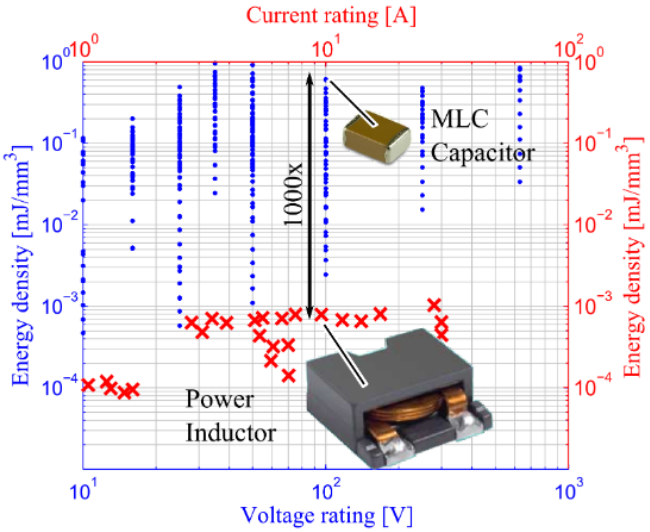


Figure 6.50: Energy density of capacitors and inductors [PIL17].

DC-bus voltage, E, the switching frequency, F_{sw}, and the converter normal inductance, $L_{Gconv\ n}$ [GOH15b]:

$$\Delta I_{pp,max} = \frac{E}{48 F_{sw} L_{Gconv\ n}} \tag{6.40}$$

From this equation, the minimum normal inductance can be calculated, $L_{Gconv\ n,min}$. If the calculated $L_{Gconv\ n}$ is lower than the minimum value, *Step 3.1* has to be reconsidered, reducing the initial guess for the capacitor voltage and computing again $L_{Gconv\ n}$ until it becomes greater than the minimum value. Otherwise, the capacitor value can be increased to reduce the required inductor, increasing the power density.

For the initial capacitor value guessed, the converter inductance is increased iteratively, up to the limit where the filter admittance is lower than the admittance limit already calculated in *Step 2*. If this procedure is performed for different SCR, bounded by a minimum SCR of 1 and a maximum SCR of 200, Figure 6.51 is obtained. As it can be seen, to fulfill the BDEW grid code, the required converter normal inductance is highly increased for weak grids. For SCRs ranging from 1 to 50, high variations in the converter inductance are required in order to meet the grid codes. In this way, if the output filter is designed to meet the grid codes for every SCR greater than 10, a normal inductance equal to 180 μH is required. If this power converter, designed for a SCR equal to 2, is connected to a stronger grid, the LCL

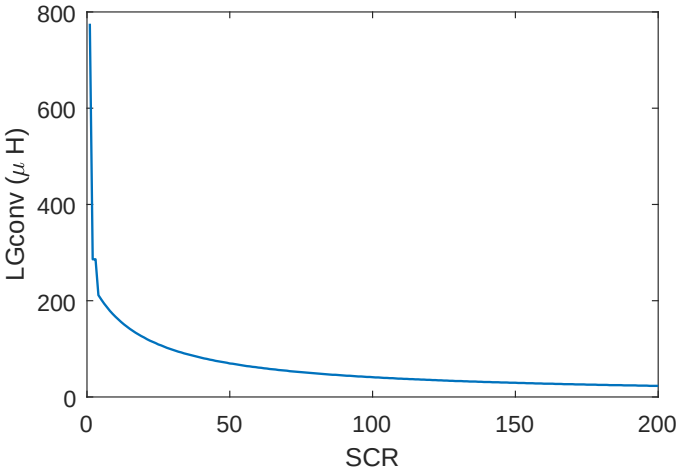


Figure 6.51: Required converter normal inductance to fulfill the BDEW for different SCR and a capacitor equal to $0.035C_b$.

would be bulkier than required, and the system dynamic response will be also penalized. If the power converter is connected to a grid with a SCR equal to 100, the required inductor to meet the grid-code is just 30 μH. Con-

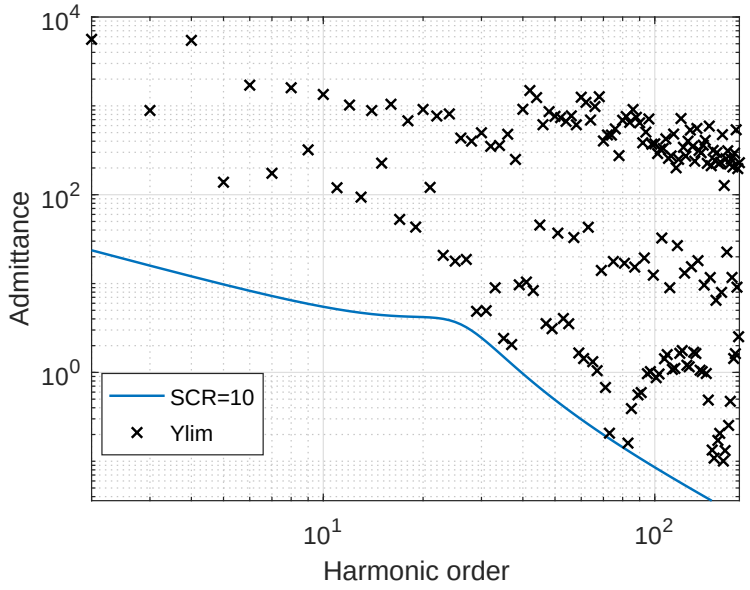


Figure 6.52: *LCL* filter admittance and limits for a SCR of 10.

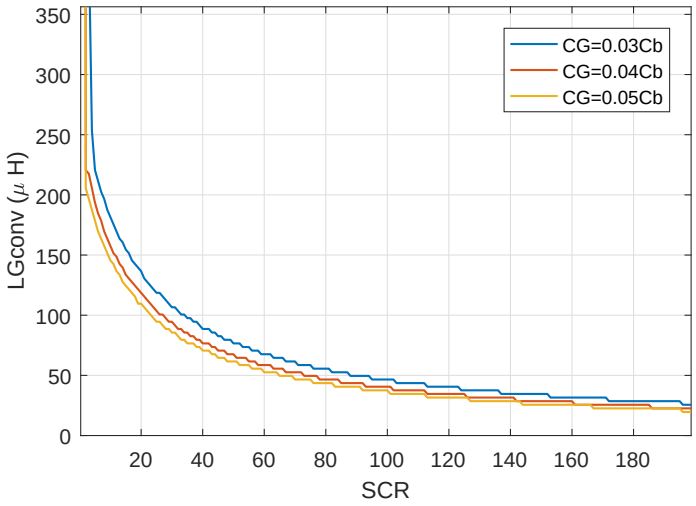


Figure 6.53: Required converter normal inductance to fulfill the BDEW for different SCR and filter capacitors.

sequently, adapting the filter design to the grid at which the power converter is connected looks as a necessity with the BDEW grid-code. Alternatively, a different output filter structure can be considered for these cases, as th low frequency admittance has a significant margin. As an example on how the design procedure guarantees the grid-code fulfillment, in Figure 6.52 for a SCR of 10, the real admittance obtained with the design procedure is represented in blue, along with the admittance limits calculated for that SCR. It can be seen that the limits are respected with the proposed design procedure.

To conclude the filter design procedure, the effect of modifying the filter capacitor values is also tested, representing in Figure 6.53 the required normal inductance for several filter capacitors and SCRs. It should be noted that for the clarity of the plot and to better compare the evolution and differences between the graphs, the required inductances for a SCR equal to 1 are not displayed. It can be seen how a bigger capacitor can reduce the normal inductance required to meet the grid code, an approach that becomes specially interesting for weak grids.

6.6.2 IPT alternatives for the single-block

The application of interleaving allows to reduce the required converter normal inductance in order to meet the grid codes. However, the originated circulating

currents, have to be limited, requiring an inductive coupling between both power converters. This inductive coupling is normally made through IPTs. In this section, the most appropriate options for the single block power converter are discussed.

6.6.2.1 Model of the IPTs

The simplest single-phase IPT that can be used to couple two power converters in parallel is represented in Figure 6.54. In this interphase transformer, only the components that are phase shifted create a magnetic flux in the core, while the rest of the components would be only limited by the IPT leakage inductance.

An equivalent model that represents the behavior of this component is developed in the following. If the mutual inductance is denoted by M and the leakage inductance is denoted by L_l, the inductance matrix correlating the total flux created in the first and second windings, ϕ_1 and ϕ_2, is given by:

$$\begin{Bmatrix} \phi_1 \\ \phi_2 \end{Bmatrix} = \begin{bmatrix} L_l + M & -M \\ -M & L_l + M \end{bmatrix} \begin{Bmatrix} I_{G1_a} \\ I_{G2_a} \end{Bmatrix} \tag{6.41}$$

The output and cross-inductances can be calculated from this matrix. If the components I_{G1_a} and I_{G2_a} are in phase, the output inductance, L_{out}, of

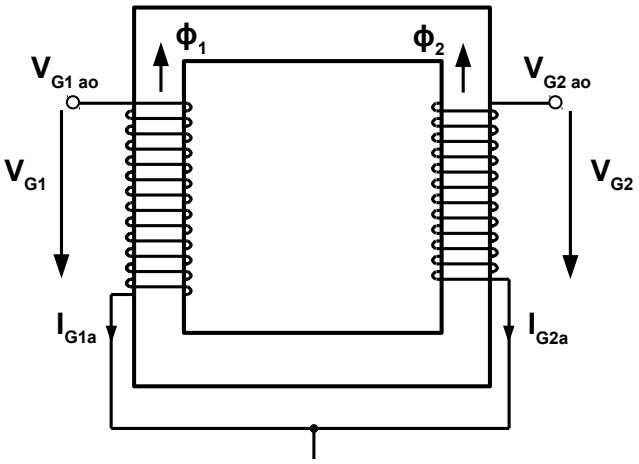


Figure 6.54: Single-phase IPT.

this IPT is given by:

$$L_{out} = L_l \tag{6.42}$$

If both current components are recirculated, meaning that they are phase shifted by 180 degrees, a cross inductance, L_{cross} can be defined as:

$$L_{cross} = L_l + 2M \tag{6.43}$$

In this way, the equivalent model of the IPT can be represented by Figure 6.55. The total inductance offered to the circulating components is $2L_l + 4M$, while the output components are only limited by $L_l/2$.

This inductance can effectively limit the circulating components, but it cannot be used to achieve the desired normal inductance of 50 μH. Integrating this inductance in the leakage inductance is not a feasible option, and for this reason, the three-column single-phase IPT [HED16] represented in Figure 6.56, is modeled in the following. By integrating the output inductance in the same component, the total required inductor volume is reduced.

Similarly to the previous single-phase IPT, the inductance matrix correlating the total flux created in the first and second windings, ϕ_1 and ϕ_2, is given by:

$$\begin{Bmatrix} \phi_1 \\ \phi_2 \end{Bmatrix} = \begin{bmatrix} L_s & -M \\ -M & L_s \end{bmatrix} \begin{Bmatrix} I_{G1_a} \\ I_{G2_a} \end{Bmatrix} \tag{6.44}$$

where L_s stands for the self-inductance and M for the mutual inductance. Consequently, the same equivalent circuit represented for the previous single-phase IPT is still valid.

However, in this case, L_s and M vary depending on the ratio of the reluctances of the middle column, dominated by the airgap, to the side columns. Consequently, the normal inductance and the effective cross-inductance also vary. If this variation is represented for several ratios, normalizing the inductors with respect to the self inductance, Figure 6.58 is obtained. It can be seen that if the reluctance of the middle column is high, meaning that the IPT has a big air gap, the middle column has no effect and the same normal and cross inductances are obtained. In the other extreme case, if the reluctance in the middle branch is lower than in the other two, the flux will tend to circulate through this column, reducing the cross inductance but increasing the normal one. If the three branches have equal reluctances the normal inductance is equal to a quarter of the self inductance, while the

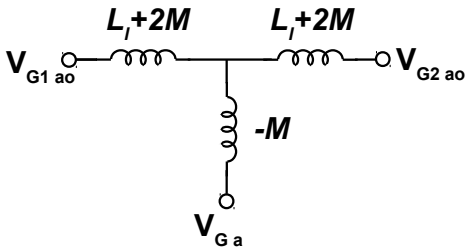


Figure 6.55: Single-phase IPT equivalent model.

cross inductance is equal to three times he self inductance. In this way, by modifying the air-gap, the relation of the inductances can be modified.

This inductor offers the possibility of integrating the cross-inductance as well as the normal inductance. However, an optimized solution can be obtained with the inductor presented in [GOH16]. This inductor that has been already presented in the state of the art, can be clearly understood and modeled after the discussion of te two previous IPTs. The integrated inductor in Figure 6.59 offers simultaneously a path for the cross-current component, as in the case of the simplest single-phase IPT, yellow dashed lines for phase a, and a different path for the flux created by the normal currents, red dashed lines for GSC2. The number of windings is minimized with this solution, as only a winding is required per phase, in opposition to the case where an IPT and a three phase inductor are combined. Furthermore, magnetic material in the core can be saved with this solution.

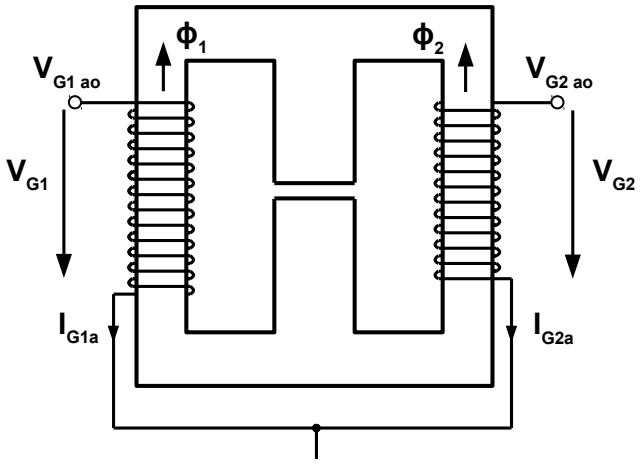


Figure 6.56: Single-phase IPT including the output inductance.

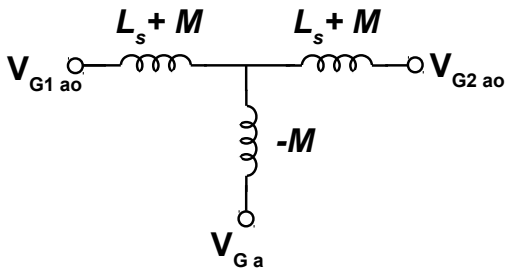


Figure 6.57: Model of the single-phase IPT including the output inductance.

Again, an inductance matrix can be defined to characterize the integrated inductor:

$$\begin{Bmatrix} \phi_{1a} \\ \phi_{2a} \\ \phi_{1b} \\ \phi_{2b} \\ \phi_{1c} \\ \phi_{2c} \end{Bmatrix} = \begin{bmatrix} L_T + L_I & -L_I & -L_T/2 & 0 & -L_T/2 & 0 \\ -L_I & L_T + L_I & 0 & -L_T/2 & 0 & -L_T/2 \\ -L_T/2 & 0 & L_T + L_I & -L_I & -L_T/2 & 0 \\ 0 & -L_T/2 & -L_I & L_T + L_I & 0 & -L_T/2 \\ -L_T/2 & 0 & -L_T/2 & 0 & L_T + L_I & -L_I \\ 0 & -L_T/2 & -0 & -L_T/2 & -L_I & L_T + L_I \end{bmatrix} \begin{Bmatrix} I_{G1_a} \\ I_{G2_a} \\ I_{G1_b} \\ I_{G2_b} \\ I_{G1_c} \\ I_{G2_c} \end{Bmatrix} \tag{6.45}$$

where L_T stands for the three-phase magnetic inductance, which is dominated

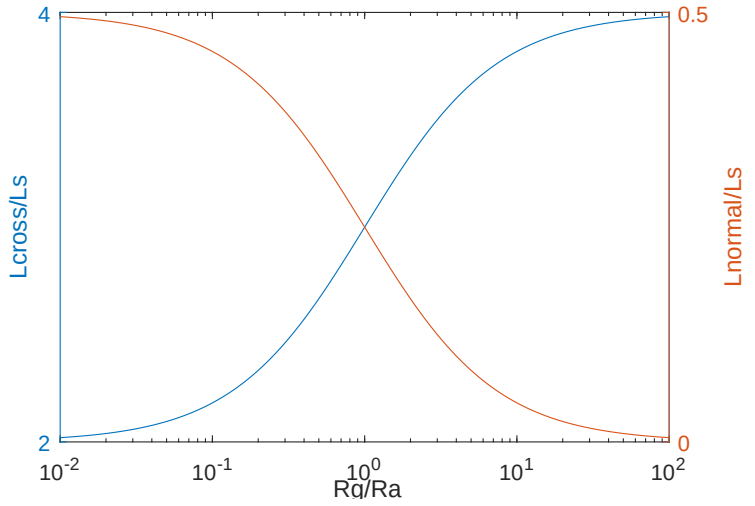


Figure 6.58: Variation of the normal inductance and cross-inductance depending on the reluctance ratios.

by the reluctance of the air-gap, and L_I is the magnetic inductance of the inner IPT between each two phases. Note that to derive this matrix two main assumptions are made. Firstly, the circulating components are considered to be closed across the single-phase IPT provided in each phase for the coupling of both power converters. This is reasonable, as in this path there is not an air-gap and it is the path with the lowest reluctance. Secondly, the three-phase inductors for the normal component of each power converter are considered to be independent. Again this is justified because it is the path with the lowest reluctance.

It can be concluded that the cross-inductance offered by this integrated inductor is equal to $4L_I$, while the normal inductance is equal to $3/2L_T$ for each converter, so the parallel of both is equal to $3/4L_T$. This integrated inductor is the one selected for the single-block, due to its potential to reduce the total inductor volume.

6.6.2.2 Reducing the size of the IPT

Several modulation strategies have been proposed for the reduction of the size of the IPT. [COU11] analyzed the influence of SVPWM7 and discontinuous modulations on the flux created in the IPT. They proposed a modulation that combines some of the state-of-the-art DSVPWM and new proposal. They proposed a modulation for two parallel power converters with common DC-bus, called PWMBCNP that can reduce the generated flux

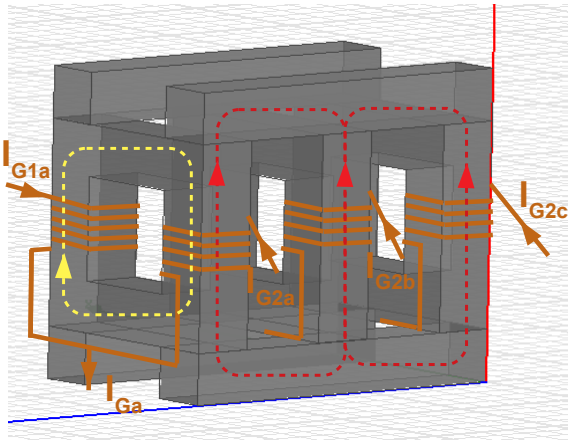


Figure 6.59: Integrated three-phase IPT representing the fluxes created.

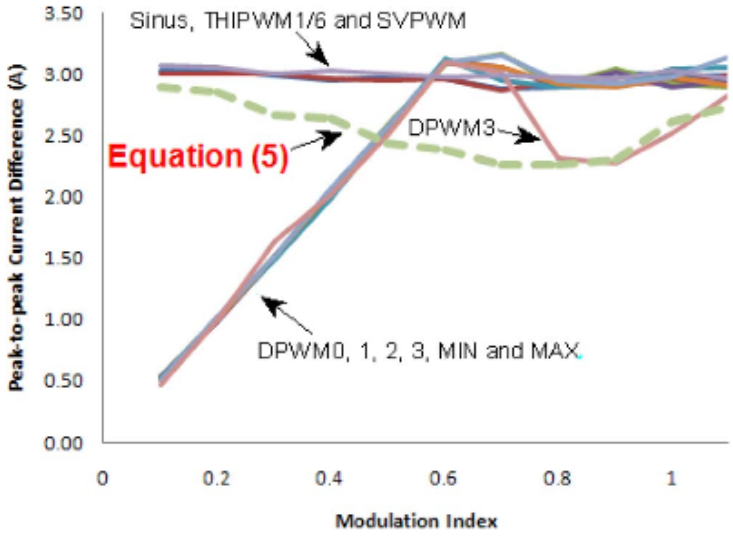


Figure 6.60: Peak-to-peak current ripple for the different modulation strategies [COU11].

in the IPT by a 20%, consequently reducing the size of this component. As represented in Figure 6.60, their modulations in based on the combination of different modulations, depending on modulation index. They choose for the different modulation indexes the one that has a lower peak-to-peak current ripple. With this strategy they can achieve considerable reductions in the IPT at low modulation indexes, however, at high indexes, those benefits disappear. Moreover, the modulation in GSC is modified so the grid current harmonic content might be negatively affected.

[ZHA12] presented also a modification of the DSVPWM in order to reduce the circulating current and reduce the IPT. Based on a modification of the modulation if the reference vectors of both power converters are located in different sub-sectors, they avoid jumps in the homopolar current. Note that in this thesis, this issue is addressed through the master slave implementation of the DSVPWM modulation. This implementation is more beneficial, as it does not imply additional commutations. In the same article [ZHA12] also proposed clamping the converter leg with highest flux in the IPT in order to reduce the maximum flux in the IPT, as represented in Figure 6.61.

Lastly, [GOH15c] modified the discontinuous modulation vector sequence to reduce the flux, and consequently the size of the IPT. By doing so, additional commutations are introduced, having 6 commutations per switching period in each VSC and losing the benefits of the implementation of DSVPWM in terms of efficiency. Their proposal achieves important reductions at low modulation

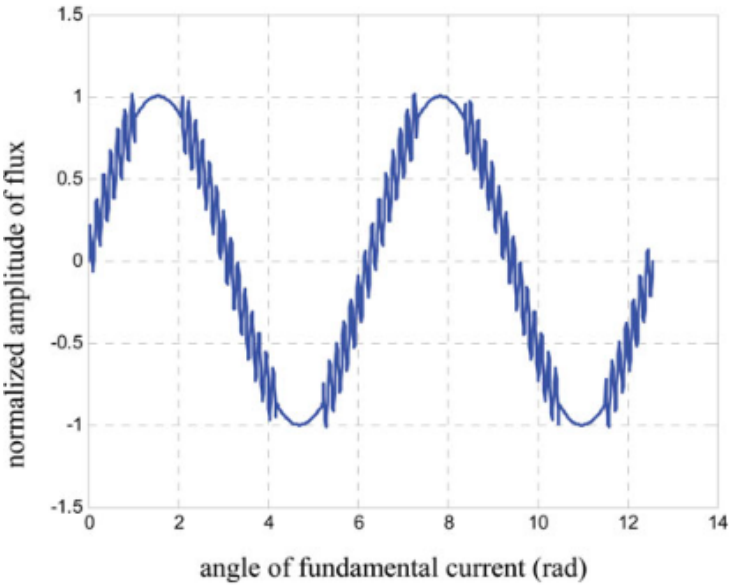


Figure 6.61: Total flux in the IPT when the legs with higher flux are clamped [ZHA12].

indexes in GSC, but it cannot provide the same benefits at higher modulation indexes, where the converter is generally operating.

All these strategies are developed for two power converters coupled in parallel with a common DC-link. However, in our topology, the DC-buses are separated, and two back-to-back power converters are coupled in parallel, meaning that from the homopolar model, four degrees of freedom to reduce the hompolar circulating current are obtained, Figure 6.62. The voltages imposed by V_{G1_h}, V_{G2_h}, V_{M1_h} and V_{M2_h} do not contribute to the normal current component, so they can be modified according to our interests to reduce the overall cross-current. Note that the differential cross-current

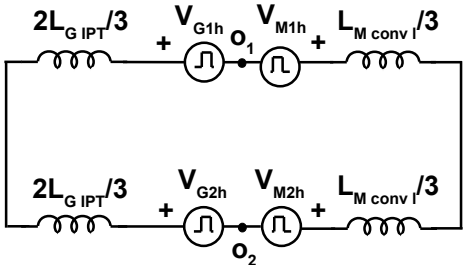


Figure 6.62: Single-block equivalent circuit for the homopolar cross-current.

cannot be modified, as it would imply modifying the differential vectors in GSC an consequently, it would affect the normal current quality. Moreover, as it is already known, the differential voltages imposed by MSC does not have an influence in the cross-current in GSC.

At this point, it has to be decided how these four homopolar voltage sources can be combined to reduce the circulating homopolar current component. MSC is forced to switch at the same time instants, as otherwise, the circulating current between both power converters, which are coupled by small three-phase inductances, will grow to unacceptable levels. This is true for the differential vectors. Nevertheless, as represented in Figure 6.62, the IPT used in GSC is also limiting the hompolar voltages modulated by MSC. In this way, during the zero vectors, MSC1 and MSC2 do not have to apply

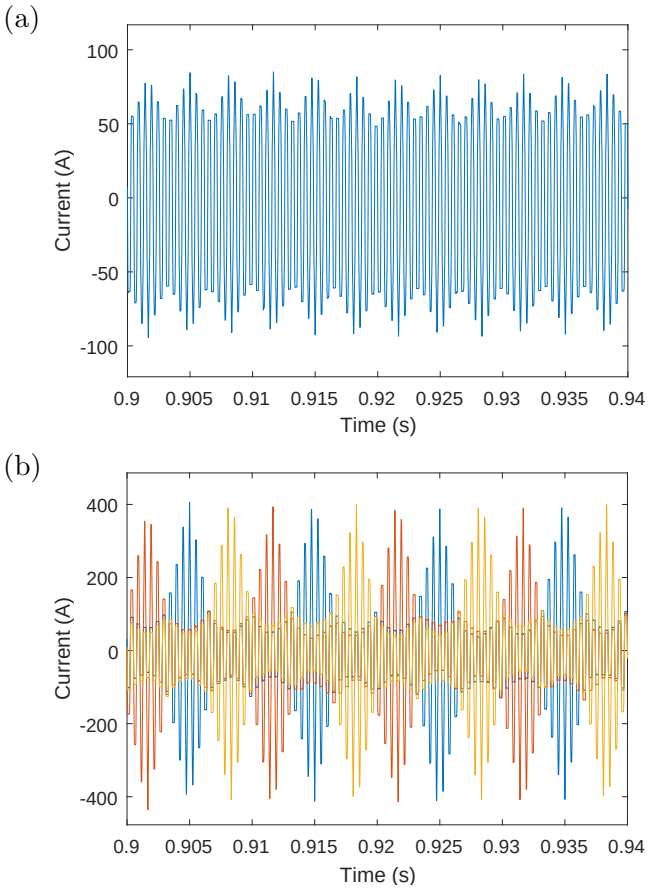


Figure 6.63: Homopolar cross-current (a) and IPT magnetizing cross-current (b).

the same zero vector. The IPTs in GSC allow the coexistence of opposite zero vectors in MSC, a characteristic that is used to reduce the magnetizing current, as it is explained in the following.

Let us suppose then that both GSC and MSC are using any DSVPWM with synchronous switching in MSC and interleaving in GSC. Initially, if no modifications are made in the modulation, the homopolar cross-current and the total cross-current obtained are represented in Figure 6.63.

The homopolar current represented in Figure 6.63 (a) is only created by GSC, as MSC is switching synchronously. However, the total magnetizing current can be reduced if MSC modifies the zero vector to compensate the one introduced by GSC. In this way, the homopolar cross-current is modified, affecting to the IPT magnetizing cross-current, that is equal to the sum of the homopolar and differential cross-currents. The modulation in MSC is modified as represented in Figure 6.64. It can be seen from this representation, that if the zero vectors in GSC and MSC have the same time duration they will cancel each other and they will not create an homopolar current. However, if the zero time duration in MSC is greater than in GSC, a reverse homopolar current component is created by MSC in opposite phase to the one that will create GSC if no additional compensations are applied in MSC. In this way, the compensation proposed to reduce the magnetizing current mainly depends on the modulation index of MSC. If this compensation is applied, it can be seen that the overall magnetizing current in the IPT is reduced as a result of a lower homopolar current component. This is represented in Figure 6.65.

As shown in Figure 6.65, the maximum peak in the magnetizing current in the IPT is reduced to 320 A, from the initial case where it was equal to 400 A, a 20% reduction. This potential reduction, in opposition to the previously presented ones, can be effective even when the modulation index in GSC is in the limit of the linear modulation region. However, it is conditioned by

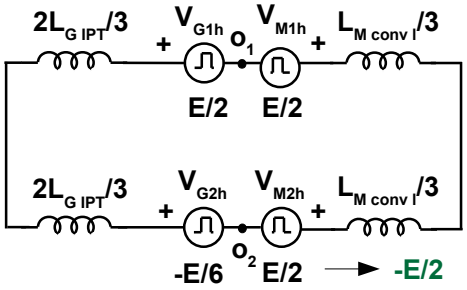


Figure 6.64: Single-block's circuit for the homopolar cross-current.

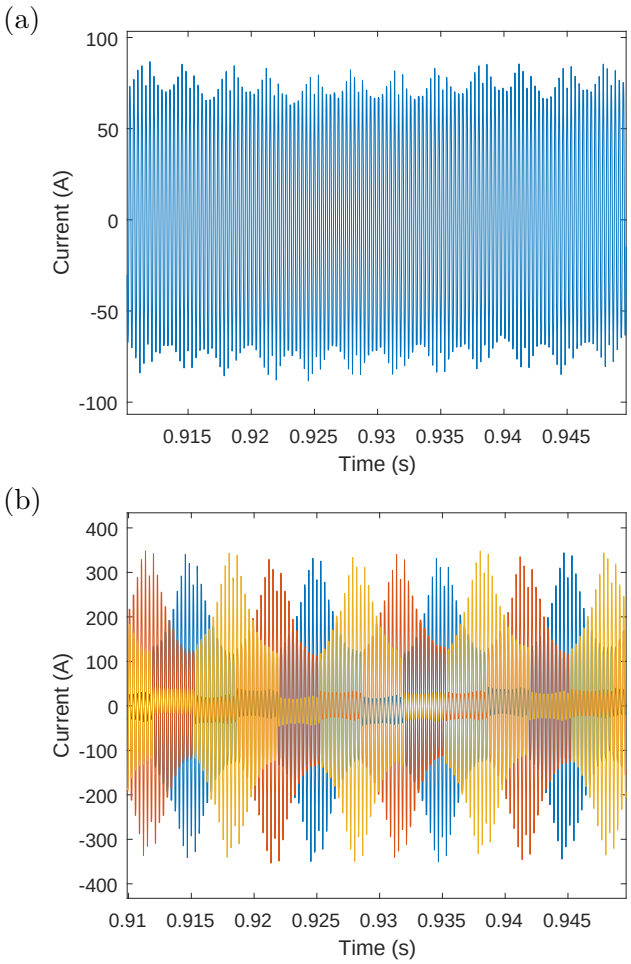


Figure 6.65: Homopolar cross-current (a) and IPT magnetizing cross-current (b).

the modulation index in MSC, and if MSC does not have zero vector, no compensation can be performed. Moreover, this strategy for parallel power converters introduces additional commutations. If the situation in Figure 6.62 is considered, MSC2 uses the negative zero vector instead of the positive one, but the same differential vector afterwards. Consequently, it is forced to switch 2 converter legs instead of just one, as MSC1 will do.

The most suitable solution to reduce the size in the IPT is increasing the switching frequency, something that can be done by taking advantage of the reduction in the losses of the GDSVPWM. With this modulation, the switching power losses are reduced by 50% if compared to the ones with SVPWM7. This means that the switching frequency can be doubled without increasing the

switching power losses.

To illustrate this idea, the switching frequency is increased by a 60%, to 3150 Hz for the GDSVPWM. With this switching frequency, the power losses are still reduced if compared with the SVPWM7. If the cross inductance is recalculated for the new switching frequency:

$$L_{cross} = \frac{E}{F_{sw}\Delta i_{Gc}} = 450\mu H \tag{6.46}$$

The required inductance is reduced from 737 μH to 450 μH, an important reduction. The three-phase integrated IPT to be used for the coupling of both power converters offers an inductance equal to $4L_I$ to the cross-current, L_I being the magnetic inductance of the IPT in the circulating path. For this reason, $L_I = 112\mu H$.

The required normal inductance to meet the grid-codes is recalculated following the previous design procedure for a capacitor 0.035 p.u. The results of the calculations are represented in Figure 6.66. If these results are compared to the ones in Figure 6.53, it can be seen that now, with a converter inductance equal to 90 μH, the grid code harmonic content is fulfilled for every SCR. However, if the SCR of the PCC is greater, the converter normal inductance

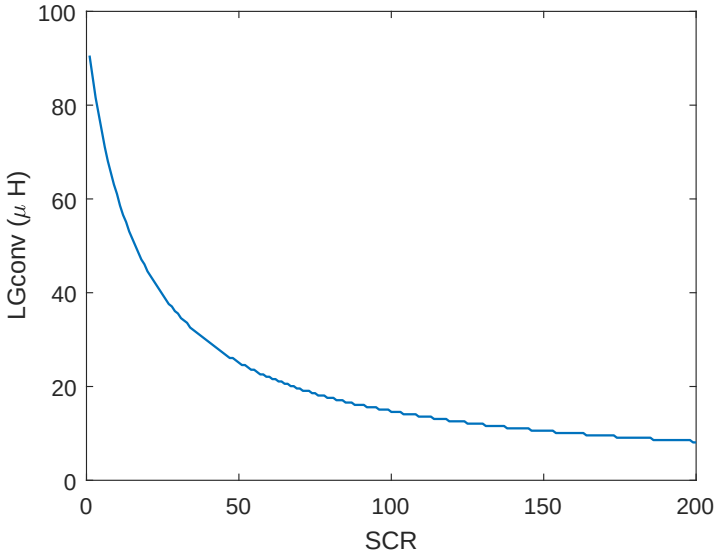


Figure 6.66: Required converter normal inductance to fulfill the BDEW for different SCR and filter capacitors.

should be decreased accordingly, to optimize the output LCL filter. This great reduction can be justified by the displacement of the switching harmonics to higher frequencies, where the filter already introduces an attenuation equal to 60 dB/dec. Consequently, to fulfill the grid codes, a lower inductor is required.

To optimize the converter output filter and the IPT, an optimization procedure should be carried out, considering the switching frequency as a variable. The implementation of the integrated inductor falls beyond the scope of this work.

6.7 Single-block solution overview

The single-block solution is the one represented in Figure 6.67. This solution has independent DC-buses. It uses the GDSVPWM in MSC with synchronous switching, the inductors in MSC are three-phase coupled inductors corresponding to the dv/dt. These inductors limit the circulating currents that can occur in MSC caused by the small differences in the switching times. In contrast, in GSC, interleaving is applied between GSC1 and GSC2 with GDSVPWM. The master-slave implementation of the generalized discontinuous modulation (GDSVPWM) is used, as proposed in this thesis, to avoid jumps in the homopolar circulating current. An integrated inductor is used to limit both the cross-current and to guarantee the fulfillment of the grid codes. In order to show the converter performance and describe the design of the current control loops, the switching frequency

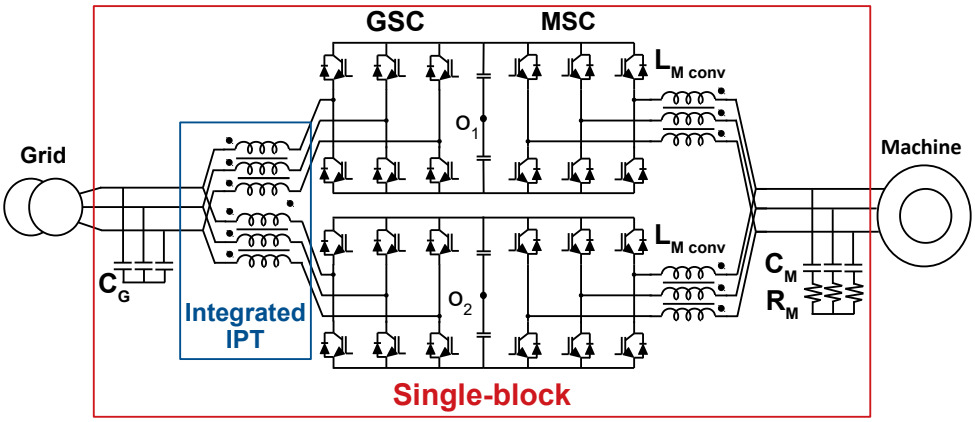


Figure 6.67: Single-block solution.

is 3150 Hz, the inductor output normal inductance is 90 μH while the cross-inductance is equal to 450 μH. A filter capacitor equal to 900 μF is used to complete the LCL filter. This filter allows to fulfill the BDEW grid-code up to a SCR equal to 1.

To conclude the analysis of the single-block power converter, its performance is verified through simulation. The simulation is performed for a SCR equal to 2. In this simulation, the grid-code compliance is verified. The cross-current is also represented, as well as the current in MSC.

In Figure 6.68 the BDEW compliance can be verified. The temporal waveforms of the current in GSC1, GSC2 and the grid current in phase a are represented in Figure 6.68 (a). In Figure 6.68 (b) the grid-code compliance is verified. The grid current harmonic content in phase a, red, is compared to

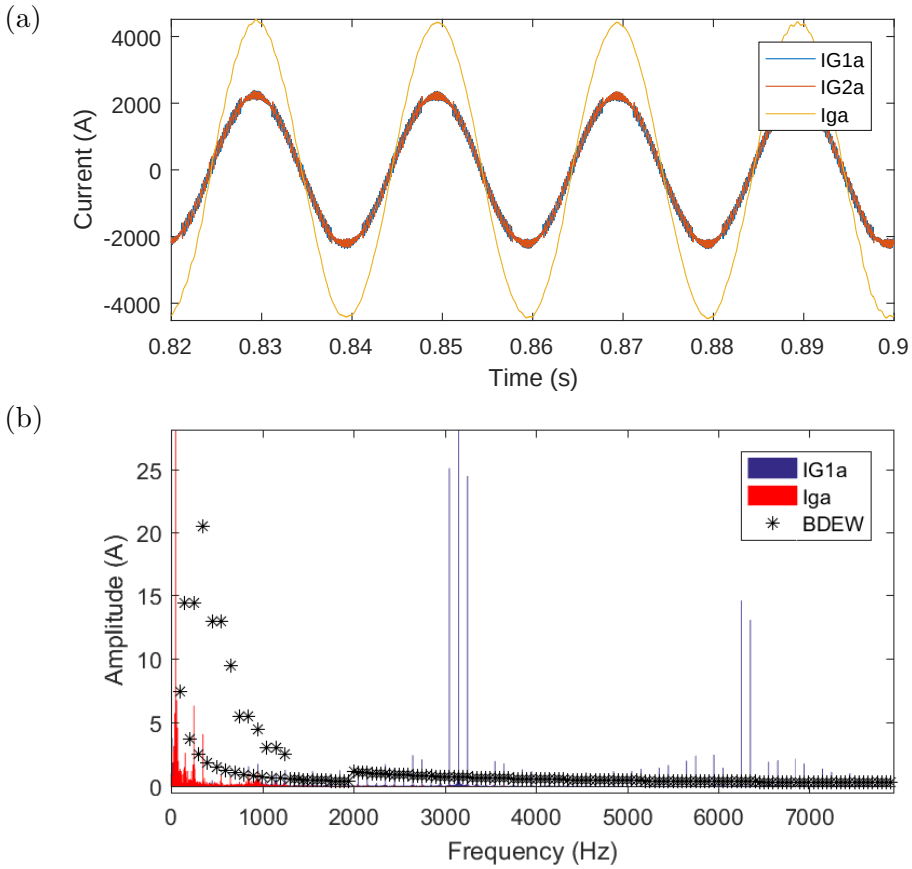


Figure 6.68: GSC1 and GSC2 converter currents and grid current (a) grid current harmonic content (b).

the limits imposed by the BDEW and with the converter current harmonic content in phase a of GSC1 (blue).

The total cross-current component in GSC is represented in Figure 6.69 (a), while the homopolar cross-current is represented in Figure 6.69 (b). It can be seen that no jumps appear in the homopolar current as a result of the proper implementation of the modulation, and consequently, no jumps are obtained in the total cross-current.

At last, the machine side current is represented in Figure 6.70, showing that even though interleaving is not applied in these power converters, the

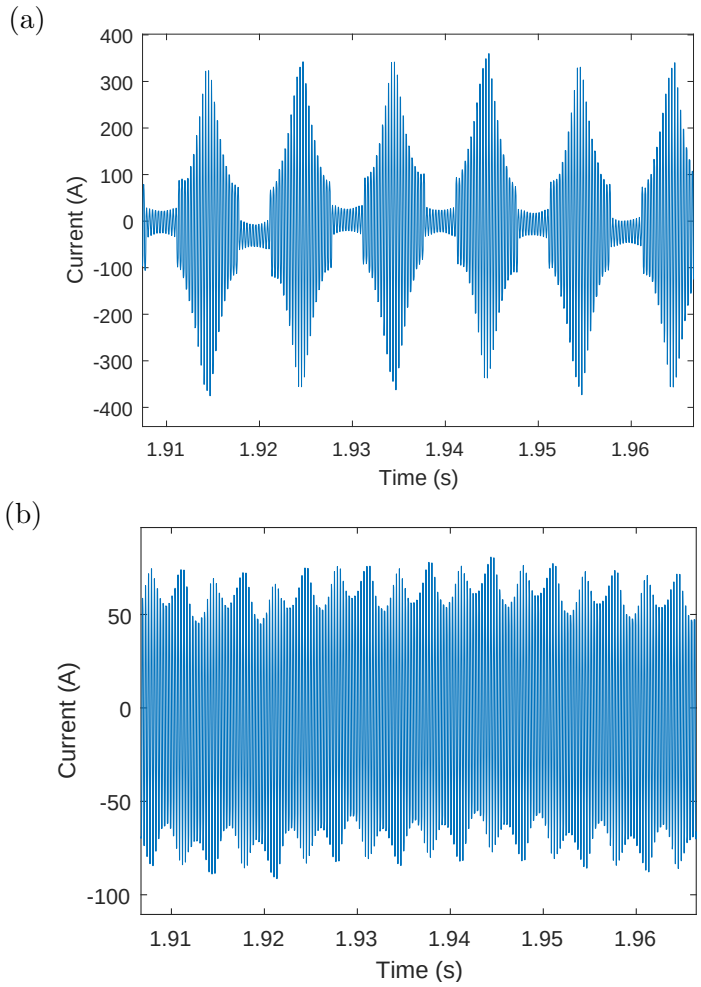


Figure 6.69: GSC total cross-current (a) and homopolar cross-current (b).

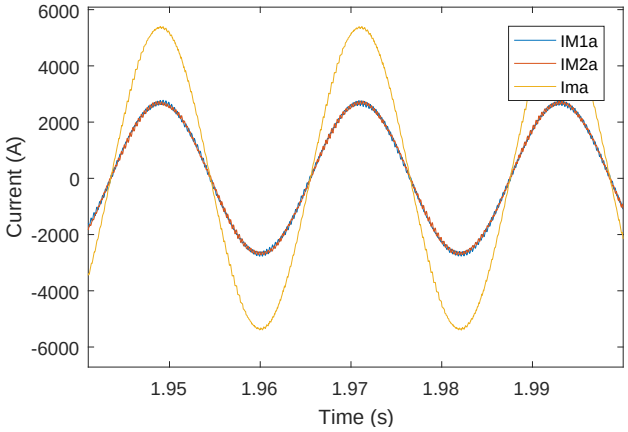


Figure 6.70: MSC1 and MSC converter currents and machine side current in phase *a*.

current has a high quality.

With the modulation selected, GDSVPWM, the switching losses are reduced by a 50%, while the conduction losses are kept at the same value. As a drawback, this modulation increases the phase-to-ground and common-mode voltages by a 16%. If these voltages have to be reduced, an inductive coupling can be used in MSC. With this couping the modulation techniques presented in Chapter 5 can be directly applied to the single-block, achieving phase-to-ground voltages bounded by $\pm 2E/3$ and common-mode voltages bounded by $\pm 2E/3$ with the CMVR1 and $\pm E/3$ with the CMVR2.

6.8 Grid-connection stability of the single-block power converter

6.8.1 General description of the control strategy

The single-block power converter is based on two parallel power converters with independent DC-buses. In MSC the power transfer to the machine is controlled in the SRF by a single controller that determines the required reference vector for both MSC1 and MSC2. The switching orders for MSC1 and MSC2 have to be equal, as they are directly coupled. However, as the IGBTs and inductors are not exactly equal, the power handled may not be equal in both power converters.

To deal with this aspect, the DC-buses of both power converters have to

be controlled independently, generating each DC-bus control a different active power reference, and consequently, a different current reference. In this way, having independent DC-buses requires independent current controllers in GS1 and GSC2. GSC1 and GSC2 are also controlled in the SRF. To control the output current two control loops in dq are implemented, meaning that there are four current control loops in GSC in order to control the active and reactive power transfer in GSC. Supposing that the neutral point in GSC is isolated, there are six currents to be controlled with five degrees of freedom, implying that five independent current control loops can be implemented.

These five current controllers are the following ones; four control loops to control GSC1 and GSC2 total output current in dq. In this way, both the normal current component and the differential cross-current component are controlled in each converter. The design of this control loop is analyzed in Subsection 6.8.2. The remaining degree of freedom is used for the control loop of the homopolar current component, this aspect is covered in Subsection 6.8.4.

The control structure for GSC and MSC previously described is represented in Figure 6.71. As indicated in the figure, in MSC the machine side current is measured and controlled. This option is the most appropriate for parallel power converters with independent DC-buses and synchronous switching. With this control strategy, it is guaranteed that the output current is equal to the reference current. A different alternative will be to measure and control the current of one of the power converters. Nevertheless, this control scheme would not guarantee that the output current is equal to the reference, as both power converters are forced to switch at the same time instants. The modulation of the proposed control scheme is calculated with the mean of the DC-bus voltage, reducing the adverse effects of uneven voltages.

In GSC the control structure is shown in Figure 6.71. As the DC-buses are independent, GSC1 and GSC2 have different current references. The current controller is formed of four current control loops for the tracking in the dq axis of the different references calculated for GSC1 and GSC2. An additional controller for the homopolar current component is also implemented, that only affects to the distribution of the zero vector. The reference vector of GSC1, GSC2 and the required homopolar action is modulated by phase shifting the carrier frequencies of both GSCs by 180 degrees.

The design of the control strategies adjusted in the following are performed for all the possible range of SCR, from 1 to 200, in order to guarantee the robust operation of the single-block.

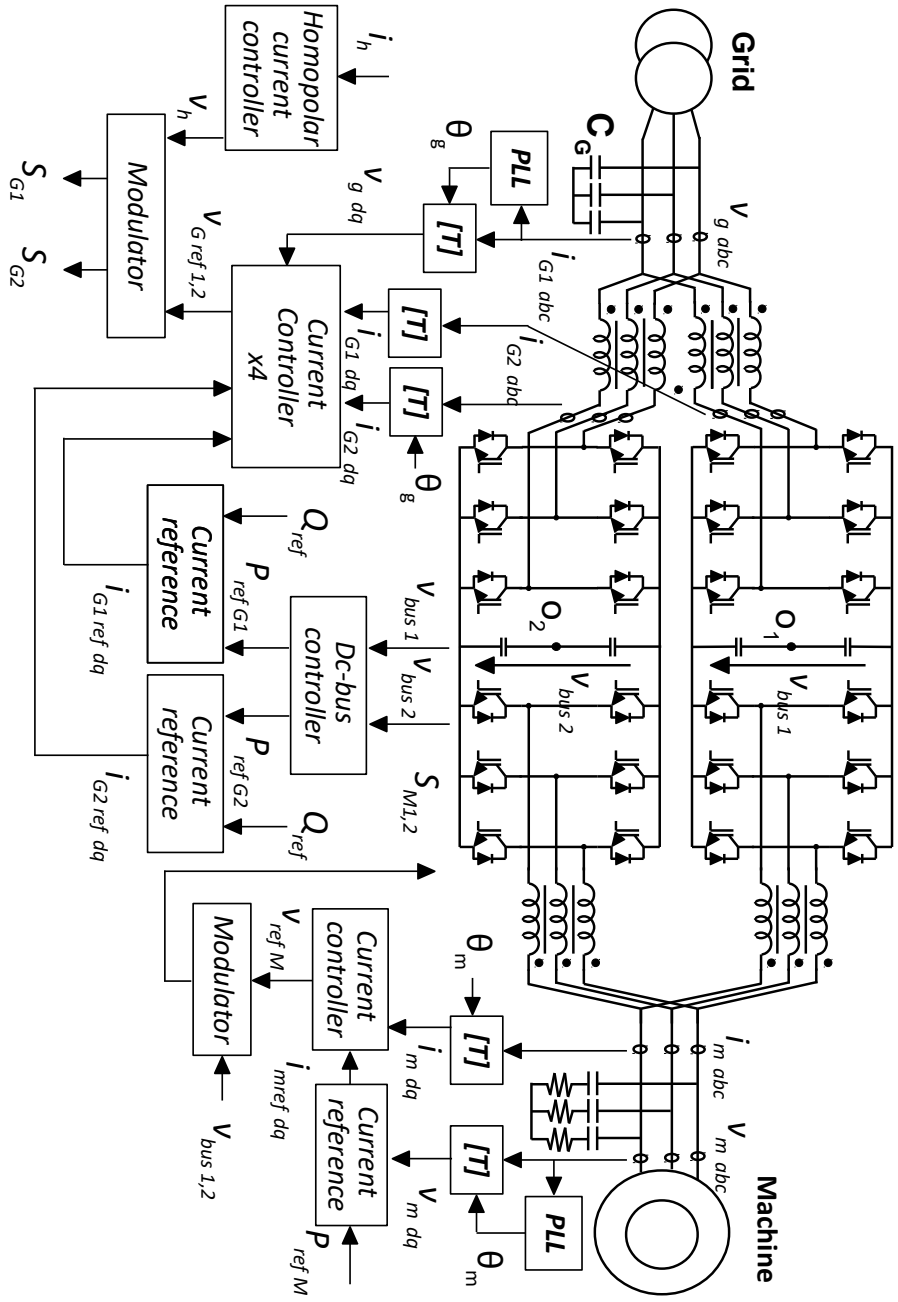


Figure 6.71: Current control loop for the single-block power converter.

6.8.2 Design of the current control loop

In this subsection, the control strategy proposed in Chapter 3 is applied to the single-block power converter. This strategy is designed for the normal-current plant model in the dq axis. The model for the normal current was developed in Section 6.3, and reproduced in Figure 6.72 for an LCL output filter. In this figure, a single phase equivalent model has been represented for simplicity, even though it is a three-phase system.

The current is controlled in the SRF, so the plant in this reference frame has to be derived. This has already been done in Chapter 2, so it is not repeated in here. Two transfer matrices have to be obtained: $[G_{iv}(s)]$, that correlates the converter current $I_{Gn\ dq}(s)$ with the converter voltage in dq axis, $V_{conv\ dq}(s)$ and $[G_{vv}(s)]$ that correlates the capacitor voltage $V_{C\ dq}(s)$ with $V_{conv\ dq}(s)$. Once both transfer matrices have been obtained, the control loop represented in Figure 6.73 can be tuned.

It is reminded that the matrix $[PF(s)]$ is added in the voltage positive-feedback path to reduce the variability at low frequencies of the plant, created by the highly variable grid inductance. $[PF(s)]$ has the following form:

$$[PF] = \begin{bmatrix} \frac{A(s)}{A(s)^2+B(s)^2} & -\frac{B(s)}{A(s)^2+B(s)^2} \\ \frac{B(s)}{A(s)^2+B(s)^2} & \frac{A(s)}{A(s)^2+B(s)^2} \end{bmatrix} \tag{6.47}$$

$A(s)$ and $B(s)$ depend on the product of the terms that represent the effect of the converter modulation, modeled by a ZOH, and the digital implementation of the controller and the measurement filters, expressed in the SRF: $A(s) = D_1(s)LPAF_1(s) - D_2(s)LPAF_2(s)$ and $B(s) = D_1(s)LPAF_2(s) + D_2(s)LPAF_1(s)$.

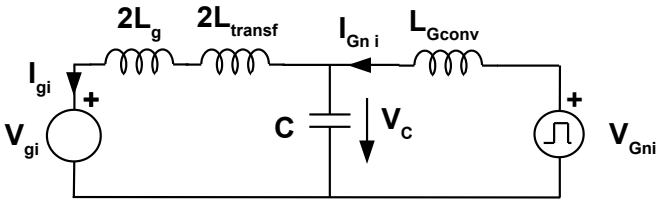


Figure 6.72: Normal current circuit for the LCL filter.

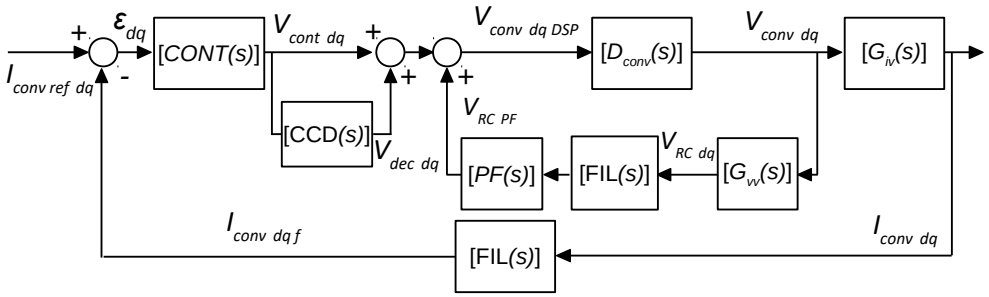


Figure 6.73: Matrix diagram of the current control loop including the decoupling strategy.

The $[CCD(s)]$ matrix is given by:

$$[CCD(s)] = \begin{bmatrix} 0 & -\frac{\omega_0 L_{Gconv}}{L_{Gconv}s+R_{Gconv\ s}} \\ \frac{\omega_0 L_{Gconv}}{L_{Gconv}s+R_{Gconv\ s}} & 0 \end{bmatrix} \tag{6.48}$$

In this control loop $FIL(s)$ is the product of a low pass hardware filter and the moving average filter (MAF) that was already introduced in Chapter 2. This filter attenuates the switching frequency harmonics and its multiples and is implemented in an FPGA running ten times faster than the DSP.

The CCD and the PI controller are adjusted by following the design process described in Chapter 3 for the parameters summarized in Table 6.3, taking into account the reference tracking performance and the grid rejection disturbance capabilities. It can be seen in Table 6.3 that the range of variation of the SCRs

Table 6.3: System parameters for the single-block.

Parameter	Symbol	Value
Converter inductance	L_{conv}	90x2 μH
Converter inductance series resistance	$R_{conv\ s}$	2 $m\Omega$
Transformer leakage inductance	L_{transf}	1 mH
Transformer series resistance	$R_{transf\ s}$	3 $m\Omega$
Filter capacitor	C	900 μF
Damping resistor	R_d	0.05Ω
Short-circuit ratio	SCR	1-200
Switching frequency	F_{sw}	3150
DSP sampling time	$T_{s\ DSP}$	158.73 μs
FPGA sampling time	$T_{s\ FPGA}$	15.873 μs
Low-pass analog filter time constant	τ_{lp}	53 μs

is limited to vary between 1 and 200. This range of variation covers all the possible grids at which the power converter can be connected, and is coherent with the design performed of the *LCL* filter adjusted to fulfill the grid-current harmonic content limits imposed by the grid codes for a SCR greater than 1. It must be noted that in Table 6.3 the converter inductance is multiplied by two, given that the calculated inductance in the filter design was the parallel between the normal inductance of GSC1 and GSC2.

The Bode plots of the eigenvalues of the open-loop transfer matrix from $I_{conv\ dqf}$ to $V_{cont\ dq}$ are represented in Figure 6.74. As it can be seen, the frequency response of the eigenvalues is symmetric with respect to 0 Hz, meaning that the system is decoupled. It can also be observed that low

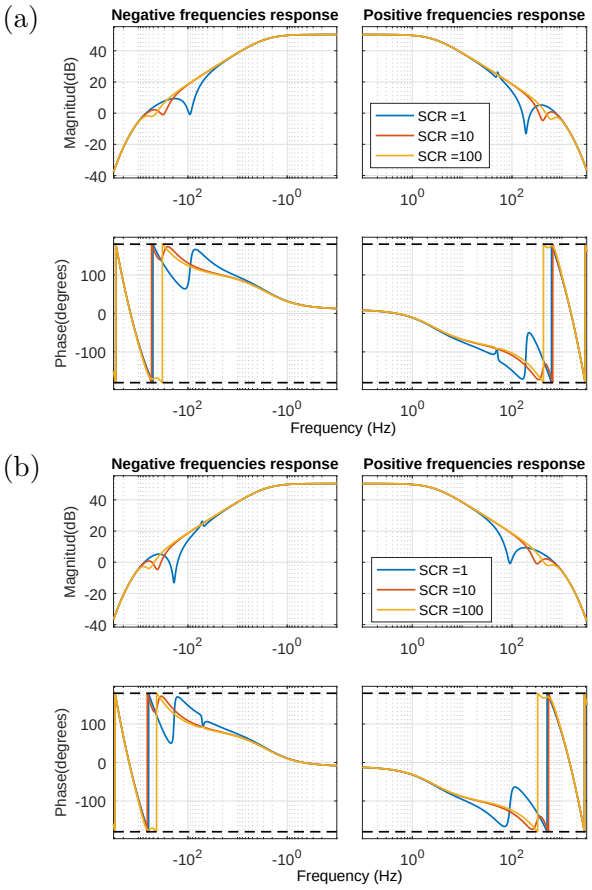


Figure 6.74: Bode plots of the eigenvalues of the open-loop transfer matrix from $I_{conv\ dqf}(s)$ to $V_{cont\ dq}(s)$.

variability exist between the plants at low frequencies, which is a desirable characteristic as explained in Chapter 3.

Adjusting a simple PI controller to achieve a cut-off frequency equal to 100 Hz with a phase margin of 40 degrees, a k_p equal to 0.1 and a T_n equal to 0.032 are obtained. The eigenvalues of the open-loop transfer matrix are represented in Figure 6.75 from $I_{conv\ dqf}(s)$ to $\varepsilon_{dq}(s)$. The emulated series resistance is selected to be three times bigger than the actual converter

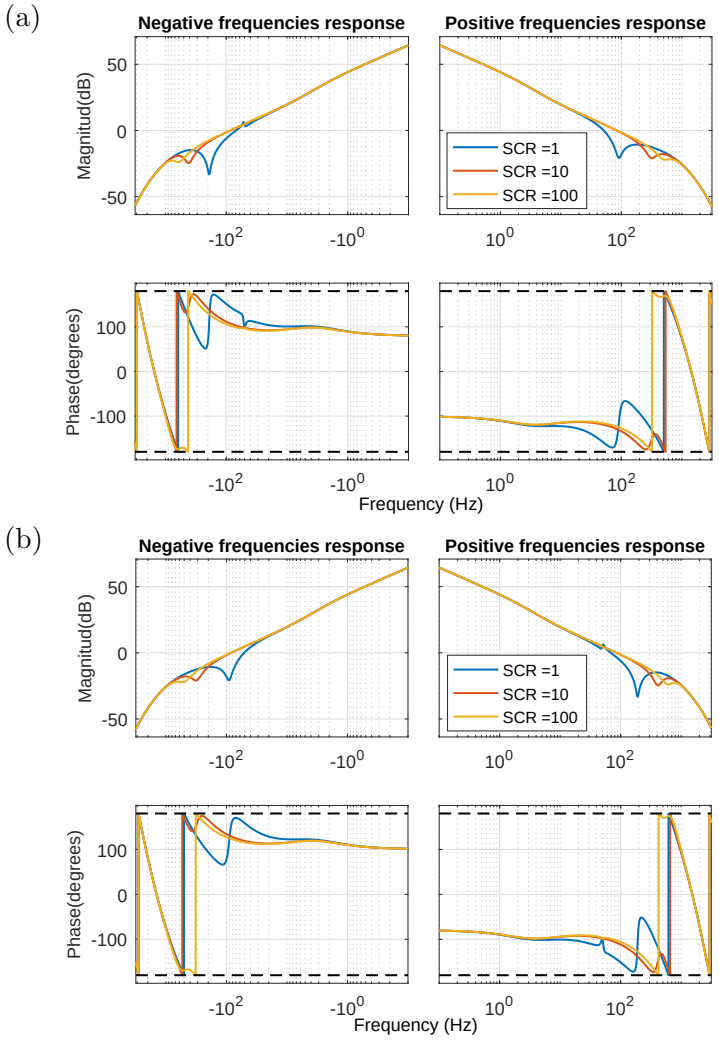


Figure 6.75: Bode plots of the eigenvalues of the open-loop transfer matrix from $I_{conv\ dqf}$ to ε_{dq}.

inductor series resistance, in order to increase the rejection to grid disturbances. The step response for the control-loop designed in this section is represented in Figure 6.76.

The designed control strategy guarantees the tracking of the normal current component. Nevertheless, this controller is also applied to the cross-current differential component. In [JUA14] was shown that if the impedance of the inductive coupling is greater than the impedance of the normal component up to the current controller bandwidth, the differential cross-current is more stable than the normal-current. This is the case under consideration thanks to the integrated inductor, so no stability problems are faced in the cross-current component.

In Subsection 6.8.5 simulation results will be shown to validate the results obtained.

6.8.3 Tuning of the AD strategy

In Subsection 6.8.2 the current control loop has been designed when the *LCL* resonance frequency is properly damped by a passive resistor. However, it has already been demonstrated that the power losses can be reduced if an active damping strategy is implemented, eliminating the passive damper. In the following, the AD strategy presented in Chapter 4 is adapted for the single-

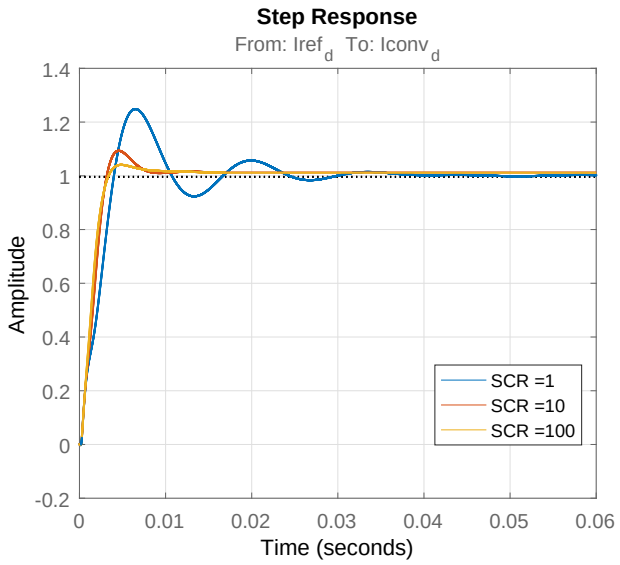


Figure 6.76: Normal current step response.

block power converter.

The matrix representation of the active damping control structure proposed in Chapter 4 is represented for the single-block structure in Figure 6.77, with the AD path in green. The adjustment of the AD strategy requires the proper implementation of the derivative $[Der(s)]$ and the adjustment of the proposed $[H_{AD}(s)]$.

Initially, the system without the AD, once the passive resistor is eliminated, is unstable for the cases with a SCR equal to 10 and 100. This instability is obtained at the LCL resonant poles, as indicated by the closed loop representation of the zero-pole map made in Figure 6.78. Four unstable poles are obtained for the SCR equal to 100, and two for the SCR equal to 10, meaning that an AD strategy is required. For the SCR of 1, the system is already stable, as the resonance frequency is low, and consequently, also the delay in the positive-feedback of the capacitor voltage. In this way, for the first SCRs, the system will be stabilized by this control loop, while for stronger grids, and AD strategy is required. If the SCR can vary from 1 to infinity, the LCL resonance frequency can vary from 625 Hz to 1306 Hz.

First of all, to damp the system, an accurate derivative is required within the limits of variation of the LCL resonance frequency. To achieve this accurate derivative the multisampled derivative performed in the already existing FPGA is used. This FPGA runs 10 times faster than the DSP, highly reducing the phase distortion of the derivative within the possible interval of LCL resonance frequencies, Figure 6.79. If the conventional

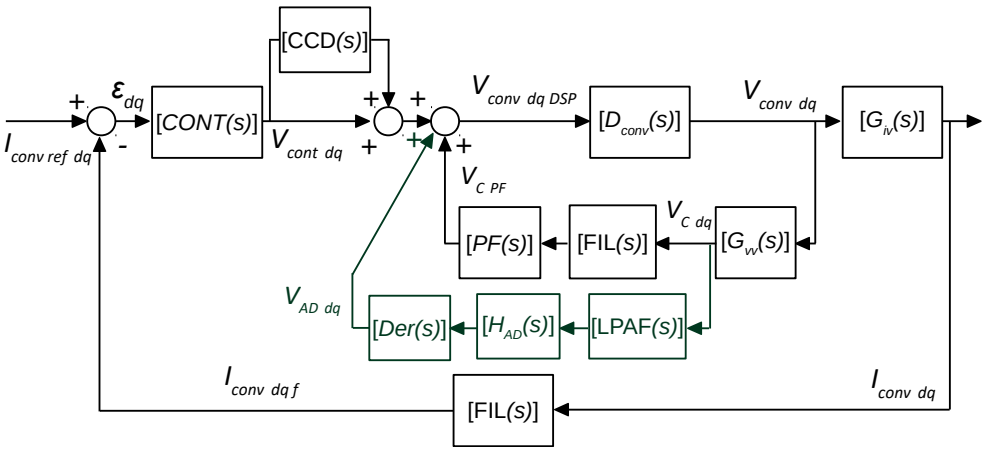


Figure 6.77: Control loop diagram including the AD of the LCL resonance.

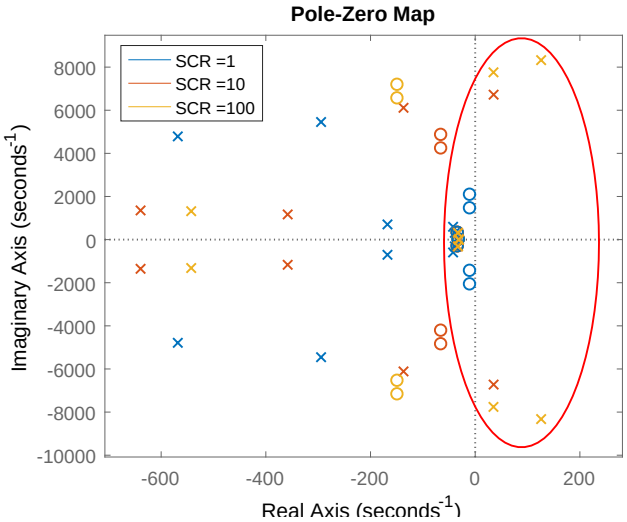


Figure 6.78: Closed-loop poles and zeros without damping the LCL poles.

derivative is used instead of the multisampled one, 40 degrees are lost at the highest possible resonance frequency.

As a high frequency derivative is performed, it also has to be guaranteed

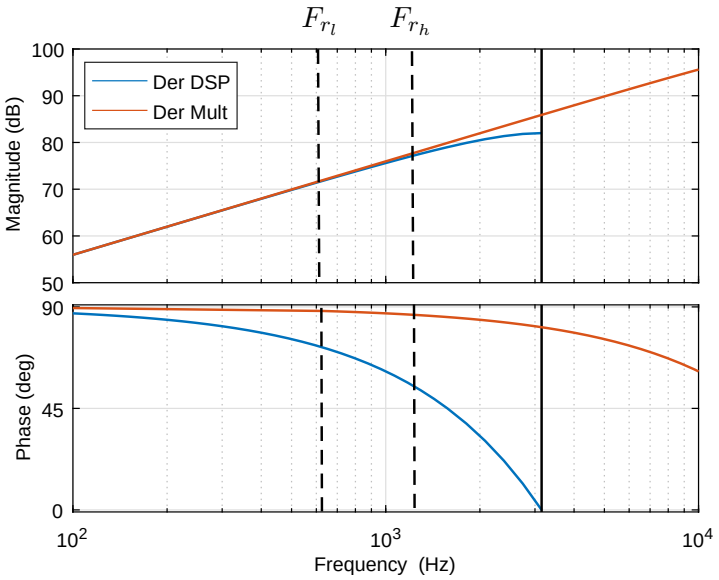


Figure 6.79: Bode plot of the multisampled derivative and the conventional derivative.

that noise amplification is avoided by a proper filtering solution. Moreover, it should be guaranteed that the delay in the AD feedback path is properly adjusted to avoid changes in the sign of the emulated virtual resistance, as it was already described in Chapter 4. Both goals are achieved by the proper adjustment of the transfer matrix $[H_{AD}(s)]$. $[H_{AD}(s)]$ is a diagonal transfer matrix, whose terms are obtained from the product of a band-pass filter, $BPF(s)$, and an adjustable delay, $DAD(s)$.

The bandpass filter is adjusted to attenuate the switching harmonics and the low frequency components of the capacitor voltage, reducing the required control action and immunizing the system against noise amplification. It must be reminded that the measured capacitor voltage is already filtered by the low-pass analog filter, $[LPAF(s)]$, as represented in Figure 6.77. In the general design procedure presented in Subsection 4.3.3, as a general rule to achieve these goals, the lower stop-band is set at half the lowest LCL resonance frequency, $F_{r_l}/2$, and the highest stop-band is set at $(F_{r_h} + F_{sw})/2$, F_{sw} being the switching frequency. By designing the filter with this approach, $BPF(s)$ has the frequency response provided in Figure 6.80. It should be noted that thanks to the application of interleaving in GSC with a phase shift of 180 degrees, the capacitor voltage used for the AD strategy has its main harmonics located at the even multiples of the switching harmonic families. This families are seen as low frequency alias

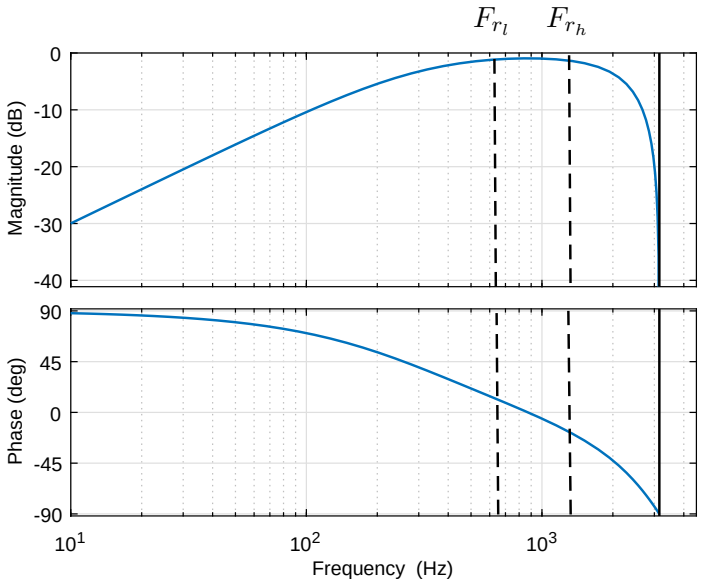


Figure 6.80: Bode plot of the band-pass filter.

according to Equation 6.49, as the DSP samples the variables twice per switching period, and are highly attenuated by the adjusted band pass-filter.

$$F_{alias} = |F_{s_{DSP}} - F_{real}| \tag{6.49}$$

After the adjustment of $BPF(s)$, the delay in the AD feedback path has to be adjusted. In Chapter 4, Equation 4.10 was proposed for the systematic adjustment of the delay, that is implemented in the DSP by the linear interpolation approach $DAD(z)$. The phase of the emulated virtual impedance, according to the representation made in Figure 6.77 depends on $[D_{conv}(s)]$, $[LPAF(s)]$ and $BPF(s)$. The information of these transfer functions is substituted in Equation 4.10, obtaining a required delay equal to 1.37 sampling times in order to have a pure virtual resistor at the central resonance frequency. With the phase adjustment, the design of H_{AD} is completed. The real part of the emulated virtual impedance is represented in Figure 6.81. Again, a pure virtual resistance is obtained at the central resonance frequency. For the lowest resonance frequencies, the resistive component is reduced by five times, providing the AD a lower damping to the resonant poles. However, this is not an issue, as the system is already stable for low SCRs by the action of the capacitor voltage positive-feedback.

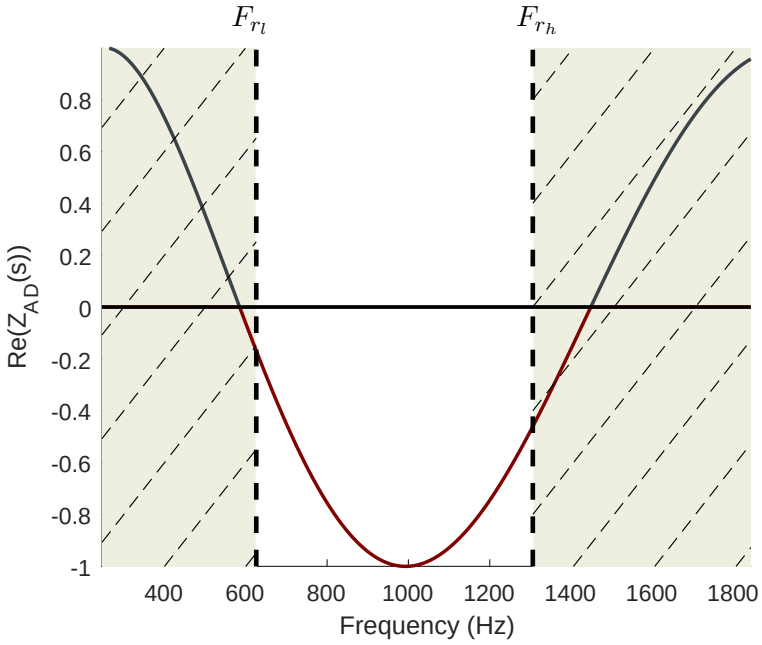


Figure 6.81: Variation of the virtual impedance real part with frequency.

To conclude the design of the CVDAD strategy, the last step is the selection of the emulated virtual resistor. The optimal damping at the LCL resonant poles is provided by an emulated virtual resistor equal to 0.55 Ω. The evolution of the resonant poles is plotted in Figure 6.82 for several resistor values and a SCR of 100, showing that a value of 0.55 Ω is the optimal value to be emulated. The four unstable poles are stabilized, proving the effectiveness of the proposed AD strategy.

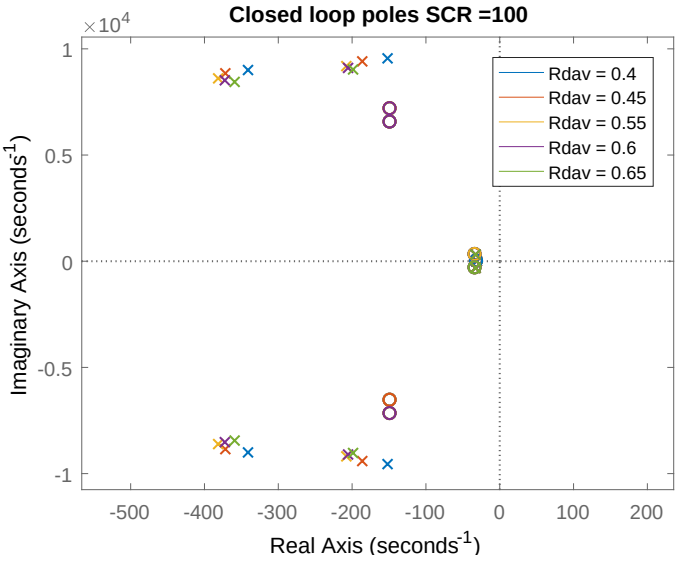


Figure 6.82: Closed-loop poles and zeros with the CVDAD strategy for a SCR equal to 100.

In Subsection 6.8.5 the performance of the AD strategy adjusted is evaluated through the simulations performed in a detailed model of the single-block power converter.

6.8.4 Homopolar current control

The differential current components, both the normal and the cross-current, are effectively controlled by means of the control loops implemented in the two previous section. However, there is a current component, the homopolar cross-current, that is not affected by the two control loops programmed in the dq axis.

Even though the master-slave implementation of the discontinuous modulation guarantees that no jumps occur in the homopolar current component, if an specific control is not implemented for this component, and

slightly different common-mode components are introduced by the two power converters connected in parallel, this current component will grow steadily. To avoid this issue, an homopolar current control-loop is tuned in this subsection.

The plant to be controlled is purely inductive, as represented in Figure 6.83. L_{GI} stands for the magnetic inductance of the IPT and $L_{Mconv\ l}$ for the leakage inductance of the converter side inductor.

MSC switches synchronously, so $V_{M1\ h}$ and $V_{M2\ h}$ are equal and do not contribute to the homopolar current component if both DC-buses are equal. The equality of both DC-buses is guaranteed in steady state by GSC1 and GSC2. In this way, the only voltage difference that drives the homoplar current is created by $\Delta V_h = V_{G1\ h} - V_{G2\ h}$. Ideally, the average homopolar voltages in every sampling period, $\bar{V}_{G1\ h}$ and $\bar{V}_{G2\ h}$ are equal, and consequently, $\Delta\bar{V}_h = 0$. However, to control the homopolar current component, the average homopolar voltage can be modified in GSC1, for example, in order to modify the circulating current component. A net homopolar voltage component can be introduced at a given sampling period by modifying the duration of the zero vectors of GSC1 without affecting the modulated reference vector. If this net homopolar voltage is introduced by GSC1, the homopolar voltage of this power converter would be equal to $\bar{V}_{G1\ h} + \delta v_h$ and $\Delta\bar{V}_h = \delta v_h$. With this definition, the average model circuit is represented by the circuit in Figure 6.84.

The plant transfer function is given by:

$$\frac{I_{hom}}{\delta v_h} = \frac{1}{L_h s} \tag{6.50}$$

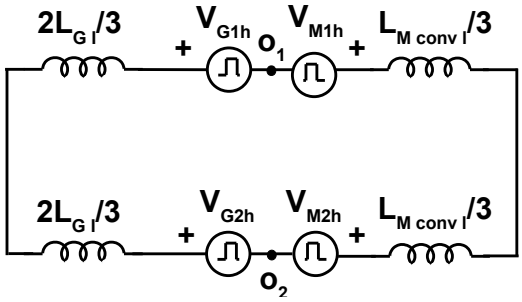


Figure 6.83: Model for the homopolar current component.

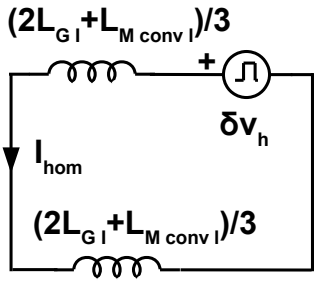


Figure 6.84: Average model for the homopolar current component control.

where L_h is equal to $2(2L_{G\ I} + L_{Mconv\ l})/3$. The homopolar current control loop block-diagram can be represented according to Figure 6.85. The homopolar current reference is zero, to which the homopolar current component is subtracted. A PI controller is responsible of calculating the required homopolar voltage in order to drive the actual homopolar current to zero. This voltage is normalized with respect to the DC-bus half voltage. It has a negative sign because the controller provides a modification of the negative zero vector, obtaining the required increment of the negative zero voltage in GSC1. As previously indicated, the homopolar control loop only actuates on the zero voltages of GSC1. If a positive homopolar current is obtained, the error is negative and the action V_h will be negative. If this action is normalized with respect to half the DC-bus voltage without the negative sign, a negative time increment on the zero vector of GSC1 will be calculated. If the time duration of the negative zero vector is decreased, δv_h will be negative and the homopolar current will be increased, creating an unstable system.

The homopolar control loop does not have to be fast, because the homopolar cross-current is created by nonidealities and small errors introduced by both power converters. This control loop tries to avoid the accumulation

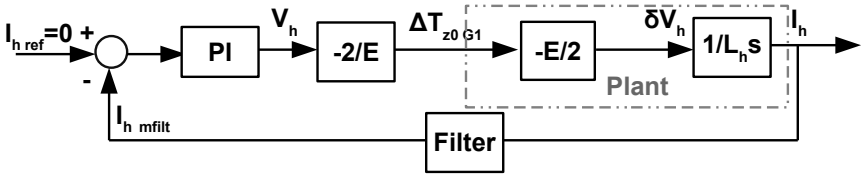


Figure 6.85: Block diagram for the homopolar current component control.

of these errors and for this reason, the homopolar control loop bandwidth is designed to be 10 Hz. All the elements in the plant are known inductors, so the design of the design of this control loop doe not present any challenges. The three phase individual current components are measured and filtered by the $LPAF(s)$ and the MAF, and added together. So the *Filter* represented in Figure 6.85 is the product of $LPAF(s)$ and MAF. With this consideration the PI parameters for the homopolar current component can be calculated. In Figure 6.86 the Bode plot of the open-loop transfer function is represented. It can be seen that with a k_p equal to 0.0063 and a T_n of 0.3183, the desired bandwidth is achieved with a phase margin equal to 85 degrees.

However, even the design of the controller is simple, the implementation of the control strategy with DSVPWM is not straightforward. This control strategy is based on the modification of the zero negative vector of GSC1 to control the homopolar cross-current. Nevertheless, if the negative zero vector is increased, the positive zero vector has to be decreased accordingly, in order to avoid a modification on the reference vector in GSC1. This can be easily done with the SVPWM7. With the DSVPWMs, only one zero vector is used in each power converter. In order to be able to implement this control strategy for the homopolar component, some intermediate states of SVPWM7 are required. This transition to SVPWM7 from DSVPWM increases the power losses, for this reason, the number of times that the correction is applied should

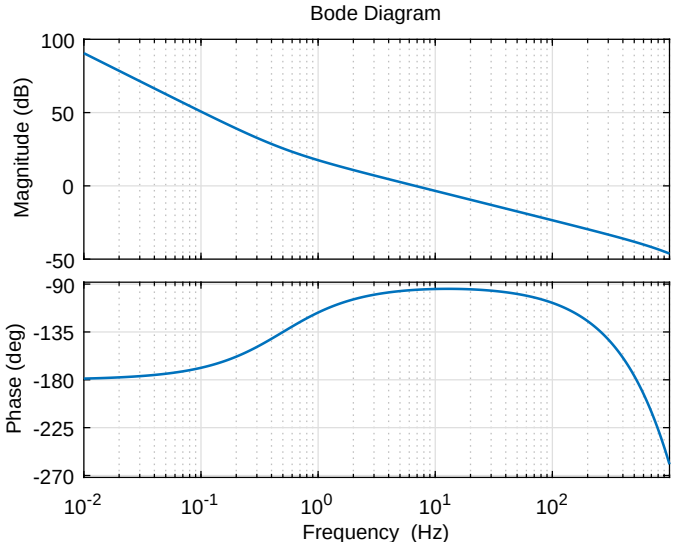


Figure 6.86: Bode plot of the open-loop homopolar current controller.

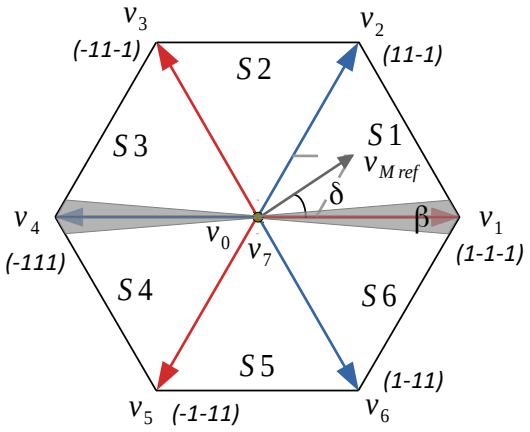


Figure 6.87: Implementation of the homopolar current control with DSPWM.

be minimized.

The homopolar current control bandwidth has been selected to be 10 Hz, five times slower than the fundamental frequency. If the action is applied twice per fundamental period, with an update frequency equal to 25 Hz, a good compromise between the increase in the power losses and the reduction of the homopolar current can be achieved. In Figure 6.87, the implementation of the control with the DSVPWM is represented. The two gray areas around v_1 and v_4 re the regions where the modulation is modified to use a SVPWM7 with the homopolar control. To guarantee that the correction is applied during a sampling period, an angle β of 2.9 degrees is defined, and if the reference vector is located within the gray area, the modulation is changes and the control actuates. In these areas, close to the transition between each sector, is where more zero vector is available, and thus, they are the best to use the compensation.

6.8.5 Simulation results

As a first step, the current control adjusted in Subsection 6.8.2 for GSC1 and GSC2 is tested. This control loop is programmed in C, and controls the power converter modeled in *Matlab* by means of the *Simpower* toolbox. The simulations are performed for a SCR of 10, as it allows to test the current controller dynamic response and the stabilizing effect of the AD at the *LCL* resonance frequency.

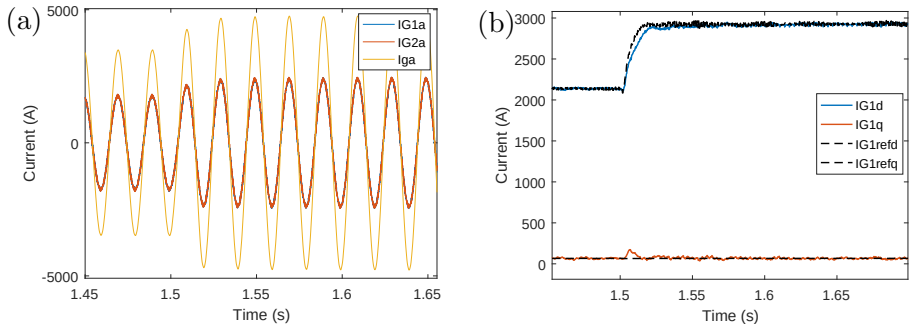


Figure 6.88: Current controller step-response: temporal waveforms (a) and decomposition in the dq axis (b).

The response of the current controller is analyzed in Figure 6.88, when a step current is injected by MSC in the DC-bus and the DC-bus voltage regulator modifies the reference current in the d-axis, as it is the axis aligned with the grid voltage. In Figure 6.88 (a) the temporal waveforms of the real converter currents in GSC1, GSC2 and the grid in phase a are represented, while in Figure 6.88 (b) the projection of the currents of GSC1 in the dq axis are represented. As it can be concluded, the tracking of the reference is achieved, with a reduced cross-coupling between both axis.

Once the reference tracking has been verified, the effectiveness of the AD

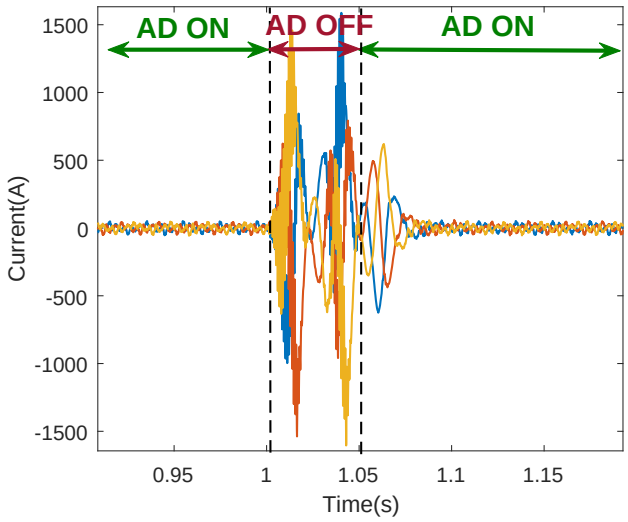


Figure 6.89: Grid current transient response as the AD is deactivated and activated again.

strategy is verified by transiently disabling the CVDAD control loop. The result of this simulation is plotted in Figure 6.89. For the representation made in Figure 6.89 the AD is transiently disabled and enabled again, representing the grid current waveforms during this period of time. Initially, the power converter is connected to the grid with an almost zero reference current. At the time instant marked with the dashed line, the CVDAD is deactivated, becoming the system unstable. As it is activated again, 50 ms later, the system recovers from instability.

6.9 Parallelization of single-blocks for higher power wind turbines

As a final step, the single block conversion structure is extended for bigger wind turbines, in the range from 8 to 9 MW. This power ratings can be achieved by using two single-block power converters in parallel. The use of a modular and scalable single-block provides greater reliability, as if one of the conversion lines has a failure and is disconnected, the wind turbine can still operate at a reduced power. However, the parallelization strategy may vary depending on the different types of wind turbines.

There are two main trends in current high power wind turbines with PMGs [AND07, BIR07]; PMGs with multiple three-phase stator windings and PMGs with a single three-phase stator winding. High power generators are constructively build out of several three-phase windings, so in general, the use of PMGs with multiple three-phase stator windings is the dominant approach. In some occasions, even though the generator is built out of electrically independent windings, they are parallelized internally so at the output there are only three phases available. Depending on the wind turbine, coupling in parallel the single-block topology developed is straightforward or requires further actions.

6.9.1 Wind turbine with multiple three-phase stator windings

This parallelization option is represented in Figure 6.90. As there is no electrical connection between the two single-blocks, no homopolar currents can be recirculated between them. Differential components can be recirculated, but those are already limited by the integrated inductor used for the parallel connection in each single-block. In this way, the parallelization of single-blocks with independent stator windings can be directly performed as represented in Figure 6.90.

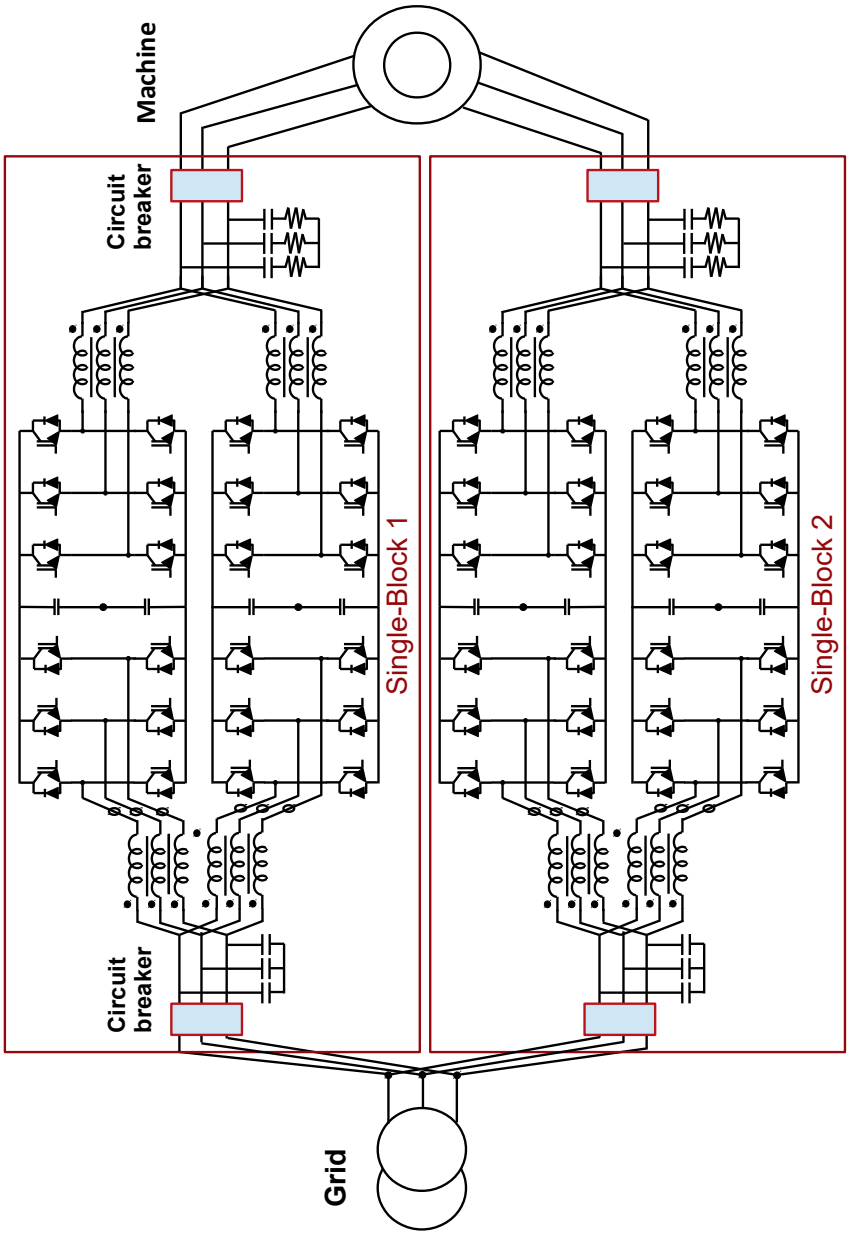


Figure 6.90: Parallelization of single-blocks with independent stator windings.

6.9.2 Wind turbine with a single stator winding

As represented in Figure 6.91, in this case, an homopolar current component can circulate between both power converters. Moreover, this current component will be only limited by the leakage inductance of the integrated inductor used in GSC and the converter leakage inductances in MSC. An additional homopolar current control loop has to be implemented for the low frequency circulating components between the two single-blocks. The first single-block power converter, is controlling with GSC1 the homopolar current component being recirculated within the conversion stage. Similarly, the homopolar circulating current component within the second singe-block is also controlled. In this way, there is not a control of the circulating homopolar current components between the two single-blocks. The single-block output current in the three-phases, already measured in MSC, can be used to implement proportional independent controllers in both single-blocks. The other alternative is using a PI controller in the first single block and no control in the second one. Additionally, to limit the high frequency homopolar circulating currents between both single-blocks, an additional inductor should be added. As an alternative, a less optimized inductor, such as the three-column singe-phase IPT could be used in GSC to limit the circulating currents, as it will offer an inductance to the homopolar current component between the two conversion structures.

The carriers have to be synchronized to avoid high circulating between the MSCs of both single-blocks, as they only include the three-phase inductors of the *dv/dt* filter.

6.10 Conclusion

In this chapter the extension of all the previous techniques to parallel power converters is addressed. This is motivated by the need of high-power low-voltage back-to-back power converters for offshore wind turbines. A basic 4 MW conversion structure denominated single-block has been established, parallelizing the single-block for WECS in the range of 8-12 MW. This single block is based on the parallelization of two back-to-back conversion structures. To achieve this solution, initially, a review of the state-of-the-art parallelization solutions of power converters is presented. This review is focused on the different approaches to couple power converters in parallel: inductive coupling and direct coupling. The inductive coupling is the most interesting option, as it allows the implementation of advanced modulation strategies between the parallel power converters, achieving reductions in the size and cost of the

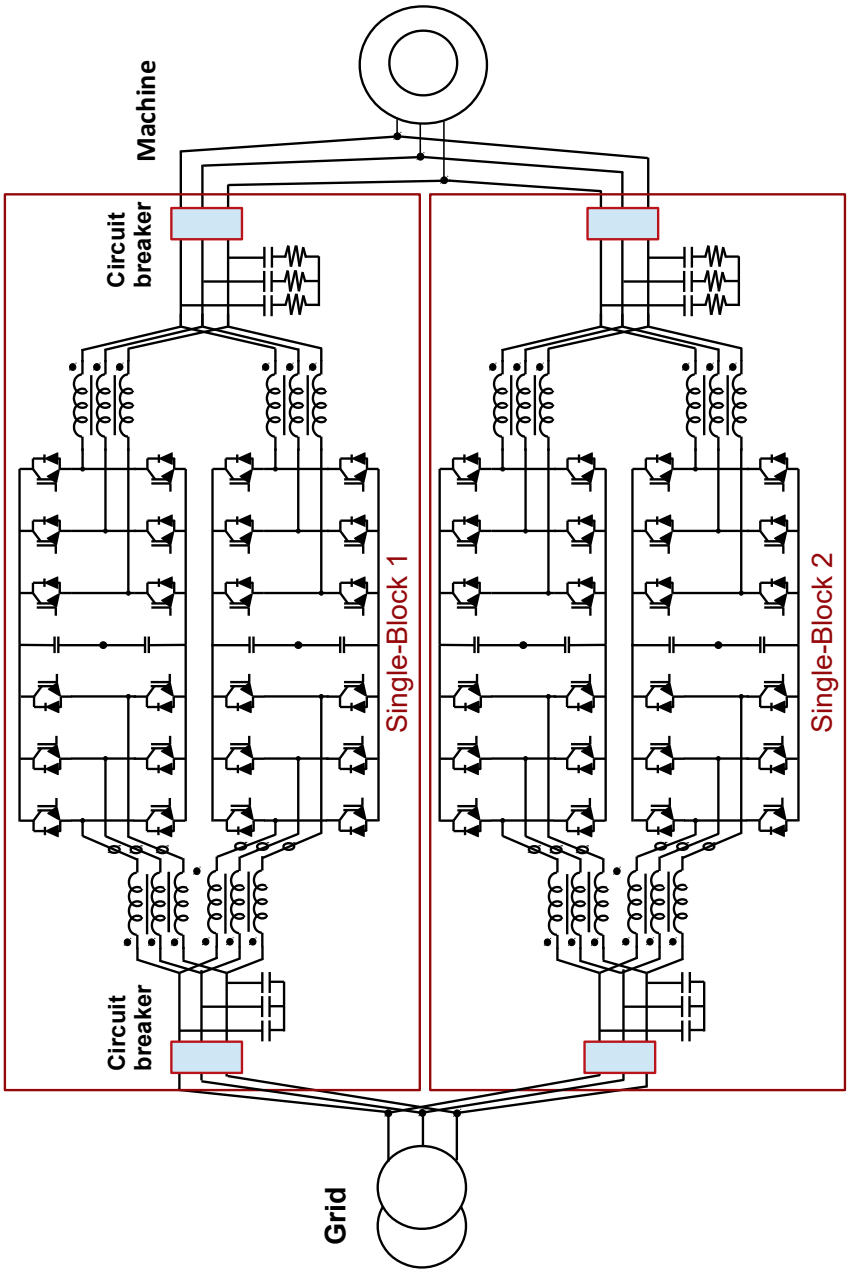


Figure 6.91: Parallelization of single-blocks with a single stator windings.

passive components; such as the DC-bus capacitors or the *LCL* output filter.

As a first step to determine the best topology for the single-block power converter, appropriate models to characterize the interaction between parallel power converters are developed. These models define the voltages and currents that determine the requirements and design of the passive components. As a result of the state of the art review and the modeling of the parallel connection of power converters, the base topology for the single-block is determined: two B2B power converters are directly coupled in MSC and through a non-isolated inductive coupling, using interphase transformers, in GSC, while the dc-buses are independent.

From these models, the influence of the modulation on the different converter components is analyzed. The modulation techniques are compared in terms of efficiency, common-mode and phase-to-ground voltages and grid-current quality. The use of GDSVPWM with a master-salve implementation in GSC is proposed. The switching losses can be reduced by a half, achieving a high quality in the grid current harmonic content by the application of interleaving. As MSC uses synchronous switching, the phase-to-ground and common-mode voltages are increased by a 16%. For this modulation an *LCL* output filter has been designed to fulfill one of the most stringent grid-codes, the German BDEW. For this grid-code, the low SCRs require greater output inductors.

The control techniques proposed in th previous chapters, can be directly applied to these systems, achieving the appropriate dynamic response of the whole system. An additional homopolar current control loop is required in the single block to control this current component to zero.

To conclude the analysis performed, the requirements to use the single-block power converter for larger wind turbines are discussed, depending on the stator winding configuration of the generator.

Chapter 7

Conclusions and future lines

7.1 Conclusions

Wind power is currently the most extended renewable energy used for electricity generation purposes, closely followed by photovoltaic power. As wind power is installed in new remote areas, its connection to weak grids is becoming more popular, arising new challenges from the power converter control point of view. Moreover, the large amount of wind turbines connected to the grid in countries such as Germany, Spain or China is bringing the development of stringent grid codes, the power converter being the main responsible of this fulfillment.

The visual impact of wind turbines, the saturation in land of the best locations for wind power generation and the steadier winds that can be found on the sea, is creating an important offshore market that is steadily growing and achieving new milestones, such as the grid connection of the first floating wind farm in Scotland in 2017. Moreover, the power ratings of the wind turbines commercially available for offshore applications are reaching nowadays the range of 8-9 MW, and models of 12 MW have been already announced.

This thesis addresses some of the issues related to the trends in wind energy conversion systems. The connection of wind turbines to weak grids brings stability problems, both in the grid current control loop and at the *LCL* output filter resonance frequency, which is strongly influenced by the grid impedance. Moreover, the grid codes demand faster transient responses to renewable facilities, in order to respond to grid transients. To properly characterize the instabilities and the system response of a grid-connected power converter, a detailed modeling approach in the synchronous reference

frame is presented in Chapter 2. This model characterizes the system accurately at low and high frequencies, where both instabilities, of the current control loop and the *LCL* resonant poles take place. This model reveals that the measurement filters, commonly neglected in the literature, have a strong influence on the stability, as reflected in Chapter 3 and Chapter 4. In this chapter, the basis for the analysis performed to the common-mode and phase-to-ground voltages are also established.

The design of a robust current controller that provides stability and the desired dynamic response for strong and weak grids is addressed in Chapter 3. In this chapter, a novel decoupling structure based on an improved capacitor voltage positive feedback and a cross-controller decoupler has been presented for a *LCL* filter controlled in the SRF. The improved capacitor voltage positive-feedback reduces the plant variability at low frequencies, a variability that is mainly introduced by the grid inductance. Once this variability is eliminated, and the behavior of a pure inductance, equal to the converter output inductance, is obtained at low frequencies, a simple first order function is used to eliminate the cross-couplings. In this thesis, the transfer fucntion of the converter inductor is used, computing the voltages required to compensate the cross-coupling. In this way, the use of the converter currents is avoided, reducing the delay. With this decoupling strategy, a greater independence of the response of both orthogonal axis is achieved, improving the converter's dynamic response. This approach presents better transient response compared to other decoupling strategies, specially in weak grids. In weak grids, without a decoupling strategy, stability problems appear, reducing the phase margins and the achievable controller bandwidth. This problems are solved with the approach proposed in Chapter 3. The decoupling strategy developed is robust against variations in the system parameters. Enhanced rejection to grid disturbances can be provided by using an inner loop that emulates a greater inductance series resistor or without adding an additional inner loop, by implementing a greater virtual resistor in the cross-controller decoupler than the actual equivalent inductor's series resistor. Moreover, the experimental results validate the approach presented, showing an almost perfect agreement between the simulations and the results obtained in the experimental set-up.

The connection of wind turbines to weak grids, which may highly change the effective grid impedance as more power is connected to the point of common coupling, brings new challenges. A variable grid impedance modifies the effective *LCL* resonance frequency, causing instability or poor harmonic content in the high frequency range as a consequence of a poor damping. Increasing the passive damping resistor is a straightforward solution, but it

increases the power losses of the converter. In Chapter 4 a robust active damping strategy based on the capacitor voltage derivative is proposed. With the approach presented, the AD stability region is adapted to the optimized design of a given *LCL* filter and all the possible resonance frequencies resulting of a variable grid inductance, instead of imposing additional constraints on the *LCL* design procedure. This goal is achieved by means of an adjustable delay, presenting a systematic procedure to tune this delay in the active damping feedback path by means of an analytical expression. The design procedure and the analytical expression provided to adjust the delay are also applicable to the capacitor current proportional feedback active damping. To overcome the limitations of the derivative close to the control Nyquist frequency, a multisampled derivative is implemented, offering greater robustness against variations in the resonance frequency, as a result of a lower delay. The detailed model developed for the *LCL* filter and the converter current control loop allows to precisely adjust the active damping strategy. The solution proposed is costless, does not increase the power losses, and is based on the measurements available in grid-connected power converters and the existing digital systems to implement the multisampled derivative. The performance and robustness of the proposed AD have been tested through simulation and experimental results.

The active damping strategy guarantees the stability of the *LCL* resonant poles in grid connected power converters, reducing the total power losses, as the damping resistor might be even eliminated. To further decrease the power losses, a key aspect in renewable energies because it brings the reduction of the cooling requirements and the LCOE, is the modification of the modulation. In Chapter 5, the implementation of DSVPWMs in back-to-back power converters is analyzed and two modulation strategies are proposed. In back-to-back power converters, if GSC and MSC are modulated independently, the common-mode and phase-to-ground voltages reach the whole dc-bus voltage. To solve this issue, a modulation is proposed for back-to-back power converters that simultaneously allow to reduce the common-mode and phase-to-ground voltages to ±2E/3. These are the same voltage levels that if the classical SVPWM7 is used in B2B power converters, but reducing the number of commutations per switching period from 12 to 8, significantly improving the efficiency. This modulation is called DSVPWM-CMVR1, and forces MSC to use the same zero vector that GSC. To further reduce the common-mode voltage to ±E/3, another modulation is proposed that also forces MSC to use the same zero vector that in GSC, but uses both zero vectors in MSC in some sampling times to avoid the peaks of ±2E/3. For this modulation, only in particular switching periods the number

of commutations is increased to 10. The number of corrections depends on the modulation used in GSC and the modulation index in MSC. This modulation is called DSVPWM-CMVR2 and achieves the best efficiency and differential voltage when it is combined in GSC with the DSVPWM3. With the proposed modulations, the switching power losses are reduced without penalizing the phase-to-ground and common-mode voltages compared to SVPWM7. Experimental results validate the reduction of common-mode and phase-to-ground voltages with the proposed modulations.

The last trend addressed in this thesis is the extension of all the previous techniques to parallel power converters. This is motivated by the need of high-power low-voltage back-to-back power converters for offshore wind turbines. In Chapter 6, a basic 4 MW conversion structure denominated single-block has been established, parallelizing the single-block for WECS in the range of 8-12 MW. This single block is based on the parallelization of two back-to-back conversion structures. To achieve this solution, initially, a review of the state-of-the-art parallelization solutions of power converters is presented. This review is focused on the different approaches to couple power converters in parallel: inductive coupling and direct coupling. The inductive coupling is the most interesting option, as it allows the implementation of advanced modulation strategies between the parallel power converters, achieving reductions in the size and cost of the passive components; such as the DC-bus capacitors or the *LCL* output filter.

As a first step to determine the best topology for the single-block power converter, appropriate models to characterize the interaction between parallel power converters are developed. These models define the voltages and currents that determine the requirements and design of the passive components. As a result of the state of the art review and the modeling of the parallel connection of power converters, the base topology for the single-block is determined: two B2B power converters are directly coupled in MSC and through a non-isolated inductive coupling, using interphase transformers, in GSC, while the dc-buses are independent.

From these models, the influence of the modulation on the different converter components is analyzed. The modulation techniques are compared in terms of efficiency, common-mode and phase-to-ground voltages and grid-current quality. The use of GDSVPWM with a master-salve implementation in GSC is proposed. The switching losses can be reduced by a half, achieving a high quality in the grid current harmonic content by the application of interleaving. As MSC uses synchronous switching, the phase-to-ground and common-mode voltages are increased by a 16%. For this modulation an *LCL* output filter has been designed to fulfill one of the

most stringent grid-codes, the German BDEW. For this grid-code, the low SCRs require greater output inductors.

The control techniques proposed previously, can be directly applied to these systems, achieving the appropriate dynamic response of the whole system. An additional homopolar current control loop is required in the single block to control this current component to zero.

To conclude the analysis performed, the requirements to use the single-block power converter for larger wind turbines are discussed, depending on the stator winding configuration of the generator.

7.2 Contributions

The main contributions of this thesis are summarized in this section.

Predoctoral scholarship

This research as been awarded with a grant from the Public University of Navarre for the training of researchers. The call was published in December the 2^{nd}, 2014, under the resolution 1488/2014, awarded in May 27^{th} 2015.

Contributions to international journals

- J. Samanes, A. Urtasun, E. Gubía, A. Petri: *Robust Multisampled Capacitor Voltage Active Damping for Grid-Connected Power Converters*. International Journal of Electrical Power and Energy Systems, Elsevier, 2018.

- J. Samanes, E. Gubía, X. Juancorena, C. Girones: *Common-Mode and Phase-to-Ground Voltage Reduction in Back-to-Back Power Converters with Discontinuous PWM*. IEEE Transactions on Industrial Electronics (Under review).

Contributions to international conferences

- J. Samanes, E. Gubía: *On the Limits of the Capacitor-Voltage Active Damping for Grid-Connected Power Converters with LCL Filter*. Nineteenth IEEE Workshop on Control and Modeling for Power Electronics, IEEE COMPEL 2018.

- J. Samanes, E. Gubía, J. Lopez: M*IMO Based Decoupling Strategy for Grid Connected Power Converters Controlled in the Synchronous Reference Frame*. Nineteenth IEEE Workshop on Control and Modeling for Power Electronics, IEEE COMPEL 2018.
- J. Samanes, E. Gubía: *Multisampled-capacitor-voltage active damping for parallel interleaved grid connected voltage source converters with LCL filter*. 19th European Conference on Power Electronics and Applications 2017 (EPE'17 ECCE).
- J. Samanes, E. Gubía: *Sensorless active damping strategy for parallel interleaved voltage source power converters with LCL filter*. Applied Power Electronics Conference and Exposition (APEC), 2017 IEEE, 3632-3639.

Participation in public R&D projects

- "Advanced electronic power converters for grid integration of wind and photovoltaic systems", R&D National Plan, DPI2016-80641-R, Spanish State Research Agency (AEI) and FEDER-UE, 2017-2019.
- "Technologies for the grid integration of renewable energies: power electronics, storage, energy management and interaction", R&D National Plan, DPI2013-42853-R, Spanish State Research Agency (AEI) and FEDER-UE, 2014-2017.

Participation in private R&D projects

This thesis has been developed in collaboration with the company Ingeteam Power Technology SA under OTRI contracts:

- OTRI 2016 024 004: Optimization of power converters for low voltage offshore applications. From March 2016 to March 2019.
- OTRI 2014 024 084: Design of a multilevel converter in parallel configuration for wind energy applications.

Supervision of undergraduate final year projects

Furthermore, three undergraduate final projects related to this research have been co-directed by the author of the thesis. The titles of the projects and the students who developed them are:

- Gracia Arriazu, Rubén: *Design of a PIR controller for a single-phase inverter connected to the grid.* Final year project, bachelor's degree in Industrial Engineering. Public University of Navarre, 2017.

- Labiano Andueza, Daniel: *Design of a PIR controller for a three-phase inverter connected to the grid.* Final year project, bachelor's degree in Industrial Engineering. Public University of Navarre, 2017.

7.3 Future lines

Validation of the design procedure and performance of the single-block conversion structure

A detailed analysis and design approach has been developed and presented in Chapter 6 for the single-block power converter. However, the results obtained have been only validated through simulation, due to the existing time constraints.

To validate the design and control strategies developed, the construction of the single-block power converter based on two parallel back-to-back power converters have to be faced. Moreover, if two of these prototypes are build, they could be used to validate the last proposed future line.

Development of selective harmonic modulation techniques

Selective harmonic elimination techniques (SHE) have been normally applied to high power converters with low switching frequencies, such as thyristor rectifiers, to eliminate some of the low frequency harmonics introduced to grid. These techniques require as many switching pulses as harmonics want to be eliminated.

However, in the past years, these techniques have been extended to power converters with higher switching frequencies and IGBTs [WEL05a, WEL05b, WEL06, FRA07, AGE08, NAP10, KON16]. In these power converters, the main goal is to adjust the harmonic content to the limits imposed by the grid-codes, reducing the required output filter. For this reason, in these applications the SHE modulations are also called selective harmonic mitigation (SHM) techniques.

In the existing literature, SHM strategies have never been applied to back-to-back power converters, nor to back-to-back parallelized power converters. In this area, there is still an interesting field of research that can

bring potential reduction of the required output filter, as well as a reduction of the power losses. However, they present some inconvenients, such as the greater complexity to reduce the common-mode and phase-to-ground voltages, or how the AD strategy, which requires a fast response, is going to affected by a modulation that is based on pre-calculated switching patterns.

Optimal design of the inductive coupling of the IPT

The inductive coupling for the single-block has been selected and modeled, however, a design for this component has not been yet faced. This design is an optimization problem in its own, in which different materials and geometries play an important role. The IPT has to guarantee the required normal inductance and cross inductance to limit the circulating currents. Once the design is performed and validated through finite elements, it should be built in order to validate the theoretical losses calculations and design.

The inputs to the integrated IPT design procedure are also the result of an optimization problem. The reduction of the switching power losses with the use of GDSVPWM in parallel interleaved power converters, allows to increase the switching frequency, consequently reducing the size of the IPT but increasing the IPT power losses. This optimization procedure is considered a future line that will lead to the last future line.

Analysis and validation of the extension of the single-block power converter for power ratings from 8 MW to 12 MW

The single-bock power converter has a rated power of 4 MW, that can be parallelized as many times as required to increase its power ratings. The use of a modular and scalable single-block power converter provides greater reliability, as if one of the conversion lines has a failure and is disconnected, the wind turbine can still operate at a reduced power.

At the end of Chapter 6, a brief discussion on the application of the power converter to higher power wind turbines, by parallelizing several single-block modules, has been provided. An in depth analysis of the circulating currents is required, specially with the isolated coupling with different stator windings in the machine, as an inductive coupling exists between these windings that might create circulating currents. This research line has great interest and can be considered as the next step after this thesis.

Bibliography

[ABE05] T. Abeyasekera, C. M. Johnson, D. J. Atkinson, and M. Armstrong: *Suppression of line voltage related distortion in current controlled grid connected inverters*. IEEE Transactions on Power Electronics, 20(6):1393–1401, 2005.

[AGE08] V. G. Agelidis, A. I. Balouktsis, and C. Cossar: *On attaining the multiple solutions of selective harmonic elimination PWM three-level waveforms through function minimization*. IEEE Transactions on Industrial Electronics, 55(3):996–1004, 2008.

[AGO11] J. L. Agorreta, M. Borrega, J. López, and L. Marroyo: *Modeling and Control of N -Paralleled Grid-Connected Inverters With LCL Filter Coupled Due to Grid Impedance in PV Plants*. IEEE Transactions on Power Electronics, 26(3):770–785, 2011.

[AKH18] A. Akhavan, H. R. Mohammadi, and J. M. Guerrero: *Modeling and design of a multivariable control system for multi-paralleled grid-connected inverters with LCL filter*. International Journal of Electrical Power & Energy Systems, 94:354–362, 2018.

[ALE12] K. Alewine and W. Chen: *A review of electrical winding failures in wind turbine generators*. IEEE Electrical Insulation Magazine, 28(4), 2012.

[AND07] B. Andresen and J. Birk: *A high power density converter system for the Gamesa G10x 4, 5 MW wind turbine*. In *Power Electronics and Applications, 2007 European Conference on*, pages 1–8. IEEE, 2007.

[BAH11] B. Bahrani, S. Kenzelmann, and A. Rufer: *Multivariable-PI-Based dq Current Control of Voltage Source Converters With Superior Axis Decoupling Capability*. IEEE Transactions on Industrial Electronics, 58(7):3016–3026, 2011.

[BAO13] X. Bao, F. Zhuo, Y. Tian, and P. Tan: *Simplified feedback linearization control of three-phase photovoltaic inverter with an LCL filter*. IEEE Transactions on Power Electronics, 28(6):2739–2752, 2013.

[BAR15] E. Barrios: *Modelado y metodología analítica de diseño de transformadores de potencia y alta frecuencia: análisis de los devanados, optimización de eficiencia y densidad de potencia e integración en el diseño de convertidores electrónicos*, 2015.

[BDE08] BDEW, *Technical Guideline: Generating Plants Connected to the Medium- Voltage Network*, 2008.

[BER16a] R. N. Beres, X. Wang, F. Blaabjerg, M. Liserre, and C. L. Bak: *Optimal Design of High-Order Passive-Damped Filters for Grid-Connected Applications*. IEEE Transactions on Power Electronics, 31(3):2083–2098, 2016.

[BER16b] R. N. Beres, X. Wang, F. Blaabjerg, M. Liserre, and C. L. Bak: *Optimal design of high-order passive-damped filters for grid-connected applications.* IEEE Transactions on Power Electronics, 31(3):2083–2098, 2016.

[BER16c] R. N. Beres, X. Wang, M. Liserre, F. Blaabjerg, and C. L. Bak: *A Review of Passive Power Filters for Three-Phase Grid-Connected Voltage-Source Converters.* IEEE Journal of Emerging and Selected Topics in Power Electronics, 4(1):54–69, 2016.

[BHI11] R. Bhide, S. Kulkarni, and P. Bhandarkar: *Analysis of five-legged transformer used for parallel operation of rectifiers by coupled circuit-field approach.* IEEE Transactions on Power Delivery, 26(2):607–616, 2011.

[BIR07] J. Birk and B. Andresen: *Parallel-connected converters for optimizing efficiency, reliability and grid harmonics in a wind turbine.* In *Power Electronics and Applications, 2007 European Conference on*, pages 1–7. IEEE, 2007.

[BLA96] V. Blasko and V. Kaura: *A novel control to actively damp resonance in input LC filter of a three phase voltage source converter.* In *Applied Power Electronics Conference and Exposition, 1996. APEC'96. Conference Proceedings 1996., Eleventh Annual*, volum 2, pages 545–551. IEEE, 1996.

[BLA06] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus: *Overview of control and grid synchronization for distributed power generation systems.* IEEE Transactions on industrial electronics, 53(5):1398–1409, 2006.

[BRI00] F. Briz, M. W. Degner, and R. D. Lorenz: *Analysis and design of current regulators using complex vectors.* IEEE Transactions on Industry Applications, 36(3):817–825, 2000.

[BRO96] A. M. D. Broe, A. L. Julian, and T. A. Lipo: *Neutral-to-ground voltage minimization in a PWM-rectifier/inverter configuration.* In *1996 Sixth International Conference on Power Electronics and Variable Speed Drives (Conf. Publ. No. 429)*, pages 564–568, 1996.

[BUE09] E. J. Bueno, A. Hernandez, F. J. Rodriguez, C. Giron, R. Mateos, and S. Cobreces: *A DSP- and FPGA-Based Industrial Control With High-Speed Communication Interfaces for Grid Converters Applied to Distributed Power Generation Systems.* IEEE Transactions on Industrial Electronics, 56(3):654–669, 2009.

[CAC99] M. Cacciato, A. Consoli, G. Scarcella, and A. Testa: *Reduction of common-mode currents in PWM inverter motor drives.* IEEE transactions on industry applications, 35(2):469–476, 1999.

[CAV10] M. C. Cavalcanti, K. C. De Oliveira, A. M. De Farias, F. A. Neves, G. M. Azevedo, and F. C. Camboim: *Modulation techniques to eliminate leakage currents in transformerless three-phase photovoltaic systems.* IEEE Transactions on Industrial Electronics, 57(4):1360–1368, 2010.

[CHE96] S. Chen, T. A. Lipo, and D. Fitzgerald: *Modeling of motor bearing currents in PWM inverter drives.* IEEE Transactions on Industry Applications, 32(6):1365–1370, 1996.

[CHI13] J. Chivite-Zabalza, C. Girones, A. Carcar, I. Larrazabal, E. Olea, and M. Zabaleta: *Comparison of power conversion topologies for a multi-megawatt off-shore wind turbine, based on commercial Power Electronic Building Blocks.* In *Industrial Electronics Society, IECON 2013-39th Annual Conference of the IEEE*, pages 5242–5247. IEEE, 2013.

[COU11] B. Cougo, T. Meynard, and G. Gateau: *Parallel three-phase inverters: Optimal PWM method for flux reduction in intercell transformers.* IEEE transactions on Power Electronics, 26(8):2184–2191, 2011.

[DAN09] J. Dannehl, C. Wessels, and F. W. Fuchs: *Limitations of voltage-oriented PI current control of grid-connected PWM rectifiers with LCL filters.* IEEE Transactions on Industrial Electronics, 56(2):380–388, 2009.

[DAN10] J. Dannehl, F. W. Fuchs, S. Hansen, and P. B. Thøgersen: *Investigation of active damping approaches for PI-based current control of grid-connected pulse width modulation converters with LCL filters.* IEEE Transactions on Industry Applications, 46(4):1509–1517, 2010.

[DAN11] J. Dannehl, M. Liserre, and F. W. Fuchs: *Filter-based active damping of voltage source converters with LCL filter.* IEEE Transactions on Industrial Electronics, 58(8):3623–3633, 2011.

[DEP77] M. Depenbrock: *Pulse width control of a 3-phase inverter with non-sinusoidal phase voltages.* In *Conf. Record of IEEE/IAS Annu. Meeting*, pages 399–403, 1977.

[DON15] D. Dong, B. Wen, D. Boroyevich, P. Mattavelli, and Y. Xue: *Analysis of Phase-Locked Loop Low-Frequency Stability in Three-Phase Grid-Connected Power Converters Considering Impedance Interactions.* IEEE Transactions on Industrial Electronics, 62(1):310–321, 2015.

[DUE51] W. Duesterhoeft, M. W. Schulz, and E. Clarke: *Determination of instantaneous currents and voltages by means of alpha, beta, and zero components.* Transactions of the American Institute of Electrical Engineers, 2(70):1248–1255, 1951.

[ERD96] J. M. Erdman, R. J. Kerkman, D. W. Schlegel, and G. L. Skibinski: *Effect of PWM inverters on AC motor bearing currents and shaft voltages.* IEEE Transactions on Industry Applications, 32(2):250–259, 1996.

[EUR18] W. Europe: *The European offshore wind industry—Key trends and statistics 2017.* Wind Europe, page 37, 2018.

[FOR07] F. Forest, T. A. Meynard, E. Laboure, V. Costan, E. Sarraute, A. Cuniere, and T. Martire: *Optimization of the supply voltage system in interleaved converters using intercell transformers.* IEEE Transactions on Power Electronics, 22(3):934–942, 2007.

[FOR09] F. Forest, E. Labouré, T. A. Meynard, and V. Smet: *Design and comparison of inductors and intercell transformers for filtering of PWM inverter output.* IEEE Transactions on Power Electronics, 24(3):812–821, 2009.

[FRA07] L. G. Franquelo, J. Napoles, R. C. P. Guisado, J. I. Leon, and M. A. Aguirre: *A flexible selective harmonic mitigation technique to meet grid codes in three-level PWM converters.* IEEE Transactions on Industrial Electronics, 54(6):3022–3029, 2007.

[GHO08] R. Ghosh and G. Narayanan: *Control of Three-Phase, Four-Wire PWM Rectifier.* IEEE Transactions on Power Electronics, 23(1):96–106, 2008.

[GLO18] B. P. Global: *BP statistical review of world energy June 2018.* Relatório. Disponível em: http://www. bp. com/en/global/corporate/energy-economics/statistical-review-of-world-energy. html, 2018.

[GOH15a] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg: *An integrated inductor for parallel interleaved VSCs and PWM schemes for flux minimization.* IEEE Transactions on Industrial Electronics, 62(12):7534–7546, 2015.

[GOH15b] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg: *Line filter design of parallel interleaved vscs for high-power wind energy conversion systems.* IEEE Transactions on Power Electronics, 30(12):6775–6790, 2015.

[GOH15c] G. Gohil, R. Maheshwari, L. Bede, T. Kerekes, R. Teodorescu, M. Liserre, and F. Blaabjerg: *Modified discontinuous PWM for size reduction of the circulating current filter in parallel interleaved converters.* IEEE Trans. Power Electron, 30(7):3457–3470, 2015.

[GOH16] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg: *An integrated inductor for parallel interleaved three-phase voltage source converters.* IEEE Transactions on Power Electronics, 31(5):3400–3414, 2016.

[GOH17] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg: *Flux-balancing scheme for pd-modulated parallel-interleaved inverters.* IEEE Transactions on Power Electronics, 32(5):3442–3457, 2017.

[GON17] A. G. Gonzalez: *Review of offshore wind farm cost components.* Energy for Sustainable Development, 37:10–19, 2017.

[GWE18] GWEC: *Global wind report: annual market update 2017.* GWEC, 2018.

[HAR98] L. Harnefors and H. . Nee: *Model-based current control of AC machines using the internal model control method.* IEEE Transactions on Industry Applications, 34(1):133–141, 1998.

[HAS87] M. Hashii, K. Kousaka, and M. Kaimoto: *New approach to a high-power GTO PWM inverter for AC motor drives.* IEEE Transactions on Industry Applications, (2):263–269, 1987.

[HAV98] A. M. Hava, R. J. Kerkman, and T. A. Lipo: *A high-performance generalized discontinuous PWM algorithm.* IEEE Transactions on Industry applications, 34(5):1059–1071, 1998.

[HAV99] A. M. Hava, R. J. Kerkman, and T. A. Lipo: *Simple analytical and graphical methods for carrier-based PWM-VSI drives.* IEEE transactions on power electronics, 14(1):49–61, 1999.

[HAV09] A. M. Hava and E. Ün: *Performance analysis of reduced common-mode voltage PWM methods and comparison with standard PWM methods for three-phase voltage-source inverters.* IEEE Transactions on Power Electronics, 24(1):241–252, 2009.

[HED16] M. H. Hedayati and V. John: *Integrated common-mode inductor design for parallel interleaved converters.* IET Power Electronics, 9(10):2130–2138, 2016.

[HOL88] J. Holtz, W. Lotzkat, and K.-H. Werner: *A high-power multitransistor-inverter uninterruptable power supply system.* IEEE Transactions on Power Electronics, 3(3):278–285, 1988.

[HOL01] D. G. Holmes and B. P. McGrath: *Opportunities for harmonic cancellation with carrier-based PWM for a two-level and multilevel cascaded inverters.* IEEE Transactions on industry applications, 37(2):574–582, 2001.

[HOL03] D. G. Holmes and T. A. Lipo: *Pulse width modulation for power converters: principles and practice*, volum 18. John Wiley & Sons, 2003.

[HOL04] J. Holtz, J. Quan, J. Pontt, J. Rodriguez, P. Newman, and H. Miranda: *Design of fast and robust current regulators for high-power drives based on complex state variables.* IEEE Transactions on Industry Applications, 40(5):1388–1397, 2004.

[HOU99] C. H. Houpis: *Quantitative feedback theory: fundamentals and applications*. CRC press, 1999.

[HOU13] C. H. Houpis and S. N. Sheldon: *Linear Control System Analysis and Design with MATLAB®*. CRC Press, 2013.

[HUR00] W. G. Hurley, E. Gath, and J. G. Breslin: *Optimizing the ac resistance of multilayer transformer windings with arbitrary current waveforms*. IEEE Transactions on Power Electronics, 15(2):369–376, 2000.

[IEE07] IEEE: *IEEE Recommended Practice for Grounding of Industrial and Commercial Power Systems*. IEEE Std 142-2007 (Revision of IEEE Std 142-1991), pages 1–225, 2007.

[IEE08] IEEE, *IEEE Application Guide for IEEE Std 1547, IEEE Standard for Interconnecting Distributed Resources With Electric Power Systems*, 2008.

[JAF17] M. Jafari, Z. Malekjamshidi, and J. Zhu: *Accurate copper loss analysis of a multi-winding high-frequency transformer for a magnetically-coupled residential microgrid*. In *Electrical Machines and Systems (ICEMS), 2017 20th International Conference on*, pages 1–6. IEEE, 2017.

[JUA14] X. Juankorena: *Conversion de enrgia en generadores eolicos con MSIP de gran potencia*. Ph. D. thesis, Universidad Publica de Navarra, 2014.

[KAU00] M. Kaufhold, H. Aninger, M. Berth, J. Speck, and M. Eberhardt: *Electrical stress and failure mechanism of the winding insulation in PWM-inverter-fed low-voltage induction motors*. IEEE Transactions on industrial electronics, 47(2):396–402, 2000.

[KAW88] T. Kawabata and S. Higashino: *Parallel operation of voltage source inverters*. IEEE Transactions on Industry Applications, 24(2):281–287, 1988.

[KHA08] K. S. Khan, W. M. Arshad, and S. Kanerva: *On performance figures of multiphase machines*. In *Electrical Machines, 2008. ICEM 2008. 18th International Conference on*, pages 1–5. IEEE, 2008.

[KNI08] A. M. Knight, J. Ewanchuk, and J. C. Salmon: *Coupled Three-Phase Inductors for Interleaved Inverter Switching*. IEEE Transactions on Magnetics, 44(11):4119–4122, 2008.

[KOL91] J. W. Kolar, H. Ertl, and F. C. Zach: *Influence of the modulation method on the conduction and switching losses of a PWM converter system*. IEEE Transactions on Industry Applications, 27(6):1063–1075, 1991.

[KON16] G. Konstantinou, J. Pou, G. J. Capella, K. Song, S. Ceballos, and V. G. Agelidis: *Interleaved operation of three-level neutral point clamped converter legs and reduction of circulating currents under SHE-PWM*. IEEE Transactions on Industrial Electronics, 63(6):3323–3332, 2016.

[KON17] G. Konstantinou, G. J. Capellá Frau, J. Pou, and S. Ceballos Recio: *Single-carrier phase-disposition PWM techniques for multiple interleaved voltage-source converter legs*. IEEE transactions on industrial electronics, (9):1–1, 2017.

[KRI15] H. S. Krishnamoorthy, P. N. Enjeti, and P. Garg: *Simplified medium/high frequency transformer isolation approach for multi-pulse diode rectifier front-end adjustable speed drives*. In *Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE*, pages 527–534. IEEE, 2015.

[LAA96] T. I. Laakso, V. Valimaki, M. Karjalainen, and U. K. Laine: *Splitting the unit delay [FIR/all pass filters design]*. IEEE Signal Processing Magazine, 13(1):30–60, 1996.

[LAB08] E. Labouré, A. Cuniere, T. Meynard, F. Forest, and E. Sarraute: *A theoretical approach to intercell transformers, application to interleaved converters.* IEEE Transactions on Power Electronics, 23(1):464–474, 2008.

[LAI04a] Y.-S. Lai, P.-S. Chen, H.-K. Lee, and J. Chou: *Optimal common-mode voltage reduction PWM technique for inverter control with consideration of the dead-time effects-part II: applications to IM drives with diode front end.* IEEE transactions on industry applications, 40(6):1613–1620, 2004.

[LAI04b] Y.-S. Lai and F.-S. Shyu: *Optimal common-mode voltage reduction PWM technique for inverter control with consideration of the dead-time effects-part I: basic development.* IEEE Transactions on Industry Applications, 40(6):1605–1612, 2004.

[LAK13] A. Laka, J. A. Barrena, J. Chivite-Zabalza, and M. Rodriguez-Vidal: *Parallelization of two three-phase converters by using coupled inductors built on a single magnetic core.* Przeglad Elektrotechniczny, 89(3a):194–198, 2013.

[LAK14] A. Laka, J. A. Barrena, J. Chivite-Zabalza, M. Á. R. Vidal, and G. Calvo: *IP-ZSBT magnetic configuration for parallelization–serialization of three-phase high power converters.* IEEE Transactions on Energy Conversion, 29(2):366–374, 2014.

[LEE01] H.-D. Lee and S.-K. Sul: *Common-mode voltage reduction method modifying the distribution of zero-voltage vector in PWM converter/inverter system.* IEEE Transactions on Industry Applications, 37(6):1732–1738, 2001.

[LI18] X. Li, J. Fang, Y. Tang, X. Wu, and Y. Geng: *Capacitor-Voltage Feedforward With Full Delay Compensation to Improve Weak Grids Adaptability of LCL-Filtered Grid-Connected Converters for Distributed Generation Systems.* IEEE Transactions on Power Electronics, 33(1):749–764, 2018.

[LIS02] M. Liserre, a. Dell'Aquila, and F. Blaabjerg: *Stability improvements of an LCL-filter based three-phase active rectifier.* 2002 IEEE 33rd Annual IEEE Power Electronics Specialists Conference. Proceedings (Cat. No.02CH37289), 3:1195–1201, 2002.

[LIS04] M. Liserre, A. Dell'Aquila, and F. Blaabjerg: *Genetic algorithm-based design of the active damping for an LCL-filter three-phase active rectifier.* IEEE Transactions on Power Electronics, 19(1):76–86, 2004.

[LIS05] M. Liserre, F. Blaabjerg, and S. Hansen: *Design and control of an LCL-filter-based three-phase active rectifier.* IEEE Transactions on industry applications, 41(5):1281–1291, 2005.

[MAC89] J. M. Maciejowski: *Multivariable feedback design. Electronic systems engineering series.* Wokingham, England: Addison-Wesley, 6:85–90, 1989.

[MAO11] X. Mao, A. K. Jain, and R. Ayyanar: *Hybrid interleaved space vector PWM for ripple reduction in modular converters.* IEEE Transactions on Power Electronics, 26(7):1954–1967, 2011.

[MEL98] M. Melfi, A. M. J. Sung, S. Bell, and G. L. Skibinski: *Effect of surge voltage risetime on the insulation of low-voltage machines fed by PWM converters.* IEEE Transactions on Industry Applications, 34(4):766–775, 1998.

[NAP10] J. Napoles, J. I. Leon, R. Portillo, L. G. Franquelo, and M. A. Aguirre: *Selective harmonic mitigation technique for high-power converters.* IEEE Transactions on Industrial electronics, 57(7):2315–2323, 2010.

[OGA90] S. Ogasawara, H. Akagi, and A. Nabae: *A novel PWM scheme of voltage source inverters based on space vector theory Ein neues Modulationskonzept für Wechselrichter mit eingeprägter Spannung.* Archiv für Elektrotechnik, 74(1):33–41, 1990.

[OHN18] S. Ohn, X. Zhang, R. Burgos, and D. Boroyevich: *Differential and Common Mode Coupled Inductor for Parallel Three-phase AC-DC Converters*. IEEE Transactions on Power Electronics, pages 1–1, 2018.

[PAN14] D. Pan, X. Ruan, C. Bao, W. Li, and X. Wang: *Capacitor-current-feedback active damping with reduced computation delay for improving robustness of LCL-type grid-connected inverter*. IEEE Transactions on Power Electronics, 29(7):3414–3427, 2014.

[PAN17] D. Pan, X. Ruan, and X. Wang: *Direct Realization of Digital Differentiators in Discrete Domain for Active Damping of LCL-Type Grid-Connected Inverter*. IEEE Transactions on Power Electronics, pages 1–1, 2017.

[PAR33] R. Park: *Two-reaction theory of synchronous machines*. Trans. AIEE, 1933.

[PAR14] S. G. Parker, B. P. McGrath, and D. G. Holmes: *Regions of active damping control for LCL filters*. IEEE Transactions on Industry Applications, 50(1):424–432, 2014.

[PEÑ14] R. Peña, M. Liserre, F. Blaabjerg, R. Sebastián, J. Dannehl, and F. W. Fuchs: *Systematic design of the lead-lag network method for active damping in LCL-filter based three phase converters*. IEEE Transactions on Industrial Informatics, 10(1):43–52, 2014.

[PER97] D. J. Perreault and J. G. Kassakian: *Distributed interleaving of paralleled power converters*. IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, 44(8):728–734, 1997.

[PIL17] R. Pilawa-Podgurski, *Extreme Power Density Converters Fundamental Techniques and Selected Applications*, 2017.

[PRA14] J. S. Prasad and G. Narayanan: *Minimization of Grid Current Distortion in Parallel-Connected Converters Through Carrier Interleaving*. IEEE Trans. Industrial Electronics, 61(1):76–91, 2014.

[PRI15] E. Prieto-Araujo, A. Junyent-Ferré, D. Lavèrnia-Ferrer, and O. Gomis-Bellmunt: *Decentralized control of a nine-phase permanent magnet generator for offshore wind turbines*. IEEE Transactions on Energy Conversion, 30(3):1103–1112, 2015.

[QUA17] Z. Quan and Y. W. Li: *A Three-Level Space Vector Modulation Scheme for Paralleled Converters to Reduce Circulating Current and Common-Mode Voltage*. IEEE Transactions on Power Electronics, 32(1):703–714, 2017.

[REM18] T. Remy and A. Mbistrova: *Offshore Wind in Europe: Key Trends and Statistics 2017*. Wind Europe: Brussels, Belgium, page 36, 2018.

[REN18] REN21: *Renewables 2018 Global Status Report*. REN21, 2018.

[RYL11] M. S. Rylko: *Magnetic materials and soft-switched topologies for high-current DC-DC converters*, 2011.

[SAÏ18] M. B. Saïd, M. Naouar, I. Slama-Belkhodja, and E. Monmasson: *Time delay consideration for robust capacitor-current-inner-loop active damping of LCL-filter-based grid-connected converters*. International Journal of Electrical Power & Energy Systems, 95:177–187, 2018.

[SHA11] D. Sha, Z. Guo, and X. Liao: *Control strategy for input-parallel–output-parallel connected high-frequency isolated inverter modules*. IEEE Transactions on Power Electronics, 26(8):2237–2248, 2011.

[SHA15] L. Shao, W. Hua, and M. Cheng: *Investigation on phase shift between multiple-winding sets in multiphase flux-switching permanent magnet machines*. In *Energy Conversion Congress and Exposition (ECCE), 2015 IEEE*, pages 6942–6947. IEEE, 2015.

[SHE12] J. Shen, S. Schröder, H. Stagge, and R. W. D. Doncker: *Precise modeling and analysis of DQ-frame current controller for high power converters with low pulse ratio.* In *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 61–68, 2012.

[SHI15] J. Shi, J. Shen, B. Qu, H. She, and Z. Tan: *High-performance complex controller for high-power converters with low pulse ratios.* In *2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, pages 2180–2187, 2015.

[SIE13] A. Siemens: *GEAFOL Cast-Resin Transformers 100 to 16,000 kVA*. Catalog, 2013.

[SMI16] V. Smil: *Energy transitions: global and national perspectives.* ABC-CLIO, 2016.

[SWA17] M. M. Swamy and M. A. Baumgardner: *New Normal Mode dv/dt Filter With a Built-In Resistor Failure Detection Circuit.* IEEE Transactions on Industry Applications, 53(3):2149–2158, 2017.

[UN09] E. Un and A. M. Hava: *A near-state PWM method with reduced switching losses and reduced common-mode voltage for three-phase voltage source inverters.* IEEE Transactions on Industry Applications, 45(2):782–793, 2009.

[VAN88] H. W. Van Der Broeck, H.-C. Skudelny, and G. V. Stanke: *Analysis and realization of a pulsewidth modulator based on voltage space vectors.* IEEE transactions on industry applications, 24(1):142–150, 1988.

[VEN02] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca: *Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters.* In *Computers in Power Electronics, 2002. Proceedings. 2002 IEEE Workshop on*, pages 36–41. IEEE, 2002.

[VID17] A. Videt, M. Messaoudi, N. Idir, H. Boulharts, and H. Vang: *PWM strategy for the cancellation of common-mode voltage generated by three-phase back-to-back inverters.* IEEE Transactions on Power Electronics, 32(4):2675–2686, 2017.

[VOG14] T. Vogt, A. Peters, N. Frohleke, J. Bocker, and S. Kempen: *Power profile based selection and operation optimization of parallel-connected power converter combinations.* In *Power Electronics Conference (IPEC-Hiroshima 2014-ECCE-ASIA), 2014 International*, pages 2887–2892. IEEE, 2014.

[WAN15] X. Wang, F. Blaabjerg, and P. C. Loh: *Virtual RC damping of LCL-filtered voltage source converters with extended selective harmonic compensation.* IEEE Transactions on Power Electronics, 30(9):4726–4737, 2015.

[WAN16] J. Wang, J. D. Yan, L. Jiang, and J. Zou: *Delay-dependent stability of single-loop controlled grid-connected inverters with LCL filters.* IEEE Transactions on Power Electronics, 31(1):743–757, 2016.

[WEL05a] J. Wells, P. Chapman, and P. Krein: *Generalization of selective harmonic control/elimination.* In *IEEE Power Electronics Specialists Conference*, volum 36, page 1358. Citeseer, 2005.

[WEL05b] J. R. Wells, B. M. Nee, P. L. Chapman, and P. T. Krein: *Selective harmonic control: a general problem formulation and selected solutions.* IEEE Transactions on Power Electronics, 20(6):1337–1345, 2005.

[WEL06] J. R. Wells, P. Krause, P. L. Chapman, and P. T. Krein: *Theoretical considerations for selective harmonic control.* In *Power Electronics Specialists Conference, 2006. PESC'06. 37th IEEE*, pages 1–7. IEEE, 2006.

[WU06] E. Wu and P. W. Lehn: *Digital current control of a voltage source converter with active damping of LCL resonance.* IEEE Transactions on Power Electronics, 21(5):1364–1373, 2006.

[XIA17] F. Xiao, L. Dong, L. Li, and X. Liao: *A frequency-fixed SOGI-based PLL for single-phase grid-connected converters.* IEEE Transactions on Power Electronics, 32(3):1713–1719, 2017.

[XIN99a] K. Xing, F. C. Lee, D. Borojevic, Z. Ye, and S. Mazumder: *Interleaved PWM with discontinuous space-vector modulation.* IEEE Transactions on Power Electronics, 14(5):906–917, 1999.

[XIN99b] K. Xing, F. C. Lee, D. Borojevic, Z. Ye, and S. Mazumder: *Interleaved PWM with discontinuous space-vector modulation.* IEEE Transactions on Power Electronics, 14(5):906–917, 1999.

[XIN16] Z. Xin, P. C. Loh, X. Wang, F. Blaabjerg, and Y. Tang: *Highly Accurate Derivatives for LCL-Filtered Grid Converter With Capacitor Voltage Active Damping.* IEEE Transactions on Power Electronics, 31(5):3612–3625, 2016.

[XU16] J. Xu, Q. Qian, S. Xie, and B. Zhang: *Grid-voltage feedforward based control for grid-connected LCL-filtered inverter with high robustness and low grid current distortion in weak grid.* In *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 1919–1925, 2016.

[YAR15] V. Yaramasu, B. Wu, P. C. Sen, S. Kouro, and M. Narimani: *High-power wind energy conversion systems: State-of-the-art and emerging technologies.* Proceedings of the IEEE, 103(5):740–788, 2015.

[YEP14a] A. G. Yepes, A. Vidal, O. López, and J. Doval-Gandoy: *Evaluation of Techniques for Cross-Coupling Decoupling Between Orthogonal Axes in Double Synchronous Reference Frame Current Control.* IEEE Transactions on Industrial Electronics, 61(7):3527–3531, 2014.

[YEP14b] A. G. Yepes, A. Vidal, J. Malvar, O. López, and J. Doval-Gandoy: *Tuning method aimed at optimized settling time and overshoot for synchronous proportional-integral current control in electric machines.* IEEE Transactions on Power Electronics, 29(6):3041–3054, 2014.

[YIM09] J. S. Yim, S. K. Sul, B. H. Bae, N. R. Patel, and S. Hiti: *Modified Current Control Schemes for High-Performance Permanent-Magnet AC Drives With Low Sampling to Operating Frequency Ratio.* IEEE Transactions on Industry Applications, 45(2):763–771, 2009.

[YU12] X. Yu and A. M. Khambadkone: *Reliability analysis and cost optimization of parallel-inverter system.* IEEE Transactions on Industrial Electronics, 59(10):3881–3889, 2012.

[ZHA10a] D. Zhang, F. Wang, R. Burgos, R. Lai, and D. Boroyevich: *Impact of interleaving on AC passive components of paralleled three-phase voltage-source converters.* IEEE Transactions on Industry Applications, 46(3):1042–1054, 2010.

[ZHA10b] R. S. Zhang, C. Wang, Z. Tan, and H. Weng, *Cross current control for power converter system*, 2010. US Patent 7,852,643.

[ZHA11a] D. Zhang, F. Wang, R. Burgos, R. Lai, and D. Boroyevich: *DC-link ripple current reduction for paralleled three-phase voltage-source converters with interleaving.* IEEE Transactions on Power Electronics, 26(5):1741, 2011.

[ZHA11b] D. Zhang, F. F. Wang, R. Burgos, and D. Boroyevich: *Common-Mode Circulating Current Control of Paralleled Interleaved Three-Phase Two-Level Voltage-Source Converters With Discontinuous Space-Vector Modulation.* IEEE Transactions on Power Electronics, 26(12):3925–3935, 2011.

[ZHA12] D. Zhang, F. Wang, R. Burgos, and D. Boroyevich: *Total flux minimization control for integrated inter-phase inductors in paralleled, interleaved three-phase two-level voltage-source converters with discontinuous space-vector modulation.* IEEE Transactions on Power Electronics, 27(4):1679–1688, 2012.

[ZHA16] M. Zhao, X. Yuan, J. Hu, and Y. Yan: *Voltage Dynamics of Current Control Time-Scale in a VSC-Connected Weak Grid.* IEEE Transactions on Power Systems, 31(4):2925–2937, 2016.

[ZHO15] S. Zhou, X. Zou, D. Zhu, Y. Kang, L. Tong, and X. Gao: *LCL type grid-connected converter no startup inrush current control method based on capacitor branch voltage feedforward.* In *IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society*, pages 001471–001476, 2015.

[ZHO17] S. Zhou, J. Liu, L. Zhou, and Y. Zhang: *DQ Current Control of Voltage Source Converters With a Decoupling Method Based on Preprocessed Reference Current Feed-forward.* IEEE Transactions on Power Electronics, 32(11):8904–8921, 2017.

[ZMO01] D. N. Zmood, D. G. Holmes, and G. H. Bode: *Frequency-domain analysis of three-phase linear current regulators.* IEEE Transactions on Industry Applications, 37(2):601–610, 2001.

[ZOR18] I. Zoric, M. Jones, and E. Levi: *Arbitrary power sharing among three-phase winding sets of multiphase machines.* IEEE Trans. Ind. Electron, 65(2):1128–1139, 2018.

Nomenclature

Symbols

C	Capacitor	F	N	Neutral point	
E	DC-bus voltage	V	o	DC-bus voltage mid-point	V
F	Switching function/Frequency	–	S	Switch/Aparent power	–
i	Current	A	T	Transformation matrix to the SRF	
L	Inductor	H	v	Voltage	V

Subscripts

α	Component in the α axis	G	Relative to the grid side converter
β	Component in the β axis	g	Grid
a	Phase a	gt	Grid + transformer
b	Phase b	L	Inductor
C	Capacitor	M	Relative to the machine side converter
c	Phase c		
CM	Common-mode	m	Machine
cm	Common-mode	PG	Phase-to-ground
$cont$	Controller	q	Component in the q axis
$conv$	Converter	R	Resistor
d	Component in the d axis	s	Series/sampling
dm	Differenctial-mode	$tranf$	Transformer

Abbreviations

AD	Active damping	AZSVPWM	Active zero space vector

pulse-width modulation

B2B Back-to-back

CCAD Capacitor-current active damping

CCD Cross-controller decoupler

CM Common-mode

CRFF Current reference feed-forward

CVDAD Capacitor-voltage derivative active damping

CVPID Complex vector proportional-integrator decoupling

DC Direct current

DFIG Doubly-fed induction generator

DSP Digital signal processor

DSVPWM Discontinuous space vector pulse-width modulation

FPGA Field-programmable-array

GDSVPWM Generalized discontinuous space vector pulse-width modulation

GSC Grid side converter

HDF Harmonic distortion factor

IPT Interphase transformer

LPAF Low-pass analog filter

LPDF Low-pass digital filter

MAF Moving-average filter

MIMO Multiple-input multiple-output

MSC Machine side converter

NSSVPWM Near state pace vector pulse-width modulation

PCC Point of common coupling

PG Phase-to-ground

PI Proportional integral

PLL Phase-locked loop

PMG Permanent magnet gnerator

RHP Right-half plane

RSSVPWM Remote state space vector pulse-width modulation

SCR Short-circuit ratio

SFD State-feedback decoupling

SHE Selective harmonic elimination

SHM Selective harmonic mitigation

SISO Single-input single-output

SRF Syncronous reference frame

SVPWM Space vector pulse-width modulation

THD Total harmonic distoortion

VSC Voltage source converter

WECS Wind energy conversion systems

WTHD Weighted total harmonic distortion

This thesis has been funded by the Public University of Navarre through a doctoral scholarship. The company Ingeteam Power Technology has supported this investigation under contracts OTRI 2016 024 004 and OTRI 2014 024 084. Moreover, the Spanish State Research Agency (AEI) and FEDER-UE have supported the investigation under grants DPI2013-42853-R and DPI2016–80641–R.