Overcome the Limitations of Performance Parameters of On-Chip Antennas Based on Metasurface and Coupled Feeding Approaches for Applications in System-on-Chip for THz Integrated-Circuits

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Abstract: **This paper proposes a new solution to improve the performance parameters of on-chip antenna designs on standard CMOS silicon (Si.) technology. The proposed method is based on applying the metasurface technique and exciting the radiating elements through coupled feed mechanism. The on-chip antenna is constructed from three layers comprising Si.-GND-Si. layers, so that the ground (GND) plane is sandwiched between two Si. layers. The silicon and ground-plane layers have thicknesses of 20μm and 5μm, respectively. The 3×3 array consisting of the asterisk-shaped radiating elements has implemented on the top silicon layer by applying the metasurface approach. Three slot lines in the ground-plane are modelled and located directly under the radiating elements. The radiating elements are excited through the slot-lines using an open-circuited microstrip-line constructed on the bottom silicon layer. The proposed method to excite the structure is based on the coupled feeding mechanism. In addition, by the proposed feeding method the on-chip antenna configuration supresses the substrate losses and surface-waves. The antenna exhibits a large impedance bandwidth of 60GHz from 0.5THz to 0.56THz with an average radiation gain and efficiency of 4.58dBi and 25.37%, respectively. The proposed structure has compact dimensions of 200×200×45μm^3. The results shows that, the proposed technique is therefore suitable for on-chip antennas for applications in system-on-chip for terahertz (THz) integrated circuits.**

Keywords: **On-chip antennas, metasurface, coupled feeding mechanism, terahertz (THz) systems-on-chip applications, CMOS silicon (Si.) technology, THz integrated circuits, ground (GND).**

I. Introduction

With the recent development in mobile communications and silicon technology, interest in new advancement of radio frequency integrated circuits (RFICs) has enhanced, containing the representation of antennas for system on-chip (SoC) applications [1, 2]. On-chip antennas are an integral part of wireless sensor networks, in low-cost silicon IC sensors, and for data communication between ICs [3]. Integrated antennas eliminate the need for external transmission line connections, sophisticated packaging and therefore make feasible manufacture of cost-effective and compact microwave and millimeter-wave devices.

On-chip antenna is the last barrier for the true System-on-Chip (SoC) solution, especially applying the Si. process [4-8]. The high permittivity and low resistivity of Si. substrate result in narrow bandwidth, low gain and low radiation efficiency of antenna. Various approaches have been presented to improve the performance of the on-chip antenna [9-12]. However, these techniques are costly as the designs are complex to implement or the antenna performance falls short of practical applications.

Proposed in this paper is a new but simple method to improve the performance parameters of on-chip antennas working on terahertz area. The antenna design is based on metasurface technology. In addition, the proposed structure is low profile, cost effective, and easy to manufacture.

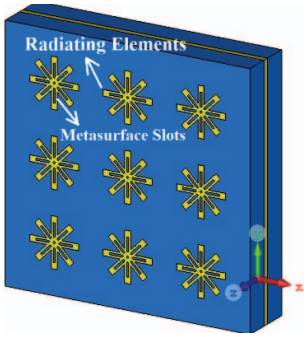
II. High Performance On-Chip Antenna

The proposed on-chip antenna design is constructed from three layers comprising silicon-ground-silicon layers, as shown in Fig.1. The two silicon layers that sandwich the ground-plane have a thickness of 20μm, and the ground-plane has a thickness of 5μm. On the top silicon layer, a 3×3 array of asterisk-shaped radiating elements is implemented, as exhibited in Figs. 1 (a) and (b). Realized in the middle ground-plane layer are three slot lines that are aligned under the asterisk-shaped elements, as shown in Figs. 1 (b) and (c), which supress the surface waves and substrate losses.

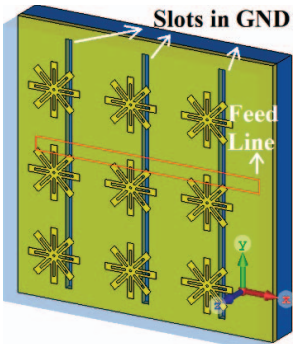
To improve the antenna's performance parameters such as the impedance bandwidth and the radiation behaviour, the metasurface slots in optimized dimensions are etched

on the asterisk-shaped elements, which enlarge the antenna's effective aperture area without affecting its dimensions. Therefore, the proposed configuration acts like a metasurface that essentially have positive effects on the radiation characteristics of the antenna.

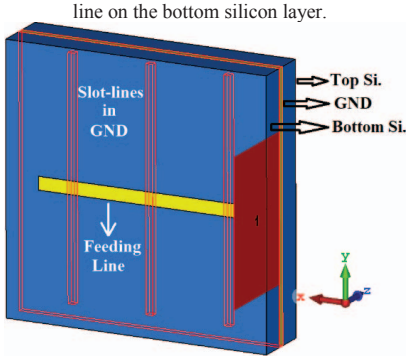
To improve impedance matching and bandwidth a simple and novel feeding mechanism to excite the antenna was employed. This consisted of an open-circuited microstrip-line implemented under the bottom silicon layer. Electromagnetic signal applied to the open-circuited line is coupled to the asterisk-shaped elements on the top substrate via the slot-lines on the GND.



(a) Top view to show asterisk-shaped elements including metasurface slots



(b) Isometric view showing asterisk-shaped elements on the top Si. substrate, slot-lines in the GND layer, and open-ended microstrip feed line on the bottom silicon layer.



(c) Back view to show open-circuited feeding line

Fig.1. On-chip antenna configuration.

The reflection-coefficient of the proposed on-chip antenna in Fig.2 indicates that the on-chip antenna operates over the frequency band from 0.5-0.56 THz for S_{11}<-15dB, that corresponds to the fractional bandwidth of ~11.3%.

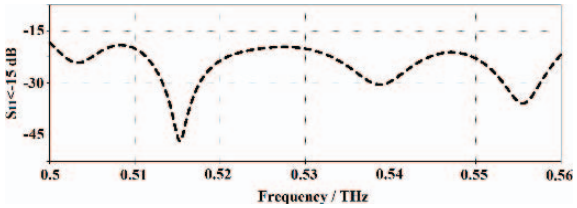
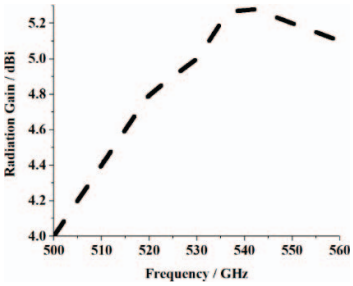
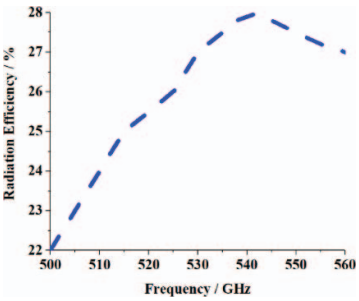


Fig.2. Frequency bandwidth (S_{11}<-15dB).

Gain and radiation efficiency responses of the proposed on-chip antenna structure are indicated in Fig.3. It demonstrates that the maximum gain and radiation efficiency are 5.3dBi and 28.15%, respectively, that are occurred at 540 GHz. The radiation characteristics over frequency are listed in details in the table I.



Gain



Efficiency

Fig.3. Radiation properties of the proposed on-chip antenna structure.

TABLE I. ON-CHIP ANTENNA RADIATION PROPERTIES

Frequency (GHz)	Gain (dBi)	Efficiency (%)
500	4 (minimum)	22 (minimum)
540	5.3 (maximum)	28.15 (maximum)
560	5.11	27.05

To enhance the validity of the proposed model, it is compared with the various publications. Table II lists the results. Obviously, the proposed structure exhibits higher performance parameters in comparison with the literature.

III. Conclusion

A novel and simple technique is described that enhances the performance parameters of on-chip antennas implemented on CMOS Silicon substrate. The proposed technique utilizes the metasurface technology to increase the effective aperture of the antenna, which leads to improve its radiation properties. The antenna is excited by the coupling electromagnetic energy through slots in the middle ground-plane layer, which is sandwiched between the two silicon layers. This type of feeding suppresses the

surface waves and substrate losses, which has caused to improve the antenna's impedance matching and its impedance bandwidth. It is shown that, the proposed technique overcomes the common drawbacks of narrow bandwidth and poor radiation specifications of on-chip antennas. The proposed technique is therefore suitable for on-chip antennas for applications in system-on-chip for terahertz integrated circuits.

TABLE II. COMPARISON TABLE

Ref.	Antenna Type	Freq. (GHz)/ BW (%)	Gain (dBi)	Eff. %	Process	Size (mm^2)	Height (mm)
[13]	Patch Fed Higher Order Mode DRA	341/7	7.9	74	0.18-μm SiGe	0.2	0.5
[14]	On-chip 3D (Yagi like concept)	340/12	10	80	0.13-μm SiGe	0.49	0.11
[15]	Slot-Loaded Magnetic Loop on SIW	340/7	3.3	45	0.13-μm SMOS	0.49	-
[16]	Patch	280/2.5	–1.6	21	0.13-μm CMOS	0.2	-
[17]	Ring Antenna	296/-	4.2	-	65-nm CMOS	0.3	-
[18]	Slot Ring Antenna + Superstrate	375/8	1.6	35	45-nm CMOS SOI	0.05	-
[19]	Ring Antenna with Silicon Lens	288/NA	18.3	65	65-nm CMOS	12.56	2.55
[20] - a	Half-Mode Cavity Fed DRA	135/13	3.7	62	0.18-μm CMOS	0.63	0.25
[20] - b	Half-Mode Cavity Fed Higher Order Mode DRA	135/7	6.2/7.5	46/ 42	0.18-μm CMOS	0.72	1.3/2.2
[21]	Slot Fed Stacked DRA (Two DRAs + Supporter)	130/11	4.7	43	0.18-μm CMOS	0.72	1.28
[22]	DRA	135/11	2.7	43	0.18-μm CMOS	0.72	0.6
This Work	Metasurface	540/11.3	5.3	28.15	CMOS	0.04	0.045

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