A Novel 0.3-0.31 THz GaAs-Based Transceiver with On-Chip Slotted Metamaterial Antenna Based on SIW Technology

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Abstract: This paper presents a novel on-chip antenna with fully integrated 0.3-0.31 THz transceiver is implemented on 0.5µm GaAs substrate, and comprises a voltage-controlled oscillator (VCO), a buffer amplifier, a modulator stage, a power-amplifier, a frequency-tripler, and an on-chip antenna. The proposed on-chip antenna design is based on metamaterial (MTM) slots and substrate integrated waveguide (SIW) technologies. The SIW antenna operates as a high-pass filter and an on-chip radiator to suppress the unwanted harmonics and radiate the desired signal, respectively. Dimensions of the on-chip antenna are 2×1×0.0006 mm³. The proposed on-chip antenna has an average radiation gain and efficiency of >1.0 dBi and ~55%, respectively. The transceiver provides an average output power of -15 dBm over 0.3-0.31 THz, which is suitable for near-field active imaging applications at terahertz region.

Keywords: On-chip antenna, metamaterial, terahertz (THz), substrate integrated waveguide (SIW), transceiver, Gallium Arsenide (GaAs) substrate, longitudinal and transverse slot arrays.

I. INTRODUCTION

High frequencies technologies in the millimetre-wave and terahertz bands have been successfully employed in various systems such as safety critical, biomedical, nondestructive detection, and non-ionizing cancer imaging [1, 2]. Such high frequency systems are fabricated using III-V semiconductor technology [3]. Although such systems can also be made from quasi-optical components [4] these are undesirable as they are physically large and uneconomic. Recent advances in complementary metal–oxide– semiconductor (CMOS) FETs and high-speed silicongermanium (SiGe) heterojunction bipolar transistors (HBTs) with significantly increased f_T and f_{max} have resulted in the realization of single-chip integrated transmitters and receivers operating at millimetre-wave [5] and terahertz (THz) bands [6-8].

This paper presents an investigation on a fully integrated on-chip antenna designed on GaAs based transceiver. The metamaterial slotted on-chip antenna is implemented on a SIW [9, 10] for integration within 300-310 GHz transceiver in order to transmit the power efficiently as well as mitigate the unwanted harmonics. In the architecture of the transceiver, a frequency tripler and SIW slotted metamaterial on-chip antenna are conjugately impedance matched to improve the transceivers performance by reducing mismatching effects.

II. TRANSCEIVER CIRCUIT DESIGN

A. Block Diagram

The simplified architecture of the proposed THz transceiver shown in Fig. 1 is constituted from six components, i.e. a voltage-controlled oscillator (VCO), a buffer amplifier, a modulator stage, a power-amplifier, a frequency-tripler, and an on-chip antenna. The frequencytripler is necessary to generate the required terahertz frequency. This is achieved by using a 0.5 μ m GaAs with f_T and fmax of 150 GHz and 220 GHz, respectively. The switchable modulator, which is fabricated on 0.5µm metal oxide semiconductor (MOS) FET, is incorporated in the transceiver architecture to enhance its functionality. Hence, the transceiver can be used for ultra-high data-rate (~10 Gbps) transmission or for highly accurate measurement applications including positioning and ranging, and Fourier-transform infrared spectroscopy (FTIR) where the modulation function needs to be disabled.



Fig.1. Schematic block diagram of the integrated terahertz transceiver attached to an on-chip SIW antenna.

B. Voltage-Controlled Oscillator (VCO)

The diagram in Fig. 2 is of the push-push cross-coupled VCO. The VCO's resonant frequency is controlled by inductance (L) and capacitance (C_I) of the varactor diode. The capacitance of the varactor diode is realized by joining HBT's emitter and base terminals and by using the collector-base junction in reverse bias mode. The total capacitance of the VCO is made up from the collector-base junction capacitance plus collector substrate parasitic capacitance. At the connection node of the HBTs (Q_I and Q_2) a $\lambda/4$ microstrip-line (TL_I) at 150 GHz is attached in order to short-circuit only the second order harmonic. This has negligible effect on other signals.



Fig.2. Circuit diagram of the voltage-controller oscillator (VCO) and the eight-stage amplifier.

C. Buffer and Power Amplifier

The circuit diagram of the eight-stage common-emitter amplifier configuration used for buffering and power amplification is shown in Fig. 2. To minimise parasitic effects and the footprint of the chip we have combined the bias network with the impedance matching network. The amplifier stages in the eight-stage amplifier were designed to be unconditionally stable over the frequency range of interest.

D. Frequency Tripler (\times 3)

Fig. 3 shows the circuit diagram of the frequencytripler. The frequency-tripler design uses nonlinear characteristics exhibited in HBT cascode (Q_1 and Q_2). In conventional designs a bandpass filter is used to eliminate undesirable frequency components, i.e. fundamental and harmonic, at the output. At such high frequencies a bandpass filter is challenging to realise for low passband loss. Hence, we have adapted an open-stub TL_1 at $2f_0$ to mitigate even harmonic components. The *LC* network (TL_2 and C_1), which is also used here in DC biasing, is used to eliminate the fundamental signal (f_0) but allow $3f_0$ signal.



Fig.3. Circuit schematic of the frequency tripler.

The frequency-tripler was internally impedance matched to the on-chip SIW antenna. This was achieved by using conjugate matching in order to minimise the footprint of the circuit and to enhance the gain. Fig. 4 shows the simulated time-domain waveforms of the frequency-tripler. It is evident that the 3^{rd} harmonic ($3f_0$) produced is significantly stronger. Fig. 4 also shows the fundamental signal (f_0). It should be noted that the fundamental frequency is filtered out by the on-chip SIW antenna, which is based on metamaterial slots having high-pass characteristic.

E. On-Chip Antenna Based on Substrate Integrated Waveguide and Metamaterial Slots

The proposed on-chip metamaterial slotted antenna design is based on SIW structure [9, 10]. The on-chip integrated antenna in Fig.5 comprises a SIW, a 4×4 longitudinal and transverse slot array, and an interconnection line for the microstrip line and SIW. The

top and bottom side of the SIW were constructed using 0.1µm aluminium pad layer and 0.5µm GaAs layer with ε_r : 12.94 and tan δ : 0.006, respectively. The bottom of the SIW is used as a ground-plane of the microstrip line. Sides of the SIW structure were created inserting metallic via-holes in the GaAs layer to the aluminium pad layer, and the longitudinal and transverse slot array were fabricated in the pad layer based on metamaterial concept [11-14] to improve the radiation performance parameters. The gap between the SIW and slot array was made $3\lambda/4$ purely because of the limitation of our fabrication facility.



Fig.4. Simulated time-domain waveform of the frequency-tripler.

Dimensions of the SIW on-chip antenna, ground-plane, diameter of via holes, distance between via holes, length & width of slots, distance between the slots in each row, length & width of microstrip line, length & width of interconnect line are $2 \times 1.5 \times 0.0001 \text{ mm}^3$, $2 \times 2 \times 0.0005 \text{ mm}^3$, 0.025 mm, 0.077 mm, 3 mm & 1 mm, 3 mm, 0.3 mm & 0.2 mm, 0.2 mm & 0.070 mm, respectively.

A SIW is used here as a high-pass structure [9] to filter out the unwanted f_0 and $2f_0$ signals. Furthermore, the SIW is in close proximity to the waveguide structure that profoundly reduces unwanted surface waves and EM interference to neighbouring devices. The impedance of the SIW on-chip antenna can be adjusted by simply changing the width of the integrated waveguide structure and the microstrip line. Hence, the proposed antenna is easily conjugate matched with a tripler to minimize the loss. In addition, to increase the radiation properties of the SIW onchip antenna, a 4×4 array of longitudinal and transverse slots was added on top of the SIW. This approach extends the effective aperture area of the on-chip antenna to optimise radiation performances.

Fig.6 shows the on-chip antenna operates over a frequency range from 300 GHz to 310 GHz. The radiation performance parameters such as gain and efficiency plots are shown in Figs. 7 and 8. The minimum and maximum radiation gain and efficiency are 0.25 dBi at 300 GHz & 1.75 dBi at 305 GHz, and 46.12% at 310 GHz & 68.34%

at \sim 305 GHz, respectively. The average value of these parameters are 1.05 dBi and 54.69%, respectively.



Fig.5. Configuration of the proposed on-chip antenna based on SIW and metamaterial technologies.



Fig.6. Reflection coefficient (S $_{11}\!\!<\!\!-10dB)$ of the proposed metamaterial on-chip antenna implemented on SIW.



Fig.7. Radiation patterns of the proposed on-chip antenna at 300, 305, and 310 GHz. Left- and right-side show the E- and H-planes, respectively.



Fig.8. Radiation gain and efficiency curves of the on-chip antenna versus operational frequency.

III. CONCLUSION

An on-chip antenna which is fully integrated on GaAs based transceiver operates across 0.3-0.31 THz. The transceiver is constructed from a voltage-controller oscillator, a buffer amplifier, a modulator stage, a power-amplifier, a frequency-tripler, and an on-chip antenna. The on-chip antenna design was constructed using SIW technology and comprises 4×4 longitudinal and transverse array slots that are realized by metamaterial technology. The on-chip antenna has a minimum gain and efficiency of 0.25 dBi and 46.12%, respectively, over 300 GHz to 310 GHz, which enable it to be applicable for near-field active imaging applications at terahertz.

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