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SHORT PAPER

Performance Comparison and Design Guidelines for Type II and Type III PLLs

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Abstract The advantages provided by Type III PLLs are poorly known, since these devices are very often considered unstable and difficult, or even impossible, to design. In this paper, a performance comparison between Type II and III PLLs is presented, based on an alternative model introduced by the authors. More precisely, the devices are exposed to chirp type and even more complex signals to demonstrate that Type III PLLs may offer better results in terms of phase margin and frequency response peaking when properly designed. As a result of our analysis, approximate closed form expressions will be proposed to evaluate Type III PLL performance and its relation to the parameters of the model.

Keywords Linear systems · PLLs · High-order PLLs · Type III · Type II · Loop filter

1 Introduction

PLLs are fascinating devices which find widespread use as frequency synthesizers, modulators and demodulators, to mention a few. Their design, and even analysis, is not an easy matter since they are strongly nonlinear devices [5,11,19]. They consist of a phase-frequency detector (PD), a voltage controlled oscillator (VCO) and a loop filter (LF). In many instances, a frequency divider is included too. While VCO accounts for the PLL frequency range of operation, its dynamic performance is mainly determined by the LF, which is responsible for the phase noise filtering properties, transient

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response and tracking properties. There are of course other mechanisms to enhance the performance and speed of PLLs [13].

Loop filter has essentially a low-pass response. In case, its DC gain is finite, and independently of its complexity (it may also contain zeros), it gives rise to a so-called Type I PLL. The main limitation of Type I PLLs is their limited hold-in range, since a nonzero signal at its input, and thus at the PD output, is required to sustain a frequency different from the VCO free running frequency. This is the reason why in many applications, LF is designed with a pole at the origin, which is compensated with a zero for stability, resulting in a so-called Type II PLL. However, this class of Type II PLLs does not have obviously infinite hold-in range, which is anyway limited by the VCO or other second-order effects, but extends this range with respect to Type I and gives more flexibility to design the PLL.

Most practical PLLs described in literature are of Type I or II [16], independently of their order, which obviously depends on the filter order. Different configurations and ratios for poles and zeros give different performance to adapt to each particular applications. However, Types I and II have limitations and an increase in the order beyond fourth- order compromises stability too. Classical literature on PLLs [5,19] describes Type III PLLs that characterize for a double pole at the origin in the LF. In this way, the capability to achieve a better performance in terms of hold-in range and, what is more important, the capability to follow fast variations in the input frequency without losing track increase. However, a Type III increases necessarily by one the order of a Type II counterpart (keeping the other poles and zeros unchanged). This is the reason why Type III PLLs have been always considered difficult to design, if not impossible [12, p. 10].

This situation is unfortunate since Type III PLLs have the potential to keep track of signals whose frequency varies following complex dynamics. Actually, early literature on PLLs [6,15,17] reports the need to track frequency ramp variations (Doppler) and even higher-order variations (jerk), which calls for PLLs with zero phase error under such variations (Type III and higher). In particular, diverse Doppler applications are of interest to different fields of medicine. One such example of that can be found in the field of Doppler echo-cardiograms, where the movement of blood cells is measured from frequency deviation of a signal projected to a person. In [14], a strategy to keep track to the input signal as long as possible is proposed. However, it is assumed that the PLL is inevitably loosing lock as long as input frequency reaches a certain level. This can be avoided by using a Type III PLL. Another example of Doppler radar for vital-sign detection is presented in [20].

Recent literature describes a few practical implementations of Type III PLLs, which are rare, but without making clear the advantages and disadvantages of such Type III with respect to Type II counterparts. Only in paper [7], authors undertake a comparison between different implementation approaches in the context of power electronics. This paper also gives some design guidelines to achieve stable Type III PLL devices, and it is interesting to note how those guidelines and conclusions follow the lines stated by us through [1–4,18].

Actually, in our previous work, we have shown how to design high-order high-type PLLs without compromising stability [18]. The procedure is mainly based on a novel model [1–3] that describes such high-order high-type PLLs as a natural extension of

lower-order ones. However, a fair comparison between Types II and III is still lacking in literature. Therefore, we give in this paper an step forward for a better understanding on the differences between these two types of PLLs. Such comparison is based on both analytic results and simulations with a Simulink model, which we have also validated in our previous work. We will mainly use for the analysis typical test signals such as frequency steps and ramps, since they constitute the basic components of more complex signals. Besides, they allow for an easy and straightforward comparison between the two types, and a direct verification of some theoretical results. We recall that an ideal Type III PLLs should keep track of a frequency ramp with a zero phase error, while a Type II should exhibit a constant phase error, losing track when such error is over a threshold. Anyway other dynamics will be also shown. In addition, we will see the response under a quadratic frequency variation pattern to make the differences between the two Types of PLLs even more clear.

No particular implementation, be discrete or integrated, is considered in this paper. The model is general enough, and valid for any order or type, so that we can focus on the comparisons between PLL Types. In the next section, we will first recall a basic analysis that will help to understand the remainder of the paper. Then, in Sects. 3 and 4, we will focus on the comparative analysis between Types II and III, showing both time and frequency domain analyses.

2 Basic Theory

A general scheme of a PLL, suited for high-order type implementations, is shown in Fig. 1. This is a single- loop design structure, opposed to the dual-loop implementations that are used in some works to achieve high-type PLLs [8–10]. Other less known design approaches of both single- and dual-loop implementations are analysed for instance in [7] and will not be considered here. According to the model presented in [3], the LF is decomposed into several low-pass filters. It is important to make two remarks about Fig. 1. First of all, LF2 and LF3 are of order one, whereas LF1 can be typically of order zero (then PLL order equals type), one (order = type + 1) or two (order = type + 2). Second, LF3 filter and its connecting wires (dashed lines) are only present in Type III PLLs. We will mainly analyse in this paper, the case of LF1 being of order one and show that the results can be extended to order two.

The LF and PLL transfer functions for third-order Type II and fourth-order Type III PLLs are shown in Table 1. The parametrization used in those equations corresponds

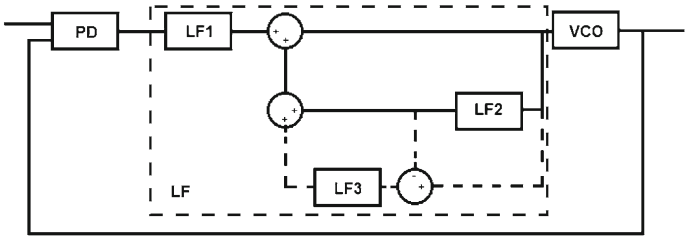

Fig. 1 General model for high-order and high-type PLLs

Table 1 Third-order Type II and Fourth-order Type III PLLs LF and system transfer functions

	Third-order Type II PLLs	Fourth-order Type III PLLs
LF(s)	$\frac{\omega_{z1}\left(1+s/\omega_{z1}\right)}{s\left(1+s/\omega_{p1}\right)}$	$\frac{\omega_{z1}\omega_{z2}\left(1+s/\omega_{z1}\right)\left(1+s/\omega_{z2}\right)}{s^2\left(1+s/\omega_{p1}\right)}$
H(s)	$\frac{K\omega_{z1}\omega_{p1}+K\omega_{p1}s}{K\omega_{z1}\omega_{p1}+K\omega_{p1}s+\omega_{p1}s^2+s^3}$	$\frac{K\omega_{z1}\omega_{z2}\omega_{p1}+K\omega_{p1}\left(\omega_{z1}+\omega_{z2}\right)s+K\omega_{p1}s^2}{K\omega_{z1}\omega_{z2}\omega_{p1}+K\omega_{p1}\left(\omega_{z1}+\omega_{z2}\right)s+K\omega_{p1}s^2\omega_{p1}s^3+s^4}$

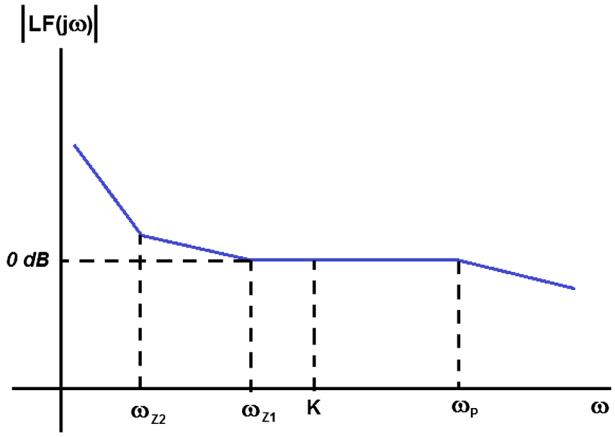

Fig. 2 Loop filter frequency response for high-order and high-type PLLs

to the one suggested by the aforementioned model through [1–3]. Thus, the pole ω_{p1} is the high-frequency pole, while ω_{z1} and ω_{z2} correspond to the zero(s) of the LF. These parameters can also be identified as the bandwidths of LF1, LF2 and LF3, respectively. Loop gain, K, accounts for the product of the PD, VCO and LF gains. The frequency response of a fourth-order Type III PLL's LF is sketched in Fig. 2, where the different roll-off slopes produced by the location of the poles and zeros can be observed. Starting from DC, the double pole at the origin provides infinite DC gain and also a −40 dB/dec slope that reduces to −20 dB/dec around the location of the first zero, ω_{z2}. The roll-off at low frequencies would be of only −20 dB/dec in a Type II, this being the main difference between Type II and Type III PLLs, assuming the same high-frequency poles (i.e. same LF1). From this point on, the appearance of the zero ω_{z1} compensates completely the falling slope of the LF frequency response, making it flat and equal to 0 dB in the region around the loop gain. This is crucial in order to consider K as a good approximation of the overall PLL bandwidth, as explained in [3].

The infinite DC gain that characterizes Type II and above PLLs brings along a zero phase error signal (PD output) under stationary conditions, independently of the reference signal frequency. This means a theoretically unlimited hold-in range, which is limited in practice by other effects (noise, VCO operating range,…). This

qualitative analysis can be further supported by simple s-domain analysis, which we outline below.

The limit value theorem helps us to estimate the error signal at the PD output when a frequency step, $\theta_i(s) = \Delta\omega/s^2$, is applied to the PLL input. For Type II devices, it gives:

$$\lim_{x\to\infty} \theta_e(t) = \lim_{s\to 0} s\theta_e(s) = \lim_{s\to 0} \frac{s^2\theta_i(s)}{1 + K \cdot \mathrm{LF(s)}} = \lim_{s\to 0} \frac{\Delta\omega}{1 + \frac{K\omega_{z1}(1+s/\omega_{z1})}{s(1+s/\omega_{p1})}} = 0 \quad (1)$$

and the same result for Type III:

$$\lim_{x\to\infty} \theta_e(t) = \lim_{s\to 0} \frac{\Delta\omega}{1 + \frac{K\omega_{z1}\omega_{z2}(1+s/\omega_{z1})(1+s/\omega_{z2})}{s^2(1+s/\omega_{p1})}} = 0 \quad (2)$$

In addition to the inherent limitations of the linear model, this results do not take into account that, during the transient, PD output may be larger than the maximum possible. Therefore, although the PLL may unlock, the infinite DC gain provided by the LF would redirect the device to a lock state. This may result in practice in a sequence of frequency hops, until zero PD output is achieved. However, there exist some differences in the transient behaviour of Type II and Type III devices even if they keep the lock state at any time. These differences are a consequence of the different frequency response that both Types exhibit.

Regarding expressions (1) and (2), they can be interpreted in terms of the model in Fig. 1 as follows. When the input frequency is fixed, and after a transient, VCO input is self- sustained by LF2 loop. Thus, its time constant must be larger than the PLL's time constant (inversely proportional to its bandwidth), $\omega_{z1} < K$, [3]. This is also true for the Type III, assuming that $\omega_{z2} < \omega_{z1}$. Therefore, for the tracking of signals whose frequency varies in steps both Types II and III perform similarly or, in other terms, Type III does not seem to offer any significant advantage over Type II. Indeed, [7] already states that the Type III behaviour in this kind of conditions is slightly worse than Type II, since the settling time obtained is higher for the Type III device. However, the comparison carried out in [7] is not fair since it is made between PLLs where zero locations are not optimized, giving different PMs. Thus, it is not possible to generalize the obtained results.

In contrast, we will make use of chirp (i.e. input frequency linearly varying with time) and quadratic variations to better analyse and compare performance of Types II and III. This kind of signals are well suited to show up the differences. Making use again of the limit value theorem for a Type II PLL, and with a chirp input with frequency slope Λ rads/s2 ($\theta_i(s) = \Lambda/s^3$), the phase error will tend to:

$$\lim_{x\to\infty} \theta_e(t) = \lim_{s\to 0} \frac{\Lambda/s}{1 + \frac{K\omega_{z1}(1+s/\omega_{z1})}{s(1+s/\omega_{p1})}} = \frac{\Lambda}{K\omega_{z1}} \quad (3)$$

This value is always different from zero, and thus a necessary condition to achieve tracking will be that it is within PD output dynamic range ($\mathrm{Max_{PD}} \geq \frac{\Lambda}{K\omega_{z1}}$). From

this, a condition for the maximum frequency slope trackable by a Type II PLL can be extracted:

$$\Lambda = K\omega_{z1}\mathrm{Max}_{\mathrm{PD}} \tag{4}$$

where $\mathrm{Max}_{\mathrm{PD}}$ represents the maximum value that the PD is able to supply. These value varies depending on the type of phase detector selected for the implementation. Some common values for $\mathrm{Max}_{\mathrm{PD}}$ are: 1 (sinusoidal PD), $\pi/2$ (triangular PD), π (saw tooth PD) or 2π (PFD).

It is important to notice from expression (4) that the maximum frequency slope achievable by a Type II PLL can be incremented by simply moving ω_{z1} rightwards in the frequency axis, thought this constitutes a reduction in the PM of the PLL, as shown in [18]. When ω_{z1} is incremented, the time delay introduced by the filter is reduced and, according to the model in Fig. 1, the voltage difference between LF2's input and output decreases faster. This allows the VCO input signal to reach higher values, while PD remains within its output range, though at the expense of ringing.

However, for Type III PLL cases, the phase error will tend to zero, i.e.:

$$\lim_{x\to\infty} \theta_e(t) = 0 \tag{5}$$

what means that zero phase error tracking is possible for any chirp signal when Type III PLLs are used. The model in Fig. 1 suggests that the contribution of LF3 complements the LF2 voltage signal and compensates the delay introduced by the later, reducing to zero the signal component provided by the PD. Despite these results are based on a linear simplified analysis, and therefore expression (5) is an approximation, it should be obvious that the ability of Type III PLLs to achieve tracking for chirp, and even more complex signals, is higher.

Unfortunately, the zero-pole pairs that make the dynamic behaviour described above possible, come along with peaking in the PLL frequency response. As a consequence, some phase noise and ringing in the transient are introduced in the PLL. Unfortunately, it is not possible to obtain closed form expressions relating that this peaking with the pole-zero frequencies that produce it. However, an approximate expression to estimate the phase margin from these frequencies and the loop gain k has been proposed by authors in [18]. In addition, a qualitative analysis of how poles and zeros influence global response, and some quantitative estimations on their ratios for a desired response were proposed [4]. Based on those analysis, in the next section, we will further explore the similarities and differences between Type II and III PLLs, what is the main objective of this paper.

3 Type II Versus Type III PLLs

In this section, we will compare the behaviour of Types II and III PLLs through extensive simulation results, making use of the Simulink behavioural model described in [3] and [18]. We will first show some representative results for a basic third-order Type II, for which free running frequency (FRF), loop gain (k) and ω_{p1} (high- frequency

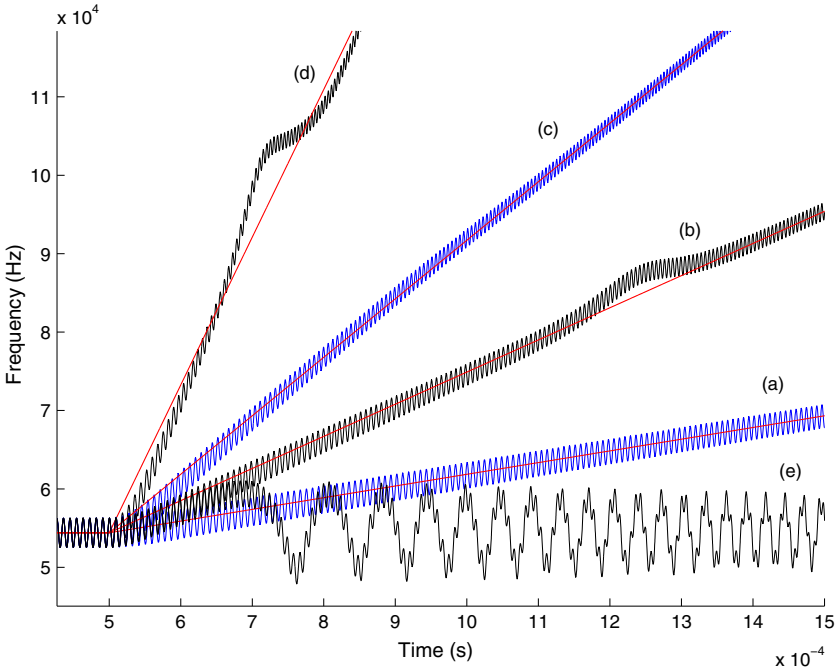

Fig. 3 Maximum frequency slope trackable for different PLLs: *a* II3 with $\omega_{z1} = 0.1K$, *b* III4 with $\omega_{z1} = \omega_{z2} = 0.1K$, *c* II3 with $\omega_{z1} = 0.5K$, *d* III4 with $\omega_{z1} = \omega_{z2} = 0.5K$ and *e* Type I PLL with no zeros

pole) have been set to 272, 20 and 400 KHz, respectively. According to [2], the maximum slope achievable by a Type II PLL is proportional to its zero frequency which is restricted to values not to close to K. Thus, there is a limitation in the frequency slope that any Type II PLL is able to keep track to.

Extensive transient simulations have been carried out with Simulink to check the validity of the theoretical predictions. Some of those results can be seen in Fig. 3. There, time responses taken at the VCO input are represented when the input signal undergoes a linear increase in its frequency, i.e. a frequency ramp, as it is the case of Doppler affected transmissions. Since depicted curves are VCO input signals, they can be considered proportional to the instantaneous frequency.

In particular, the maximum frequency slopes trackable by different PLLs are depicted. Curves (a) and (c) correspond to third-order Type II PLLs with $\omega_{z1} = 0.1K$ and $\omega_{z1} = 0.5K$, respectively. The maximum slopes shown in Fig. 3 are very close to the values predicted by (4) for Type II PLL (sinusoidal PD) and therefore support its validity. In contrast, curves (b) and (d) belong to fourth-order Type III devices where we have added the second pole at the origin, and a zero $\omega_{z2} = \omega_{z1}$. The selection of both zeros at the same frequency responds to the limitation in the tracking capability imposed by the higher time constant present in the loop. Thus, the maximum frequency slope achieved is maximized with double zeros. Finally, the time response of a second-order Type I PLL is shown in curve (e) for comparison purposes. This device obviously loses track since there are no low-frequency zeros in its LF, and thus

Table 2 Maximum frequency slope, peaking and PM (theoretical and approximated) for different PLLs

PLL	Curve	ω_{z1} (Hz)	ω_{z2} (Hz)	$\text{Slope}_{\text{Max}}$ (Hz/s)	Peak (dB)	PM (°)	$\text{PM}_{\text{approx}}$ (°)
II3	(a)	$0.1K$	–	$0.099K^2$	0.6	81.4	82.0
III4	(b)	$0.1K$	$0.1K$	$0.26K^2$	1.3	75.8	76.7
II3	(c)	$0.5K$	–	$0.48K^2$	2.2	62.4	60.8
III4	(d)	$0.5K$	$0.5K$	$1.23K^2$	5.7	40.6	34.3
III4	(a')	$0.038K$	$0.038K$	$0.099K^2$	0.5	82.8	83.3
III4	(c')	$0.19K$	$0.19K$	$0.48K^2$	2.3	66.2	67.2

it presents finite DC gain. A more detailed analysis of Type I devices is presented in [2]. Comparing curve (e) with the previous ones, the differences between the keep and lose of track can be observed in the time domain.

Even though the maximum slope is theoretically infinite for Type III PLLs, this is not the case in practice, where some cycles might slip before locking if frequency variation is quick enough. We have represented in Fig. 3 the slope where cycle slipping begins and considered it as the maximum achievable slope. Taking this into account, the figure shows the increase in maximum slope achieved by introducing ω_{z2} to achieve a Type III PLL. Actually, the improvement can be quantified as a factor of 2.5 in the slope, approximately. Further details can be seen in Table 2.

In addition to that, Type III transient behaviour differs from that of Type II in the presence of a "bump" that can be clearly seen in Fig. 3, curves (b) and (c). This phenomenon marks the instant when LF3 starts to compensate the phase error signal, so the later decreases to zero. If the frequency slope is too high, the phase error compensation process can take too long, the bump also lasts longer, and consequently the PLL might slip some cycles.

In order to complement, the time domain comparison between Type II and III PLLs, we have also tested them under a quadratic variation in the input signal's frequency. This kind of complex signals, suggested in [17] and [6], are sometimes taken into account, as for example, in Doppler effect applications. In Fig. 4, we show a transient analysis in different nodes of the LF. The quadratic term of the input frequency has been chosen such that both PLLs lose the lock state at some instant. However, in Type II (left column), this happens almost instantaneously, while Type III keeps locked longer. The first row of the figure shows the LF1 output which is a filtered version of the phase error. There, the unlock instant is clearly observed for both devices when the phase error reaches the maximum allowed by the PD. The second row shows LF2 filter contribution (see Fig. 1), which is almost negligible for Type II, while in Type III grows as it does the input frequency. Although LF2 output and VCO input seem to have the same quadratic variation pattern they have not. In fact, it is the result of adding both LF2 and LF3 output signals which have that quadratic pattern, since LF3 corrects the growing delay introduced by LF2 until the PLL unlocks. Finally, the last row shows the output of the LF, i.e. the VCO control signal. Here, the input signal frequency has been depicted in red dash to ease the comparison, since VCO input signal must follow it to keep lock.

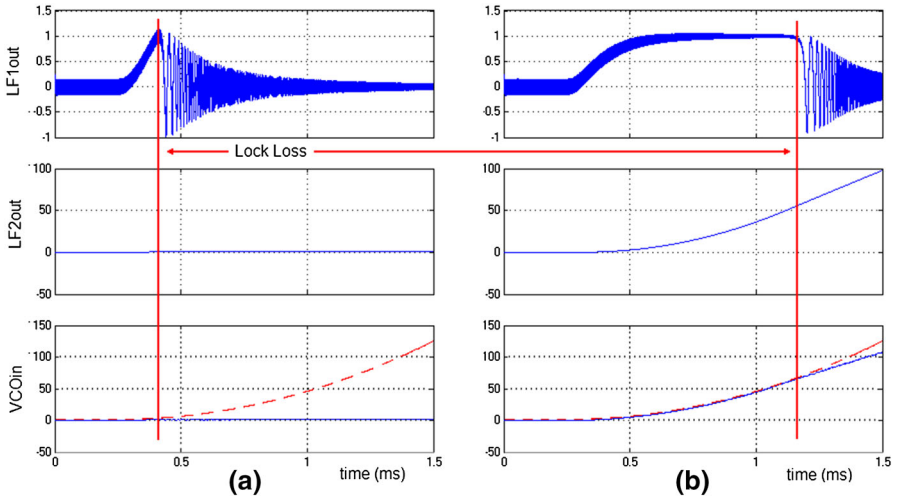

Fig. 4 Transient response comparison between Type II (**a**) and Type III (**b**) PLLs against a quadratic frequency variation in the input signal

Regarding the frequency response and focusing on the peaking behaviour, we show the corresponding results in Fig. 5.1. The increasing trend in the peak magnitude from curve (a) to (d) can be interpreted as follows: first, the closer the zero is to K, the stronger the peaking is. Second, the introduction of the new zero also increases the peak magnitude in Type III PLLs (Table 2). Expression (6) shows that both of them have also a certain influence in the phase margin (PM) of the PLL, as demonstrated by authors in [18]. The relation between the zeros and pole frequencies and the loop gain, K, appears as a critical aspect in the design of stable PLLs, specially high-order and high-type ones where stability is such a pursued characteristic.

$$\mathrm{PM} = 90 - 53\left(\sum_{i=1}^{N}\frac{\omega_{zi}}{K} + \sum_{j=1}^{M}\frac{K}{\omega_{pj}}\right) \tag{6}$$

Theoretical and approximated PM values for the simulated PLLs can be analysed and compared in Table 2. They clarify how strong the relation between the pole and zero frequency ratios (frequency divided by K) and the resultant PM is. Thus, order and/or type increments need to be done with extreme care to preserve the stability of the device. Due to that, there is always a trade-off between the chirp signal tracking capability of Type III PLLs and their poorer stability and peaking. In other words, the use of a Type III PLL instead of a Type II cannot be accomplished by simply adding a new pole/zero in the same position. It has to be completely redesigned to achieve the desired performance, but placing the poles correctly to preserve the same, or even better, phase margin and peaking.

To see how this can be done, we can make the same analysis from a different perspective: we design and calculate Types II and III PLLs to achieve and track the same maximum slope, making use of the results shown so far. To this end, expression

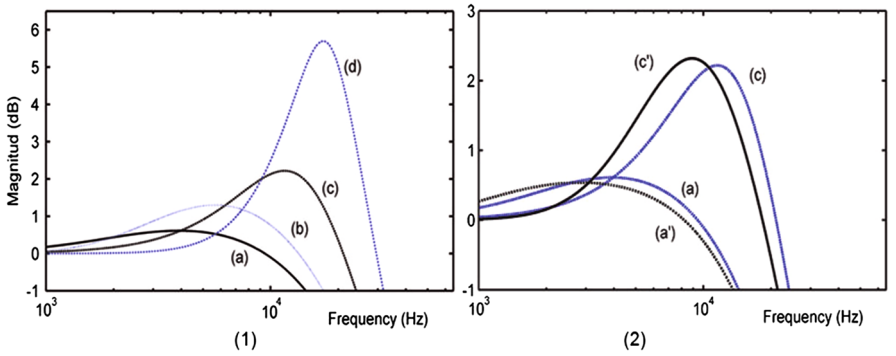

Fig. 5 Subfigure **1** magnitude response of the PLLs in Table 2. *a* II3 with $\omega_{z1} = 0.1K$, *b* III4 with $\omega_{z1} = \omega_{z2} = 0.1K$, *c* II3 with $\omega_{z1} = 0.5K$ and *d* III4 with $\omega_{z1} = \omega_{z2} = 0.5K$. Subfigure **2** peaking comparison between Type II and Type III PLLs with the same maximum slope: *a* II3 with $\omega_{z1} = 0.1K$, *a'* III4 with $\omega_{z1} = \omega_{z2} = 0.038K$, *c* II3 with $\omega_{z1} = 0.5K$ and *c'* III4 with $\omega_{z1} = \omega_{z2} = 0.19K$

(4) allows to calculate the zero location for a Type II PLL which maximizes the slope. For Type III PLLs, the calculation of the zeros (we assume both in the same position) has to be done experimentally, with the aid of the empirically obtained factor of 2'5 that, according to our previous results, relates maximum slopes in Types II and III (see Fig. 3).

In Fig. 5.2, we show the magnitude responses obtained with each one of the devices described above. Lines (a) and (c) correspond to the original Type II devices, while (a') and (c') correspond to the Type III PLLs experimentally extracted to present the same maximum slope frequency. All of them are properly described in Table 2.

Analysing Fig. 5.2, it can be concluded that the peaking performance of the Type III devices is slightly better than it is for Type II ones. At the same time, the PM values (theoretical and approximate), shown in Table 2, are also better for Type III devices. Obviously, when the zero(s) frequency(ies) gets closer to K, the performance of Type III PLLs worsens in terms of peaking. Despite of that, the PM of Type III remains higher than Type II's since ω_{z1} in these cases is greater than the sum of ω_{z1} and ω_{z2} in Type III ones. Therefore, the advantages of Type III become even more clear for zeros closer to K.

4 High-Order and High-Type Generalization

At this point, in order to generalize the results and conclusions obtained above, the influence of the high-frequency pole ω_{p1} will be evaluated. With this purpose, all the PLLs (both Type II and Type III) shown so far have to be redesigned with different ω_{p1} values. The selected values are $2K$ and $4K$ (much closer to K than the original $20K$), which will make the effect of ω_{p1} in all the results more evident.

Figure 6a shows the relation between the zero(s) frequencies and the maximum frequency slopes obtained following the process described above. Two different groups of lines can be seen. Dash-dotted lines correspond to Type II devices, while solid ones show Type III results. First to notice is that ω_{p1} value influence is negligible, since the

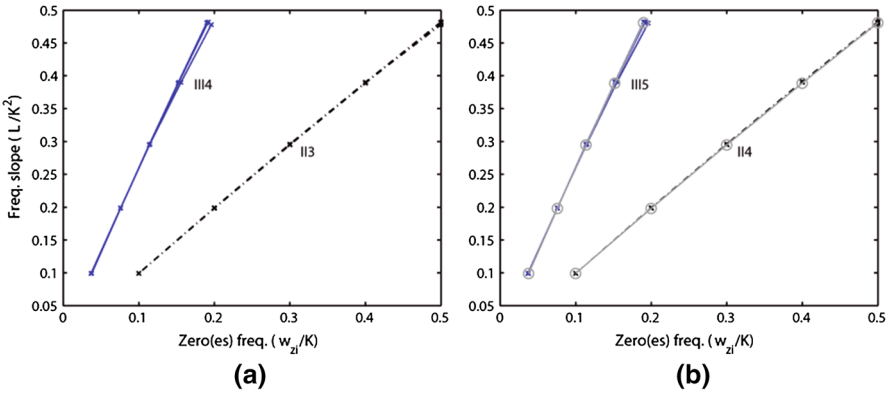

Fig. 6 **a** Relation between maximum slope achievable and zero frequency for (**a**) II3 and III4 PLLs, **b** II4 and III5 PLLs

three lines (corresponding to the three values assigned to ω_{p1}) are almost overlapped for each case. Secondly, in all the cases, the relation between the maximum frequency slope and the zero(s) frequency(ies) is approximately linear. This means that is possible to approximately extract one from the other very easily.

To complete the comparison between Type II and Type III devices, the cases that satisfy the condition order = type + 2 (i.e. LF1 is second order) are studied. In order to do that, another high-frequency pole is added to all the devices before simulating again. The followed criteria to establish the location of the high- frequency poles are equivalent to that used with the zeros: both at the same frequency. Besides, that frequencies are selected using expression (6) such that the PM is not affected, i.e. double than the original: $40K$, $8K$ and $4K$, respectively.

In Fig. 6b, the relation between zero frequencies and maximum frequency slope is shown for fourth-order Type II (dash-dotted lines) and fifth-order Type III PLLs (solid lines). To ease the comparison between Fig. 6a, b, two references from the former have been included with circled lines. As can be seen, the differences between these two figures are almost unnoticeable. This corroborates the previous conclusion that the high-frequency poles (number and location) do not affect significantly the PLL behaviour in terms of the differences between Type II and III.

Once the poles influence has been neglected, we can extract an empirical relation between the zero frequency and the maximum slope achievable. For any Type II PLL, the linear approximation found is:

$$\left(\frac{\Lambda}{K^2}\right) \approx 0.95 \left(\frac{\omega_{z1}}{K}\right)_{\text{II}} \tag{7}$$

which is in agreement with (3). For Type III case, the same relation can be expressed in the form:

$$\left(\frac{\Lambda}{K^2}\right) \approx 2.46 \left(\frac{\omega_{z1}}{K}\right)_{\text{III}} \tag{8}$$

where Λ is the frequency slope of the signal applied to the PLL and $\left(\frac{\omega_{z1}}{K}\right)_{\mathrm{II}}$ and $\left(\frac{\omega_{z1}}{K}\right)_{\mathrm{III}}$ are the respective zero frequencies (in Type III case $\omega_{z1} = \omega_{z2}$).

Taking into account that the slope values represented are the exact same Type II, and Type III cases Fig. 6a, b suggest as well that there exists a relation between $\left(\frac{\omega_{z1}}{K}\right)_{\mathrm{II}}$ and $\left(\frac{\omega_{z1}}{K}\right)_{\mathrm{III}}$ that make possible each maximum slope. From (7) and (8) this relation can be approximated as:

$$\left(\frac{\omega_{z1}}{K}\right)_{\mathrm{III}} \approx 0.39 \left(\frac{\omega_{z1}}{K}\right)_{\mathrm{II}} \tag{9}$$

This means that any Types II and III PLLs (no matter the number or location of high-frequency poles) whose zero frequencies are related by expression (9) will be limited to the same maximum slope when following chirp signals. Obviously, the phase error will be zero for the Type III PLL, while nonzero for the Type II one. Furthermore, particularizing expression (6) for a Type III PLLs and substituting (9), the relation between Type II and Type III phase margin results:

$$\mathrm{PM}_{\mathrm{III}} \approx \mathrm{PM}_{\mathrm{II}} + 11.87 \left(\frac{\omega_{z1}}{K}\right)_{\mathrm{II}} \tag{10}$$

which means, despite the accurateness of expression (10), that for any Type II and Type III pair of PLLs (with the same high-frequency poles) designed as described above the Type III's PM will be always greater. This result contradicts the extended belief that high-order PLLs are of no practical use and very difficult to make stable [12].

5 Conclusions

A comparison between Type II and Type III PLLs behaviour has been presented in this work. More precisely, the performance of each one has been studied in terms of response against signals with ramp-varying frequency, i.e. chirp kind signals. In order to do that, we have used the PLL model presented in [1–3,18].

First of all, we have demonstrated that both Type II and Type III are capable of tracking chirp type signals being the maximum frequency slope limited by ω_{z1}, ω_{z2} (in Type III cases) and K. Moreover, there are two main differences between the behaviour of them. The first one consists in the presence of a nonzero phase error signal in Type II PLLs (responsible for the limit in de maximum frequency slope), while the phase error signal remains zero in Type III devices. The second difference is more obvious and important: Type II devices are unable to get back in track once the slope has trespassed the limit, while Type III devices always get track back after, in the worse case, losing some signal cycles.

Secondly, we have seen that both Type II and III devices experiment an increment in the peaking value proportional to the number of zeros and its proximity to K, along with the logic reduction in the PM since it is directly related to the peaking. We have found that PM is always higher in Type III PLLs compared with Type II ones when designed to exhibit the same maximum frequency slope. This contradicts the general belief that Type III PLLs are very difficult to make stable: they can be even better

in terms of stability and peaking when properly designed. Furthermore, a quasilinear relation between the zero(s) frequency(ies) and the maximum frequency slope have been shown for both Type II and III devices, which brings another relation between those zero frequencies themselves.

Finally, the study of order = type + 2 devices (i.e. LF1 of second order) has verified the conclusions extracted from order = type + 1 PLLs. Moreover, it has been demonstrated that the number and location of high-frequency poles does not affect the chirp kind signal tracking capability of the PLL.

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