Low-power wide-bandwidth CMOS indirect current feedback instrumentation amplifier

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Abstract

The analysis and design trade-offs of a simple and economical technique to implement wideband low-voltage CMOS instrumentation amplifiers (IAs) based on indirect current feedback (ICF), are described. The input and an output transconductors consist of two super-source-followers and a resistor. As a result, the overall performance of the IA is enhanced. A thorough analysis of the proposed technique provided valuable insight on its operation. Two different realizations in 0.35-μm CMOS technology of an IA operating with a supply voltage of 3 V, are presented. In particular, a wide bandwidth single-stage IA with fixed voltage gain equal to 50 V/V and a low-power two-stage IA with externally programmable voltage gain, have been designed and characterized by extensive simulations. The simulated results of both circuits showed an improved response in terms of bandwidth, noise and power consumption, while their overall performance is comparable to other proposed approaches in terms of common-mode rejection ratio (CMRR) and linearity (THD).

Keywords: indirect current feedback, instrumentation amplifier, source degeneration, super-source-follower, wide bandwidth

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1. Introduction

Instrumentation amplifiers (IAs) play an essential role in the conditioning of signals coming from sensors, as well as in many other data acquisition systems [1–36]. IAs are analog blocks required in precision applications with a high gain to amplify low-level voltage differences between two signals, i.e., the differential-mode (DM) component, and a high input impedance. Along with the above features, it is also required that IAs cancel out any voltage signal common to both inputs terminals, that is, the common-mode component (CM). Inadequate rejection of DC and AC CM signals causes errors that result very difficult to be removed from the IA output signal. It is very usual to express the elimination of CM signals in an IA by also considering the DM voltage gain, thus invoking the common-mode rejection ratio (CMRR). In [1] a comprehensive description of all IA magnitude specifications and performance, is provided.

A wide variety of techniques may be found in the literature, either to improve the general performance of the IA or to optimize some particular characteristics in a given application. The conventional IA, based on the use of three operational amplifiers with resistive feedback [2–5], does not result appealing for a monolithic implementation and multiple approaches have been used for embedding IAs in an IC [2]. Among them, current feedback (CF) [6–15], supply current sensing (SCS) [16, 17], differential difference amplifiers (DDAs) [2, 18] or current-mode solutions [19, 20] may be enumerated. Besides, techniques such as auto-zero [21], correlated-double sampling [22], chopping [23–34], AC-coupling [35] or discrete-time signal processing [36] are often used, especially in low-frequency high-gain applications where $1/f$ noise and offset voltage play a critical role.

In this contribution the analysis and design trade-offs of a simple and economical approach to implement a CMOS IA suitable for wideband, low-voltage and low-power operation, are presented and its performance is compared to other solutions previously proposed. In particular, the aim of the proposal is to include the designed IA in an analog front-end for electrical bioimpedance

spectroscopy. The rest of the manuscript has been organized as follows. Section 2 reviews two classical approaches of IAs based on resistive feedback and CF, respectively. A CF IA, which is obtained by incorporating high-performance voltage-to-current (V-to-I) converters, is described in Section 3. Section 4 deals with an analysis of the key characteristics of the proposed transconductor, while in Section 5 two realizations in 0.35-μm CMOS technology of an IA operating in a 3 V supply are presented. In Section 6 simulated results are provided and discussed, while, finally, conclusions are drawn in Section 7.

2. Resistive feedback *vs* current feedback IAs

The operation of the most commonly used IAs is based on two main techniques known as resistive feedback and current feedback, respectively. The resistive feedback approach, also known as three-opamp IA, carries out the amplification process in two steps. A first stage, consisting of two opamps configured as noninverting voltage followers with the help of several resistors, is used to provide the IA with high input impedance. In this circuit section the CM component of the signal is processed with unity gain [16], while the DM signal is conveniently amplified with a gain adjunstement that relies on only one resistor. The second stage, which is the core of the IA, is made up of a difference amplifier, which cancels out the CM input component, while usually no (or, at most, small) DM gain is provided.

The three-op-amp IA solution presents several drawbacks. On the one hand, its use in ASICs realizations increases the silicon occupied area as well as the power consumption. Secondly, the CMRR relies on the matching of the feedback resistors in the difference amplifier, which must be trimmed to improve this metric. Last, but not least, the coupling of the CM signals of the first and the second stage may restrict seriously the input CM voltage of the IA.

CF is a competitive and popular alternative to resistive feedback technique mainly for implementing monolithic IAs. The general configuration of a CF IA consists of two transconductors whose output currents are forced to be equal

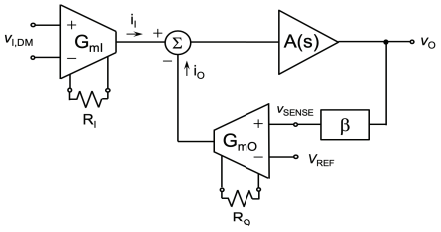


Figure 1: Block diagram of an IA based on indirect current feedback.

by means of a negative feedback action [6]. If there is a single feedback loop around the input and output transconductors the IA may be classified as direct current feedback (DCF) [8] or indirect current feedback (ICF) [9]. DCF employs two stacked transconductors, thus leading to lower power consumption. Nevertheless, this arrangement finds limitations to operate with a low supply voltage. ICF uses two cascaded transconductors instead, thus leading to higher power consumption but resulting more appropriate for operation in low-voltage environments. Alternatively, when there are two different feedback loops controlling the input and output transconductors the technique is known as local current feedback (LCF) [6, 10, 12–14].

The principle of operation of the ICF technique can be described with the block diagram of Fig. 1, disregarding resistors R_I and R_O for the moment. As observed, it consists of two V-to-I converters, transconductors G_{mI} and G_{mO}, a summing section, where the inverse operation of I-to-V conversion takes place, and a gain stage, $A(s)$. The input DM voltage signal, $v_{I,DM}$, is applied to transconductor G_{mI}, thus obtaining a proportional output current, i_I. Similarly, the feedback transconductor, G_{mO}, provides a current i_O from the voltage difference $v_{SENSE} - V_{REF}$, where v_{SENSE} is equal to the output voltage, v_O, scaled down by the feedback factor, β, and V_{REF} is a reference voltage used as the desired DC voltage level at the output of the IA. If the gain of the feedback loop is high enough, its action forces currents i_I and i_O to be

equal. Then, the DC voltage gain for the IA is given by the expression:

$$A_v \equiv \frac{v_O}{v_{I,DM}} \approx \frac{G_{mI}}{G_{mO}} \frac{1}{\beta} \tag{1}$$

where β is in practice implemented as a simple resistive divider.

Unlike in conventional resistive feedback IAs, CM rejection in an ICF IA takes place mainly at the input stage. Besides, resistive source degeneration is used in the input and feedback transconductors [7], as it had been made explicit by including resistors R_I and R_O in Fig. 1. The use of this linearization technique is twofold. On the one hand, it helps to increase the input DM voltage range of the transconductors. On the other hand, transconductances G_{mI} and G_{mO}, and hence A_v in (1), become a function of R_I and R_O, respectively.

3. Improving the *V*-to-*I* conversion in ICF IAs

As stated previously, the performance of V-to-I converters used for implementing the input and feedback transconductors impacts strongly on the overall performance of an ICF IA. An idealized implementation of a V-to-I converter is shown in Fig. 2a, which consists of a passive resistor, R, and two ideal unity-gain voltage followers. Indeed, when signals v_I^+ and v_I^- are applied to the voltage buffers, they are replicated to the resistor terminals, namely v_A and v_B, and a corresponding current is linearly generated. The effective transconductance may be expressed as

$$G_{m,IDEAL} \equiv \frac{i_O}{v_{I,DM}} = \frac{i_O}{v_{AB}} \frac{v_{AB}}{v_{I,DM}} = \frac{2}{R} \tag{2}$$

where the factor of 2 accounts for the fact that each of the two voltage buffers provides the summing stage with a copy of the signal current.

The key point of this transconductor approach is the actual implementation of the voltage followers, as they usually introduce a systematic offset voltage and their voltage gain may vary from the ideal value of unity. It should also be pointed out that the realization of the voltage follower must facilitate collecting the current signal generated in the resistor for its subsequent processing.

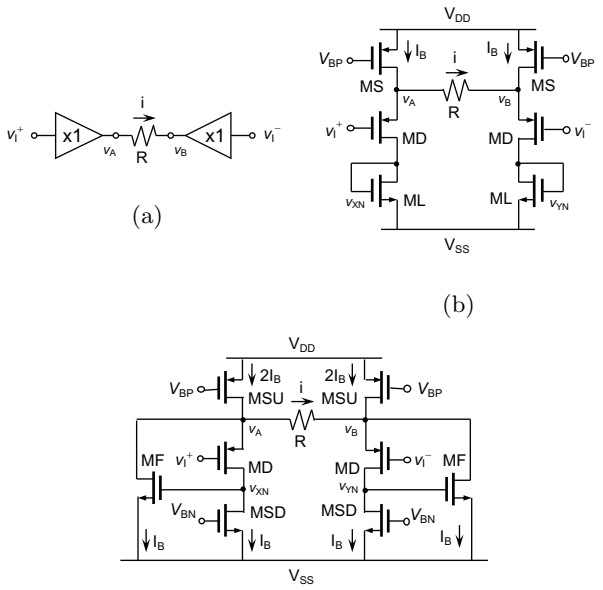


Figure 2: V-to-I converters based on the (a) ideal voltage follower, (b) source-follower (SF), and (c) super-source-follower (SSF).

A conventional approach to build a practical V-to-I converter, illustrated in Fig. 2b, is based on using the source follower (SF) as voltage buffer in order to isolate the preceding stage from the resistor in which V-to-I conversion takes place [8–10]. A PMOS implementation has been selected in order to avoid the body effect in an n-well technology, while the goal of transistors ML is to collect and reflect to subsequent stages the current signal generated in the transconductance cell. However, the use of a SF as voltage buffer presents two main drawbacks. First, its output resistance approximately coincides with

$$R_{out,SF} \approx \frac{1}{g_{mD}} \tag{3}$$

where g_{mD} is the transconductance of the driver transistors MD. In general, this value of the output resistance is not low enough as compared to values of R implementable in IC technologies and, hence, the SF with resistive degeneration

suffers from significant load regulation. This effect may be clearly denoted by considering the voltage gain of the followers in Fig. 2b. In such case the corresponding voltage gain is given by:

$$A_{v,SF} \equiv \frac{v_A}{v_I^+} = \frac{v_B}{v_I^-} = \frac{1}{1 + \frac{2}{R}\frac{1}{g_{mD}}} \tag{4}$$

As observed, $A_{v,SF}$ decreases as the value of resistor R is reduced. In addition, it is worth to point out that the current flowing through transistors MD is a function of the input signal, which limits the intrinsic linearity of the circuit.

The overall performance of the voltage follower may be greatly improved with minor modifications, such as replacing each SF by a super-source-follower (SSF) [37] to drive resistor R. The resulting circuit is depicted in Fig. 2c [15]. Now, the output resistance of the voltage buffer is given by the following expression:

$$R_{out,SSF} \approx \frac{1}{g_{mD}\frac{g_{mF}}{g_{oD}+g_{oSD}}} \tag{5}$$

where every symbol keeps its usual meaning. Comparing (3) and (5), the output resistance of the improved follower is the SF counterpart reduced by an amount equal to the voltage gain of the feedback loop formed by transistors MF and MD, i.e., $g_{mF}/(g_{oD} + g_{oSD})$. This improvement in R_{out} highly reduces the load regulation of the voltage buffer and brings the gain value of the voltage followers in Fig. 2c much closer to the ideal value of unity, as it may be inferred from:

$$A_{v,SSF} = \frac{1}{1 + \left(1 + \frac{2}{R}\frac{1}{g_{mD}}\right)\left(\frac{g_{oD}+g_{oSD}}{g_{mF}}\right)} \tag{6}$$

In this case, and compared to $A_{v,SF}$ in equation (4), the term relying on the value of resistor R is divided by the gain of the feedback loop implicit in the SSF and, hence, the voltage gain results very close to unity.

It is worth to point out that the input CM voltage range of the transconductors based on the SF and the SSF solutions includes the region around midsupply, resulting of direct application for signals with a DC voltage level close the analog ground. Besides, the operating voltage range may easily reach

the negative rail, provided that transistors ML (Fig. 2b) and MF (Fig. 2c) do not to force the input devices, MD, to operate is the linear region. This may be achieved by selecting for transistors ML and MF such an aspect ratio, (W/L), that their corresponding gate voltage is conveniently set with respect to V_{SS}. This feature results essential in case the signal to be acquired is not superimposed to a DC voltage [9]. On the contrary, the input CM voltage range of both V-to-I converters finds a hard limitation close V_{DD}, as the PMOS implementations in Figs. 2b and 2c require a margin equal to a source-to-gate voltage plus a source-to-drain saturation voltage with respect to the positive rail to, respectively, turn the input devices on and keep the current sources operating in saturation. Thus, if the signal to be processed has a DC voltage level around V_{DD} an NMOS implementation of the transdoncuctor should be selected.

4. Design considerations

An analysis of the main characteristics of the used transconductor is carried out next. The results obtained are used for performance comparison of the proposed ICF IA with respect to the approach in which the V-to-I converters are based on SF counterpart. Besides, they will also facilitate the design optimization of the proposed IAs.

4.1. DM effective transconductance

The effective transconductance of a V-to-I cell, G_m, may be defined as the output current obtained in response to a purely DM voltage signal, $v_{I,DM}$, applied at the input terminals. When the transconductance block is implemented by using the SF as voltage buffer, Fig. 2b, the effective transconductance coincides with:

$$G_{m,SF} = \frac{2}{R}\frac{1}{\left(1+\frac{2}{R}\frac{1}{g_{mD}}\right)} \tag{7}$$

As observed, the effective transconductance consists of the product of two terms. The first one, which represents the ideal behavior, is inversely proportional to

Table 1: Transistor aspect ratios (μm/μm) and biasing currents (μA) for the SF (Fig. 2b) and SSF (Fig. 2c) V-to-I converters.

Device	**SF**	**SSF**
MD	300/3	300/3
MS	40/2	—
ML	10/1	—
MF	—	10/1
MSD	—	10/2
MSU	—	80/2
I_B	20	20

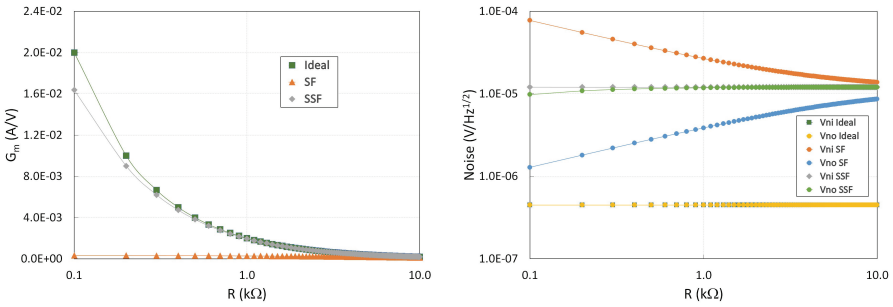
the value of the passive resistor R. The second term arises for the loading effect of the resistor on the voltage followers. If the effective transconductance wants to be increased, the value of the resistor must be decreased accordingly. However, this fact impacts negatively the loading effect, thus decreasing the attenuation factor and, hence, the effective transconductance.

An analysis of the equivalent small-signal circuit of the SSF transconductor, Fig. 2c, leads to the following expression for the effective transconductance:

$$G_{m,SSF} = \frac{2}{R} \frac{1}{\left[1 + \left(1 + \frac{2}{R}\frac{1}{g_{mD}}\right)\left(\frac{g_{oD}+g_{oSD}}{g_{mF}}\right)\right]} \tag{8}$$

Now, the load regulation effect is greatly reduced by the negative feedback action carried out in the voltage follower. Indeed, it may be observed in the denominator of the most right term in (8) that the expression depending on R is now divided by the gain of the feedback loop implemented by transistors MF and MD. As a consequence, the attenuation term is very close to unity even for values of R relatively low.

The impact of the value of resistor R on the effective transconductance of the V-to-I converters based on the SF and the SSF solutions, is depicted in Fig. 3a. In particular, the simulated value of G_m is represented as a function of R for the two transconductor implementations illustrated in Figs. 3(b) and 3(c), with the transistor aspect ratios and biasing currents shown in Table 1. The response of the ideal case in Fig. 2a, where an ideal behavior of the voltage follower is assumed, is also included for the sake of comparison. The different plots in Fig.



(a) (b)

Figure 3: (a) Effective transconductance and (b) input referred voltage noise of SF and SSF approaches as a function of resistor R.

3a show that the transconductance response of the SSF V-to-I converter is very close to the ideal behavior of G_m, given by eq. (2), and is inversely proportional to R. The response of the SF remains far from the intended operation, which becomes especially evident for low values of resistor R.

4.2. CM residual transconductance

The main contribution of the input and output transconductors of the ICF IA to the overall transconductance is due to the response to the input DM voltage, $v_{I,DM}$. Nevertheless, there is a second-order effect over the DM effective transconductance due to the joint action of input CM voltage, $v_{I,CM}$, and mismatches. This additional term may be neglected in the case of the output transconductor, as it represents just a minor component of the overall output transconductance. Nevertheless, it results critical for the input V-to-I converter. In fact, it is the main mechanism for the degradation of the CMRR, which constitutes a key performance parameter of an IA. The residual transconductance associated to the response to $v_{I,CM}$ may be defined as follows:

$$\Delta G_m \equiv \frac{\Delta i_O}{\Delta v_{I,DM}} \tag{9}$$

In case of perfectly matched V-to-I converter circuits in Figs. 2b and 2c, the result of (9) would be equal to zero. Nevertheless, unavoidable random mis-

Table 2: Main contributions to ΔG_m for SF- and SSF-based transconductors.

Parameter	ΔG_{mSF}	ΔG_{mSSF}
Δg_{mD}	$\frac{2}{R}\frac{\Delta g_{mD}}{g_{mD}}\left(\frac{g_{oD}+g_{oS}}{g_{mD}}\right)\frac{1}{\left(1+\frac{2}{R}\frac{1}{g_{mD}}\right)}$	$\frac{2}{R}\frac{\Delta g_{mD}}{g_{mD}}\frac{g_{oD}}{g_{mD}}\frac{1}{\left[1+\frac{2}{R}\frac{1}{g_{mD}}\left(\frac{g_{oD}+g_{oSD}}{g_{mF}}\right)\right]}$
Δg_{oD}	$\frac{2}{R}\frac{\Delta g_{oD}}{g_{mD}}\frac{1}{\left(1+\frac{2}{R}\frac{1}{g_{mD}}\right)}$	$\frac{2}{R}\frac{\Delta g_{oD}}{g_{mF}}\frac{1}{\left[1+\frac{2}{R}\frac{1}{g_{mD}}\left(\frac{g_{oD}+g_{oSD}}{g_{mF}}\right)\right]}$
Δg_{oS}	$\frac{2}{R}\frac{\Delta g_{oS}}{g_{mD}}\frac{1}{\left(1+\frac{2}{R}\frac{1}{g_{mD}}\right)}$	—
Δg_{mF}, Δg_{oF}, Δg_{oSU}, Δg_{oSD}	—	Negligible

matches always cause a non-zero response to input CM voltages. The different contributions to ΔG_m have been determined through simulations, by varying the small-signal transconductance, g_m, and output conductance, g_o, of the different transistors involved in the SF and SSF transconductors with respect to its nominal value. In particular, when parameter g_i is considered, values equal to $g_i + \Delta g_i/2$ and $g_i - \Delta g_i/2$, respectively, are assumed for symmetrical devices in every implementation. The main contributions to ΔG_m have been derived from a thorough hand analysis and included in Table 2. As observed, for implementations based on SF all mismatch contributions are significant, while for the SSF alternative the influence of the feedback transistor, MF, and the current source transistors, MSU and MSD, may be neglected. Besides, it is worth to note that the implicit feedback in the SSF structure again reduces its load regulation. As a consequence, its CM residual transconductace, $\Delta G_{m,SSF}$, experiments the same boosting as the DM effective transconductance, $G_{m,SSF}$, in (8).

Both G_m and ΔG_m have been quantified for the SF and the SSF approach by taking into account the different terms in (7), (8) and Table 2. To this end, the nominal values of the small-signal parameters of the devices, corresponding to the sizes and biasing currents in Table 1, have been considered. Besides, a mismatch error equal to $\pm 1\%$ and a nominal value of resistor R of 400 Ω have been assumed. Under these assumptions, the small-signal ratios $(G_{m,SF}/\Delta G_{m,SF})$ and $(G_{m,SSF}/\Delta G_{m,SSF})$ have been determined to be equal to 86.6 dB and 95.1

dB, respectively. In order to obtain a more realistic result, a 500 runs Monte-carlo analysis was carried out to determine the value of metrics G_m and ΔG_m in the case of the SF and the SSF solutions, considering in this case realistic models of the devices and parameters spreads well characterized in the fabrication technology used. The ratios $(G_{m,SF}/\Delta G_{m,SF})$ and $(G_{m,SSF}/\Delta G_{m,SSF})$ obtained from the statistical analysis were 117.1 dB and 133.0 dB, respectively, thus resulting more favorable for the SSF solution. The DM-to-CM transconductances ratio, $G_m/\Delta G_m$, provides an approximate estimation of the CMRR of the IA.

4.3. Noise

In general, IAs operate with low-level input voltages and hence, it is important to minimize the noise that the amplifier adds to the signal. In a wide bandwidth IA thermal noise is dominant as compared to flicker noise [12]. The decrease of the value of resistor R in the transconductors in Figs. 2b and 2c leads to a drop of the thermal noise contribution, along with an evident reduction in the required silicon area. Nevertheless, it may be inferred from Fig. 3a and eq. (7) that for low values of R the effective transconductance of the SF solution is highly attenuated. This fact should lead to a corresponding increase of the input referred voltage noise of this approach as compared to the case in which the SSF structure is used. The spectral density of the input referred voltage noise of the SF and SSF implementations, respectively, may be expressed in terms of its thermal component as follows:

$$\frac{v_{iNth,SF}}{\Delta f} = \left(1 + \frac{2}{R}\frac{1}{g_{mD}}\right)^2 4kT\left[R + 2\frac{2}{3}\left(g_{mD} + g_{mS}\right)R^2\right] \tag{10a}$$

$$\frac{v_{iNth,SSF}}{\Delta f} = \left[1 + \left(1 + \frac{2}{R}\frac{1}{g_{mD}}\right)\left(\frac{g_{oD} + g_{oSD}}{g_{mF}}\right)\right]^2 4kT\left[R + 2\frac{2}{3}\left(g_{mD} + g_{mF} + g_{mSU} + g_{mSD}\right)R^2\right] \tag{10b}$$

where k is the Boltzmann's constant and T is the absolute temperature. In both expressions, the first term corresponds to the output to input voltage noise conversion factor, while the second term accounts for the noise contributions of the devices involved in each respective circuit implementation. Thus, while in the case of the SF structure the conversion factor is far from unity, for the SSF this term reaches a value very close to one for a wide range of values of resistor R. Therefore, it may be concluded that, even though the SSF transconductor realization contains a few more devices contributing to the noise as compared to the SF counterpart, its input referred voltage noise is lower thanks to the behavior of its voltage gain.

The input and output voltage noise of the SF and SSF V-to-I converters is represented in Fig. 3b for different values of resistor R. The noise contribution of the ideal transconductor in Fig. 2a is also included for comparison purposes. Indeed, in the latter approach the gain of the voltage buffers is exactly equal to one and, hence, the output to input voltage noise conversion factor pointed out above is exactly equal to unity. It may be observed that the noise behavior of the SSF implementation is very similar to the ideal case, that is, input and output noises remain very constant for values of R varying over two decades, due to the fact that the voltage gain of the followers hardly relies on the value of the source degeneration resistor. Conversely, in the case of the SF cell the input referred noise sensibly increases for decreasing values of R, due to the degradation of the voltage gain of the followers for low values of the resistor.

4.4. Frequency response and feedback loop stability

Any IA must provide, in general, a sufficiently wide bandwidth according to the frequency response requirements of the particular application. The ICF IA approach operates connected in the feedback configuration illustrated in Fig. 1. The overall closed-loop transfer function of the IA may be written as:

$$H(s) \equiv \frac{v_o(s)}{v_i(s)} = \frac{G_{mI}\left(R_{out} \parallel \frac{1}{sC_{out}}\right) A(s)}{1 + \beta G_{mO}\left(R_{out} \parallel \frac{1}{sC_{out}}\right) A(s)} \tag{11}$$

where R_{out} and C_{out} are the output resistance and capacitance of the summing stage, respectively, and $A(s)$ represents the additional gain stage. The stability of the system is determined by analyzing the loop gain, that is, the transfer function of the feedback loop, which from (11), can be expressed as:

$$LG(s) = \beta G_{mO} R_{out} \left(\frac{1}{1 + sR_{out}C_{out}} \right) A(s) \tag{12}$$

System stability relies on the order of $A(s)$ and on the amount of output signal fed back, that is, on β. Indeed, in a single stage IA [12] $A(s) = 1$ and, hence, there is only one dominant pole, which ensures circuit stability by properly setting the value of capacitor C_{out}. If the gain stage $A(s)$ has a one-pole transfer function, i.e., $A(s) = 1/(1 + s/\omega_1)$, then a frequency compensation technique is required. These two cases are discussed in detail in Section 5.

5. Proposed ICF IA: two realizations

In order to illustrate the feasibility of the technique used for V-to-I conversion in high-performance ICF instrumentation amplifiers, two different circuits have been designed. Firstly, a single-stage IA with a fixed voltage gain by means of the ratio of the resistors in the input and output transconductors, has been considered. Besides, a two-stage IA with programable gain has been configured by providing the amplifier with an output stage and setting the voltage gain through the feedback factor value determined by two external resistors. Both designs have been carried out in standard 0.35-μm CMOS technology and 3 V of total supply voltage.

5.1. Single-stage ICF IA with fixed voltage gain

Figure 4 illustrates the circuit implementation of the proposed single-stage (SS) ICF IA. The input and output V-to-I converters are based on the SSF approach in Fig. 2c. The currents generated by input and output transconductors are summed by current-mirroring, with the help of transistors M1A-M1B and M2A-M2B. Indeed, the configuration in which transistors MF are connected

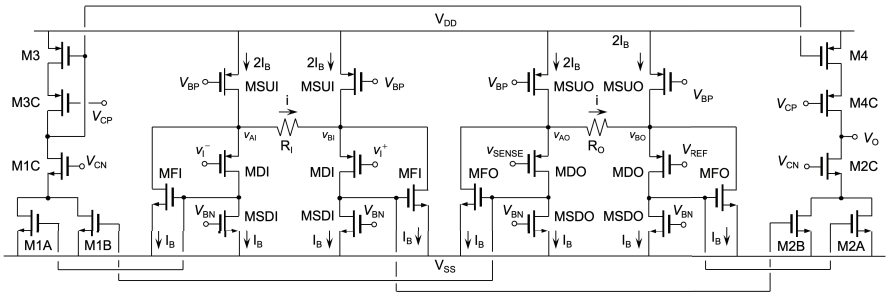


Figure 4: Circuit schematic of the SS ICF IA with fixed voltage gain.

makes convenient to use current mirrors rather than a folded-cascode solution. Besides, differential-to-single conversion is carried out by the current mirror consisting of transistors M3-M4. As observed in Fig. 4, the current mirrors of the summing stage incorporate cascode transistors so that the voltage gain of the overall feedback loop is increased. The feedback factor is made equal to unity, $\beta = 1$, by applying the output voltage, v_O, to one of the input terminals of the output transcoductor, i.e., v_{SENSE}. It is worth to note that the absence of an additional gain stage is equivalent to considering $A(s) = 1$. Therefore, particularizing eq. (11) to this case, the transfer function of the SS ICF IA is:

$$H(s) = \frac{\frac{G_{mI}}{G_{mO}}}{1 + s\frac{C_{out}}{G_{mO}}} \tag{13}$$

From (13) the closed-loop DC voltage gain and bandwidth of the IA are determined in a straightforward way and, taking (8) into account, may be expressed respectively as

$$A_{v,SS} = \frac{G_{mI}}{G_{mO}} \approx \frac{R_O}{R_I} \tag{14a}$$

$$BW_{SS} = \frac{G_{mO}}{C_{out}} \approx \frac{2}{R_O C_{out}} \tag{14b}$$

As expected, the IA voltage gain is fixed by the ratio of the values of the resistors in the output and input transconductors, R_O and R_I, respectively. Nevertheless, when the value of these resistors is not equal, the term representing the

load regulation of the voltage followers in the SSF transconductor, see eq. (8), introduces an error that could be noticeable for extremely different values of R_I and R_O. Besides, the closed-loop bandwidth of the SS IA, BW_{SS}, corresponds to the gain-bandwidth product (GBW) of the loop gain, LG_{GBW}, which is approximately equal to the unity gain frequency, f_u, in a single-pole system.

The recommended design procedure is to size first resistors R_I and R_O, in order to obtain the desired value of the IA gain according to (14a). Once R_O is set, the value of G_{mO} is fixed and, hence, loop stability is easily ensured by properly choosing the size of capacitor C_{out} so that any non-dominant pole is sufficiently above the value of f_u. Closed-loop stability is ensured by setting the minimum phase margin around 60º, which also guarantees an optimal closed-loop time settling.

5.2. Two-stage ICF IA with programmable voltage gain

The IA may be provided with programmability by using two external resistors, R_1 and R_2, as shown in Fig. 5a. In such a case, an additional output stage able to drive the feedback resistor R_2 is required in the IA. The transistor level implementation of the proposed two-stage (TS) ICF IA is illustrated in Fig. 5b. As observed, the input and summing stages are basically identical to those used in the SS approach introduced previously. Additionally, the amplifier presents a class-A output stage, transistors MOP and MON, whose driving capability is suitable if the value of external resistor R_2 is properly selected. As observed in Fig. 5b, the current mirror carrying out the differential-to-single conversion, M3-M4, is PMOS type. For this reason, the class-A output stage consists of a PMOS-type driver transistor and an NMOS current source, so that a robust cancellation of the systematic offset voltage may be achieved. In case the maximum value of the external resistors used to set the voltage gain is constrained by any specification of the IA, as for instance the noise, a class-AB approach may be easily followed to implement the IA output stage [38].

The pole introduced by section $A(s)$ in Fig. 1, leads to a two-pole response

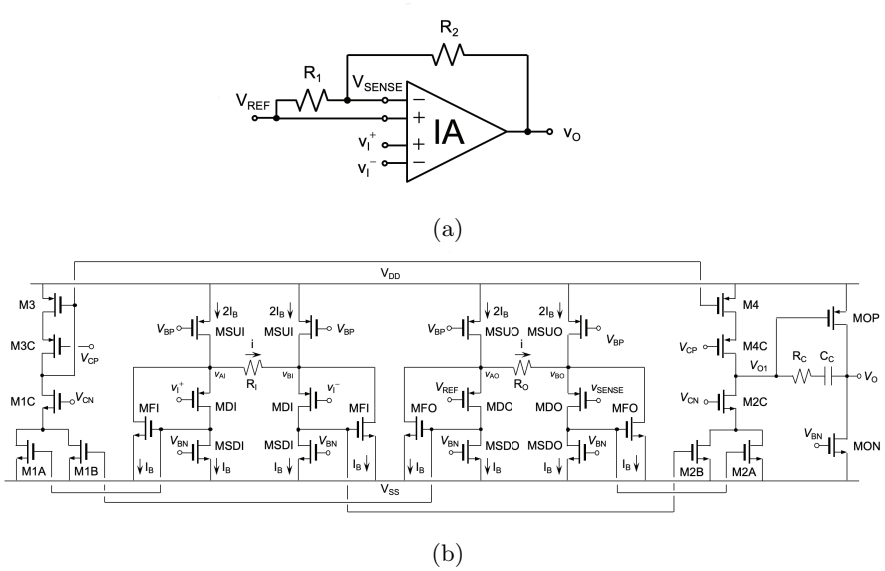


Figure 5: TS ICF IA with programmable voltage gain: (a) conceptual block diagram and (b) circuit schematic.

of the ICF IA and the corresponding transfer function is given by the expression:

$$H(s) = \frac{\frac{G_{mI}}{G_{mO}}\frac{1}{\beta}}{1 + \frac{s}{\frac{\beta G_{mO} A}{C_{out}}} + \frac{s^2}{\frac{\beta G_{mO} A \omega_1}{C_{out}}}} \tag{15}$$

where A accounts for the DC gain of block $A(s)$, that is, of the IA output stage, and ω_1 is the pole associated to this additional circuit section. Frequency compensation of the two-stage structure has been carried out by means of a passive network consisting of the series connection of capacitor C_C and resistor R_C in Fig. 5b. The C_C-R_C passive network leads to pole splitting and allows cancellation of the right half-plane zero. As a consequence, an appropriate phase margin around 60º may be easily obtained ensuring the stability of the feedback loop.

From eq. (15), the DC gain and bandwidth of the IA may be obtained. In particular, R_I and R_O are chosen equal in order to minimize the residual error

induced by the loading effect on the voltage followers of the SSF cell, and thus

$$A_{v,TS} = \frac{G_{mI}}{G_{mO}} \frac{1}{\beta} \approx 1 + \frac{R_2}{R_1} \tag{16a}$$

$$BW_{TS} = \frac{\beta G_{mO}}{C_C} \approx \frac{R_1}{R_1 + R_2} \frac{2}{R_O C_C} \tag{16b}$$

The DC voltage gain may be completely fixed by external components and is inversely proportional to the feedback factor $\beta = R_1/(R_1 + R_2)$, provided that input and output transconductors are equal. Besides, the bandwith of the IA relies on the value of the output transconductor, G_{mO}, the compensation capacitor, C_C, and the feedback factor, β. There is a design trade-off for selecting the value of resistors R_I and R_O. Indeed, large resistors values lead to increased silicon area and input referred noise. Conversely, low values of the resistors in the input and output transconductors increase the bandwidth of the IA, thus being necessary a larger compensation capacitor, C_C, for proper frequency response.

6. Simulated results

The two IA approaches described in previous Section have been designed in standard 0.35-μm CMOS technology to operate with a supply voltage of 3 V ($V_{DD} = -V_{SS} = 1.5$ V). The nominal threshold voltages for NMOS and PMOS transistors were equal to 0.50 V and -0.65 V, respectively. The source degeneration resistors were implemented with the available polysilicon layer, while current sources were in all cases single-transistor structures. The device sizes of the main transistors and bias currents in each realization are detailed in Table 3. In both cases, resistor R_I has been sized as small as possible in order to reduce silicon area and input referred noise.

The SS ICF IA has been designed to have a voltage gain equal to 50 V/V. To this end, the values of the resistors in the input and output transconductor, R_I and R_O, were set equal to 400 Ω and 20 kΩ, respectively. A load capacitor, C_L, of 1.5 pF was connected to the output terminal of the IA to set its bandwidth ensuring loop stability. Besides, a voltage buffer was required at the output of

Table 3: Transistor aspect ratios (μm/μm), resistor (kΩ) and biasing currents (μA) of the main devices in the SS and TS ICF IA in Figs. 4 and 5b.

Device	**SS ICF IA**	**TS ICF IA**
MDI	300/3	
MDO	100/1	
MSDI, MSDO	10/2	
MSUI, MSUO	80/2	
MFI, MFO	10/1	
M1A, M1B, M2A, M2B	10/1	
M1C, M2C	20/1	
M3, M4	30/1	
M3C, M4C	60/1	
MON	—	40/2
MOP	—	60/1
R_I / R_O	0.4 / 20	2 / 2
I_B / I_{BO}	20 / —	20 / 80

the IA for test purposes, consisting on a highly linear source follower. The input capacitance of the test buffer, C_{in}, contributes to the overall value of C_{out}. A Montecarlo analysis, with 500 runs and considering process and mismatch variations, revealed a DM voltage gain of (46.5±1.0) V/V. The error existing with respect to the nominal gain, equal to 7.0%, is ascribed to the loading effect implicit in G_{mI} and G_{mO}, given by (8), which deviates the real gain form the expected value of R_O/R_I. Besides, the CM voltage gain was determined to be (−66.2±9.6) dB, which leads to a CMRR of (99.5±9.8) dB. An outstanding characteristic of the proposed single-stage IA is the wide achievable bandwidth, which is due to the single feedback loop existing in the ICF approach. Moreover, it is worth to note that the proposed IA exhibits a very linear response, as the current flowing through the driver transistors in the input and output transconductors does not rely on the level of their input signal. This fact is confirmed by the THD results given below.

Regarding the TS ICF IA, the voltage gain is determined by two external resistors, as depicted in Fig. 5a. Thus, R_I and R_O were selected to be equal in order to optimize matching and, thus, the voltage gain accuracy of the IA. It is worth noting that there is a design trade-off involving the value of the source

Table 4: Different metrics of the TS ICF IA as a function of the source degeneration resistors value.

$R_I = R_O$ (kΩ)	C_C (pF)	BW (kHz)	ΔA_v (%)	$CMRR$ (dB)	V_{iN} (μV_{rms})
0.1	300	143.7	36.8	108.6	9.0
0.2	150	166.2	9.6	105.5	9.3
0.5	60	183.0	4.0	99.0	10.3
1	30	189.3	2.2	94.5	11.5
2	15	192.6	1.2	90.2	14.1
5	6	195.0	0.6	82.8	23.5
10	3	195.7	0.4	76.8	40.5

degeneration resistors, R_I and R_O, and the size of the passive element C_C in the frequency compensation network. Indeed, it is convenient to fix the value of R_I and R_O as low as possible, in order to improve certain parameters, such as the input referred noise. Nevertheless, R_O determines the value of G_{mO} and, hence, of the IA bandwidth, given by eq. (16b). As a consequence, low values of R_O require larger values o f the compensation capacitor, C_C, in order to obtain sufficient phase margin, i.e., $R_O \propto 1/C_C$. In Table 4 different metrics of the TS ICF IA are provided for values of $R_I = R_O$ varying in two decades, from 100 Ω to 10 kΩ. In particular, the value of C_C, BW, voltage gain error, CMRR and input referred voltage noise are included. As, according to (16a), the gain of the IA with an external resistive feedback network is always higher than unity, due to the noninverting feedback configuration adopted, the design criterion to achieve stability was to ensure a phase margin of at least 60° for a voltage gain equal to 2 V/V, i.e., for the case in which $R_1 = R_2$. In view of the results in Table 4, the value $R_I = R_O = 2\ k\Omega$ represents a reasonable choice to minimize silicon area (which depends on the values of R_I, R_O and C_C), voltage gain error and input referred noise, while maximizing the CMRR of the IA.

The simulated performance of the SS and TS ICF IA is summarized in Table 5, while Table 6 provides a comparison of the IAs designed with previous contributions reported in the literature. To this end, the noise efficiency factor (NEF) [8] and the power efficiency factor (PEF) [36] have been used as figures

Table 5: Simulated performance of the designed ICF IAs (Technology: 0.35-μm CMOS, V_{DD} = 3.0 V, $A_{v,nom}$ = 50 V/V).

Parameter	SS ICF IA	TS ICF IA
Voltage gain (V/V)	46.5±1.0	50.6±0.9
Voltage gain error (%)	7.0	1.2
BW (MHz)	7.6	0.1926
Output offset voltage (mV)	1.4±57.6	6.3±146.1
THD 1 mV_{pp} |100 kHz (dB)	−97.9	−92.9
THD 10 mV_{pp} |100 kHz (dB)	−57.4	−72.9
V_{in} THD = −40 dB, 100 kHz (mV_{pp})	16	60
SR^+ / SR^- (V/μs)	9.2 / 9.3	1.1 / 1.1
CMRR DC (dB)	99.5±9.8	90.2±9.9
CMRR BW (dB)	75.0±5.8	88.5±8.3
$PSRR+$ DC (dB)	67.7±10.5	92.2±9.5
$PSRR^+$ BW (dB)	41.7±5.8	88.5±8.3
$PSRR^-$ DC (dB)	79.6±10.0	99.4±9.8
$PSRR^-$ BW (dB)	41.6±4.9	82.5±1.5
$V_{iN,rms}$ [1Hz-BW] (μV_{rms})	32.4	14.1
I_{DD} W/O (with) buffer (μA)	250.6 (1420)	333.1

of merit, which are defined as:

$$NEF = V_{iN,rms}\sqrt{\frac{2I_{supply}}{\pi V_T 4kTBW}} \tag{17}$$

$$PEF = NEF^2 V_{DD} \tag{18}$$

where I_{supply}, V_T, k and T are the total DC current flowing through the different branches of the IA, the thermal voltage, the Boltzmann constant and the temperature, respectively. All results expressed as the mean value plus/minus the standard deviation in Table 5 were obtained from a 500 runs Montecarlo analysis. It is worth to point out that signals coming from the supply will affect in a similar way both branches of the input and output transconductors of the IA. Therefore, both CM signals and supply noise will be largely rejected, thus leading to suitable values for the CMRR and the PSRR. Furthermore, in view of expressions in Table 2 and equations (14a) and (16a), mismatches between resistors R_I and R_O do not lead to a degradation of the CMRR, but just to a negligible deviation of the voltage gain of the IA. The CMRR values provided in

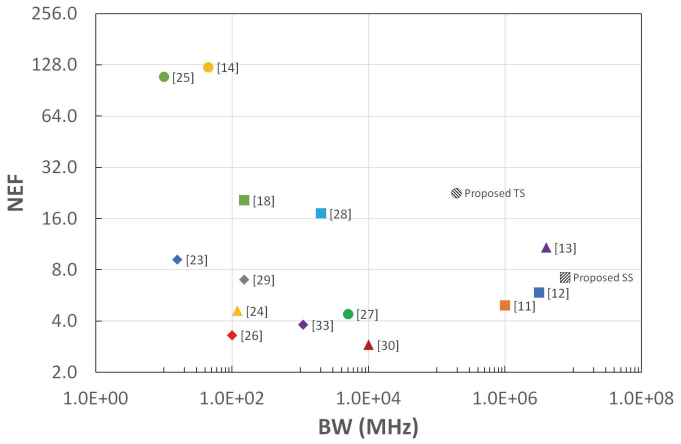


Figure 6: NEF *vs* BW performance of the proposed IAs in comparison with other contributions in the literature.

Table 5 are in accordance with this consideration. Therefore, in the case of the single-stage IA, in which the resistors setting the value of A_v are integrated, this fact may be alleviated by means of appropriate layout techniques, whereas any deviation of R_I with respect to R_O in the two-stage IA may be counteracted by means of the external resistors R_1 and R_2 in Fig. 5a.

In Table 6 instrumentation amplifiers with a wide bandwidth have been selected, in order to compare the proposed solutions with other similar contributions. Besides, a more complete comparison with the state-of-the-art is shown in Fig. 6, where the NEF of different IAs is represented against their bandwidth. As observed, the SS ICF IA presented in this work has the largest bandwidth in the comparative, with a NEF similar to other approaches, especially taking into account that no particular technique has been used to reduce $1/f$ noise. Furthermore, the TS ICF IA presents a higher NEF and a lower BW, which is ascribed to the fact that it has been designed to provide optimized stability at a voltage gain equal to 2 V/V, thus presenting a sensibly narrower bandwidth at the gain selected for its simulated characterization, i.e., 50 V/V. Besides, stable frequency and time responses at a low gain require in this case a higher power dissipation.

7. Conclusion

The overall performance of an ICF IA may be enhanced by improving the particular performance of the input and output V-to-I converters present in the circuit implementation. The SSF is a circuit technique suitable to be used in the design of an improved linearized transconductor. Besides, balancing and isolation features provided by this cell, along with other desirable characteristics, result also appropriate to build a high performance ICF IA in terms of low noise, high linearity and high CMRR. Two instrumentation amplifiers, including SSF voltage followers and operating at a 3-V supply, have been comprehensively analyzed, designed and extensively characterized by simulations. The proposed technique results very suitable to implement a monolithic wide-bandwidth SS ICF IA, as the overall voltage gain relies on on-chip devices and is easily predictable. A TS ICF IA may be also built in a straightforward way, being in this case the voltage gain programmed by means of external resistors.

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Table 6: Performance comparison of the designed ICF IAs with other contributions in the literature.

Parameter	[11] ISCAS'06	[26] JSSC'09	[12] TCAS1'11	[13] (*) IMCSSD'12	[29] TIM'14	[31] TCAS2'16	[17] IJEC'18	This work SS (*)	This work TS (*)
Technology	0.35-μm CMOS	0.35-μm CMOS	0.35-μm CMOS	0.35-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	0.35-μm CMOS	0.35-μm CMOS
Technique	LCF	V-to-I I-to-V	LCF	LCF	Chopping	Chopping	SCS	ICF	ICF
Supply voltage (V)	3	36	3	2	2.7	1.25	1.8	3	3
Supply current (μA)	140	3000	285	240	27.6	1.7	427.8	250.6	333.1
Gain (dB)	20.0	-18 / 42	34	8	40	32	0 / 18	34	34
BW (MHz)	1.0	2.0	2.0	4.0	0.002	0.01	83.0	7.6	0.193
CMRR (dB)	100 @ 1 MHz	120	>90 @ DC	80 @ 1 MHz	120 @ 10 Hz	85	71	99.5 @ DC	90.2 @ DC
PSRR (dB)	N.A	>130	71	N.A.	46	N.A.	N.A.	67.7 / 79.6 @ DC	92.2 / 99.4 @ DC
THD (dB) @ V_{in} (mV_{pp})	N.A.	N.A.	-56.2 @ 10	N.A.	N.A.	N.A.	-44.4 @ 30	-57.4 @ 10	-72.9 @ 10
$V_{iN,rms}$ (μV_{rms})	10.8	283	16	36	3.76	5.7	N.A.	32.4	14.1
NEF	4.9	423.1	5.9	10.8	17.1	2.9	N.A.	7.2	22.6
PEF	73.0	$6.4{\cdot}10^6$	104.4	231.7	784.9	10.3	N.A.	154.7	1534.0

(*) Simulated results

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