High-Linearity Tunable Low-G_m Transconductor based on Bootstrapping

O. J. Cinco-Izquierdo, C. A. de la Cruz-Blas *Member, IEEE,* and M. T. Sanz-Pascual, *Member, IEEE,*

***Abstract*—In this brief, a novel pseudo-differential low-transconductance amplifier is proposed based on the bootstrapping technique. The transconductor is implemented using two voltage follower topologies as amplifiers with their outputs connected to both terminals of a resistor, thus bootstrapping the voltages at these terminals to increase the equivalent resistance value, and achieve a very low transconductance without the need for large passive components. In this way, a highly-linear compact structure is designed whose transconductance can be tuned by external current sources. The circuit was fabricated in a standard $0.18\mu m$ CMOS process. The experimental results show a tunable transconductance in the range of tens of nA/V, with a total harmonic distortion lower than $-40dB$ at $350mVpp@1kHz$. The power consumption of the amplifier is $4\mu W$ under a $1.8V$ supply voltage.**

***Index Terms*—Analog CMOS, Bootstrapping, Low G_m OTA**

I. Introduction

LOW frequency filters are key building blocks in biosignal detection systems, earthquake prediction systems, structure health monitoring and stabilization control circuits, where the frequencies of interest typically range from DC to a few tens of kHz [1-3]. In order to achieve such low cut-off frequencies, large capacitors and/or large resistors are required, which are impractical in fully integrated solutions. For this reason, other approaches to achieve large time-constants have been proposed in the literature, such as the use of capacitance multipliers or pseudo-resistors [4-5]. However, these techniques suffer from large area and high non-linearity, respectively, limiting their application. A popular approach to achieve low frequencies without sacrificing area or linearity is to use G_m-C filters based on very low G_m OTAs [6-7].

There are several techniques to design low G_m transconductors. In the triode region, for example, it is possible to exploit the benefits of the smaller g_m/I_D ratio, obtaining small transconductances without increasing the power consumption; however, the linearity is degraded [8]. Another way to reduce transconductance is to use the bulk-driven approach, as the bulk transconductance g_{mb} is typically 0.2 to 0.4 times g_m, however, the input impedance depends in this case on the input signal value [9,10]. Current attenuation, consists in reducing the output current of the OTA by using current mirrors with large division factors. These current mirrors are sometimes based on series-parallel transistor structures to achieve a small copy factor, increasing the area of the circuit [11]. Another current attenuation technique is the so called current-steering approach, which provides programmability and current reduction using voltage-controlled current mirrors implemented via unbalanced differential pairs [12]. The main disadvantage of this technique is the control voltage range, which limits the transconductance range, and that some times the current of one of the branches is waisted. The current cancellation technique, in turn, reduces the equivalent G_m of the OTA by splitting each input transistor in the differential pair into two parallel transistors, one of them carrying N times the current through the other. When cross-coupling the drains of these split input transistors, the transconductance is reduced by a factor $(N-1)/(N+1)$. This configuration is sensitive to mismatch, so N cannot be arbitrarily close to 1 and therefore the reduction in G_m is limited [13]. Another alternative is the use of a capacitive network at the input of the OTA to reduce its transconductance [14]. The main disadvantages of this technique are the DC offset and the increased area due to the capacitors. Although the input voltage attenuator can also be implemented with an active cell to reduce the required area, this implies an increase in the noise contribution of the OTA. Finally, many authors use a combination of two or more of these techniques to further reduce G_m, without avoiding the trade-offs of each of them [9,13].

In this paper, a novel pseudo-differential low G_m OTA is proposed to overcome the above mentioned restrictions. It shows high linearity, high input impedance, low power consumption, low G_m even in the presence of mismatch and moderate area consumption. The proposed topology is based on bootstrapping, which is achieved through the use of two amplifiers, namely source followers, connected to the terminals of a resistor to increase its equivalent value, and a current mirror to provide the output current. Although bootstrapping is widely used to increase the input impedance of some circuits, and has been also reported to increase the output resistance of amplifiers [15,16], to the best of our knowledge it has not been applied in the way here proposed.

The paper is organized as follows: Section II presents the proposed transconductance reduction technique. The proposed low-G_m transconductor and its experimental results are provided in Section III. Second order effects are analyzed in Section IV and, finally, conclusions are drawn in Section V.

II. Proposed Gm Reduction Technique

The bootstrapping technique is often used to increase the input resistance of amplifiers or to act as a constant current

O. J. Cinco-Izquierdo, M. T. Sanz-Pascual are in Electronic Department, Instituto Nacional de Astrofísica, Óptica y Electrónica (INAOE), Tonantzintla, Puebla 72840 México (e-mail: {oscar.cinco, materesa}@inaoep.mx)

C. A. de la Cruz-Blas is with the Department of Electrical, Electronic, and Communication Engineering, Public University of Navarre (UPNA), Pamplona, Navarra 31006 España (e-mail: carlos.aristoteles@unavarra.es)

to bias output stages [17]. The technique is applied using a resistor R connected between the input and output of a gain amplifier A, as shown in Figure 1a. Assuming the input impedance of A is infinite, the current through R is given by $V_{in} = (1 - A)/R$. Therefore, the equivalent input resistance of the circuit is $R_{eq} = R/(1-A)$, and can be very high if the gain of the amplifier is close to 1, i.e., if similar voltages are forced at both terminals of the resistor. The same operation principle is used in the proposed technique, shown in Figure 1b, using in this case two voltages amplifiers to set similar voltage levels at both terminals of R. The current through R is now given by $V_{in}(A_1 - A_2)/R$, and is copied to the output with a current controlled current source. If A_1 and A_2 are similar, only a small current flows through R, and therefore a low G_m transconductance is achieved, which is given by $G_m = (A_1 - A_2)/R$.

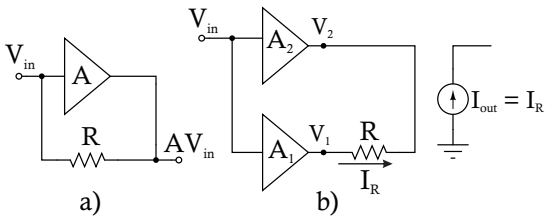

Fig. 1. a) Bootstrapping technique, b)Proposed resistance boosting technique.

If both amplifiers are designed with similar gains, a very low transconductance can be achieved. The technique can be implemented using two source followers, namely M_{SF1} and M_{SF2} in Figure 2. M_{SF1} also acts as a common-gate, routing the current through R to the output. In this way, low transconductance is achieved, which can be adjusted by means of the bias currents I_{B1} and I_{B2}. Current I_B is required to subtract the DC component of the transconductor namely $I_B = I_{B1} + I_{IRDC}$; this last current is the DC component that flows through I_R when $V_{in} = 0$. A PMOS configuration was chosen to avoid body-effect by tying bulk and source together.

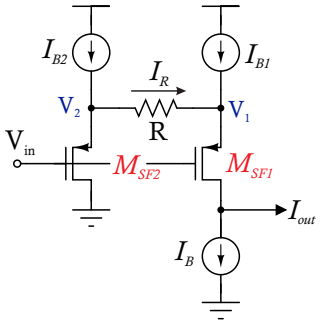

Fig. 2. Implementation of the Proposed Resistance Boosting Technique.

A. DC Analysis

As transistors are biased in weak inversion, the voltages at nodes V_1 and V_2 are given by:

$$V_{1,2} = V_{in} - nV_t \cdot \ln\left[\frac{I_{SF1,2}}{I_S}\right] \tag{1}$$

where $I_{SF1} = I_{B1} + I_R$, $I_{SF2} = I_{B2} - I_R$, V_t is the thermal voltage, n is the slope factor and I_S is the characteristic current. If $I_R << I_{B1}, I_{B2}$, as will be the case, a truncated Taylor expansion can be used to find the approximate value of I_R:

$$I_R \approx \frac{-nV_t I_{B1} I_{B2}}{RI_{B1}I_{B2} + nV_t(I_{B1} + I_{B2})} \cdot \ln\left[\frac{I_{B1}}{I_{B2}}\right] \tag{2}$$

From this equation, it is observed that a DC current is established through R if the bias currents I_{B1} and I_{B2} are not equal. Furthermore, ideal current sources have been considered in this analysis and, as a result, the gain of both source followers is forced to be A_1=A_2=1, so the transconductance of the proposed circuit is $G_m = 0$, as expected.

B. Small Signal Analysis

Let r_{B1} and r_{B2} be the output resistances of the current sources I_{B1} and I_{B2}, respectively. If $r_{B1}r_{B2}R >> r_{B1}, r_{B2}$, R, it can be shown that the small signal current i_R which flows through R_S is given by:

$$i_R = \frac{(g_{m1}r_{B1} - g_{m2}r_{B2}) \cdot v_{in}}{R(g_{m1}r_{B1} + g_{m2}r_{B2}) + r_{B1}r_{B2}(g_{m1} + g_{m2} + g_{m1}g_{m2}R)} \tag{3}$$

where g_{m1} is the transconductance of M_{SF1} and g_{m2} is the transconductance of M_{SF2}. Assuming $g_{m1}r_{B1} >> 1$ and $g_{m2}r_{B2} >> 1$, equation (3) can be approximated by:

$$G_m = \frac{\Delta(g_m \cdot r_B)}{g_{m1}g_{m2}r_{B1}r_{B2}R} \tag{4}$$

where $\Delta(g_m r_B)$ represents the difference between $g_{m1}r_{B1}$ and $g_{m2}r_{B2}$. If both branches are designed to be identical, with the same bias current I_{B1}=I_{B2}, the ideal transconductance is $G_m = 0$, since A_1=A_2, as expected. In practice, however, the actual transconductance under these conditions would be determined by mismatch, and it would not be possible to predict its polarity, resulting in potentially unstable systems if using the OTA in closed loop configurations. For this reason, it is not advised to use the same bias current in both branches. Nevertheless, even if $I_{B1} \neq I_{B2}$, $g_{m1}r_{B1}$ and $g_{m2}r_{B2}$ can still be similar, and the high-value resistance in the denominator in equation (4) still ensures a low equivalent transconductance. Finally, note that, as will be shown in Section IV.A, the output resistance r_{B1} of the bias current I_{B1} sets a minimum transconductance limit.

III. Proposed Low-Gm Transconductor

The proposed pseudo-differential low-G_m OTA, shown in Figure 3, consists of two G_m-reduction blocks with PMOS input transistors M_1 to M_4 acting as source followers. Bias current sources are implemented with single transistors M_{11} to M_{14}, whose currents are set through I_{B1} and I_{B2}. The output current of each block is copied to the output branch through simple current mirrors so that the DC component is ideally cancelled out. In order to validate the proposed technique, these current mirrors have no gain, though an attenuation factor could be added to further reduce G_m. The equivalent transconductance of the OTA is twice the G_m shown in

equation (4), where r_{B1} is the output resistance of M_{13}-M_{14}, r_{B2} the output resistance of M_{11}-M_{12} and g_{mSF1} and g_{mSF2} the transconductance of M_1-M_2 and M_3-M_4, respectively.

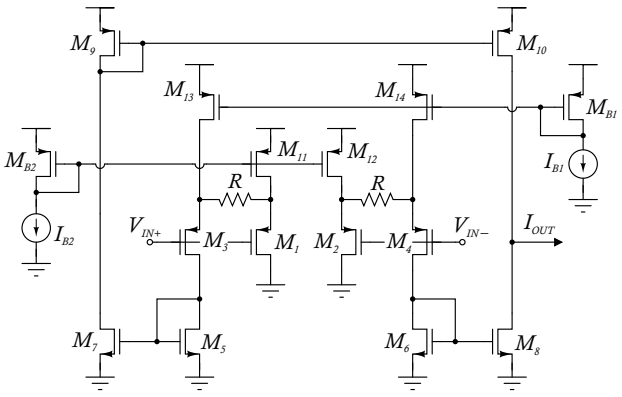

Fig. 3. Proposed Low-Gm Transconductor.

The transconductor was fabricated in a $0.18\mu m$ standard CMOS process with $1.8V$ supply voltage. The chip microphotograph and layout are shown in Figure 4. The area of the circuit is $110\mu m$x$90\mu m$, which includes the high resistivity polysilicon degeneration resistors R, designed to be $100k\Omega$ each. In order to achieve good matching, interdigitation was used in the layout and transistor lengths were set to $0.36\mu m$. For experimental characterization the bias current I_{B2} was set to $1\mu A$, whereas I_{B1} was varied from 20.5 to $72nA$. Each current was generated via an external potentiometer and a two channel signal generator was used to apply the differential input voltage. A transimpedance amplifier, implemented with the general purpose amplifier TL081 and a feedback resistor $R_F = 2.2M\Omega$, was connected to the output of the transconductor in order to convert the output current into an output voltage. The transconductance was measured by applying a $100Hz$ triangle wave to the input from 0 to V_{DD} and obtaining the derivative of output voltage with respect to the input voltage, $G_m = (1/R_F)(dV_{out}/dV_{id})$, with a digital oscilloscope. The OTA exhibits a power consumption of $4\mu W$, and provides a variable G_m from $15nA/V$ to $18.5nA/V$, as shown in Figure 5. Therefore, it can be used to design low-frequency G_m-C filters, as the equivalent $15nA/V$ transconductance would allow reaching cutoff frequencies as low as $238Hz$ with a $10pF$ load capacitor, or $48Hz$ with a $50pF$ capacitor. Note that special techniques can be used to reduce the area of the required capacitors, such as capacitance multipliers [4] or the use of MOS capacitors [22]. To achieve these transconductance levels in a classical source degeneration topology a resistor R in the order of $60M\Omega$ should be used. Thus, the proposed technique provides an approximate resistor multiplication factor of 100, which results in a reduction of two orders of magnitude in both the area and noise power contribution of the resistor. The bandwidth of the OTA remains almost constant and equal to $15kHz$. Figure 6a shows the total harmonic distortion (THD) for a sine differential input voltage at $1kHz$ and with amplitude varying from $50mVpp$ to $350mVpp$. The characterization was carried out at each G_m setting and it shows that, in all cases, the THD remains below $-40dB$ for input voltages up to $350mVpp$.

Table I shows a comparison with previous low-G_m OTAs found in the literature. The highest linearity is achieved in [20] and [23], at a cost of high voltage supply and high power consumption, in the first case, and, though not mentioned in the paper, at a cost of variable input impedance due to the rail-to-rail input operation in a bulk-driven configuration [10], in the second case. In contrast, the proposed transconductor shows high linearity with moderate power consumption, low noise contribution and low area consumption. In particular, THD is 1% for a $350mVpp$ sine input signal at $1kHz$, and decreases down to 0.15% for a $100mVpp$ input. This THD would be even lower if simple current mirrors in the topology were replaced by cascode configurations, as will be shown in Section IV. It must also be noted that large bias currents were used during the characterization process due to experimental limitations. Even so, the power consumption is reduced when compared to OTAs based on current attenuation, such as [20] and [22], since there is no current waste. Furthermore, simulations show that the power consumption of the proposed topology can be decreased down to the order of hundreds of nW.

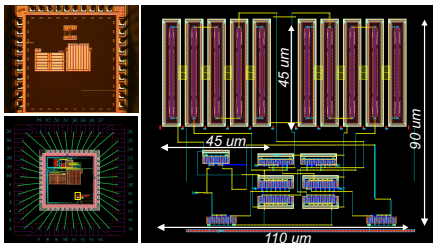

Fig. 4. Microphotograph and Layout of the Low-Gm Transconductor.

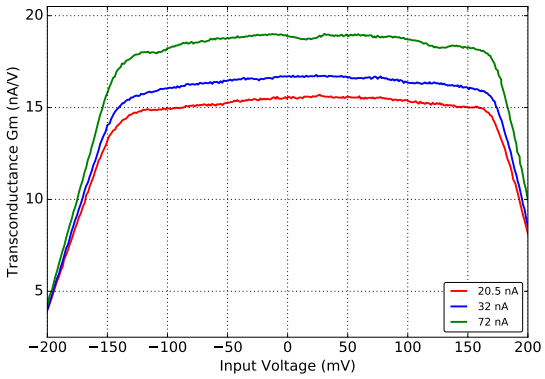

Fig. 5. Measurement results of transconductance as a function of the differential input voltage, for several I_{B1}.

IV. Second Order Effects

In order to gain more in-depth understanding of the proposed OTA operation, some simulations are provided that show the impact of the chosen current mirrors and mismatch on the characteristics.

TABLE I
PERFORMANCE COMPARISON WITH OTHER LOW-G_m TRANSCONDUCTORS

Parameter	[8]'08*	[18]'12	[19]'14	[20]'14	[21]'19	[22]'19	[23]'20	**This Work**
$Process(\mu m)$	0.35	0.35	0.13	0.35	0.18	0.18	0.18	0.18
$Supply(V)$	1.5	0.8	0.25	$\pm$2.5	0.3	1.8	1	1.8
$Technique$	Triode Region	Bulk Driven	Bulk Driven	Current Attenuation	Bulk Driven	Current Attenuation	Bulk Driven	Boots-trapping
$Gm(nA/V)$	1 - 12	66	22	39.5 - 367	68 - 460	0.5 - 5000	0.62 - 6.28	15 - 18.5
$BW(Hz)$	14.6	195	-	-	50 - 334	5.2 k	100	15 k
THD	1 % @200 mVpp -	1 % @100 mVpp 10 Hz	0.53 % @100 mVpp -	0.13 % @ 2 Vpp $1kHz$	0.47 % @100 mVpp $100Hz$	1 % @220 mVpp $5Hz$	0.18 % @2 Vpp -	1 % @ 350 mVpp $1kHz$
Input Referred Noise PSD $(\mu V/\sqrt{Hz})$	74 @10 Hz	-	-	-	1.3 ** @10 Hz	-	-	70.3 @100 Hz
Input Referred Noise V_{rms} (μV_{rms})	-	80 (0.2 - 200) Hz	100 (0.1 - 200) Hz	332 (10 - 30k) Hz	-	16.3 (0.06 - 5) Hz	760 (1 - 100) Hz	475 (1 - 1k) Hz
$Power(\mu W)$	<0.3	0.04	0.01	160	0.05	5.4	0.27	4
$Area(mm^2)$	-	0.04	0.0053	0.006	0.035	0.014	0.027	0.0099

*Simulation results. ** Thermal Noise level, the corner frequency for $1/f$ noise was around $4Hz$ (stated in ref [21])

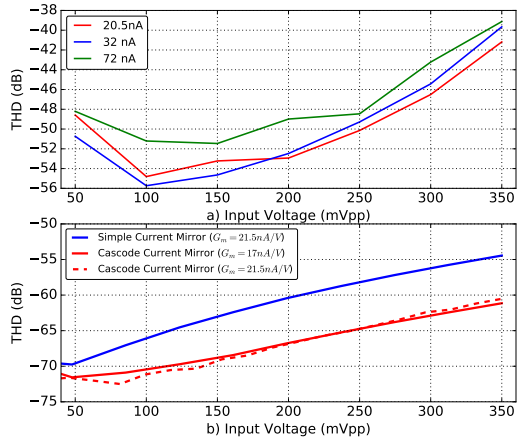

Fig. 6. a) Measurement results of THD versus input voltage for several I_{B1} values. b) Simulation results of THD with different current mirrors.

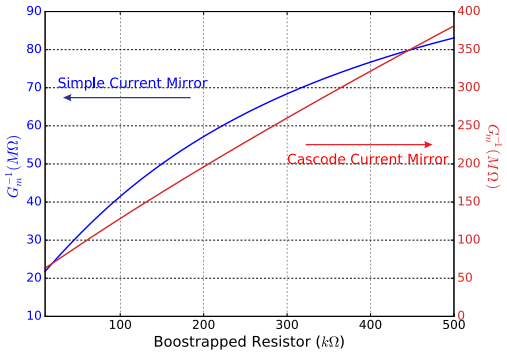

Fig. 7. Equivalent resistance G_m^{-1} using simple and cascode current mirrors.

A. Impact of r_{B1}

The OTA shown in Figure 3 is the simplest implementation derived from the proposed resistance boosting technique, and was integrated to prove the effectiveness of this approach. However, in an extreme case, when the signal current flowing through R is much lower than the current through the output resistor r_{B1} of the bias current source (M_{13}, M_{14}), r_{B1} actually sets a minimum transconductance limit. To show the effect of this limitation, simulations were carried out to see the dependence of G_m^{-1} on the value of R, both with simple current sources and when replacing M_{13} and M_{14} by cascode configurations. As shown in Figure 7, the value of G_m^{-1} when using simple current sources tends to saturate as R increases, due to the limit established by r_{B1}. As for the case with cascode current sources, with an output resistance about 20 times higher, the value of G_m was decreased (as predicted by equation (4)) and no saturation of G_m^{-1} is observed in the considered range of R.

B. Current Mirror Effects

From the DC analysis in Section II it was shown that the proposed resistance boosting technique can provide very high linearity, as the output current is independent of the input voltage in a first order approximation. In practice, the linearity of the integrated OTA will be limited by the distortion introduced by the output current mirrors, M_5-M_{10}. To prove this, simulations wee carried out where these current mirrors were substituted by cascode current mirrors, which not only provide higher output resistance and accuracy in the copy, but also higher linearity. By doing so, the transconductance of the OTA with $I_{B1} = 72nA$ was decreased from $21nA/V$ to $16.5nA/V$, due to a more accurate current copy to the output. Figure 6b shows the THD in both cases, for sine input voltages ranging from $40mVpp$ to $350mVpp$ at $1kHz$. In order to compare the THD also at the same output levels, I_{B1} was increased to $100nA$ in the cascode current mirror implementation to obtain the same $Gm = 21nA/V$ than in the simple case. As shown, the harmonic distortion in mainly determined by the current mirrors, and an improvement in their linearity highly impacts on the THD of the whole topology. In particular, the use of cascode current mirrors reduced the THD of the OTA around 0.05%.

C. Mismatch Effects

In order to determine the impact of mismatch on G_m and THD, Monte Carlo simulations (1000 runs each) of the proposed OTA with $I_{B1} = 70nA$ and $I_{B2} = 1\mu A$ were carried out. Figure 8a shows the impact of mismatch on G_m, at three different input voltage amplitudes ($-100mV, 0mV$ and $100mV$). The red line in the box plot indicates the mean value of the transconductance, which is $21.5nA$ in all three cases and a standard deviation of $1.5nA/V$. As shown, the distribution is symmetric. The boxes cover the interquartile range of the distribution, i.e., 50% of the measurement lie in the range, from $19.7nA/V$ to $22nA/V$. Figure 8b shows the THD histogram, for an input voltage of $350mVpp$ at $1kHz$, which has a mean value of 0.15% and 0.06% standard deviation.

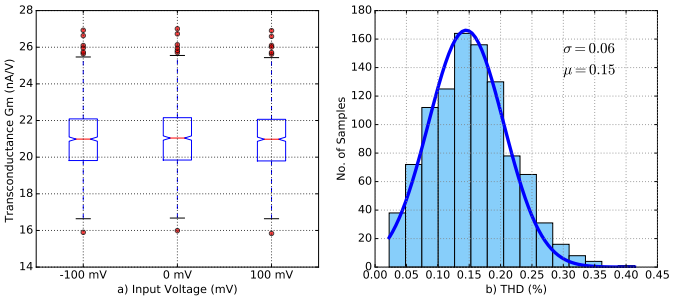

Fig. 8. a) Transconductance Box Plot and b) THD Histogram from Monte Carlo Analysis.

V. Conclusion

A low transconductance amplifier with tuning capability and high linearity has been presented in this paper. The proposed topology uses a bootstrapping technique to increase the equivalent impedance of high resistivity polysilicon resistors. Although other implementations are possible, in this particular case source followers are used to force similar voltages at the terminals of each resistor in the pseudo-differential configuration, and current mirrors generate the output current. The proposed circuit was fabricated in a $0.18\mu m$ CMOS process with $1.8V$ supply. Experimental results show a transconductance range from $15nA/V$ to $18.5nA/V$ with THD below 1% for differential input signals $350mVpp$ at $1kHz$. The use of cascode current mirrors can further reduce transconductance and increase linearity. As a conclusion, the proposed OTA achieves low transconductance with a good trade-off between linearity, noise and power consumption. In a practical case, a tuning circuit can be used to ensure that the required value of G_m is established even under process and temperature variations.

Acknowledgment

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