Wide-Swing Class AB Regulated Cascode Current Mirror

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***Abstract*—A micropower regulated cascode CMOS current mirror is presented, combining floating gate and quasi floating gate MOS transistors to achieve both wide swing and class AB operation, respectively. Measurement results for a 0.5 µm CMOS test chip prototype are included, showing that the current mirror can provide a THD at 100 kHz of -44 dB for a supply voltage of ±0.75 V and input current amplitudes 20 times larger than the bias current.**

Keywords—Current Mirror, Regulated Cascode, Floating Gate Transistor, Quasi-Floating Gate Transistor, Analog integrated circuits, CMOS integrated circuits, Class AB circuits.

I. INTRODUCTION

High-performance current mirrors are critical building blocks in modern analog integrated circuits. They are required in multiple applications such as amplifiers, current conveyors, voltage to current converters, filters, etc. Current mirrors usually require minimum input impedance, maximum output impedance, low quiescent power dissipation, high linearity, accurate current copy and wide current and voltage swings. Nowadays reduction in the MOS transistor intrinsic gain often leads to the need of cascode current mirrors with enhanced output impedance. A popular approach is the regulated cascode current mirror (RCCM) [1], a possible implementation is shown in Fig. 1(a). Transistors M_{P4} and M_{N4} enhance output resistance by a factor $g_{mP4,N4}(r_{oP4,N4}||r_B)$, with g_{mi} and r_{oi} the transconductance and output resistance of transistor M_i and r_B the resistance of current source I_B. Transistor M_{P7} decreases input resistance by a factor $g_{mP7}(r_{oP7}||r_B)$ and sets the input voltage to $V_B+V_{SG,P7}$, an approximately constant voltage due to the constant current through M_{P7}. Transistors M_{N3} and M_{P3} improve matching and hence current copy accuracy. Input and output resistances are approximately:

$$R_{in} \approx [g_{mN1}g_{mP7}(r_{oP7}||r_B)]^{-1} \quad (1)$$

$$R_{out} \approx g_{mN6}g_{mN4}r_{oN2}(r_{oN4}||r_B)r_{oN6} \,||\, g_{mP6}g_{mP4}r_{oP2}(r_{oP4}||r_B)r_{oP6} \quad (2)$$

A drawback of the circuit of Fig. 1(a) is that it operates in class A, limiting the maximum current swing to I_B. To reduce static power dissipation without restricting current swing, class AB operation is required. This can be efficiently implemented using quasi-floating gate (QFG) techniques as shown in Fig. 1(b) [2]. Capacitor C_{bat} and pseudo resistor M_{PR} do not affect static operation and allow transfer of AC voltages from the gate of $M_{N1,2}$ to the gate of $M_{P1,2}$, leading to maximum currents not limited by I_B. However, despite the improved current swing, minimum supply voltage and output voltage swing are still limited as in Fig. 1(a). The reason is that the drain-source voltages of $M_{N1,2}$ and $M_{P1,2}$ are still set by the gate-source voltages of $M_{N3,4}$ and $M_{P3,4}$ and are therefore larger than the minimum required value $V_{DS,sat}=V_{GS}-V_{TH}$ to operate in saturation (unless $|V_{GS}| > 2|V_{TH}|$ is chosen for $M_{N1,2}$ and $M_{P1,2}$ [1]). Hence the circuit requires larger supply voltage than the conventional wide-swing cascode current mirror [2]. Various approaches have been proposed to solve this limitation, e.g. the implementation presented in [3], but they inevitably require additional branches that increase static power consumption and add extra poles and zeros.

In this paper, an alternative class AB regulated cascode current mirror is proposed. It employs floating gate (FG) MOS transistors to improve voltage swing and reduce the minimum supply voltage required, without including extra branches or increasing static power consumption. The paper is organized as follows. Section II summarizes the basic operation of multiple-input FGMOS devices. Section III deals with the detailed description of the proposed class AB regulated cascode current mirror. Influence of second-order effects is analyzed in Section IV. Measurement results from a test chip prototype fabricated in a 0.5 µm CMOS 2-poly process are discussed in Section V. Finally, some conclusions are drawn in Section VI.

II. FGMOS TRANSISTORS

Fig. 2 shows the layout, equivalent circuit and symbol of a two-input *n*-type FGMOS device. Note that the two inputs are coupled to the floating gate by capacitors C_1 and C_2. These capacitors are usually implemented by a second polysilicon layer overlapping the polysilicon gate, as shown in Fig. 2(a). The voltage at the floating gate V_{FG} can be easily calculated since the gate is floating in DC and hence the total charge remains constant:

$$V_{FG} = \frac{1}{C_T}\left(\sum_{k=1}^{2} C_k V_k + C_{GS}V_S + C_{GD}V_D + C_{GB}V_B + Q_0\right) \quad (3)$$

where $C_T = C_1+C_2+C_{GS}+C_{GD}+C_{GB}$ is the total capacitance connected to the gate, which includes the main intrinsic capacitances. Note that the floating gate voltage is a weighted averaging of the two input voltages plus some other terms. The term Q_0 corresponds to the residual charge trapped in the floating gate due to the photolitographic fabrication process. In our design Q_0 is avoided since the floating gate terminal was connected to all the metal layers available in the CMOS process employed. This way, the gate is discharged during deposition of each metal layer and becomes finally floating after etching of the last metal layer [4].

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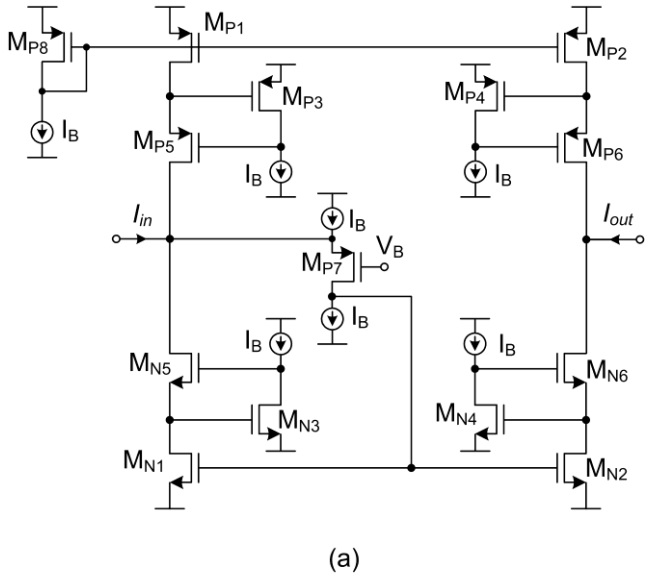

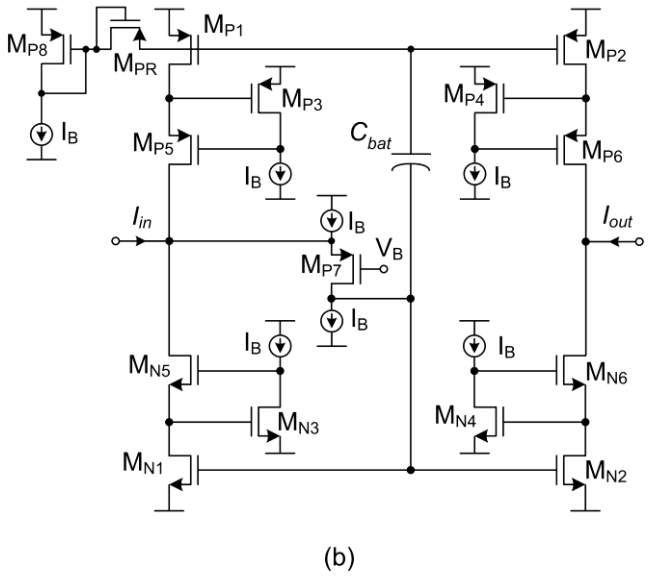

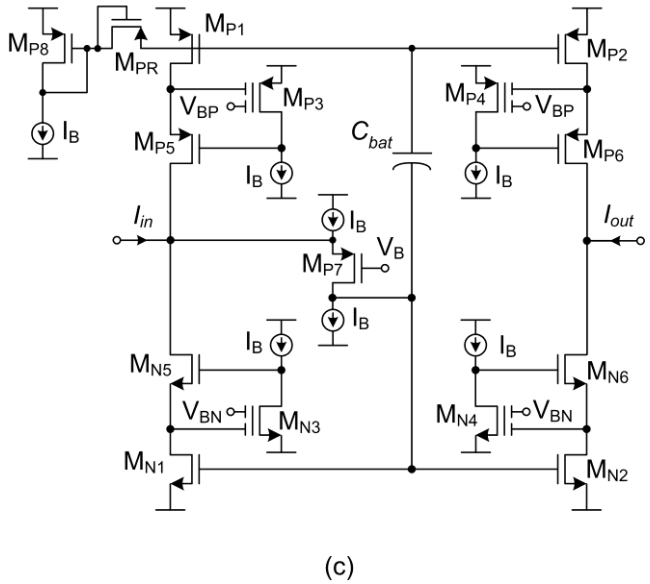

Fig. 1. Regulated cascode current mirrors (a) Conventional class A RCCM (b) Class AB RCCM. (c) Proposed class AB FGMOS RCCM.

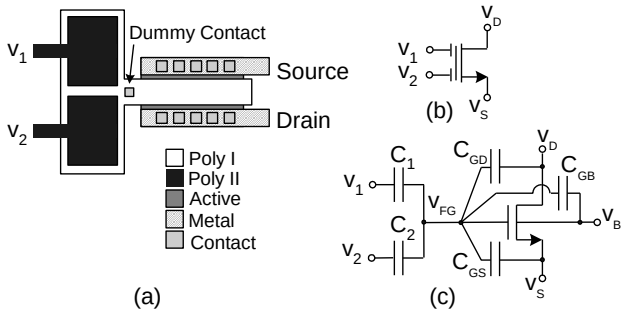

Fig. 2. Two-input Floating-gate MOS transistor (a) Device layout (b) Symbol (c) Equivalent circuit

III. Circuit Description

Replacing in Fig. 1(b) $M_{N3,4}$ and $M_{P3,4}$ by two-input FGMOS transistors, the proposed circuit of Fig. 1(c) results, where the V_{DS} of $M_{N1,2}$ and $M_{P1,2}$ can be controlled by C_1, C_2, V_{BN} and V_{BP}. From (3) and choosing C_1 and C_2 large enough so that parasitic terms can be neglected, the drain voltages of $M_{N1,2}$ and $M_{P1,2}$ become:

$$V_{D,N1,2}=(V_{SS}+V_{GS,N3,4})(1+C_1/C_2)-V_{BN}(C_1/C_2) \quad (4)$$

$$V_{D,P1,2}=(V_{DD}-|V_{GS,P3,4}|)(1+C_1/C_2)-V_{BP}(C_1/C_2) \quad (5)$$

Therefore, the V_{DS} voltages of $M_{N1,2}$ and $M_{P1,2}$ can be set to their minimum value to operate in saturation ($V_{DS,sat}$) by properly choosing V_{BP}, V_{BN} and C_1/C_2. This way the output voltage swing increases by $V_{THn}+|V_{THp}|$ (around 1.6 V in the CMOS process employed in this work). If C_1/C_2 is chosen adequately, V_{BN} and V_{BP} can be set to V_{DD} and V_{SS}, respectively, simplifying biasing.

The price paid for the proposed approach is the extra area required for capacitors C_1 and C_2, and that transconductance of $M_{N3,4}$ and $M_{P3,4}$ is reduced by a factor C_2/C_T due to the FGMOS input capacitive divider, which leads to a reduction of R_{out} by the same factor compared to the conventional regulated cascode current mirror. Noise contribution of $M_{N3,4}$ and $M_{P3,4}$ is also slightly increased due to their reduced transconductance, but its effect in noise performance is negligible as noise contribution of $M_{N1,2}$ and $M_{P1,2}$ is strongly dominant.

IV. Second-Order Effects

Process, supply voltage and temperature (PVT) variations have little effect on the current copy of transistors M_{N1}-M_{N2} and M_{P1}-M_{P2} since this copy does not rely on absolute parameter values of these transistors but on their matching. However PVT variations may influence the loop gain of the regulated cascode transistors as well as the input and output voltage range. Hence, proper design must take into account these variations, particularly choosing conservative values of C_1/C_2, V_{BP} and V_{BN} that preserve operation in saturation of M_{N1}-M_{N2} and M_{P1}-M_{P2} despite such PVT variations. If bias currents I_B are made insensitive to PVT variations, then the quiescent currents of the current mirror remain unaltered since they are set by current mirrors. PVT variations on C_{bat} and M_{PR} are not important, they can only slightly modify the cutoff frequency (which is typically around 1 Hz) of the first order

high-pass filter formed by these two devices and hence the minimum signal frequency transferred from the gate of M_{N1}-M_{N2} to the gate of M_{P1}-M_{P2}.

Regarding geometric and parametric mismatch, high matching accuracy is required between transistors M_{N1}-M_{N2} and M_{P1}-M_{P2} to preserve high linearity, so adequate layout techniques should be employed. Threshold voltage mismatch is the most critical one, degrading linearity as it is commonly found in other output stages [5]. In our case, large devices areas, interdigitation and dummy devices were used to improve matching. Mismatch in the FGMOS transistors has less influence on accuracy as they act just as auxiliary amplifiers. This mismatch leads to slightly different drain voltages in M_{N1}-M_{N2} and in M_{P1}-M_{P2}.

Channel-length modulation effects in the current copy accuracy are avoided due to the use of a cascode topology. Concerning body effect, its impact is negligible as it only affects cascode transistors M_{N5}-M_{N6} and M_{P5}-M_{P6} and pseudo-resistor M_{PR}. The rest of transistors have their source terminal tied to a supply rail (or to the *n*-well for M_{P7}).

V. Measurement Results

The three current mirrors of Fig. 1 were included on a test chip prototype fabricated in a 0.5 µm two-poly three-metal N-well CMOS process with nominal *n*MOS and *p*MOS threshold voltages of 0.67 V and –0.96 V, respectively. The transistor aspect ratios employed are listed in Table I. Poly-poly capacitors were used to implement C_1, C_2 and C_{bat}. The value of C_{bat} is 850 fF, while C_1 = 500 fF and C_2 = 1 pF for $M_{N3,4}$ and $C_1 = C_2$ = 500 fF for $M_{P3,4}$. A microphotograph of the proposed current mirror of Fig. 1(c) is shown in Fig. 3.

The three current mirrors were tested with a supply voltage of ±0.75 V and a bias current I_B = 10 µA. Voltage V_B was set to -0.6 V. The measurement setup employed is shown in Fig. 4. The input voltage was generated by an Agilent 33522A arbitrary waveform generator. A Howland current made with a CA3140E opamp was used for voltage to current conversion (V/I block). The output current was converted to voltage by a transresistance amplifier using another CA3140E opamp, and then a Hewlett Packard 89410A Vector Signal Analyzer was employed for distortion analysis.

Figure 5 shows the measured Total Harmonic Distortion for a sinusoidal input current of 10 kHz and 100 kHz and varying input amplitude. Note that the current mirror of Fig. 1(a) is only able to operate with input amplitudes lower than I_B due to its class A operation. Larger input currents lead to prohibitive distortion levels. The class AB current mirror of Fig. 1(b) can operate with larger input currents, but linearity is modest since the supply voltage employed is not enough for proper operation of the regulated cascode structure. Transistors in Fig. 1(b) implementing current sources I_B in $M_{N3,4}$ and $M_{P3,4}$ enter triode region, strongly decreasing gain of the regulated cascode loop. Note the improvement obtained by the proposed current mirror of Fig. 1(c), which achieves a THD at 10 kHz of -45 dB for an input current 20 times larger than the bias current, 8 dB lower than the circuit of Fig. 1(b). This improvement is even higher when a simple load resistor is used, since the improved output voltage swing of the proposed circuit is then more evidenced. When the transresistance amplifier is used for output I-V conversion the output is a signal ground with constant voltage.

TABLE I - TRANSISTOR ASPECT RATIOS

Transistor	W/L (µm/µm)
M_{N1}, M_{N2},	100/1
M_{N3}, M_{N4}	100/0.6
M_{N5}, M_{N6}	100/0.6
M_{P1}, M_{P2}	100/0.6
M_{P3}, M_{P4},	100/0.6
M_{P5}, M_{P6}	200/0.6
M_{P7}	100/1
M_{P8}	100/0.6
M_{P8}	100/0.6
M_{PR}	1.5/0.6

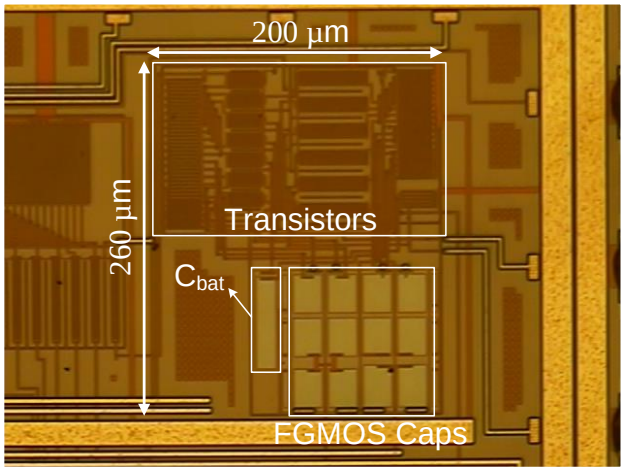

Fig. 3. Microphotograph of the circuit.

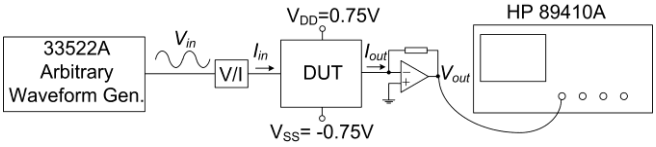

Fig. 4. Measurement setup.

The silicon area of the proposed current mirror (test pads not included) is approximately 0.042 mm^2 (a 31 % increase vs Fig. 1(b)) and the static power consumption is 120 µW, the same as the other current mirrors in Fig. 1.

Table II summarizes the main performance parameters of the current mirrors of Fig. 1 and other class AB current mirrors formerly published. Note that results in [2] correspond to the circuit of Fig. 1(b) but using a supply voltage of 3.3 V. It can be seen that R_{out} in Figs. 1(a) and 1(b) is not very large since the supply voltage employed is not enough for these circuits, as mentioned above. The decrease in input resistance of Fig. 1(b) and 1(c) versus Fig. 1(a) is due to the additional transconductance provided by M_{P1} at the input stage thanks to the QFG technique. Note from Table II that the proposed circuit of Fig. 1(c) allows preserving the excellent performance of a regulated cascode topology with reduced supply voltage.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

PARAMETER	Fig. 1(a)	Fig. 1(b)	Fig. 1(c)	[2]	[6]	[7]	[8]
Technology	0.5µm CMOS	0.5µm CMOS	0.5µm CMOS	0.5µm CMOS	0.5µm CMOS	0.5µm CMOS	0.18 µm CMOS
Supply Volt. (V)	±0.75	±0.75	±0.75	±1.65	1	±1.65	1.8
R_{in} (Ω) (*)	35	21	21	16	5010	20	89
R_{out} (MΩ) (*)	3	3	177	651	3.6	12	2.4
BW (MHz) (*)	56	63	66	98	140	97	2.6
THD	-3 dB @100 kHz, 0.4 mA_{pp}	-38 dB @100 kHz, 0.4 mA_{pp}	-44 dB @100 kHz, 0.4 mA_{pp}	-57dB @100 kHz, 0.4 mA_{pp}	-42dB @100 kHz, 0.1 mA_{pp}	-58 dB @100 kHz, 0.4 mA_{pp}	-53 dB @10 kHz, 0.06 mA_{pp}
Eq. input noise @1MHz (pA/√Hz)(*)	4.70	4.76	4.82	4.41	--	4.34	--
Static power (µW)	120	120	120	264	--	165	48
Fabricated? (Y/N)	Y	Y	Y	Y	N	Y	Y
Area (mm^2)	0.030	0.032	0.042	0.032	--	0.011	0.006

(*) Simulation

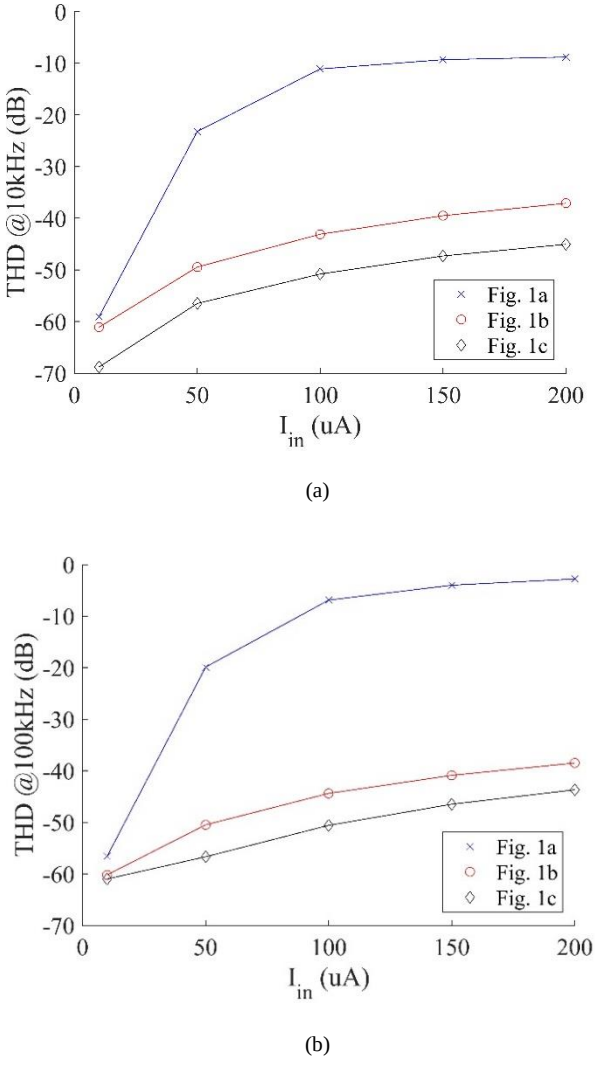

Fig. 5. Measured THD vs input current amplitude
(a) 10 kHz input (b) 100 kHz input

VI. CONCLUSION

It has been experimentally verified that floating gate techniques can be efficiently employed to increase voltage swing and reduce supply voltage requirements of class AB regulated cascode current mirrors. As can be noticed from Table II, the proposed current mirror in Fig. 1(c) allows maintaining a wide current swing (much larger than the bias currents) and at the same time reducing the required supply voltage significantly. Applications may include current followers for low-voltage amplifiers and transconductors, and in general current-mode circuits requiring large output resistance.

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