A Highly Efficient Composite Class-AB–AB Miller Op-Amp With High Gain and Stable From 15 pF Up To Very Large Capacitive Loads

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***Abstract*— In this paper, a highly power-efficient class-AB–AB Miller op-amp is discussed. The structure uses g_m enhancement based on local common-mode feedback to provide class-AB operation with enhanced effective g_m, open-loop gain, unity-gain frequency, and slew rate (SR) without significant increase in quiescent power consumption. Utilization of a nonlinear load leads to large symmetric positive and negative SRs. Stability over an extremely wide range of capacitive loads is achieved through a combination of Miller and phase-lead compensations. The unity-gain frequency does not show sensitivity to capacitive load values. A test chip prototype fabricated in 0.18-μm CMOS technology shows 90.8-dB open-loop gain, 12.5-MHz bandwidth for a 25-pF load capacitance, and a factor 60 SR enhancement with maximum output current close to 1-mA and 43-μA total static current.**

***Index Terms*— C_L-independent pole–zero cancelation, class-AB op-amps, g_m boosting, nonlinear load, phase-lead compensation.**

I. Introduction

TWO-STAGE (Miller) op-amps can drive resistive loads and have close to rail-to-rail output swing. One-stage op-amps (OTAs) are not well suited for resistive loads since their open-loop gain (A_{OL}) depends on the output resistance (R_{out}). Besides, in order to achieve high R_{out} they require cascode transistors in the output branches. This reduces output swing, which is of special concern in modern IC technology operating from reduced supply voltages. The main advantage of one-stage amplifiers is that their phase margin (PM) increases with increasing load capacitance C_L and they also have symmetrical positive and negative slew rate (SR). On the other hand, Miller compensated op-amps with internal dominant pole decrease their PM as C_L grows and are stable over a relatively narrow range of C_L values only. In addition, they have highly non-symmetrical SR. In a conventional class-A two-stage Miller op-amp (Fig. 1) with nMOS (pMOS) input stage, negative SR^- (SR^+) is in general limited to an approximate value $SR^- = I_{Qout}/(C_L + C_c) = 2I_{bias}/(C_L + C_c)$, where C_c is the Miller compensation capacitor and I_{bias} and I_{Qout} are the bias current of the unit transistors and the output branch, respectively. Increasing I_{Qout} can increase SR at the expense of higher static power consumption.

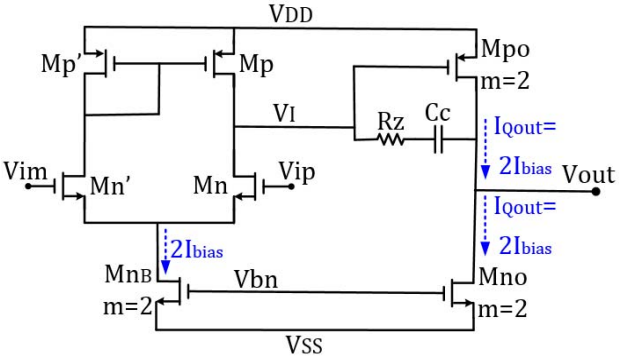

Fig. 1. Conventional two-stage class-A Miller op-amp.

Class-AB op-amps [1]–[21] can deliver maximum output currents which are higher than I_{Qout} without increasing essentially the static power consumption. They can be compared using $CE = I_{outMAX}/I_{totbias}$, where CE is the current efficiency and $I_{totbias}$ is the total op-amp quiescent current. In most class-AB Miller op-amps, the gain bandwidth (GB) product is determined by the transconductance gain g_{mDP} of the differential input stage according to the well-known expression $GB = g_{mDP}/(2\pi C_c)$. In order to increase GB for a given C_c it is required to increase the quiescent current. This results again in increased power consumption. Given that to increase the speed of an op-amp it is required to increase simultaneously SR and bandwidth (BW) at similar rates, a global FOM (FOM_G) can be defined as $FOM_G = (FOM_L FOM_S)^{1/2}$. Terms $FOM_L = I_{outMAX}/P_{diss}$ and $FOM_S = (GBC_L)/P_{diss}$ [22] are the commonly used large and small-signal FOMs, respectively, where P_{diss} is the total power dissipation.

A simple technique with adaptive load is used in [1] to achieve class-AB operation; however, a high CE is not

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achieved ($CE \sim 1.58$). This is because the maximum output current depends on the maximum source-gate voltage of the output pMOS transistor which cannot go close to lower rail V_{SS}. In addition, $GB = g_{mDP}/(\pi C_c)$ has only a factor of two increase compared to the GB of the conventional Miller op-amp. These reduce both FOM_L and FOM_S. The structure in [2] has the same problem of low CE (SR). This is due to the fact that it uses current starved CMOS inverters as output stages. From the point of view of GB, scheme in [2] performs as a conventional two-stage Miller op-amp without g_m, A_{OLDC}, and GB enhancement. It also does not provide a high PM. The op-amp in [3] has class-AB operation while focusing on lowering the supply voltage using the body-driven (BD) technique [3], [23]–[25]. In BD op-amps, the bulk transconductance (g_{mb}) is usually a factor 4–5 lower than the gate transconductance (g_m). This degrades the GB, dc open-loop gain (A_{OLDC}), and also leads to higher input-referred noise, offset, etc. In addition, for relatively moderate swings a p-n junction in the well of the input transistors can turn ON and increase significantly the input leakage current. The class-AB circuit in [5] has the ability of driving moderately high capacitive loads but its stability is provided by three compensation capacitors and resistors which increase essentially the complexity and area requirements. In addition, CE does not have a high value ($CE = 6.4$) for the same reason as in [1]. Another disadvantage of [1]–[3] and [5] is that they are not capable to drive a very wide range of capacitive loads which is rather important in applications such as peak detectors, microelectromechanical systems (MEMS), liquid-crystal displays (LCDs), and line drivers [20], [21]. The class-AB scheme in [4] is a one-stage operational transconductance amplifier that uses local common mode feedback (LCMFB) to increase the g_m, the BW, SR, and I_{outMAX}. The structure uses a phase-lead compensation resistor at the output to provide the stability over a wide range of C_L loads [26]. However, the pole–zero cancelation provided by phase-lead compensation, only holds over a limited range of C_L loads which results in long settling times [27]. To achieve a high gain, output transistors in [4] are cascoded, though this cannot be used in submicrometer technologies due to the low supplies. On the other hand, cascode output transistors reduce the swing of output, SR, and the I_{outMAX}. The maximum output current is also limited by the phase-lead compensation resistor.

In this paper, a composite class-AB-AB Miller op-amp is presented that has high CE (SR), essentially improved BW and A_{OLDC} (both over factor 10), and the ability to drive a very wide range (over four decades) of capacitive loads starting from relatively low C_L values and maintaining a constant f_{UG}, high PM approximately insensitive settling time to C_L loads. This is achieved by using a combination of Miller and phase-lead compensations with a C_L-independent pole–zero cancelation. The op-amp uses LCMFB to boost the effective g_m, the SR, and the dynamic output current of the first stage. It also uses a nonlinear load to implement a push–pull output stage with large symmetrical dynamic and well-defined low quiescent output currents. The combination of LCMFB and nonlinear load results in a cumulative effect of class-AB (denoted as class-AB-AB) leading to higher FOM_L and FOM_S compared to other recent references. In addition, a detailed and careful design procedure is discussed.

The rest of this paper is organized as follows. Section II describes the proposed class-AB-AB design. Simulation and experimental results of a test chip and a comparison with other recent class-AB structures are discussed in Section III. Conclusions are drawn in Section IV.

II. Fundamentals of the Proposed Circuit

A. Circuit Operation

Fig. 2(a) and (b) shows the architecture and transistor level implementation of the proposed op-amp, respectively. The first stage is a composite stage that consists of a differential pair with resistive LCMFB followed by a shell formed by transistors Mp1, Mp1′, Mn1, and Mn1′.

Assuming $(r_{oMp} \| r_{oMn}) \gg R$, the small-signal differential voltage $(V_X - V_X')$ can be expressed by

$$V_X - V_X' = A_X(V_{ip} - V_{im}) = A_X V_i \approx g_{mDP} R V_i \quad (1)$$

where V_i is the differential input voltage. The output current of the first stage is given by

$$I_{outI} = A_X g_{mp1} V_i = g_{meff} V_i \quad (2)$$

where $g_{meff} = A_x g_{mp1}$ is the effective transconductance of the composite first stage. The gain A_I of the input stage is expressed by

$$A_I = g_{meff} R_{oI} = g_{meff} r_{oMp1} || r_{oMn1} \quad (3)$$

where $R_{oI} = r_{oMp1} || r_{oMn1}$ is the output resistance of the composite first stage. It can be seen that the input stage has an effective transconductance and gain which are boosted by the factor A_X. In addition, due to the linear load R, the maximum voltage variations $(V_X - V_X')_{MAX} \approx 2I_{bias}R$ lead to peak currents in the shell transistors that can be much larger than I_{bias}. Therefore, the first stage shows class-AB operation since it can provide a maximum current $I_{outIMAX} \gg 2I_{bias}$ at node V_I. This, as opposed to a conventional differential input stage with active load that generates a maximum output current of only $2I_{bias}$ at V_I. This can limit the SR in the internal node V_I (and of the op-amp) even if a push–pull output stage is used. The pMOS transistor Mpo of the push–pull output stage is driven by V_I while the nMOS output transistor Mno is driven by V_I' which is in phase with V_I and it is derived from V_X through an inverting amplifier with gain $-A'$. Amplifier A' has a quiescent output voltage V_{IQ}' that generates a quiescent current $I_{Qout} = 2I_{bias}$ in Mno equal to the current of Mpo. This sets a well-defined quiescent current in the output stage (I_{Qout}). Amplifier A' uses a nonlinear load that, as explained below, provides large output impedance and dynamic output current for large input signals at node X while for small input signals the gain and output impedance are low ($|A'| \approx 1$).

The dc open-loop gain of the op-amp is given approximately by $A_{OLDC} = A_I A_{II}$ where $A_{II} = g_{mpo} R_{oII}$ and R_{oII} is the output resistance of the output stage. Assuming pMOS and nMOS unit transistors have the same transconductance

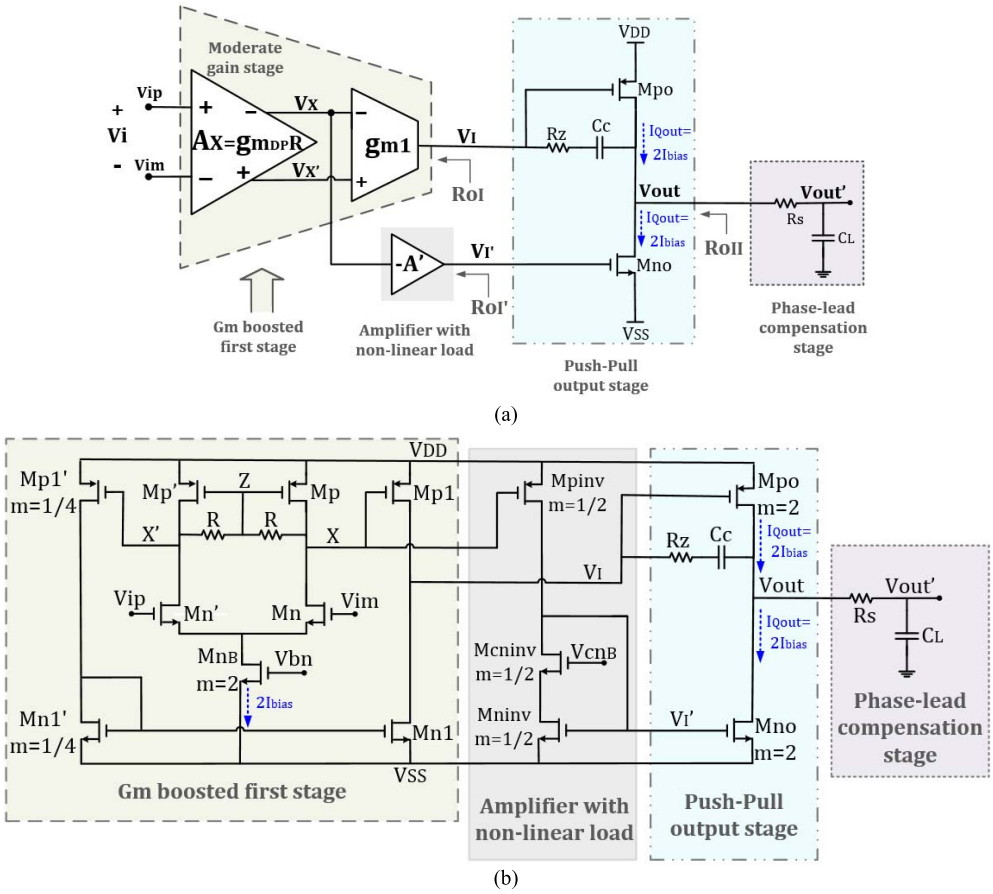

Fig. 2. (a) Architecture of the proposed class-AB–AB op-amp. (b) Transistor level implementation.

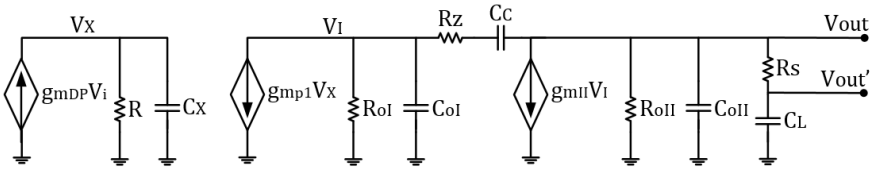

Fig. 3. Simplified small-signal equivalent circuit of the amplifier of Fig. 2.

gain g_m, the open-loop gain can be expressed by the following equation:

$$A_{OLDC} = g_{meff} R_{oI} g_{mII} R_{oII} = g_{mDP} R \left(\frac{g_m r_o}{2}\right)^2. \quad (4)$$

It is a factor A_X higher than the gain of a conventional two-stage op-amp. Note that the gain contribution through A' (and Mno) has been neglected since $|A'| \approx 1$ for small signals. The sizes of transistors Mp1′, and Mn1′ are scaled down by factor 4 in order to save area, and power consumption.

Note that in the proposed class-AB-AB amplifier, the g_m boosted first stage introduces a high frequency pole at nodes X and X'. Therefore, in addition to Miller compensation, a phase-lead compensation resistor R_s connected between the output V_{out} and C_L is required in order to add a left half-plane (LHP) zero to improve the PM [26].

Operation of the Nonlinear Load: The cascode voltage V_{cnB} is selected so that under quiescent conditions, transistor Mninv operates in saturation close to the boundary between triode and saturation. Therefore, at dc transistors Mninv and Mno operate as a current mirror. The quiescent output current in Mno is the same as the quiescent current in Mpo ($I_{Qout} = 2I_{bias}$). For small-signal currents transistor Mninv represents a low impedance load $1/g_m$ for amplifier A' which results in a magnitude of gain $|A'| \approx 1$. For large signal currents in the nonlinear load, Mninv enters triode operation and develops large voltage variations at node V_I'. These lead to negative output currents in Mno which can be much larger than the quiescent current.

B. Small-Signal Analysis

The simplified small-signal equivalent circuit of the amplifier of Fig. 2(b) is shown in Fig. 3. The transfer function is given by the following equation:

$$A(s) = \frac{V_{out}}{V_i} = \frac{A_{OLDC}\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{\left(1+\frac{s}{\omega_{pd}}\right)\left(1+\frac{s}{\omega_{pnd1}}\right)\left(1+\frac{s}{\omega_{pnd2}}\right)} \quad (5)$$

TABLE I

EXPRESSIONS FOR A_{OLDC}, UNITY-GAIN FREQUENCY, AND POLE–ZEROES IN THE PROPOSED CLASS-AB–AB CIRCUIT OF FIG. 2

Pole-Zeroes	General expression	$C_L << g_{mII}R_{oI}C_c$ Dominant C_c	$C_L >> g_{mII}R_{oI}C_c$ Dominant C_L	Changing with C_L??
ω_{pd}	$\frac{1}{(g_{mII}R_{oI}R_{oII}C_c + R_{oII}C_L)}$	$\approx \frac{1}{g_{mII}R_{oI}R_{oII}C_c}$	$\approx \frac{1}{R_{oII}C_L}$	Yes
ω_{pnd1}	$\frac{C_L + g_{mII}R_{oI}C_c}{R_{oI}(1+g_{mII}R_s)C_cC_L}$	$\frac{g_{mII}}{(1+g_{mII}R_s)C_L}$	$\frac{1}{R_{oI}(1+g_{mII}R_s)C_c}$	Yes
ω_{pnd2}	$\frac{1}{(R\|\|R_{oI})C_X} \approx \frac{1}{RC_X}$	$\approx \frac{1}{RC_X}$	$\approx \frac{1}{RC_X}$	**No**
ω_{z1}	$\frac{1}{R_sC_L}$	$\frac{1}{R_sC_L}$	$\frac{1}{R_sC_L}$	Yes
ω_{z2}	$\frac{1}{(R_z - \frac{1}{g_{mII}})C_c}$	$\frac{1}{(R_z - \frac{1}{g_{mII}})C_c}$	$\frac{1}{(R_z - \frac{1}{g_{mII}})C_c}$	**No**
A_{OLDC}	$g_{meff}R_{oI}g_{mII}R_{oII} = g_{mDP}R(\frac{g_mr_o}{2})^2$	$g_{meff}R_{oI}g_{mII}R_{oII} = g_{mDP}R(\frac{g_mr_o}{2})^2$	$g_{meff}R_{oI}g_{mII}R_{oII} = g_{mDP}R(\frac{g_mr_o}{2})^2$	**No**
ω_{UG}	$\frac{g_{meff}g_{mII}R_s}{C_c(1+g_{mII}R_s)}$	$\frac{g_{meff}g_{mII}R_s}{C_c(1+g_{mII}R_s)}$	$\frac{g_{meff}g_{mII}R_s}{C_c(1+g_{mII}R_s)}$	**No**

It has a dominant pole ω_{pd}, two nondominant poles ω_{pnd1}, ω_{pnd2}, and two LHP zeroes ω_{z1}, ω_{z2}. The dc open-loop gain A_{OLDC} is defined in (4).

Table I shows expressions for the poles and zeroes derived by assuming: C_{oI}, C_{oII}, $C_X \ll C_c$, C_L, and $1/R$, $1/R_s$, $1/R_z$, g_{mDP}, g_{mp1}, $g_{mII} \gg 1/R_{oI}$, $1/R_{oII}$, where C_X is the parasitic capacitance at node X. Since the zero ω_{z2}, and nondominant pole ω_{pnd2} are independent of the load C_L, selecting C_c or alternatively R_z based on (6) causes the pole ω_{pnd2} to approximately match the zero ω_{z2}

$$C_c = \frac{RC_X}{\left(R_z - \left(\frac{1}{g_{mII}}\right)\right)} \text{ or alternatively } R_z = \left(\frac{RC_X}{C_c}\right) + \left(\frac{1}{g_{mII}}\right). \tag{6}$$

This means that approximate pole–zero cancelation takes place under all loading conditions and in this case, the transfer function can be further simplified as follows:

$$A(s) \approx \frac{A_{OLDC}\left(1 + \frac{s}{\omega_{z1}}\right)}{\left(1 + \frac{s}{\omega_{pd}}\right)\left(1 + \frac{s}{\omega_{pnd1}}\right)}. \tag{7}$$

Table I also shows simplified expressions for f_{pd}, f_{pnd1}, and f_{z1} for two cases. Case (a) is for $C_L \ll g_{mII}R_{oI}C_c$ which is denoted as dominant C_c, while case (b) is called dominant C_L for $C_L \gg g_{mII}R_{oI}C_c$.

In spite of the fact that the dominant pole $f_{pd} = \omega_{pd}/(2\pi)$ changes with C_L, it is shown next that the open-loop unity-gain frequency (f_{UG}) is not dependent on C_L and for a wide range of C_L values it remains constant.

1) Case (a), Dominant Cc: In this case, f_{z1} is higher than f_{pnd1} [Fig. 4(a)]. Note that f_{z1} and f_{pnd1} change at the same rate, while the dominant pole f_{pd} remains approximately constant with changes in C_L. The response in blue broken lines shows the equivalent one pole response obtained by reducing the open-loop gain by a factor ΔA_{OL} from A_{OLDC} to a value $A_{OLDC}{}'$ where ΔA_{OL} is given by

$$\Delta A_{OL} = \Delta f = \frac{f_{z1}}{f_{pnd1}} \tag{8}$$

$$A_{OLDC}{}' = \frac{A_{OLDC}}{\Delta A_{OL}} = \frac{A_{OLDC}}{\frac{f_{z1}}{f_{pnd1}}}. \tag{9}$$

The equivalent dominant pole of the response in blue broken lines is f_{pd}. This leads to a unity-gain frequency f_{UG} given by

$$f_{UG} = A_{OLDC}{}' f_{pd} = \frac{A_{OLDC}}{\frac{f_{z1}}{f_{pnd1}}} f_{pd} = \frac{A_{OLDC}}{f_{z1}} f_{pd} f_{pnd1}. \tag{10}$$

2) Case (b), Dominant C_L: In this case, f_{z1} is smaller than f_{pnd1} [Fig. 4(b)]. Note that f_{z1} and f_{pd} change at the same rate, while f_{pnd1} remains approximately constant with changes in C_L. The response in blue broken lines shows the equivalent one pole response obtained by increasing the open-loop gain by a factor ΔA_{OL} from A_{OLDC} to a value $A_{OLDC}{}'$ where ΔA_{OL} is given by

$$\Delta A_{OL} = \Delta f = \frac{f_{z1}}{f_{pnd1}} \tag{11}$$

$$A_{OLDC}{}' = \frac{A_{OLDC}}{\Delta A_{OL}} = \frac{A_{OLDC}}{\frac{f_{z1}}{f_{pnd1}}}. \tag{12}$$

The equivalent dominant pole of the response in blue broken lines is again f_{pd} which leads to a unity-gain frequency f_{UG} given by

$$f_{UG} = A_{OLDC}{}' f_{pd} = \frac{A_{OLDC}}{\frac{f_{z1}}{f_{pnd1}}} f_{pd} = \frac{A_{OLDC}}{f_{z1}} f_{pd} f_{pnd1}. \tag{13}$$

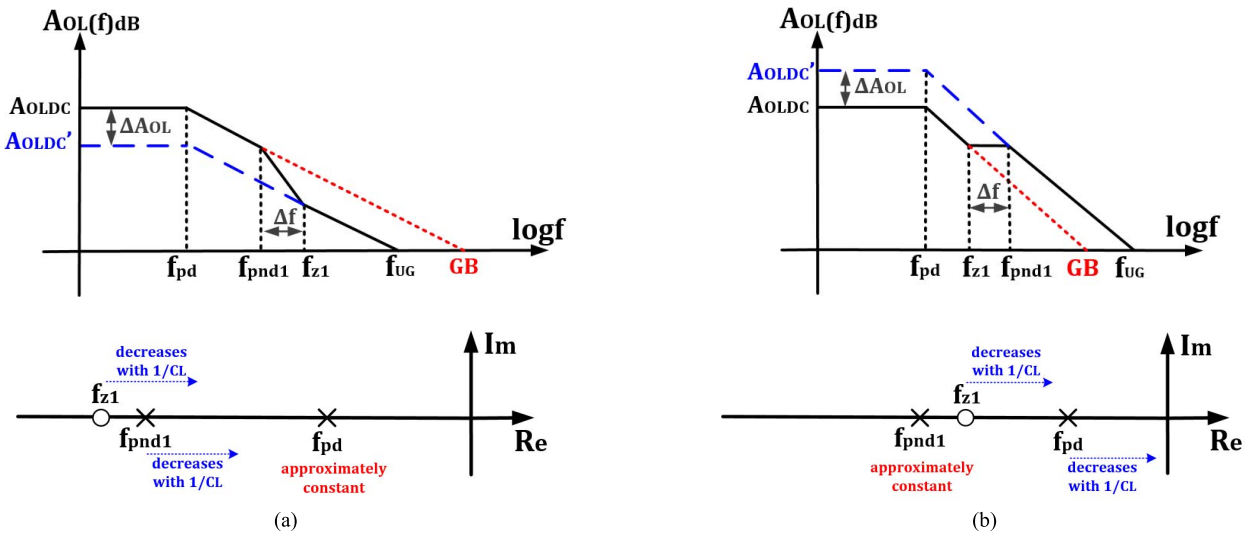

Fig. 4. Open-loop response (top) and pole–zero location (bottom) of the proposed circuit. (a) f_{z1} larger than f_{pnd1}. (b) f_{z1} smaller than f_{pnd1}.

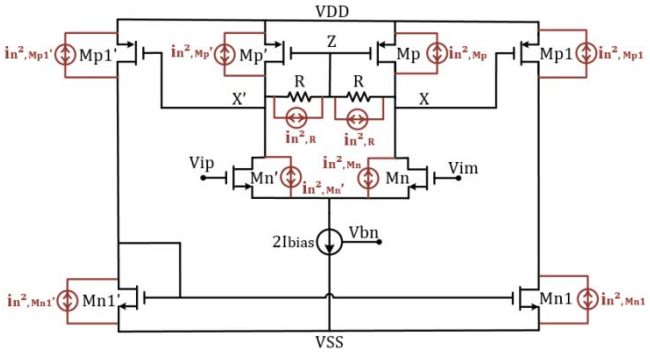

Fig. 5. Simplified model for input-referred noise of the proposed class-AB–AB op-amp of Fig. 2 including dominant noise sources.

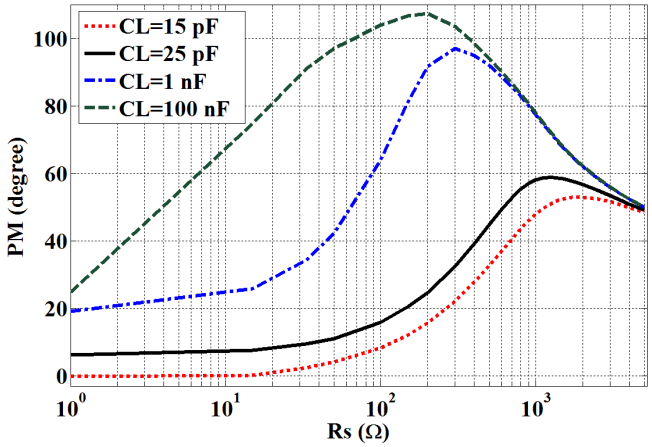

Fig. 6. Simulated PM of the proposed circuit with R_s changing over the range 1 Ω < R_s < 5 kΩ and four different values C_L = 15 pF, 25 pF, 1 nF, and 100 nF.

Using the general expressions for A_{OLDC}, f_{z1}, f_{pd}, and f_{pnd1} from Table I, (10) and (13) are reduced to

$$f_{UG} = \frac{g_{meff}\, g_{mII}\, R_s}{2\pi\, C_c (1 + g_{mII} R_s)}. \tag{14}$$

It can be seen that in spite of the fact that f_{z1}, f_{pnd1}, and f_{pd} are all dependent on C_L, the unity-gain frequency f_{UG} which approximately corresponds to the closed-loop BW at V_{out} remains the same and independent on C_L.

C. Stability

The PM of the proposed circuit can be expressed by

$$PM \approx 90° - \tan^{-1}\left(\frac{f_{UG}}{f_{pnd1}}\right) + \tan^{-1}\left(\frac{f_{UG}}{f_{z1}}\right). \tag{15}$$

Consider the following cases.

1) *Dominant C_L [Fig. 4(b)]:* In this case, stability is enforced since $f_{z1} < f_{pnd1}$ and the phase shift of f_{z1} mostly cancels the phase shift of the dominant pole f_{pd}, the only remaining phase shift at the unity-gain frequency is due to f_{pnd1}. This leads always to a high PM for large C_L values.

TABLE II
PARAMETER VALUES OF THE PROPOSED CIRCUIT [FIG. 2(b)]

Parameter	Value	Parameter	Value
$(W/L)_{NMOS}$ (µm/µm)	20/0.7	C_c (pF)	10
$(W/L)_{PMOS}$ (µm/µm)	100/0.7	C_X (pF)	0.4
g_{mDP} (µA/V)	109	R_z (kΩ)	6
g_{mp1} (µA/V)	137	R_{oI} (kΩ)	435
g_{mpo} (µA/V)	428	g_{mII} (µA/V)*	866
g_{mno} (µA/V)	438	R_{oII} (kΩ)	125
g_{meff} (µA/V)	1724	g_{mpinv} (µA/V)	73.8
R (kΩ)	150	g_{mninv} (µA/V)	74.3

* at low frequencies g_{mII}=g_{mpo} and at high frequencies g_{mII}=g_{mpo}+g_{mno}.

2) *Dominant C_c [Fig. 4(a)]:* In this case, $f_{z1} > f_{pnd1}$, and the ratio $f_{z1}/f_{pnd1} = (1 + g_{mII} R_s)/g_{mII} R_s$ is constant independent of C_L. However, they both shift closer to the unity-gain frequency f_{UG} as C_L decreases

TABLE III

SIMULATED POLE AND ZEROES IN THE PROPOSED CIRCUIT OF FIG. 2(b) FOR THREE DIFFERENT CAPACITIVE LOADS

Pole-Zeroes	Dominant C_c: C_L=25 pF	Neither C_c nor C_L dominant: C_L=1 nF	Dominant C_L: C_L=10 nF	Changing with C_L??
f_{pd}	733 Hz	465 Hz	105 Hz	Yes
f_{pnd1}	1.94 MHz	73.2 kHz	32.4 kHz	Yes
f_{pnd2}	3.62 MHz	3.62 MHz	3.62 MHz	**No**
f_{z1}	7.07 MHz	176.8 kHz	17.7 kHz	Yes
f_{z2}	3.05 MHz	3.05 MHz	3.05 MHz	**No**
f_{UG}	12.05 MHz	12.05 MHz	12.05 MHz	**No**

TABLE IV

SIMULATED SETTLING TIME OF THE PROPOSED OP-AMP OF FIG. 2(b) BY ADDING ±20% MISMATCHES TO THE NOMINAL VALUES OF C_c, R_z, C_X, AND R

Cases: -20%<mismatches<+20%	C_c (pF)	R_z (kΩ)	C_X (pF)	R (kΩ)	Settling time (ns) (0.5%)
a: (nominal values)	10	6	≈0.4	150	156
b:	8	4.8	≈0.48	180	148
c:	12	7.2	≈0.48	120	175
d:	10	4.8	≈0.4	120	155
e:	12	6	≈0.48	180	166
f:	8	7.2	≈0.4	150	149

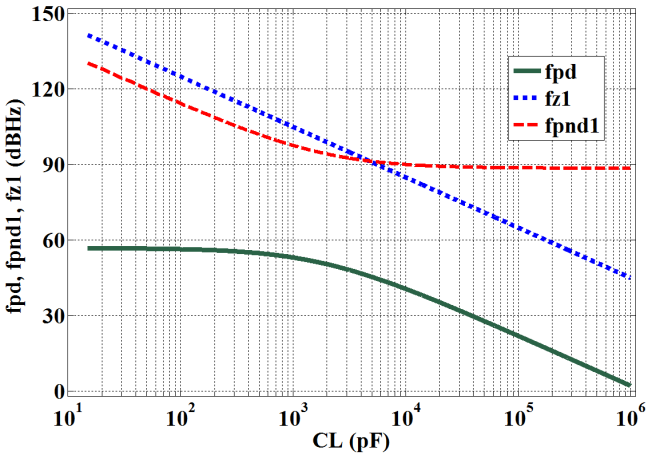

Fig. 7. Locations of dominant pole f_{pd}, nondominant pole f_{pnd1}, and zero f_{z1} for $R_s = 900\ \Omega$ over the C_L range 15 pF < C_L < 1 μF.

which decreases PM and consequently the lowest PM corresponds to C_{Lmin}. For a given value C_{Lmin} it is possible to find a value R_s that satisfies stability with a reasonable PM as it is illustrated with a design example in Section III-A. The phase-lead compensation resistor R_s determines also the maximum output current which has a value $I_{outMAX} = V_{outMAX}/R_s \approx V_{DD}/R_s$ and this limits the maximum value of R_s.

In practice, other high frequency poles neglected in the analysis slightly degrade PM. Note that as opposed to conventional Miller op-amps, the combination of Miller and phase-lead compensation allows to design pseudo two-stage op-amps with high PM over an extremely wide range capacitive loads starting from low C_L values.

D. Slew Rate Analysis

Based on the discussion made in Section II-A, the maximum voltage variation at nodes X, and X' ($\Delta V_{X,MAX}$), the maximum source-gate voltage variations of transistors Mp1 ($\Delta V_{VSGMp1MAX}$) and Mpinv ($\Delta V_{VSGMpinvMAX}$) and also the maximum currents at nodes V_I($I_{outV_I,MAX}$) and $V_I{}'$ ($I_{outV_I',MAX}$) are defined as follows:

$$\begin{aligned}\Delta V_{X,\mathrm{MAX}} &= \Delta V_{VSGMp1MAX} \\ &= \Delta V_{VSGMpinvMAX} = I_{bias}R \qquad (16)\\ I_{outV_I,MAX} &= K_{Mp1}\left(V^{Q}_{SGMp1}-|V_{thP}|+\Delta V_{VSGMp1MAX}\right)^2 \\ &= K_{Mp1}(V_{SDsatMp1}+I_{bias}R)^2 \qquad (17)\\ I_{outV_I',MAX} &= K_{Mpinv}\left(V^{Q}_{SGMpinv}-|V_{thP}|+\Delta V_{VSGMpinvMAX}\right)^2 \\ &= K_{Mp1}(V_{SDsatMpinv}+I_{bias}R)^2 \qquad (18)\end{aligned}$$

where

$$K_p = \frac{\mu_p C_{ox}}{2}\frac{W}{L}. \qquad (19)$$

Further, V_{thP} and μ_p are the nominal value of the threshold voltage and the mobility for pMOS, respectively. Also C_{ox} is the gate capacitance of the MOSFET. Maximum currents at nodes V_I, and V_I'; $I_{outVI,MAX}$, and $I_{outVI',MAX} \gg 2I_{bias}$ lead to large source-gate (gate–source) variations in pMOS and nMOS output transistors ($\Delta V_{I_{MAX}} = \Delta V_{VSGpoMAX} \approx V_{SS}$ and $\Delta V_{I'MAX} = \Delta V_{VGSnoMAX} \approx V_{DD}$).

These large voltage variations at nodes V_I and V_I' result in large values of I^{+}_{outMAX} and I^{-}_{outMAX}. However, the maximum output current $I_{outMAX} = \min(I^{+}_{outMAX}$ and $I^{-}_{outMAX})$ is

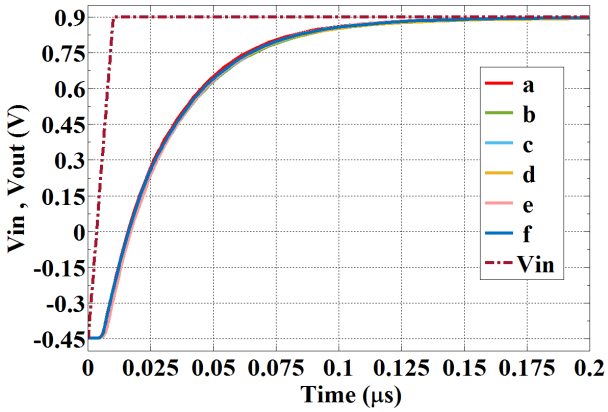

Fig. 8. Simulated settling time of the proposed class-AB–AB op-amp of Fig. 2(b) for all cases of mismatches shown in Table IV. The input signal is a 1.35-$V_{p\text{-}p}$ square waveform, for $C_L = 25$ pF.

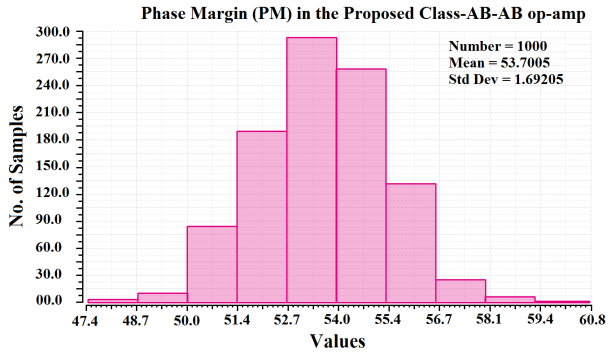

Fig. 9. Checking robustness of PM by performing 1000 Monte Carlo runs including the process and mismatch data ($C_L = 25$ pF).

limited by the phase-lead compensation resistor R_s

$$I_{outMAX} = \frac{V_{outMAX}}{R_s} \approx \frac{V_{DD}}{R_s}. \tag{20}$$

Furthermore, the SR of the proposed class-AB-AB op-amp can be defined in the following equation:

$$SR \approx \frac{I_{outMAX}}{C_c + C_L} = \frac{V_{DD}}{R_s(C_c + C_L)}. \tag{21}$$

E. Noise Analysis

Considering that noise is provided mainly by the composite first stage, the model including noise sources of the proposed op-amp of Fig. 2 is shown in Fig. 5.

Current noise $i^2_{n,Mi}$ in each MOSFET can be modeled by thermal noise ($\overline{i^2_{n,\text{th}}} = 4kT\gamma\, g_{mMi}$) and flicker noise ($\overline{i^2_{n,1/f}} = (K(g_{mMi})^2)/((C_{ox}WLf))$ and in each resistor R can be modeled by thermal noise ($\overline{i^2_{n,R}} = 4kT/R$)

$$\overline{i^2_{n,\text{Mi}}} = \overline{i^2_{n,\text{th}}} + \overline{i^2_{n,\frac{1}{f}}}. \tag{22}$$

Further k, T, γ, and g_{mMi} are Boltzmann's constant ($k = 1.38 \times 10^{-23}$ J/K), the absolute temperature ($T = 300$ K), transconductance gain of transistor, and channel thermal noise coefficient ($\gamma \approx 2/3$), respectively. In addition, K, C_{ox}, W, L, and f are the process-dependent constant ($K = 10^{-25}$ V$^2\cdot$F), oxide capacitance, width of transistor, length of transistor's channel and frequency, respectively.

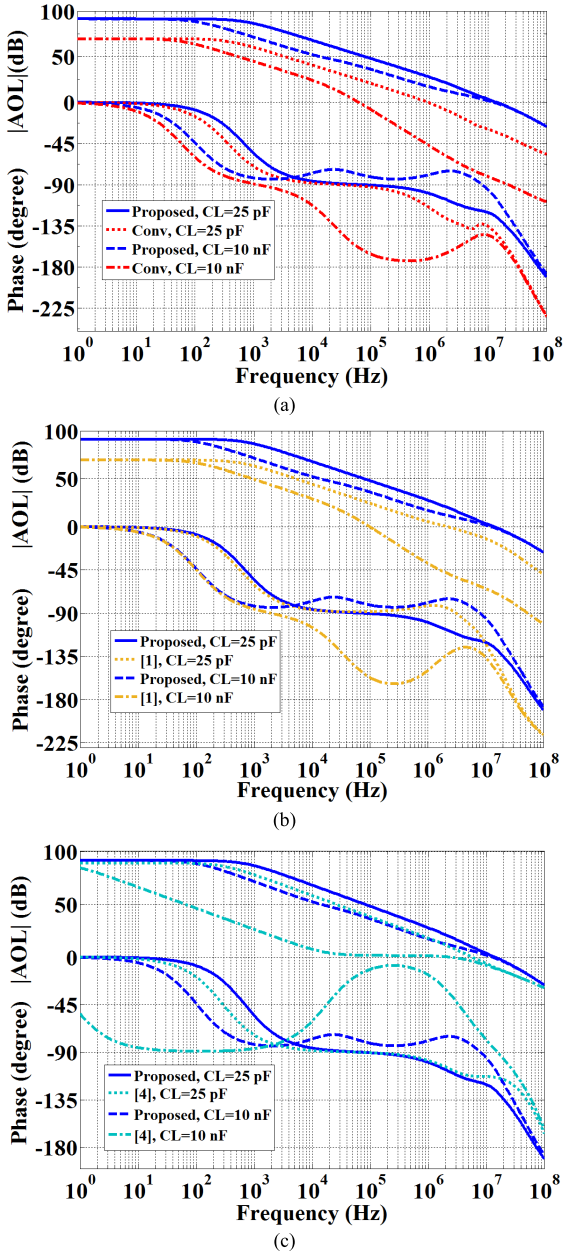

Fig. 10. Simulated open-loop response for two capacitive loads $C_L = 25$ pF and a large-size $C_L = 10$ nF. (a) Response of the proposed and conventional op-amps. (b) Response of the proposed op-amp and scheme in [1]. (c) Response of the proposed op-amp and the circuit in [4].

The equivalent input-referred noise is derived from the following equation:

$$\overline{v^2_{n,\text{in}}} = \frac{1}{(g_{mn,n'})^2}\left[\overline{i^2_{n,Mn}} + \overline{i^2_{n,\text{Mn}'}} + \overline{i^2_{n,\text{Mp}}} + \overline{i^2_{n,\text{Mp}'}} + \overline{i^2_{n,R}} + \overline{i^2_{n,R}} + \frac{1}{(g_{mp1,p1'}R)^2}\left(\overline{i^2_{n,\text{Mn1}}} + \overline{i^2_{n,\text{Mn1}'}} + \overline{i^2_{n,\text{Mp1}}} + \overline{i^2_{n,\text{Mp1}'}}\right)\right]. \tag{23}$$

TABLE V

CORNER SIMULATION RESULTS OF THE PROPOSED CIRCUIT [FIG. 2(b)] ($C_L = 25$ pF, $R_s = 900\ \Omega$, $V_{DD} = 0.9$ V, $V_{SS} = -0.9$ V, AND $I_{bias} = 5\ \mu$ A)

Corner: T=27° C	TT	SS	FF	SF	FS
$I_{totbias}$ (µA)	42.67	40.4	46.06	42.24	43.57
f_{UG} (MHz)	12.05	11.25	13.38	12.19	12.16
I_{outMAX} (µA)	995	955	1088	942	1085
FOM_G ($\sqrt{\mu AMHzpF}/\mu W$)	7.13	7.13	7.28	7.05	7.32
A_{OLDC} (dB)	91.2	91	91.27	91.2	91.1
PM (°)	58.4	58	58.9	58.6	58.5
THD* (%)	0.094	0.123	0.086	0.110	0.090
Corner: T=125° C	**TT**	**SS**	**FF**	**SF**	**FS**
$I_{totbias}$ (µA)	39.84	37.12	43.5	38.6	41.37
f_{UG} (MHz)	10.84	10.30	11.32	10.58	8.87
I_{outMAX}(µA)	933	882	961	877	1004
FOM_G ($\sqrt{\mu AMHzpF}/\mu W$)	7.01	7.13	6.66	6.93	6.34
A_{OLDC} (dB)	90.6	90.4	90.6	90.4	90.6
PM (°)	58.6	57.4	55	59.2	58
THD* (%)	0.106	0.116	0.097	0.111	0.101
Corner: T=-40° C	**TT**	**SS**	**FF**	**SF**	**FS**
$I_{totbias}$ (µA)	48.9	50.43	52.21	52.39	49.1
f_{UG} (MHz)	10.57	10.44	10.28	10.10	10.73
I_{outMAX} (µA)	1036	932	1094	972	1088
FOM_G ($\sqrt{\mu AMHzpF}/\mu W$)	5.94	5.43	5.64	5.25	6.11
A_{OLDC} (dB)	91.3	91	91.4	91.2	91.2
PM (°)	51.7	45.5	51.1	46.2	52.8
THD* (%)	0.121	0.4	0.081	0.278	0.087

* Total harmonic distortion *THD* @ 100 kHz, 1-Vp-p input signal.

Note that in (23) the effect of shell transistors' noise can be neglected since it is reduced by a factor $(g_{mp1,p1'}R)^2$. Considering this and also assuming $g_{mn,n'} = g_{mDP}$, simplifies (23) to (24)

$$\overline{v_{n,in}^2} = \frac{2\left[\overline{i_{n,\mathrm{Mn}}^2} + \overline{i_{n,\mathrm{Mp}}^2} + \overline{i_{n,R}^2}\right]}{(g_{mDP})^2} = 2\left[\frac{4kT\gamma}{g_{mDP}} + \frac{K}{(C_{ox}W_nLf)} + \frac{4kT\gamma\, g_{mp}}{(g_{mDP})^2} + \frac{K(g_{mp})^2}{((C_{ox}W_pLf)(g_{mDP})^2)} + \frac{4kT}{R(g_{mDP})^2}\right]. \quad (24)$$

It can be seen that differential pair transistors (Mn, Mn′) have dominant effect on the equivalent input-referred noise of the proposed op-amp.

III. SIMULATION AND MEASUREMENT RESULTS

A. Simulation Results

The proposed circuit of Fig. 2(b) was designed in a 180-nm CMOS technology and simulated with dual supplies

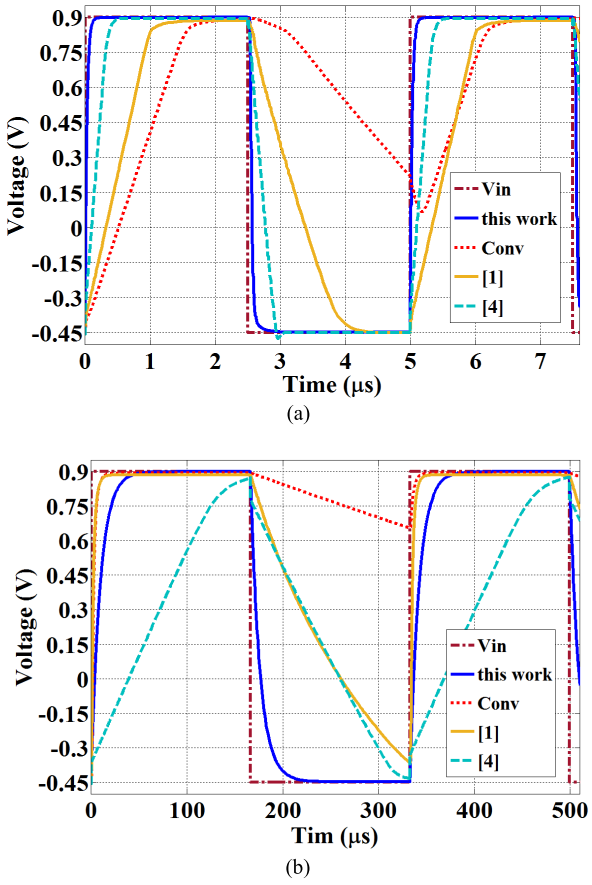

Fig. 11. Simulated transient response of the proposed class-AB–AB op-amp of Fig. 2(b) compared to the conventional Miller op-amp and also amplifiers in [1] and [4]. The input is a 1.35-$V_{p\text{-}p}$ square waveform. (a) For $C_L = 25$ pF. (b) For a large size, $C_L = 10$ nF.

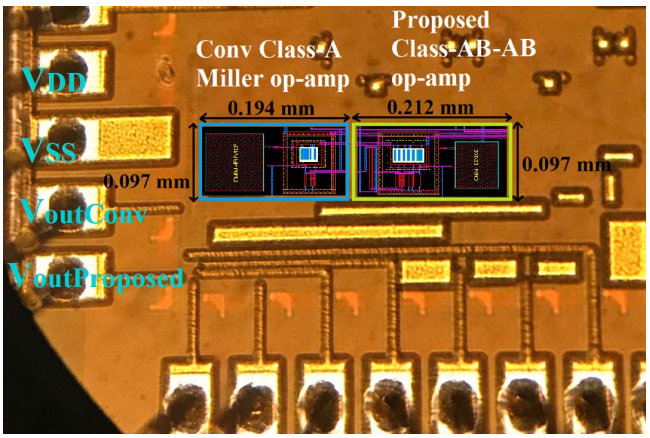

Fig. 12. Micrograph of fabricated chip in 180-nm CMOS technology. It includes the proposed class-ABs–AB Gm-enhanced op-amp [Fig. 2(b)] and a conventional two-stage Miller op-amp (Fig. 1).

$V_{DD} = +0.9$ V and $V_{SS} = -0.9$ V, threshold voltages $V_{thP} \approx V_{thN} \approx 0.45$ V, and $I_{bias} = 5\ \mu$A. Transistors' dimensions, output resistances, and small-signal transconductance gains (R_{oI}, R_{oII}, and g_m) are listed in Table II. The parasitic capacitance at node X (C_X) is calculated from

$$C_X \approx C_{gsMp1} + C_{gsMpinv} + C_{gdMp} + C_{gdMn} + C_{dbMn} + C_{dbMp}. \quad (25)$$

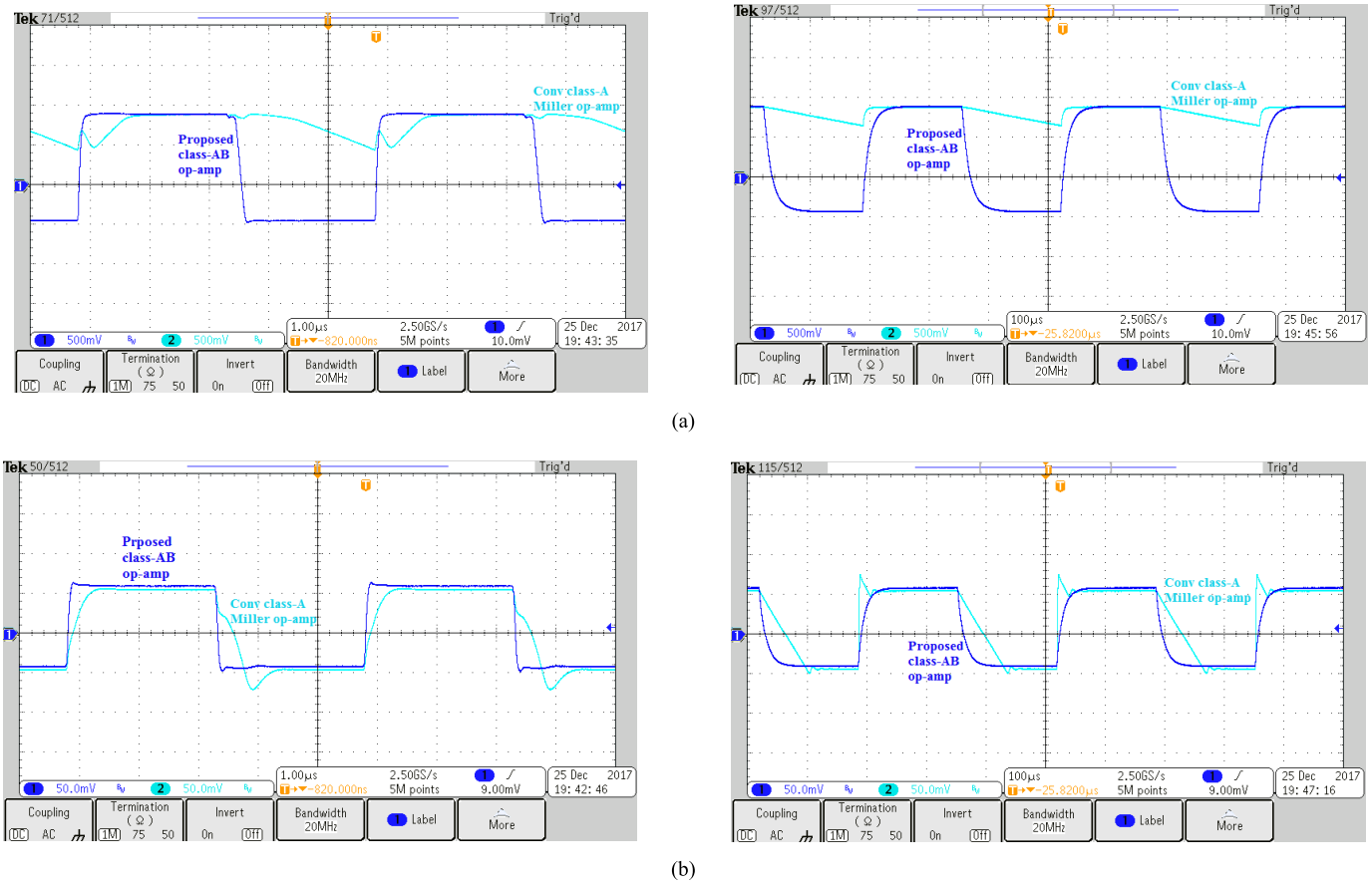

Fig. 13. Experimental transient response of the proposed class-AB–AB and conventional class-A Miller op-amps to two different input square waveforms. (a) 1.35-$V_{p\text{-}p}$ input square waveform, for $C_L = 25$ pF (left) and for $C_L = 10$ nF (right). (b) 0.1-$V_{p\text{-}p}$ input square waveform, for $C_L = 25$ pF (left) and for $C_L = 10$ nF (right).

With $C_{ox} = 8.78$ fF/μm^2 in 0.18-μm CMOS and transistors' dimensions in Table II result in a value $C_X \approx 0.4$ pF. By selecting $C_c = 10$ pF, a value $R_z = 6$ kΩ is obtained from $R_z = (RC_X/C_c) + (1/g_{mII})$ in order to achieve C_L-independent pole–zero cancellation of $f_{pnd2} \approx f_{z2} \sim$ (3–4) MHz (see Section II-B).

The next step is to determine the value of the phase-lead resistance R_s which is critical for stability and also for the maximum output current ($I_{outMAX} = V_{outMAX}/R_s$). Fig. 6 shows the simulated PM in the proposed circuit with R_s changing from 1 Ω to 5 kΩ and C_L parametrized with values $C_L = 15$ pF, 25 pF, 1 nF, and 100 nF. It can be seen in Fig. 6 that as expected, in the range shown for R_s, higher C_L values lead to higher PM. For $R_s \geq 800$ Ω, a $PM > 45°$ results over the entire range of C_L values. In this paper, $R_s = 900$ Ω was selected, which leads to $I_{outMAX} \approx V_{DD}/R_s = 1$ mA and a $PM > 45°$ for $C_L > 15$ pF. For lower maximum output currents I_{outMAX} a higher resistance R_s can be used. This allows utilization of lower C_{Lmin} values.

Fig. 7 shows the dominant pole f_{pd}, nondominant pole f_{pnd1}, and zero f_{z1} for $R_s = 900$ Ω over the range of 15 pF $< C_L <$ 1 μF. It can be seen that the change in their location is in agreement with the discussion in Sections II-B and II-C.

Table III provides the simulated values of poles, zeroes, and f_{UG} for three different capacitive loads: $C_L = 25$ pF ($C_L \ll g_{mII}R_{oI}C_c$: dominant C_c), $C_L = 1$ nF ($C_L \approx g_{mII}R_{oI}C_c$), and $C_L = 10$ nF ($C_L \gg g_{mII}R_{oI}C_c$: dominant C_L). Note that the simulated values of the pole–zeroes closely follow their expressions listed in Table I. As expected, in all simulations with different capacitive loads C_L, the values of f_{z2} and f_{pnd2} remain constant and close to each other; $f_{z2} = 3.05$ MHz and $f_{pnd2} = 3.62$ MHz. This validates the discussion made about C_L-independent pole–zero cancelation in Section II-B.

Pole–zero cancellation can lead to long settling time when there is large mismatch between the pole and zero [27]. In the proposed circuit, the mismatch between C_L-independent f_{z2} and f_{pnd2} is determined by manufacturing tolerances of the order of 20% for each element (i.e., C_c, R, C_X, R_z, ...). This mismatch as well as the location of f_{z2} and f_{pnd2} relative to the location of f_{UG} does not have significant effect on the settling time. This is verified with transient simulations shown in Fig. 8 and Table IV, where $C_L = 25$ pF and f_{z2} and f_{pnd2} are purposely mismatched by adding capacitances connected to nodes X and X', and also manipulating the values of C_c, R_z, and R by $\pm$20%. It can be seen that in all cases (a, b, c, d, e, and f) a negligible effect on transient response is observed. The input signal is a 1.35-$V_{p\text{-}p}$ square waveform. Above discussion applies to a wide range of C_L loads since the values of f_{z2} and f_{pnd2} are not dependent on C_L.

TABLE VI

MEASUREMENT RESULTS OF THE PROPOSED CLASS-AB–AB OP-AMP AND COMPARISON TO OTHER REFERENCES

Parameters	Conv. Miller op-amp	[4] (2002)	[6] (2005)	[2] (2011)	[5] (2012)	[1] (2014)	[7] (2016)	[3] (2016)	[8] (2017)	[9] (2017)	[10] (2017)	This work Fig. 2(b)	
CMOS Process (µm)	0.18	0.5	0.5	0.13	0.5	0.35	0.18	0.18	0.5	0.18	0.18	**0.18**	
Single-Stage	No	Yes	Yes	No	No	No	Yes	No	Yes	Yes	Yes	**No**	
Supply (V)	±0.9	±2.5	±1	1.2	±1.25	±1.65	1.8	0.7	±1	±0.9	±0.9	**±0.9**	
$I_{totbias}$ (µA)	20.78	160	60	91.67	175	420	6611.1	36.28	60	8	40	**43**	
P_{diss} (µW)	37.4	800	120	110	437.5	1380	11900	25.4	120	14.5	72	**80**	
A_{OLDC} (dB)	69	-	43	70	63.4[b]	68	79	57.5	81.7[b]	67	77	**90.8**	
C_L (pF)	25	5	80	>5.5	25	30	200	20	70	23	25	**Small C_L= 25 pF**	**Large C_L= 10 nF**
SR^+ (V/µs)	0.77	11	100	19.5	2.7	22	74.1	1.8	9.8	24.11	43.1	**31**	**0.107**
SR^- (V/µs)	0.31	-	78	-	3.3	24	-	3.8	7.6	23.33	-	**28**	**0.105**
I_{outMAX} (µA)	11	55	-	107.25	1120	660	14820	-	685.2	536.6	1077	**980**	**1045**
CE (µA/µA)	0.53	0.34	104	1.17	6.4	1.58	2.24	-	11.42	67.08	27	**22.8**	**24.3**
GB (MHz)	1.1	20[c]	0.725	35	4.9[b]	21.8	86.5	3	4.75	0.57	2.65	**12.5[c]**	**12.5[c]**
PM (°)	64	-	89.5	>45[a]	83[b]	73	50	60	60[b]	82	86	**58.4[b]**	**78[b]**
FOM_L (µA/µW)	0.29	0.07	59.33	0.98	2.56	0.48	1.25	2.2	4.43	37.3	15	**12.66**	**13.06**
FOM_S (MHz·pF/µW)	0.74	0.13	0.48	1.75	0.28	0.47	1.46	2.36	2.77	0.9	0.92	**3.90[f]**	**2.25[f]**
$\frac{FOM_G}{(\sqrt{\mu AMHzpF/\mu W})}$	0.46	0.1	5.34	1.31	0.85	0.475	1.35	2.28	3.5	5.8	3.71	**7.03**	**5.42**
Offset (mV)	6.18	-	-	-	-	0.2	-	11	6	-	-	**2.48**	
Input Noise (nV/√Hz)	25	-	230	14.14	-	-	0.8	100	35	-	-	**27**	
CMRR (dB)	72	-	68	-	80[b]	75	-	19	78	73.2	-	**68**	
PSRR+ (dB)	76	-	55	-	61.2	78	-	52.1	72	44.1	-	**64**	
PSRR- (dB)	70	-	58	-	-	75	-	66.4	74	41.8	-	**66**	
THD[d] (% or dB)	-42[e]	-	-56	-	-47.1[b]	-54	-	<%1	-41	-48	-	**-50**	
ICMR (V)	1.35	-	-	-	-	2.65	-	0.55	-	1.28	-	**1.35**	
Area (mm^2)	0.019	0.045	0.024	0.012	0.029	0.034	0.070	0.0198	0.024	0.030	0.007	**0.021**	

[a] Assuming closed-loop gain of 2
[b] Simulated
[c] Unity gain frequency f_{UG}
[d] @ 100 kHz, 1-Vp-p input signal
[e] @ 100 kHz, 0.1-Vp-p input signal
[f] The *BW* used for *FOMs* is measured at V_{out}'

On the other hand, robustness of PM (stability) is checked by performing 1000 Monte Carlo runs including the process and mismatch data. The capacitive load in these simulations is considered $C_L = 25$ pF. The result of these simulations is illustrated in Fig. 9.

The simulated open-loop response (magnitude $|A_{OL}|$ and phase) of the proposed (with $R_s = 900\ \Omega$) and conventional op-amps of Figs. 1 and 2(b), respectively, are illustrated in Fig. 10(a) for two extreme values of capacitive loads $C_L = 25$ pF and $C_L = 10$ nF. A low value $C_L = 25$ pF is used for simulations since it corresponds to the parasitic load capacitance in the chip test setup. The conventional class-A Miller op-amp has the same parameters (W/L, R_z, I_{bias}, etc.) as the proposed op-amp with exception of C_c that has a value $C_c = 15$ pF.

It can be seen that in the proposed class-AB-AB op-amp $|A_{OLDC}| = 91.2$ dB, as expected, equal values of unity-gain frequency $f_{UG} \approx 12$ MHz are obtained for both capacitive loads. This validates the discussion in Section II-B. In addition, nominal $C_L = 25$ pF and large $C_L = 10$ nF result in $PM \approx 60°$ and $PM \approx 80°$, respectively, in the proposed circuit. The simulated PMs can be validated using values in Table III and (15). On the other hand, the conventional op-amp has $|A_{OLDC}| = 70$ dB. The phase margin is $PM \approx 66°$ for nominal $C_L = 25$ pF and only $PM \approx 21°$ for large $C_L = 10$ nF. In addition, the simulated open-loop (ac) response of the proposed op-amp and the amplifiers in [1] and [4] are shown and compared in Fig. 10(b) and (c), respectively. Furthermore, the large-signal transient response of the proposed op-amp is simulated and compared in Fig. 11 for two C_L loads; $C_L = 25$ pF [Fig. 11(a)] and $C_L = 10$ nF [Fig. 11(b)]. For transient behavior, the amplifier was measured in voltage follower configuration (node V_{out} connected to the negative input terminal) and the output (V_{out}') was considered after R_s. For a fair comparison, all amplifiers are simulated in 180-nm CMOS technology with the same parameters (W/L, C_c, R_z, R_s, I_{bias}, etc). Fig. 10(b) validates that for any C_L, the proposed class-AB–AB op-amp has higher $|A_{OLDC}|$, f_{UG}, SR, I_{outMAX}, and PM than the scheme in [1] [$f_{UG[1]} = g_{mDP}/(\pi C_c)$].

On the other hand, Fig. 10(c) shows that for different C_L loads, f_{UG} of the proposed op-amp ($f_{UG} = ((g_{meff} g_{mII} R_s)/(2\pi C_c(1 + g_{mII} R_s)))$) remains constant while in [4] $f_{UG[4]} = g_{meff}/(2\pi C_L)$ highly decreases for

$C_L = 10$ nF. Note that in [4], for $C_L = 10$ nF, the zero $f_z = 1/(2\pi R_s C_L)$ moves below the constant nondominant pole $f_{pA} = 1/(2\pi R_A C_A)$ and the C_L dependent pole–zero cancelation is disturbed. This movement increases PM; however, based on discussion made before, the settling time increases. This is demonstrated in Fig. 11(b). The transient results of Fig. 11 show that for any C_L loads, SR (CE) and the settling time of the proposed class-AB–AB op-amp are better than those of the conventional Miller op-amp and the schemes in [1] and [4].

The robustness of the proposed circuit of Fig. 2(b) with $C_L = 25$ pF, $R_s = 900\ \Omega$, $V_{DD} = 0.9$ V, $V_{SS} = -0.9$ V, and $I_{bias} = 5\ \mu$A was simulated over process corners (TT, SS, FF, SF, and FS) and temperature variations ($T = -40$ °C, 27 °C, and 125 °C). The results are summarized in Table V. It can be seen that the performance of the proposed op-amp shows relatively small changes with process and temperature variations.

B. Measurement Results

Fig. 12 shows the micrograph of the test chip including the proposed class-AB–AB op-amp [Fig. 2(b)] and a conventional Miller op-amp (Fig. 1) fabricated in the same 180-nm CMOS technology used for the simulations. Since the opaque passivation hides the active devices, the layouts of op-amps are superimposed in Fig. 12. The dimensions of the conventional and proposed circuits are 194 μm × 97 μm (0.019 mm^2) and 212 × 97 μm (0.021 mm^2), respectively.

In both proposed and conventional op-amps, the same parameters (W/L, R_s, V_{DD}, V_{SS}, I_{bias}, etc.) as in simulations were used for fabrication and testing. The measured transient responses of both op-amps in voltage follower configuration to two different 1.35-$V_{p\text{-}p}$ and 0.1-$V_{p\text{-}p}$ input square waveforms are depicted in Fig. 13. Two extreme values of $C_L = 25$ pF (Fig. 13, left waveforms) and $C_L = 10$ nF (Fig. 13, right waveforms) are used for this purpose. Table VI summarizes the performance parameters of the proposed op-amp [experimental results of Fig. 2(b) for $C_L = 25$ pF and $C_L = 10$ nF] and compares it to other recent class-AB schemes as well as to the conventional Miller op-amp (Fig. 1). Note that in the proposed circuit, the mismatches for each element (i.e., C_L, R_s, R, ...) are determined by manufacturing tolerances of ∼20%. Table VI also includes the input-referred noise density (nV/$\sqrt{\text{Hz}}$) at 1 MHz and also the total harmonic distortion of the output voltage of the two proposed class-AB op-amps in voltage follower configuration for 1-$V_{p\text{-}p}$ input at 100-kHz frequency and for the conventional class-A Miller op-amp for 0.1-$V_{p\text{-}p}$ input at 100-kHz frequency. It is noticeable that Fig. 2(b) circuit has essential performance improvements in most of the parameters especially CE, FOM_L, FOM_S, and FOM_G.

IV. Conclusion

A simple power-efficient pseudo two-stage class-AB-AB Miller op-amp that is stable over a wide range of capacitive loads starting at $C_{Lmin} = 15$ pF is introduced. Stability is enforced using a combination of Miller and phase-lead compensations as well as C_L-independent pole–zero cancelation. This provides stability, a constant f_{UG}, and approximately constant settling time over a wide range of C_L loads. Its class-AB-AB operation is based on combination of g_m boosting technique and a nonlinear load to achieve high output current enhancement factors. The g_m boosting also provides enhanced BW and gain. The proposed scheme of Fig. 2(b) was experimentally verified with a test chip prototype fabricated in 180-nm CMOS technology. The proposed class-AB–AB op-amp showed higher performance in terms of A_{OLDC}, CE, FOM_G (both $FOMs$, and FOM_L), compared to other class-AB schemes reported in the literature.

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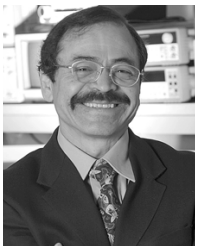

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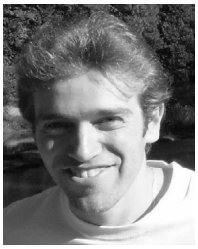

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