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Dual Voltage-Current Control to Provide Grid-Forming Inverters with Current Limiting Capability

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Abstract—The rapid uptake of renewable energy sources is causing synchronous generators (SG) to be replaced by power electronic inverters meaning these inverters need to offer the characteristics traditionally associated with SG. As a result, it has been proposed that the inverters should be controlled in grid-forming mode in order to support the voltage of the microgrids. Given that these inverters are controlled as a voltage source, temporary events such as short-circuits or overloads could cause currents that are far higher than the rated current. As the semiconductors used in power electronics are highly sensitive to overcurrents, this paper proposes a dual voltage-current control that provides the grid-forming inverters with the capability to quickly limit the current under any overload or short-circuit condition. The proposed method has been validated through experimental tests in stand-alone mode.

Index Terms—Grid-forming control, voltage control, current control, short-circuit, overload.

I. INTRODUCTION

The present environmental crisis is driving the increase in demand for renewables and energy storage systems onto the high-power microgrids [1]. The connection of these generation units, made through central inverters, is leading to the total replacement of synchronous generators, giving rise to the more frequent appearance of inverter-based high-power microgrids that can work connected to the main grid, islanded or in both operating modes [2], [3]. However, until now, the synchronous generators have played a key role in maintaining the quality and stability of these systems. This is due to their operation as a voltage source and their overcurrent capability under fault conditions, as well as their active power management, harmonics and unbalance compensation and the provision of inertia to the system, among others [4]. Therefore, in inverter-based microgrids, electronic converters will need to provide these functionalities traditionally provided by synchronous generators.

To this end, new control strategies have been proposed for these electronic converters, coming under the grid-forming concept, such as droop control [5]–[7], the virtual synchronous generator or synchronverter [8]–[10], Power Synchronization Control (PSC) [11]–[13] or Virtual Oscillator Control (VOC) [14], [15]. In all these strategies, the electronic converter acts like a voltage source, either directly or indirectly. As a result, there is a need to develop control strategies that make it possible to quickly limit the current and protect the inverter in events such as overloads or short-circuits.

For this purpose, a widespread strategy consists in the implementation of a cascaded control with an outer voltage loop and an inner current loop, whose current references are saturated at the maximum permissible current value [16], [20], [21]. This technique requires a sufficient separation between the control bandwidths of the voltage and current loops (around one decade [18]) to guarantee an adequate operation. Therefore, in high-power inverters in which the crossover frequency of the current control is limited by the low switching frequencies [19], the bandwidth of the outer voltage loop is strongly restricted [18]-[22]. In turn, the functioning of the cascaded control with low dynamics further constrains the bandwidth of the outer loops related to the grid-forming strategy [22], [23]. Furthermore, the cascaded control results in a greater harmonic distortion of the output voltage, should harmonic current components be demanded of the electronic converter. This is due to the fact that the equivalent output impedance offered at these harmonic components is higher than the actual system impedance for those frequencies that are within the current control bandwidth but are outside the voltage control bandwidth [24]. Resonant controllers have been proposed to resolve this problem, tuned to the typical frequencies at which these harmonics generally appear ($\pm 5f_0$, $\pm 7f_0$ y $\pm 11f_0$ with $f_0 = 50$ or 60 Hz), thereby reducing the output impedance at these frequencies, although increasing it at others [25]. In the presence of voltage flickers or non-linear loads such as cycloconverters, in which the harmonics do not always appear at the same frequency, this results in a highly distorted voltage.

To deal with these issues, the implementation of a single voltage control has been proposed for high-power inverters. A widespread technique to limit the current with a single voltage loop consists in emulating a transient virtual impedance at the control references. This aims to limit the current value by acting

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on the voltage references [26], [27]. The disadvantage of this control is that it does not guarantee current control in the initial fault instants [26], as the dynamics of the voltage control introduces a delay in the limitation of the current. This can be solved by emulating the transient virtual impedances directly at the PWM signals [28]. In any case, the emulation of transient virtual impedances presents the disadvantage that the current is not controlled directly, so the value to which the current is finally limited depends on the type of fault or overload and its location in the system. Generally, the selection of the virtual impedance parameters is carried out to limit the current to a desired maximum magnitude in the worst case scenario, which means considering a bolted fault at the output of the inverter [29]. Hence, in the presence of other disturbances, the current will be limited to a lower value, underusing the inverter capacity.

Another proposed method consists in using a single voltage loop to calculate the maximum amplitude of the voltage that could be generated by the electronic converter without an overcurrent risk, based on the voltage measurement at the output [30]. Given that the voltage reduction is performed in an open loop, this method does not provide any current limiting precision either. Furthermore, being an RMS control, the method is slow and unable to limit the overcurrents in the first instants of the fault.

Other authors propose switching the control mode of the inverter from voltage source to current source once the overcurrent risk is detected [31]–[33]. In this technique, it is necessary to also include a fault detection mechanism that requires a time to trigger the changing of control mode. This time delay means that this method is not rapid enough to limit the currents in the first instants of these events and an additional method is required to ensure the safe operation of the inverter.

With regard to the last three methods mentioned, some authors supplement their method with the implementation of a hardware current limiter, such as [33], [34], in order to avoid the overcurrent during the first instants of the fault. This inhibits the semiconductor pulses if the current exceeds a given maximum value, with the subsequent increased complexity of the system. Moreover, the abrupt inhibition of the pulses causes the switching frequency to change, leading to a strong current distortion.

This paper proposes a novel dual voltage-current control strategy that gives inverters controlled in grid-forming mode an overcurrent limiting capability. This method controls the inverters as a voltage source in normal operating conditions when the instantaneous currents of the three phases are below the maximum current. While, when the instantaneous current of a phase approaches to the maximum, either positive or negative, the method controls that phase as a current source until the instantaneous current distances from the maximum. Consequently, the inverter phases are not permanently controlled as current sources during overloads or faults, but the control selected changes as the current is alternating. The shift between both controls happens automatically by comparing the instantaneous values of the reference voltages calculated by each control. Based on this, the dual voltage-current control

integrates both controls and selects autonomously the most restrictive output. Thus, there is only one operation mode in the inverter and therefore there is no need to implement fault detection mechanisms or any mode transition. Furthermore, in comparison with the aforementioned cascaded controls, there is no need to decouple the voltage and current loops given that both are implemented in parallel. Thanks to this, the dynamics of the voltage regulator are not affected by the bandwidth of the current control. The performance of the dual voltage-current control has been validated by simulation and experimental results obtained for a high-power inverter under stand-alone operation.

The rest of this paper is organized as follows. Section II describes the proposed dual voltage-current control, including the criterion used to calculate the final reference voltages. In Section III the design and operation of the proposed current control is analyzed under different conditions. The simulation results are presented in Section IV and the proposed dual control is experimentally verified in Section V. Finally, the conclusions are drawn in Section VI.

II. PROPOSED DUAL VOLTAGE-CURRENT CONTROL METHOD

A. Description of the Dual Control Method

The system under study is a three-phase grid-forming inverter that can operate in either grid-connected or island mode, as shown in Fig. 1. An LCL filter is also included at the converter output, where *L* is the converter-side inductor, *C* is the filter capacitor, and L_{out} is the output inductance, which could be formed by the leakage inductor of the transformer and the line inductance. As can be observed, reference frequency f^* , reference voltage V^* , measured inductor currents $i_{L,abc}$, and output capacitor voltages $v_{C,abc}$, are taken by the inverter control to calculate the final reference voltages $e_{f,abc}$, that are imposed on the inverter.

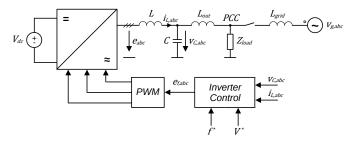


Fig. 1. Overall schematic diagram of a three-phase grid-forming inverter that can operate in grid-connected and island modes.

Figure 2 shows the dual voltage-current control method, including the voltage control together with the current control. The voltage control calculates, the reference voltages $e_{v,abc}$ that must be generated in each phase by the inverter in order to behave as a voltage source in the three phases. The voltage setpoints of the voltage control are calculated by the selected grid-forming method, such as droop control. At all times, the proposed current control calculates the reference voltages $e_{i,abc}^+$ and $e_{i,abc}^-$ that must be generated in each phase by the inverter in order to behave as a current source of either maximum

positive value, I_{max} , or maximum negative value, $-I_{max}$. Then, for the three phases, the reference voltages of both controls are compared and the most restrictive are selected as the reference voltages for the dual voltage-current control, $e_{dual,abc}$.

The voltage control is a single loop structure and can be implemented by using any of the methods proposed in the literature such as instantaneous open-loop or closed loop in dq synchronous or $\alpha\beta$ stationary coordinate frame, among others, [27], [26], [35].

B. Description of the Current Control

The proposed current control includes two instantaneous branches per phase to independently control currents $i_{L,abc}$, as shown in Fig. 2. Both control branches, where C_i is the current controller, are executed continuously and are necessary since the currents under control are alternating. The positive branch calculates the reference voltage e_i^+ that must be generated by the converter to control the current to I_{max} , whereas the negative branch calculates the reference voltage e_i^- that must be generated to control the current to $-I_{max}$. This control makes it possible to dynamically set the maximum current value, I_{max} , providing the inverter with greater flexibility to carry out tasks such as protecting the inverter from overheating or increasing its level of current at the beginning of the fault in order to help trigger the opening of the short-circuit protections.

Furthermore, a feedforward compensation of the capacitor voltage, v_C , is added at the controller output in order to control the inductor current independently of the overload or short-circuit. This provides the method with the capability to

quickly respond in the event of an overcurrent, making it unnecessary to implement hardware protection to limit the current during the first instants of the fault. More details about the design and operation of the current control are provided in Section III.

C. Selection of the Dual Control Reference Voltages

In the proposed dual voltage-current control, the voltage and the current controls always operate concurrently. At all times, and for the three phases, the overall control calculates the reference voltages ($e_{v,abc}$, $e_{i,abc}^+$, $e_{i,abc}^-$) that are required to regulate the converter according to the purpose of each control. These voltages are compared separately in each phase so as to select the reference voltages, $e_{dual,abc}$, that need to be imposed on the converter (see Fig. 2).

When focusing on one phase, the most restrictive reference voltage of the three will be selected as the reference voltage of the dual control. The selection is carried out according to the relationship among the voltages calculated by the voltage and current controls. This relationship primarily depends on the value of i_L and the maximum current, I_{max} . Initially, an ideal current controller, C_i , is considered to facilitate the understanding of the relationship among electrical variables. Whenever the current i_L is lower than I_{max} , the positive branch of the current control tries to increase the voltage generated by the converter to impose $i_L=I_{max}$, leading to $e_i^+ > e_v$. Conversely, when $i_L > -I_{max}$, the negative branch tries to control the current to $-I_{max}$, resulting in $e_i^- < e_v$.

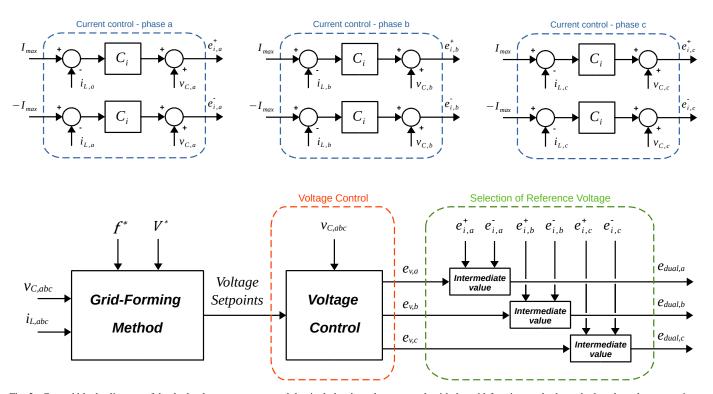


Fig. 2. Control blocks diagram of the dual voltage-current control that includes the voltage control, with the grid-forming method to calculate the voltage setpoints, the current control, formed by two branches per phase, and the selection of the dual control reference voltages.

Therefore, there are three possible situations in terms of the relationship among the reference voltages:

1. When there is no overcurrent risk $(-I_{max} < i_L < I_{max})$, i.e. normal operation, the converter must be controlled as a voltage source and the voltages relationship remains

$$e_i < e_v < e_i^+. \tag{1}$$

2. When there is risk of positive overcurrent, the converter must be controlled as a current source by the positive branch of the current control $(i_L \approx I_{max})$. In this situation the positive branch of the current control calculates a lower voltage $(e_i^+ < e_v)$ in order to maintain i_L equal to I_{max} , as the generation of e_v would cause i_L to increase to above I_{max} . As a result, the relationship between voltages changes to

$$e_i^- < e_i^+ < e_v^-. \tag{2}$$

3. When there is risk of negative overcurrent, the converter must be controlled as a current source by the negative branch of the current control $(i_L \approx -I_{max})$. Under these circumstances, voltage e_v would cause i_L to decrease to below $-I_{max}$, so the negative branch calculates a higher voltage $(e_i > e_v)$ to maintain i_L equal to $-I_{max}$. Hence, the voltages are sorted as follows

$$e_v < e_i^- < e_i^+. \tag{3}$$

As can be observed, in the three situations, the reference voltage with an intermediate value must be selected in order to ensure the correct operation of the converter within the current limits. If necessary, an anti-windup strategy must be adopted in the voltage controllers when the selected voltages are not those from the voltage control.

With this parallel operation of the voltage and current controls, the converter will behave in the three phases as a voltage source in normal operation. However, if the current of one phase tends to instantly exceed the current limits, then the converter will change in that phase in order to use the current control to limit the current.

D. Calculation of the final reference voltages

Once the reference voltages to be generated by the inverter in the three phases have been selected, $e_{dual,abc}$, an issue arises related to the zero component, i.e. homopolar component, of these voltages. In three-phase inverters, the voltages generated in the three phases are coupled through the zero component that behaves as a disturbance for the three voltages finally generated by the inverter. When the current control acts in at least one phase, the homopolar component differs from zero causing a loss of accuracy in the limitation of the current. This can be avoided by removing the zero component of $e_{dual,abc}$ with the algorithm shown in Fig. 3 which calculates the final reference voltages $e_{f,abc}$, based on $e_{dual,abc}$.

This is carried out according to two requisites: cancelling the uncontrolled homopolar component introduced by the selection of the voltages, while at the same time giving priority to the phase controlling the current. For this purpose, the differential

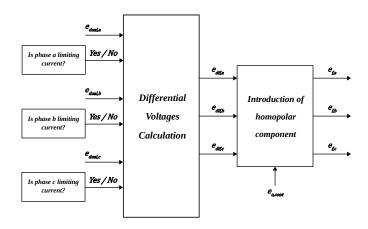


Fig. 3. Algorithm to calculate the final reference voltages based on the dual control reference voltages.

voltages, e_{dif} , are defined equal to the dual control voltages, e_{dual} , in the phase(s) in which the e_{dual} comes from the current control. Then, in the other phase(s), in which the e_{dual} comes from the voltage control, the differential voltage, e_{dif} , will be defined so that the homopolar component is removed. Table I shows how to determine the three differential voltages, $e_{dif,abc}$, according to which phase requires current control.

 TABLE I

 DIFFERENTIAL VOLTAGES CALCULATION

 ACCORDING TO WHICH PHASES REQUIRE CURRENT LIMITATION

ACCORDING TO WHICH PHASES REQUIRE CURRENT LIMITATION					
How many ph.	Which ph.	e _{dif,a}	e _{dif,b}	e _{dif,c}	
None	-	$e_{dual,a}$	$e_{dual,b}$	$e_{dual,c}$	
1	а	$e_{dual,a}$	$\frac{e_{dual,b} - e_{dual,a} - e_{dual,c}}{2}$	$\frac{e_{dual,c} - e_{dual,a} - e_{dual,b}}{2}$	
	b	$\frac{e_{dual,a} - e_{dual,b} - e_{dual,c}}{2}$	$e_{dual,b}$	$\frac{e_{dual,c} - e_{dual,a} - e_{dual,b}}{2}$	
	С	$\frac{e_{dual,a} - e_{dual,b} - e_{dual,c}}{2}$	$\frac{e_{dual,b} - e_{dual,a} - e_{dual,c}}{2}$	$e_{dual,c}$	
2	a - b	e _{dual,a}	e _{dual,b}	- $(e_{dual,a} + e_{dual,b})$	
	a - c	$e_{dual,a}$	- $(e_{dual,a} + e_{dual,c})$	e _{dual,c}	
	b - c	- $(e_{dual,b} + e_{dual,c})$	$e_{dual,b}$	e _{dual,c}	
3	a - b - c	It is imposed e _{dif,i} = e _{dual,i} in the two phases with higher i _L			

For example, if phase "*a*" requires current control, then its differential voltage, $e_{dif,a}$, will be defined equal to $e_{dual,a}$, while the differential voltages of phases "*b*" and "*c*", $e_{dif,bc}$, will be calculated by modifying equally the dual control voltages, $e_{dual,bc}$, in order to remove the undesired homopolar component, as follows

$$e_{dif,b} = e_{dual,b} - \frac{\sum e_{dual,abc}}{2},$$

$$e_{dif,c} = e_{dual,c} - \frac{\sum e_{dual,abc}}{2}.$$
(4)

If phases "*a*" and "*b*" require current control, then their differential voltages, $e_{dif,ab}$, will be defined equal to $e_{dual,ab}$, respectively, and the homopolar component will be removed by modifying the voltage of phase "*c*", $e_{dual,c}$, obtaining differential voltage $e_{dif,c}$ as

$$e_{dif,c} = e_{dual,c} - \sum e_{dual,abc}.$$
 (5)

It might also happen that the three phases are required to control the current such as in the first instants of a harsh fault. However, the dual control voltages cannot be imposed in the three phases since the uncontrolled homopolar component would not be cancelled. Therefore, the phase with the instantaneous current furthest from the limits, i.e. the one with the lowest absolute value, $|i_L|$, is identified and its differential voltage is calculated by (5) to cancel the homopolar component. Thanks to this, the differential voltages of the other two phases, with higher overcurrent risk, are defined equal to their respective dual control voltages.

According to Fig. 3, after calculating $e_{dif,abc}$, a controlled homopolar component, $e_{o,cont}$, could be added to increase the maximum ac voltage that can be generated by the converter. Thus, the final system of reference voltages, $e_{f,abc}$, which must be imposed on the converter, is obtained.

III. DESIGN AND OPERATION OF THE CURRENT CONTROL

A. Modeling of the Current Loops

The proposed current control shown in Fig. 2, consists in controlling currents $i_{L,abc}$ by means of implementing two instantaneous branches per phase. Both control branches are exactly identical, with the same control parameters, and only differ in their reference currents, which are I_{max} and $-I_{max}$ for the positive and negative branches, respectively. As a result, both current loops present the same dynamics and symmetrical behavior. Figure 4 shows the model of the current closed loop for the grid-forming inverter shown in Fig. 1.

Regarding the control part, C_i represents the current controller, D_s models the computation and zero-order hold delays and H_i and H_v the transfer functions of the current and voltage anti-aliasing filters, respectively. At the current controller output, a feed-forward compensation of v_C is added in order to actively dampen the resonance of the LC filter. This feed-forward loop includes a lead-lag compensator, *LLC*, which is designed to compensate the delay introduced in v_C by H_v and D_s at the rated frequency, α_{r_0} . These control blocks are defined as

$$C_{i} = K_{p}, \quad D_{s} = e^{-T_{s} \cdot s} \cdot \frac{1 - e^{-T_{s} \cdot s}}{T_{s} \cdot s},$$

$$H_{i} = H_{v} = \frac{\omega_{Cf}}{s + \omega_{Cf}}, \quad LLC = \frac{\tau_{z} \cdot s + l}{\tau_{p} \cdot s + l},$$
(6)

where K_p is the gain of the proportional controller, T_s is the sampling time, ω_{Cf} is the cutoff frequency of the anti-aliasing filters and τ_z and τ_p are the time constants of the zero and the pole of the *LLC*, respectively.

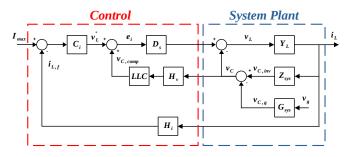


Fig. 4. Model of the current closed loop.

In relation to the system plant, Y_L represents the admittance of the converter-side inductor, Z_{sys} the equivalent impedance of the system which links i_L and $v_{C,inv}$ and G_{sys} the relationship between v_g and $v_{C,g}$. These transfer functions are defined as

$$Y_L = \frac{I}{L \cdot s + R_{CS}},\tag{7}$$

$$Z_{sys} = \frac{v_{C,inv}}{i_L} = \frac{Z_C \cdot (Z_{out} + Z_p)}{Z_C + Z_{out} + Z_p},$$
with $Z_p = \frac{Z_{load} \cdot Z_{grid}}{Z_{load} + Z_{grid}},$
(8)

where *L* is the converter-side inductor and R_{CS} the converter-side parasitic resistance, which includes the inductor losses, the switching conduction losses and the switching delays effect [36]. Then, Z_C models the impedance of the filter capacitor, Z_{out} the impedance of the output LCL filter inductor, Z_{load} the impedance of the loads connected to the system, Z_{grid} the grid impedance, which depends on the operating mode and the grid stiffness (short-circuit ratio, SCR), and Z_p the parallel impedance of Z_{load} and Z_{grid} . Equation (8) is valid for grid -connected and also for island mode since $Z_{grid} \rightarrow \infty$ and thus $Z_p = Z_{load}$ in this operating mode. The transfer function G_{sys} is not shown as it does not affect the dynamics of the closed loop.

B. Design of the Current Controller

During overloads or faults, the dual control alternates between the voltage and the current controls. Thus, a proportional controller is selected for the current control in order to avoid a complex anti-windup strategy. As will be shown, this controller makes it possible to achieve a fast response with low steady state error.

Several cases in which the current control would act have been analyzed in order to reliably design its proportional gain. The impedance Z_{load} variation range is taken between 0.02 pu (short-circuit) and 1 pu (rated load), as for higher values the inverter will not be overloaded and the current control will not act. Moreover, various load power factors (PF_{load}) have been considered. With respect to the grid, Z_{grid} could change from values close to 0.05 pu, for strong grids (SCR=20), to 0.67 pu, in extremely weak grids (SCR=1.5), which is practically the same as considering that the system is operating in island mode. Table II shows the values considered for the parameters of the control and system plant in the design of the current controller.

From the analysis of all mentioned cases, the resistive short-circuit with Z_{load} =0.02 pu is found to be the worst-case

TABLE II CONTROL AND SYSTEM PLANT PARAMETERS CONSIDERED IN THE DESIGN OF C_1

Symbol	Description	Value
Sn	Inverter Rated power	1.12 MVA
V_n	Rated voltage	400 V
Imax	Maximum peak current	$\sqrt{2} \cdot 1615 \text{ A}$
V_{DC}	dc-bus voltage	720 V
f_o	Rated frequency	50 Hz
f_{sw}	Switching frequency	3 kHz
f_s	Sampling frequency	6 kHz
$\alpha_{_{f_o}}$	LLC delay compensation at fo	5.6°
Ľ	Converter-side filter inductor	0.14 pu
R_{CS}	Converter-side parasitic resistance	0.03 pu
С	Filter capacitance	0.03 pu
Lout	Output inductance	0.07 pu
Zload	Load impedance	0.02-1 pu
PF_{load}	Load power factor	0-1
Z_{grid}	Grid impedance	0.05-0.67 pu
K_p	Proportional gain of C_i	0.5 pu

scenario in terms of stability margins (gain and phase margins). Furthermore, as this short-circuit would decouple the inverter and the grid, the dynamic performance of the current control would be similar in both grid-connected and island modes. Thus, the selection of the proportional gain is carried out in this scenario by applying the bode criterion to the open-loop transfer function, L(s). This transfer function is calculated as

$$L(s) = C_i \cdot Y_{eq} \cdot H_i, \tag{9}$$

where Y_{eq} is the equivalent plant seen by the controller and can be obtained as (see Fig. 4)

$$Y_{eq} = \frac{i_L}{v_L^*} = \frac{D_s}{Z_L + Z_{sys} \cdot (l - D_s \cdot LLC \cdot H_v)}.$$
 (10)

Fig. 5 shows the Bode diagram of the transfer function L(s) with K_p equal to 0.5 pu for four different cases: resistive short-circuit, island mode operation with a 100% overload, and grid-connected mode operation considering both a strong (SCR=20) and an extremely weak (SCR=1.5) grid conditions. As can be observed, K_p has been defined in a way that the minimum gain margin (with resistive short-circuit) is greater than 6 dB. As a result, the crossover frequency, f_c , varies between 123 Hz and 160 Hz and the phase margins between 35° and 72.3°, depending on the operating conditions, as shown in Fig. 5.

C. Actuating Limit of the Current Control

Considering one phase, Fig. 6(a) shows the evolution of the reference voltages e_v , e_i^+ and e_i^- during a fundamental cycle for $I_{load}=0.75$ pu. As there is no risk of overcurrent, e_v has the intermediate value during the whole cycle and will always be selected, meaning that the current control will not act. The increase of the demanded current I_{load} causes e_i^+ and e_i^- to get closer to e_v so that the current control is closer to acting. Indeed, if the level of current continues to increase, there is a value of I_{load} , close to I_{max} and defined as the limit current $I_{L,L}$, for which e_v is equal to e_i^+ and e_i^- at only one point. These operating

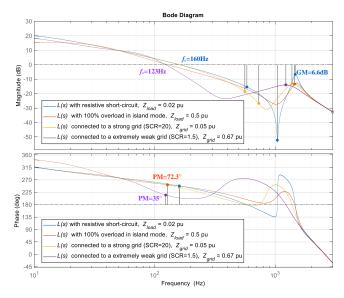


Fig. 5. Bode Diagram of the transfer function L(s) for four different cases.

conditions represent the actuating limit of the current control and are shown in Fig. 6(b). Then, if the current provided is further increased, reference voltages e_i^+ and e_i^- will be selected and thus the current control will be active in two portions of the fundamental cycle, as shown in Fig. 6(c) for $I_{load}=1.1$ pu.

As can be observed in Fig. 6, the operation of the dual voltage-current control is completely symmetrical in the positive and the negative semi-cycles. Therefore, only the positive branch of the current control is considered in the following analysis.

In order to calculate $I_{L,L}$, the actuating limit of the current control is studied in further detail. This operating point presents the characteristic that e_v and e_l^+ are equal and also tangent at the angle $\theta_L = \omega_0 \cdot t_L$. Hence, the following two equations, with $\omega_0 \cdot t_L$ and $I_{L,L}$ as unknown values, apply

$$e_{v}(t_{L}) = e_{i}^{+}(t_{L}),$$

$$\frac{de_{v}}{dt}\Big|_{t_{L}} = \frac{de_{i}^{+}}{dt}\Big|_{t_{L}}.$$
(11)

As the converter is still controlled as a voltage source, voltage e_v is defined considering

$$e(t) = \mathcal{L}^{-1}[D_s \cdot e_v(s)] = v_L(t) + v_C(t), \quad (12)$$

where v_L is the voltage drop at the converter-side inductor, which is

$$v_L(t) = L \cdot \frac{di_L(t)}{dt} + R_{CS} \cdot i_L(t).$$
(13)

According to Fig. 4, the voltage e_i^+ is defined considering

$$\mathcal{L}^{-1}[D_s \cdot e_i^+(s)] =$$

$$K_P \cdot I_{max} \cdot K_p \cdot \mathcal{L}^{-1}[D_s \cdot i_{L,f}(s)] + \mathcal{L}^{-1}[D_s \cdot v_{C,comp}(s)] = (14)$$

$$K_p \cdot I_{max} \cdot K_p \cdot \mathcal{L}^{-1}[D_s \cdot H_i \cdot i_L(s)] + \mathcal{L}^{-1}[D_s \cdot H_v \cdot LLC \cdot v_C(s)].$$

The analysis is carried out considering only the fundamental components at the rated frequency, f_0 , thereby current i_L is defined as

$$i_L(t) = I_{L,L} \cdot sin(\omega_0 \cdot t), \text{ with } \omega_0 = 2\pi \cdot f_0.$$
(15)

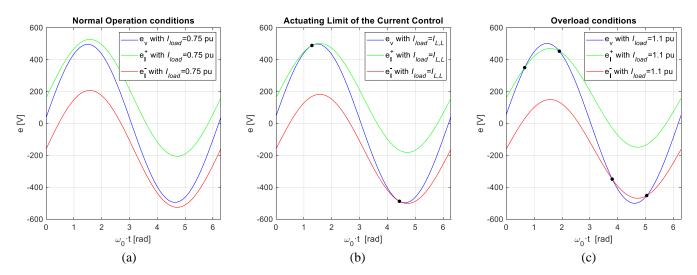


Fig. 6. Comparison of the reference voltages calculated by the voltage and current controls for different operation points. (a) Normal operation with $I_{load}=0.75$ pu (b) Actuating limit of the current control (c) Overload conditions with $I_{load}=1.1$ pu.

In relation to (14), at the frequency f_0 the module $|D_s(\omega_0 \cdot j) \cdot H_i(\omega_0 \cdot j)| \approx 1$ and the delay introduced by D_s and H_i is α_{f_0} . Thus, from (14) and (15), the following applies

$$\mathcal{L}^{-I}[D_s \cdot i_{L,f}(s)] = I_{L,L} \cdot sin\left(\omega_0 \cdot t - \alpha_{f_0}\right).$$
(16)

Additionally, it can be considered that

$$v_C(t) \approx \mathcal{L}^{-1}[D_s \cdot H_v \cdot LLC \cdot v_C(s)], \qquad (17)$$

thanks to the introduction of the LLC in the feed-forward loop.

On account of these considerations, applying (12)-(17) to the system in (11) makes it possible to obtain θ_L and $I_{L,L}$ of the actuating limit as

$$\theta_{L} = \omega_{0} \cdot t_{L} = atan \left(\frac{R_{CS} + K_{p} \cdot sin\left(\alpha_{f_{0}}\right)}{\omega_{0} \cdot L - K_{p} \cdot cos\left(\alpha_{f_{0}}\right)} \right),$$
(18)

$$I_{L,L} = I_{max} \cdot \frac{K_p}{\sqrt{\left(\omega_0 \cdot L - K_p \cdot sin\left(a_{f_0}\right)\right)^2 + \left(R_{CS} + K_p \cdot cos\left(a_{f_0}\right)\right)^2}}.$$
 (19)

According to the data given in Table II and the selected K_p , the actuating limit of the current control in our case study is $I_{L,L}=0.934 \cdot I_{max}$. However, the actuation of the current control for load current levels between $I_{L,L}$ and 1 pu will be small and the voltage generated by the inverter is barely affected in this range, as will be shown in the following sections.

IV. SIMULATION RESULTS

To analyze the performance of the proposed dual voltage-current control, the three-phase grid-forming inverter shown in Fig. 1, has been simulated in island mode for different operating points. The main parameters of the system are shown in Table II. Fig. 7 shows the voltage control employed, where the frequency and voltage setpoints are calculated by the well-known droop control considering the rated frequency and voltage, f_0 and V_n . This voltage control, which is widely used, consists in implementing a closed-loop to control the

fundamental component's RMS of the output capacitor voltages, V_C , to the voltage setpoint by means of E_v . The phase $\theta_{e,v}$ is directly calculated by integrating f^* [5]. In relation to the calculation of the final reference voltages, a controlled homopolar component is not introduced, i.e. $e_{o,cont} = 0$, since the dc-bus voltage V_{DC} , shown in Table II, is high enough to generate the rated voltage V_n .

It is worth noting that, in case that a cascaded control was employed, the outer voltage loop should be tuned to a bandwidth several times lower than the current loop to ensure decoupling them [18]. For the case study, recalling Fig. 5, the current control could exhibit a minimum crossover frequency of 123 Hz, thus the voltage controller could be difficultly designed to a bandwidth higher than 25 Hz. With this cascaded control, the inverter would offer an equivalent impedance higher than the actual one to those harmonic components whose frequency is between the bandwidths of both nested loops leading to a greater harmonic distortion at the output voltage. This is due to the fact that the outer voltage loop does not act in this frequency range, while the current loop rejects the harmonic components. In contrast, with the implemented option of the proposed dual voltage-current control, the voltage control does not react to the harmonic components and the inverter offers an impedance that only depends on the LCL filter. Therefore, for the harmonic components below the LCL-filter resonance frequency the per unit inductance is $L + L_{out} = 0.21$ pu, presenting a value similar to the subtransitory inductance offered by the SG to these harmonic components.

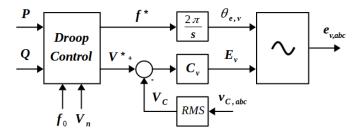


Fig. 7. Voltage control with droop control implemented in the grid-forming inverter [5].

Figure 8 shows the waveforms obtained with two grid-forming inverters connected in parallel, first in normal operation with a load change and then when a 20% permanent overload occurs. As can be observed, the currents of both inverters are similar in all cases, meaning that the droop control together with the dual voltage-current control ensures the load sharing between inverters independently of the operating conditions.

In normal operation with low load (from t = 0.96 s to t = 1 s), the currents of both inverters are considerably lower than the maximum and the reference voltages of the current control present high values. The relationship among voltages is $e_i^- < e_v < e_i^+$ with high differences between them, so the reference voltages of the voltage control are the most restrictive. Thus, the current control is far from acting and the inverters are controlled as voltage sources resulting in sinusoidal waveforms in the PCC voltages and currents. When the load increases before the overload (from t = 1 s to t = 1.04 s), the currents increase and the reference voltages of the current control decreases. This causes that the reference voltages e_i^+ and e_i^- get closer to e_v but without crossing since the currents are still below the maximum current.

When the converters transfer from normal operation to overload (from t = 1.04 s to t = 1.1 s), the currents reach the maximum value and the reference voltages of the current control immediately decrease. As a result, either the reference voltages of the positive or negative current branches are the most restrictive in parts of the fundamental cycle and start to be selected in both inverters. In this way, the currents are immediately limited to the maximum value without requiring a change of control mode unlike other methods. The maintenance of the instant current as equal to I_{max} and $-I_{max}$ when the current control acts results in an RMS current slightly higher than the rated value. In fact, this effect is studied in further detail in Section V.C showing that the RMS current is around 1.01 pu in the presence of a 20% overload. Although the action of the current control causes the voltage to decrease at the PCC, this remains within the voltage limits $(\pm 0.2 pu)$ born by the loads. Therefore, the proposed method allows the converters to continue feeding the loads in the presence of low overloads (up to 20%) with no risk of damage. Furthermore, the inverters remain synchronized during the overload and maintain the frequency of the system as the dual voltage-current control also generates the frequency setpoint while the current is limited.

Fig. 9 shows the waveforms obtained when a three-phase symmetrical short-circuit, with a short-circuit voltage $U_{CC} = 5\%$, occurs at the output of an islanded inverter. At the beginning of this event, the current is rapidly regulated by the current control despite the severity of the short-circuit. As can be observed, the currents increase up to 1.3 pu at the first instant of the fault, but this overcurrent lasts less than 1ms (≈ 0.6 ms). Considering this duration, a 1.3 pu overcurrent does not represent any thermal risk for the high-power inverter

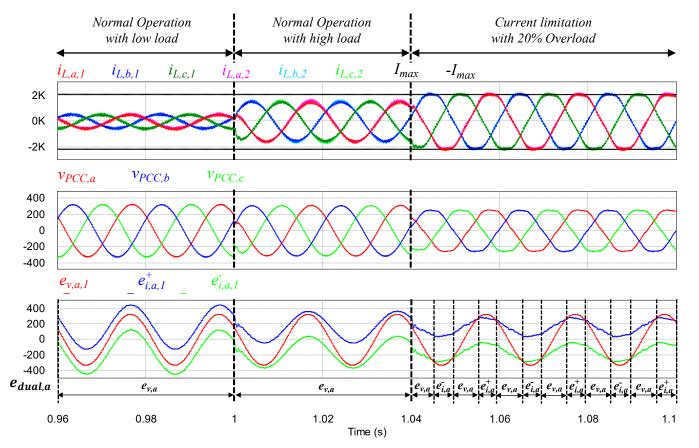


Fig. 8. Simulation waveforms obtained with two grid-forming inverters connected in parallel, first in normal operation during a load change and then transferring to current limiting due to a 20% overload condition.

semiconductors since their transient thermal impedance junction-case, $Z_{th,(j-c)}$, is almost a 90% lower in this time scale than the thermal resistance in steady state, e.g. $Z_{th,(j-c)} = 0.0065$ K/W (in 1ms) vs $R_{th,(j-c)} = 0.056$ K/W for the SEMiX453GD17E4C [37]. Consequently, additional hardware-protection is not required to guarantee the safe operation of the inverter at all times, even in the initial instants of the overcurrent events. Additionally, the rapid limitation of the current by the current control causes the immediate mitigation of the initial DC component that generally appears in SG-based systems at the first instants of the faults. Likewise, the PCC voltage rapidly recovers as the converter returns to normal operation when the fault is cleared.

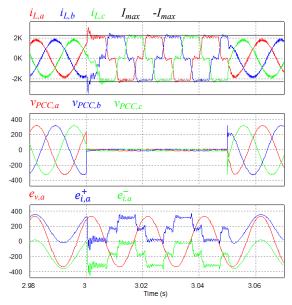


Fig. 9. Simulation waveforms obtained with a three-phase symmetrical short-circuit, from normal operation to short-circuit and reverse.

Fig. 10 gives the waveforms when a phase-to-phase, a-b, short-circuit, with $U_{CC} = 5\%$, occurs at the output of an islanded inverter. It can be noticed that the current is correctly limited in the two phases (a-b) where the short-circuit occurs. In order to ensure this, the voltage of phase "c" must also be modified, otherwise it would not be possible to limit the current of the overload phases.

The simulation results make clear that the proposed dual voltage-current control is able to rapidly limit the converter currents under overloads and short-circuits, symmetrical and asymmetrical, without changing the control mode or requiring hardware protection, even in severe faults.

V. EXPERIMENTAL VALIDATION

In order to further validate the effectiveness and behavior of the proposed dual voltage-current control, the commercial inverter INGECON SUN STORAGE Power1000V, shown in Fig. 11, was experimentally tested. The system under study is described in Section IV. The parameters of the filters and the control are shown in Table II.

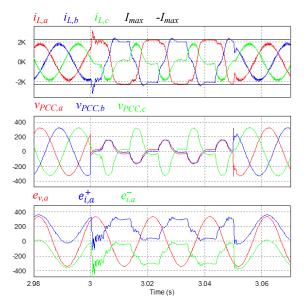


Fig. 10. Simulation waveforms obtained with a phase-to-phase asymmetrical short-circuit, from normal operation to short-circuit and reverse.



Fig. 11. 1.12 MVA used for the experimental validation.

A. Response in the Presence of Short-Circuits

Two cases of those introduced in Section IV were replicated, namely three-phase and phase-to-phase short-circuits, in order to verify the response of the proposed current control in worst-case conditions.

Figure 12 shows the measured waveforms of two currents, in phases "a" and "b", when the inverter transfers from open-circuit to a three-phase symmetrical short-circuit. When the severe short-circuit occurs, the currents are rapidly controlled to the maximum value and the waveforms are similar to those obtained in the simulation results.

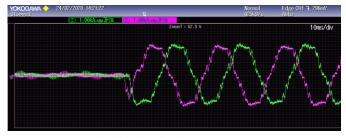


Fig. 12. Experimental validation when the inverter transfers from open circuit to a three-phase symmetrical short-circuit, CH2: Phase "a" inductor current, CH3: Phase "b" inductor current.

Figure 13 shows the experimental results after a phase-to-phase short-circuit, from phase "a" to "b". In this case, the phase-to phase-voltage *a*-*c* is also included. Furthermore, the current of phase *b* was reversed. Since phase "*c*" remains in open circuit, it can be observed that $i_{L,a} = -i_{L,b}$. The currents of the short-circuited phases are correctly limited, while the phase-to-phase voltage *a*-*c* decreases only to 0.8 pu as in the simulation results.

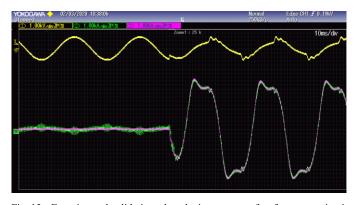


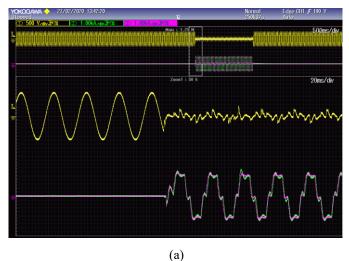
Fig. 13. Experimental validation when the inverter transfers from open circuit to a phase-to-phase short-circuit, CH1: Phase-to-phase PCC voltage *a*-c, CH2: Phase "*a*" inductor current, CH3: Phase "*b*" inductor current reversed.

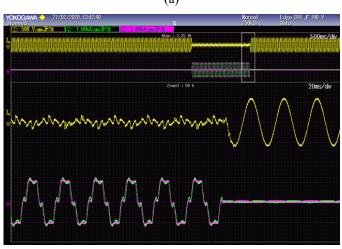
Furthermore, the dual voltage-current control was tested with two grid-forming inverters operating in parallel. Figure 14 gives the experimental waveforms under a three-phase symmetrical short-circuit in the PCC with two inverters operating in parallel. Fig. 14(a) and Fig. 14(b) show the dynamic response of the system transferring from open-circuit to short-circuit and back, respectively. At the beginning, the currents of both inverters are rapidly controlled to the maximum current, I_{max} , similarly to the case with one inverter. Then, the PCC voltage recovers immediately and the system goes back to normal operation when the fault is cleared. Thus, these experimental results show that the proposed dual control method provides effective performance with one or more inverters in parallel, both during the fault and after its clearance.

B. Actuating Limit of the Current Control

In order to verify the expression (19), which defines the current amplitude $I_{L,L}$ from which the current control starts to act, the two mentioned grid-forming inverters with droop control, were operated in parallel under a no load condition. The experiment comprises of forcing the inverters to exchange real power by increasing the difference between the reference frequencies, $f_1^* - f_2^*$, until the actuating limit of the current control is reached.

Operating the inverters at the actuating limit of the current control, Fig. 15 shows the exchanged currents for phase "a" of both inverters, and the phase-to-phase PCC voltage a-c. Moreover, Fig. 16 shows the dual control reference voltages, which are measured by the DSP, for phase "a" of inverter 1. It can be seen that the actuating limit has been reached since the reference voltages of the voltage and current controls are practically tangent. The level of current conducted by the inverters at this operating point is approximately 0.938 pu that coincides with the $I_{L,L}$ calculated theoretically of 0.934 pu.





(b)

Fig. 14. Experimental validation with 2 inverters in parallel under three-phase symmetrical short-circuit. (a) From open circuit to short-circuit. (b) From short-circuit to open-circuit. CH1: Phase-to-phase PCC voltage *a-c*, CH2: Phase "*a*" inductor current of inverter 1, CH3: Phase "*a*" inductor current of inverter 2.

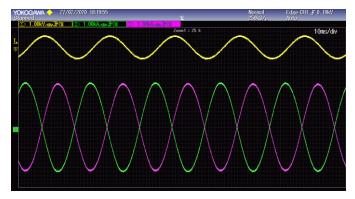


Fig. 15. Experimental validation with 2 inverters operating in parallel at the actuating limit of the current control. CH1: Phase-to-phase PCC voltage *a-c*, CH2: Phase "*a*" inductor current of inverter 1, CH3: Phase "*a*" inductor current of inverter 2.

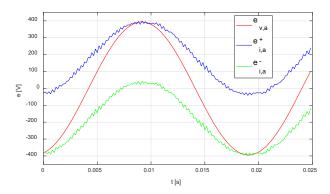


Fig. 16. Experimental validation with 2 inverters operating at the actuating limit of the current control. Phase "a" dual control reference voltages of inverter 1.

C. RMS Current during Overload and Short-Circuit

The dual voltage-current control limits the current when it tends to be higher than the maximum limits. Therefore, the shape of the current waveform changes according to the level of overload or short-circuit. For example, in Fig. 8 and Fig. 9, although the current is limited to the same value in both cases, the current waveform is squarer in the second since the current control has to act in a higher portion of the fundamental cycle. This fact results in a slight variation of the RMS current, $I_{L,RMS}$, which depends on the overload level or short-circuit severity.

Figure 17 shows the values of $I_{L,RMS}$ and THD_i obtained under different load impedances, Z_{load} , which cause the operation of the current control by means of simulation and experimental results. According to the simulation results, the level of current increases slightly with the overload level, reaching the maximum $I_{L,RMS}$ (1.07 pu) for the short-circuit case ($Z_{load}=0$) as shown in Fig. 17(a). In the experimental setup, two points were obtained from the previous tests, which validates the operation of the dual control in the actuating limit and under short-circuit conditions.

The dual voltage-current control provides a satisfactory performance in this operating range, since I_L remains close to 1 pu for any Z_{load} , while the current is rapidly limited under any overload or fault. Furthermore, the maximum current value, I_{max} , can be dynamically set to provide the inverter with flexibility to carry out tasks such as protecting the inverter from overheating or increasing its level of current at the beginning of the fault in order to help trigger the opening of the short-circuit protections.

According to Fig. 17(b), the actuation of the current control distorts the current slightly with small overloads as the THD_i remains lower than 4% up to overload levels of 20%, $Z_{load} = 0.83$ pu. For higher overload levels, the distortion increases up to a maximum of 23% in simulation and a 20% in experimental results. In stand-alone mode, this does not represent a problem since the highest values of THD_i appear in the presence of short-circuits or transient overloads. Nevertheless, in grid-connected mode, the mentioned values of THD_i are not accepted by the grid codes making necessary the implementation of an extra strategy to fulfill the requirements. One alternative could be reducing the voltage setpoint of the voltage control to decrease the actuation of the current control,

thereby improving the current distortion [33]. Indeed, the next step will be addressing this issue in order comply with the grid regulations.

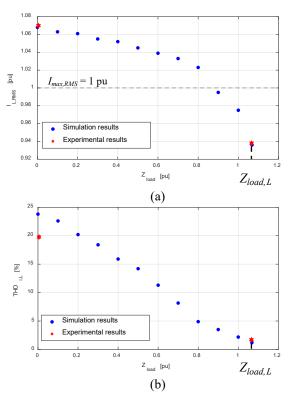


Fig. 17. Operation of the dual voltage-current control under different load conditions in which the current control acts. (a) Variation of the level of current $I_{L,RMS}$ with Z_{load} . (b) Variation of the total harmonic distortion of the current THD_i with Z_{load} .

VI. CONCLUSION

This article presents a dual voltage-current control for grid-forming inverters to provide them with an overcurrent limiting capability. The main characteristic of this method is that the voltage and the proposed current controls are concurrently operated. This makes it possible to control the three-phase inverter as a voltage source in normal operation, but in the event of an overcurrent risk the current regulation takes control. One advantage of this method is that the selection of the control is automatic and immediate without changing the mode or requiring any mechanism to detect the fault. Furthermore, the proposed current control is rapid enough to limit the current at the start of the faults so that no hardware protection is required. As a result of this rapidity, the current is distorted according to the overload level or short-circuit severity. Should it be necessary to operate the inverter for a long period under these conditions, then the voltage setpoint of the voltage control could be reduced to decrease the actuation of the current control and thereby improve the current distortion.

The theoretical analysis of the proposed dual voltage-current control has been validated by means of simulation and experimental results obtained under stand-alone operation. The experimental verification has been carried out testing a commercial high-power inverter in normal operation and under symmetrical and asymmetrical faults. The proposed dual voltage-current control could be a promising technique when operating connected to the grid, but further work is required to comply with the current and future grid codes. Exploring this line is part of the authors future work.

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